



Allegro X Engineering Cockpit

Schematic and Layout Editor in a Single Environment

Michael Catrambone – Product Engineering Architect

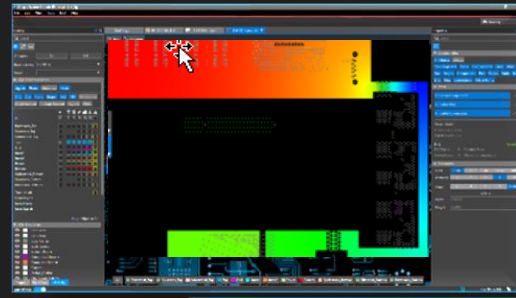
Allegro X Engineering Cockpit

Schematic and Layout Editor in a Single Environment

- Introducing a complete PCB layout solution integrated into Schematic
- Review the new, modern, intuitive interface to perform Placement, Routing, and Analysis, including export to Manufacturing
- Manage design constraints visually and hierarchically inside a docked Constraint Panel
- Generate fabrication and assembly documentation quickly and easily using LiveDoc.



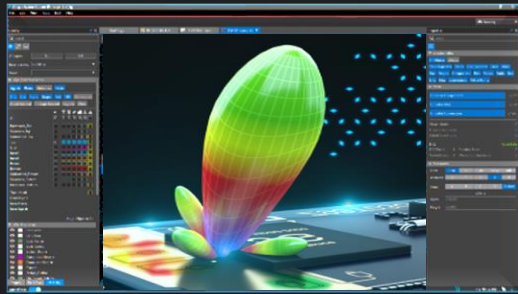
Supply chain / BOM optimization



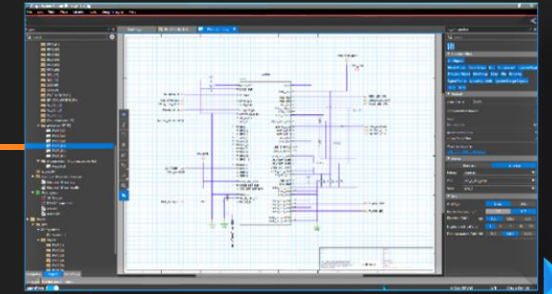
Analysis



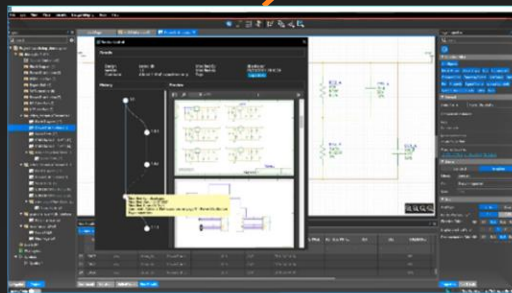
Reliability



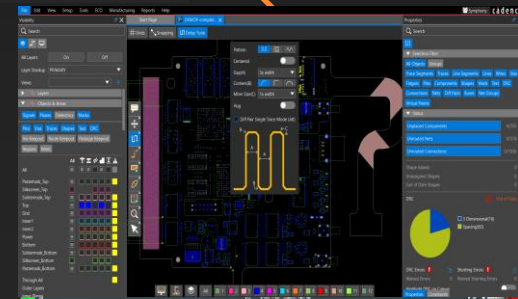
AWR RF Design



System Capture Schematic



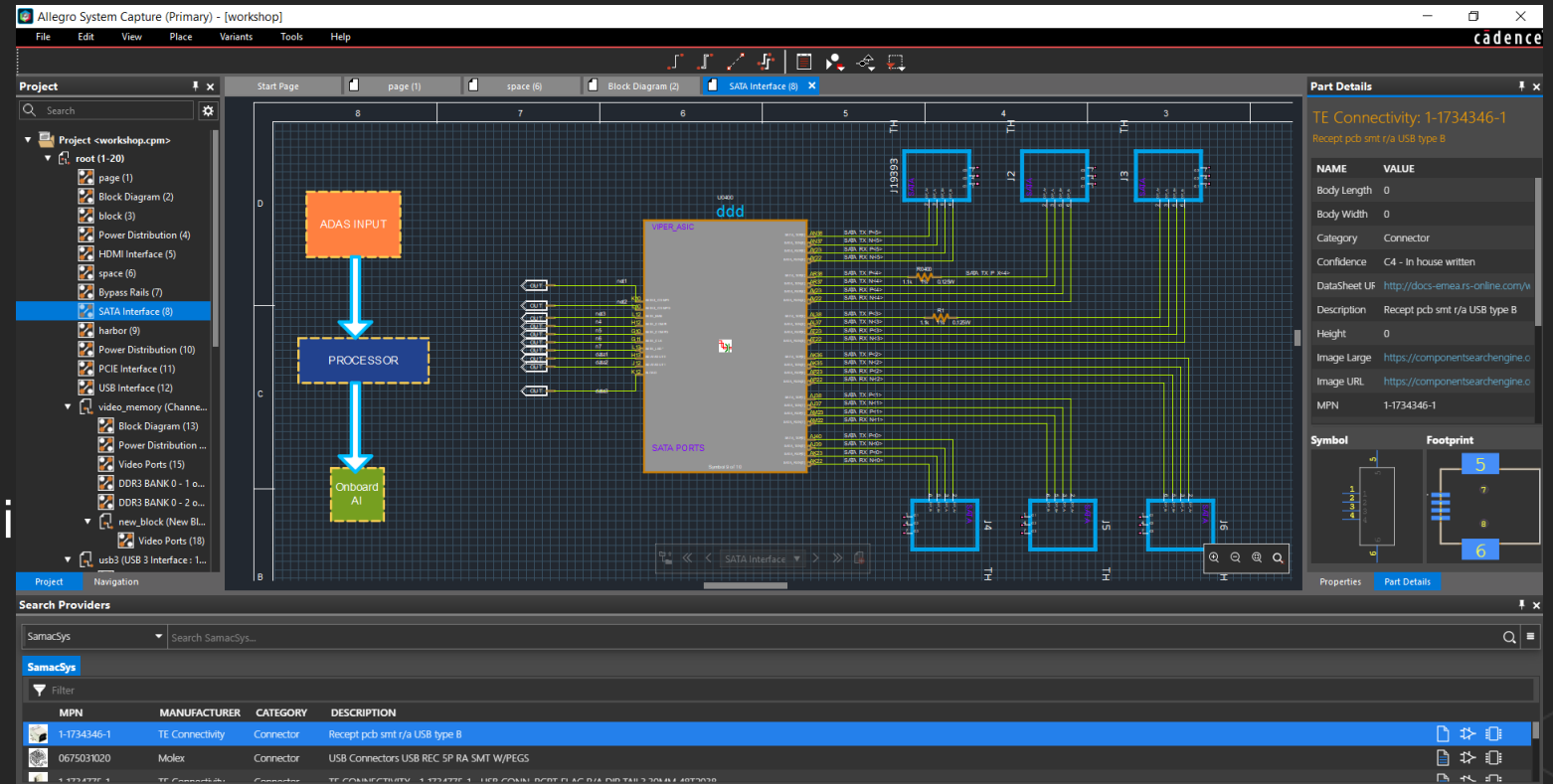
Design Data management



Integrated PCB editor

Allegro X – System Capture

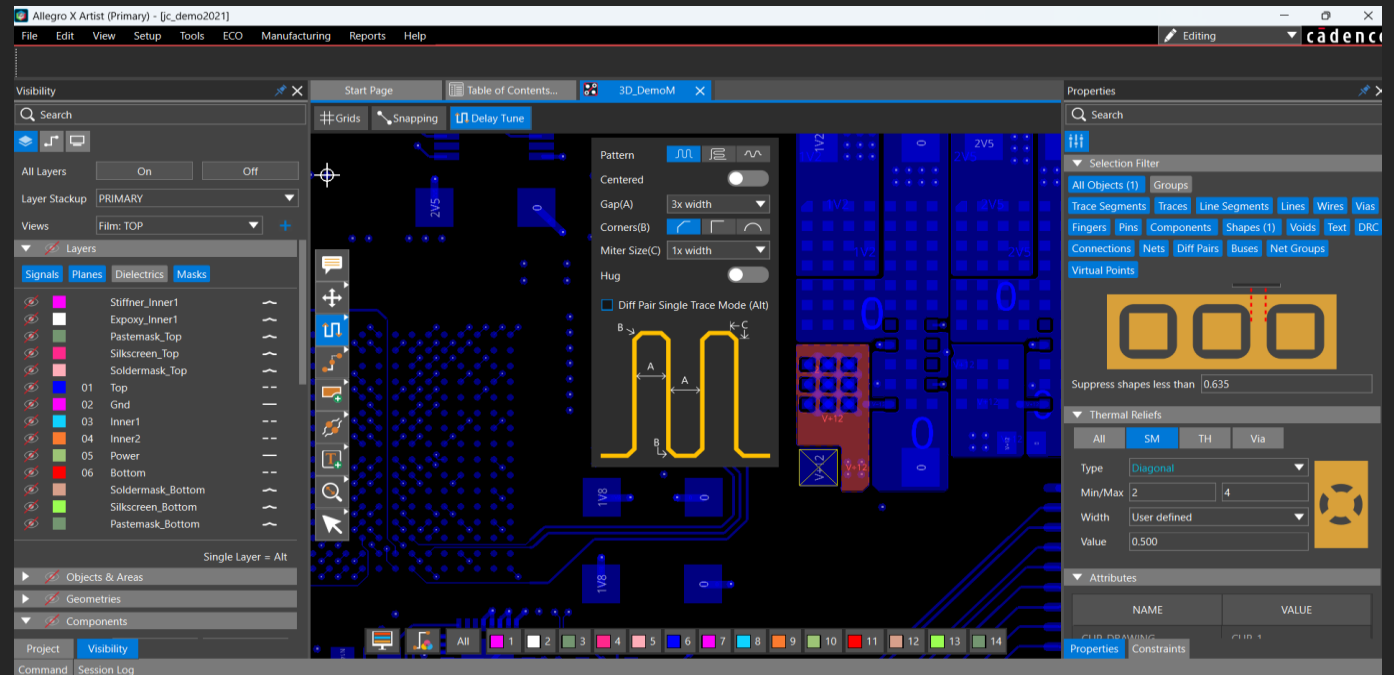
- Multi board system design
- Integrated PCB editor
- Team Design
- Reliability
- Advanced Rule Checking
- Constraint Management
- High Speed simulation
- Power Planning
- Thermal analysis and floor planning
- Variants
- Intelligent Block Diagram
- Built in revision control
- PSpice



Modern User Interface

Allegro X Integrated Layout Editor

- Complete layout solution integrated into System Capture
- Common, intuitive UI
 - Placement
 - Routing
 - Design review
 - Analysis
 - Reports
 - Export to manufacturing
 - ECAD MCAD



Allegro X Integrated Layout Editor

ECAD/MCAD Collaboration

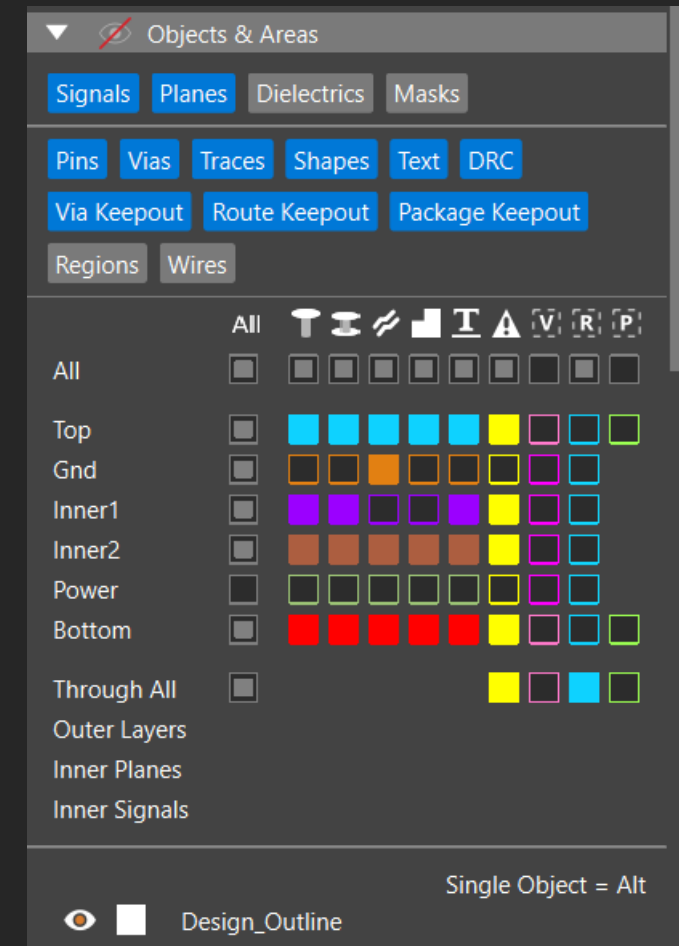
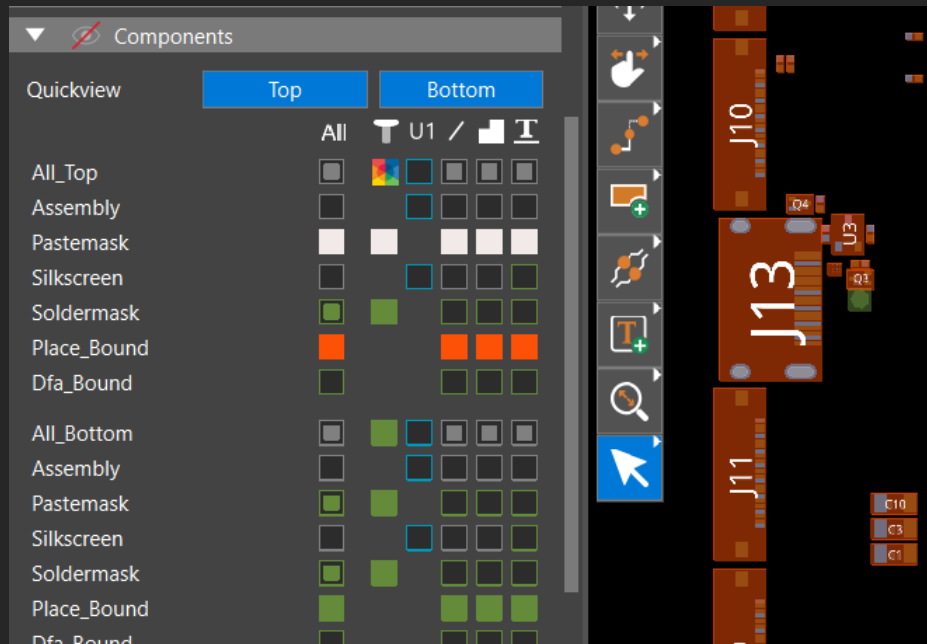
- Codesign between ECAD and MCAD using industry leading tools
 - Dassault Solidworks & Catia (MCADX)
 - PTC Creo (IDX)
 - Siemens NX (IDX)
 - Autodesk Fusion (IDF)
- Bi-directional communication using IDX & IDF
- Bi-directional transfer of design objects between both domains
 - Board Outline, cutouts, keepouts, copper, silkscreen, critical placement and 3D models
- Baseline and Incremental file exchange
- Preview requested changes, Accept or Reject changes with Revert capability



Allegro X Integrated Layout Editor

Superior Display control

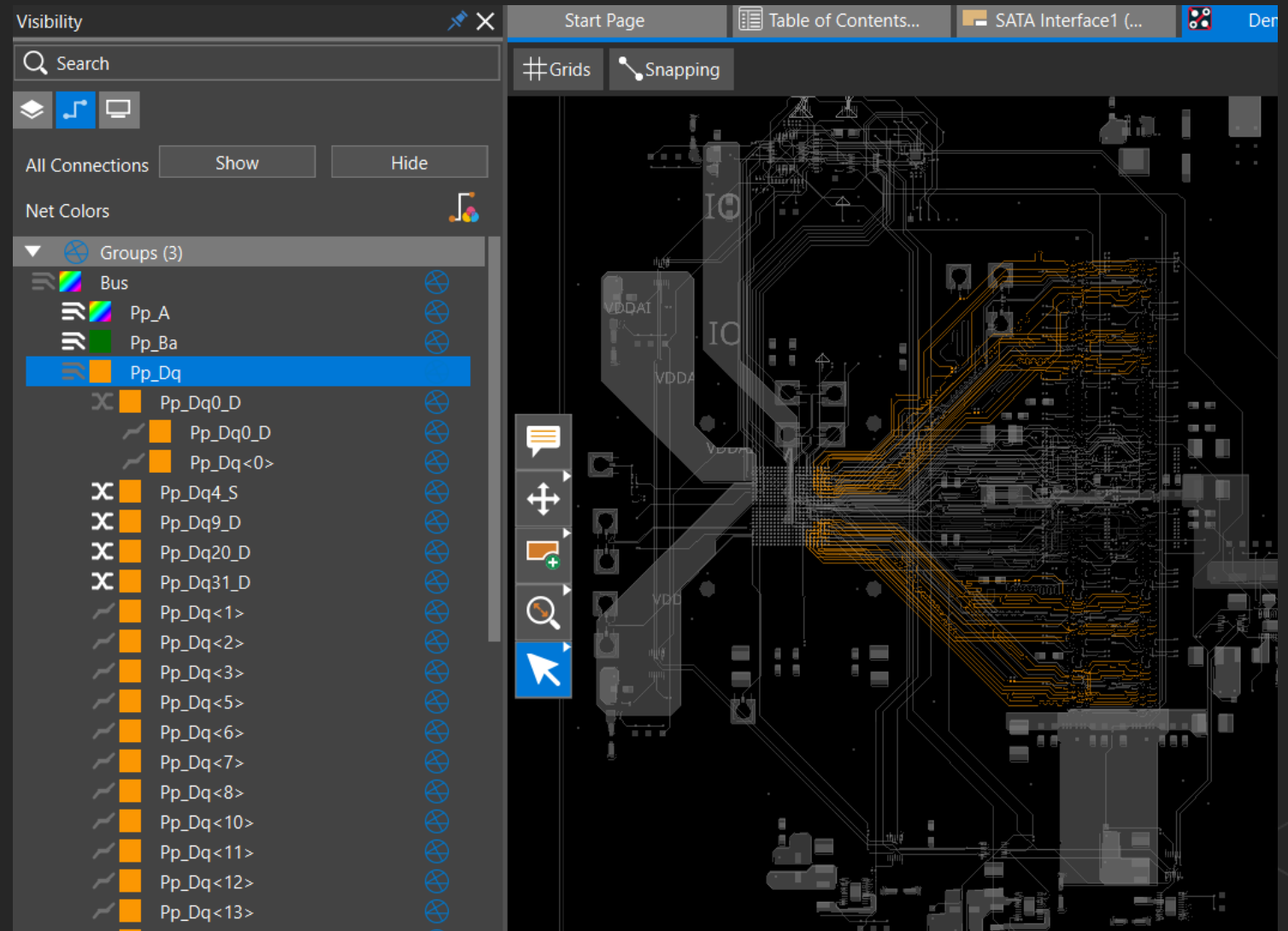
- Separate visibility control for shapes and traces
- Easily enable the display of keepouts and regions
- Easy way to enable the design outline
- Clear and easy display control for components



Allegro X Integrated Layout Editor

Net Navigator

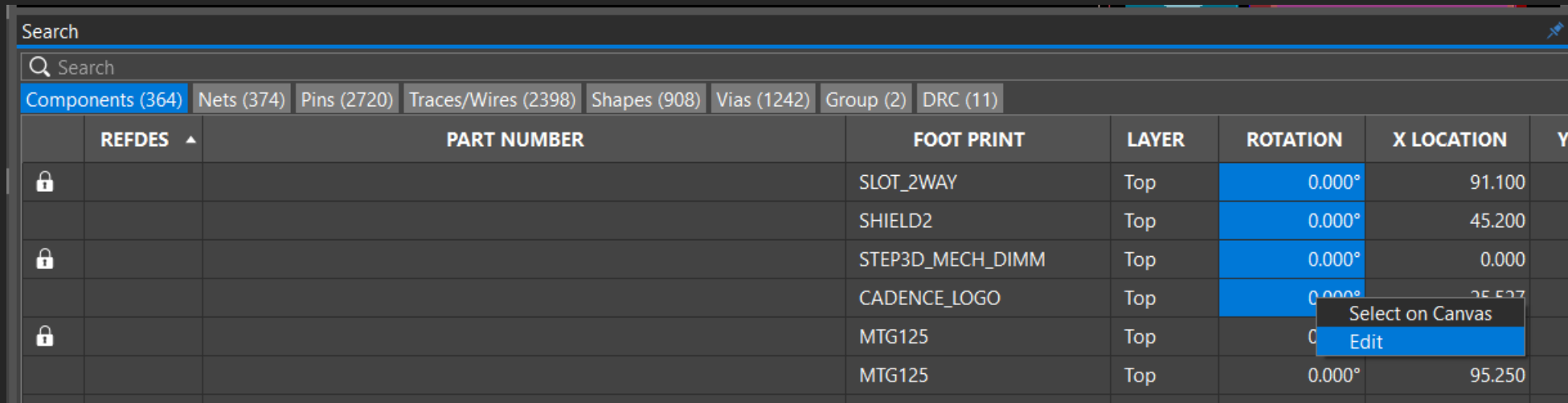
- Hierarchical net navigator
- Set colors
- Control rat display
- Ultra shadow display gives user an efficient way to find nets or other objects in the design



Allegro X Integrated Layout Editor

Search table

- The entire database is represented in an interactive data table with filters and searching
- Powerful way to interact with your design based on data objects instead of the design canvas
 - Find all capacitors with a certain footprint and part number and apply a desired fanout pattern
 - Find all traces of a certain width for a certain net on a certain set of layers and change their width
 - Find all pads of a certain name and replace them



Search							
Search							
Components (364) Nets (374) Pins (2720) Traces/Wires (2398) Shapes (908) Vias (1242) Group (2) DRC (11)							
	REFDES ▲	PART NUMBER	FOOT PRINT	LAYER	ROTATION	X LOCATION	Y
🔒			SLOT_2WAY	Top	0.000°	91.100	
			SHIELD2	Top	0.000°	45.200	
🔒			STEP3D_MECH_DIMM	Top	0.000°	0.000	
			CADENCE_LOGO	Top	0.000°	25.527	
🔒			MTG125	Top	0.000°		
			MTG125	Top	0.000°	95.250	

Allegro X Integrated Layout Editor




Interactive DRC chart

- Interactive, real time, DRC pie chart in properties panel
- Immediate feedback on the number and type of DRCs in the design
- Use DRC Pie chart by clicking into the DRC categories to get more granular DRC display
- The Pie chart works dynamically with Search table enabling user a way to click through and navigate DRCS
- User can also use filters in the search table to things like “show me all the DRC’s for a certain net on layer top”

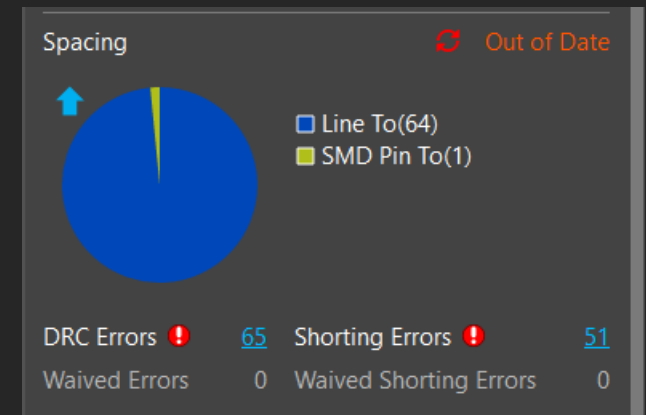
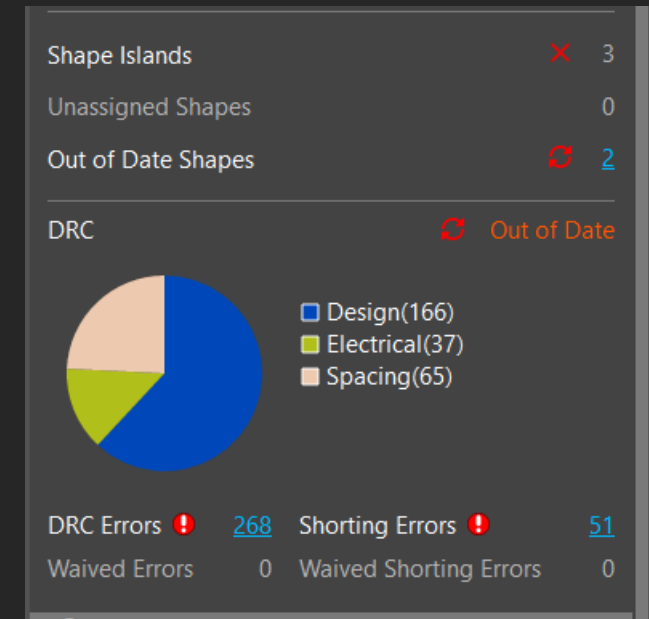
Search

Q Drc Errors

DRC (65)

CONSTRAINT	REQUIRED VALUE	ACTUAL VALUE	WAIVE DRC ST
Line to SMD Pin Spacing	0.2 MM	  	
Line to SMD Pin Spacing	0.2 MM		
Line to Line Spacing	0.2 MM		
Line to SMD Pin Spacing	0.2 MM		

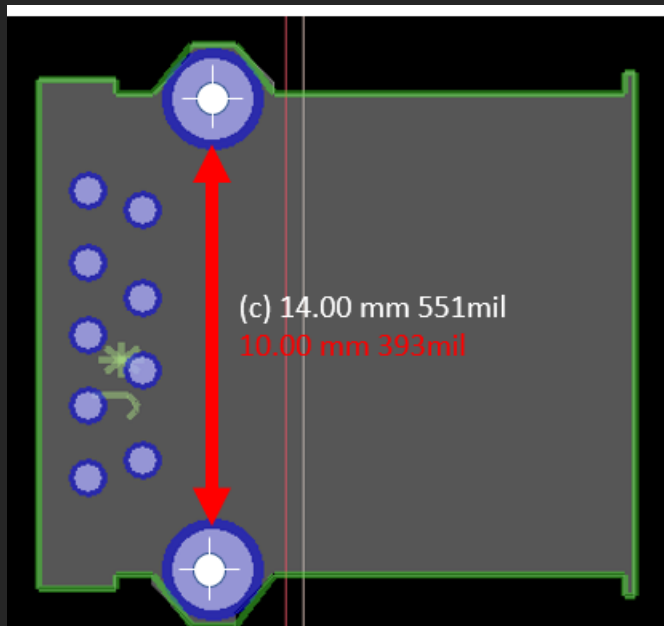
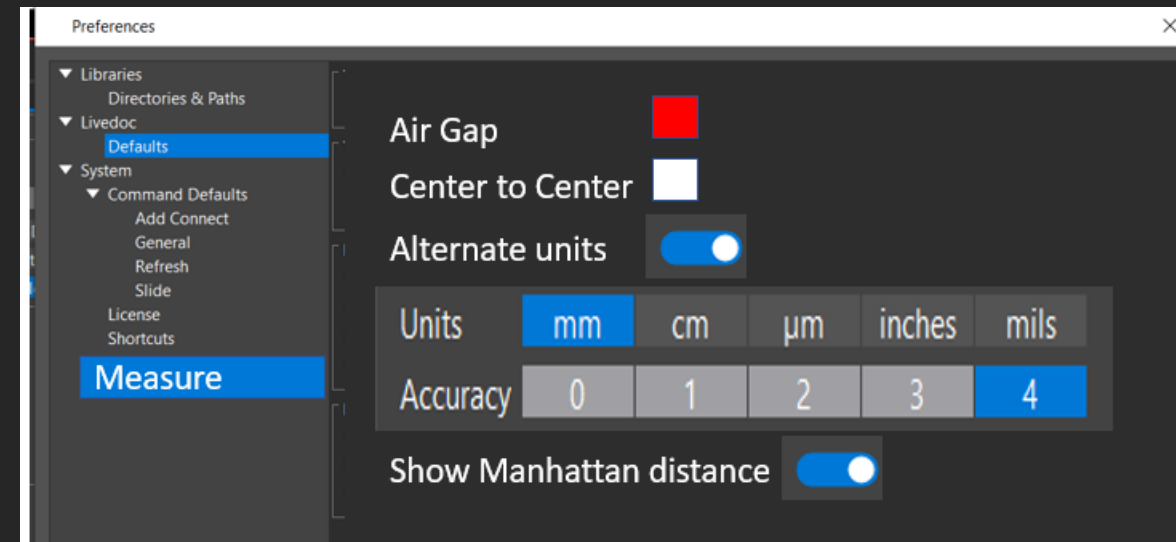
OK Cancel



Allegro X Integrated Layout Editor

Measure command

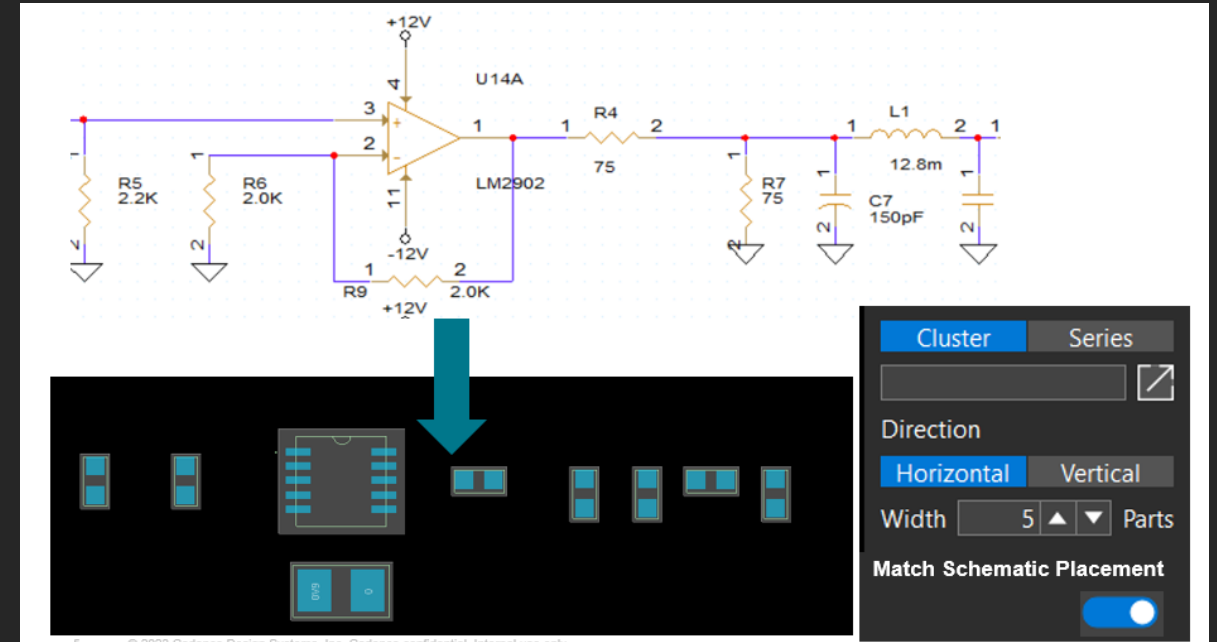
- Measure air gap
- Measure center to center
- Measure Manhattan
- Dual units



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PCB Placement

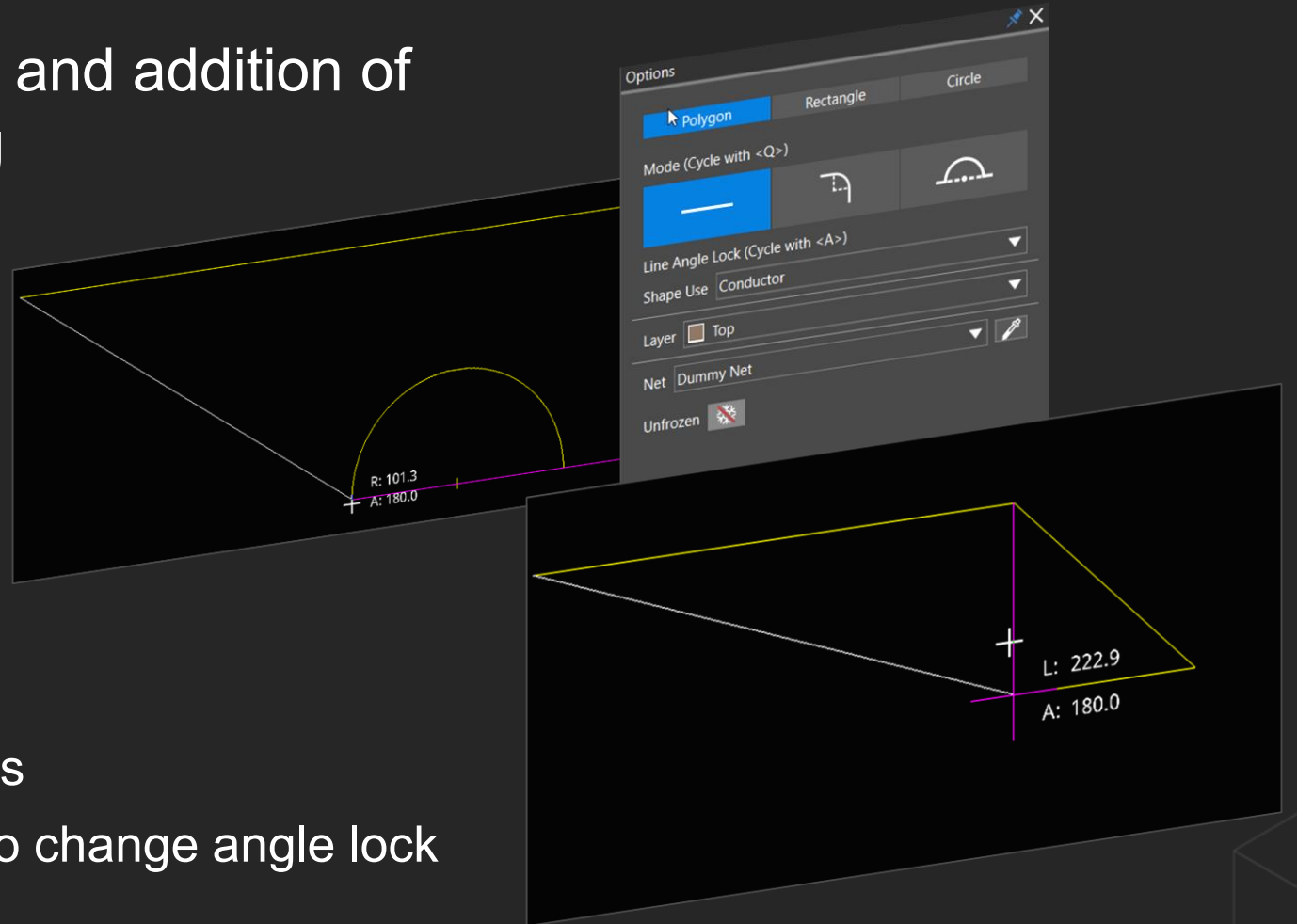
- Place groups of footprints based on:
 - Schematic window selection (Cross probe)
 - Presto search panel
- Benefits
 - Simplifies placement of multiple footprints
 - Removes the need of specifying a room and using quick place by room
 - Window selection in schematic maintains identical orientation in PCB layout – match schematic placement option
 - Especially helpful when placing analog circuitry



Allegro X Integrated Layout Editor

PCB Shape Creation

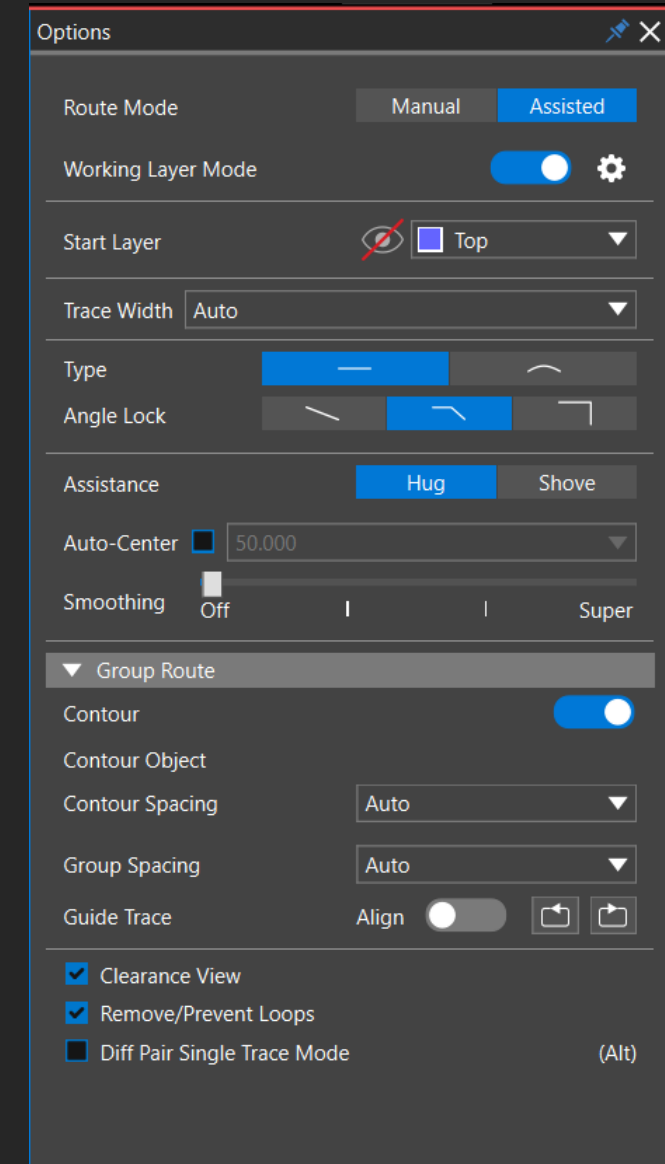
- Improvements to visual indicators and addition of hotkeys to simplify shape drawing
- Benefits
 - Heads up display
 - Length
 - Angle
 - Radius
 - Parallel segments
 - Vertex snapping
 - Change line/arc mode using shortcuts
 - Q to change drawing mode & A to change angle lock



Allegro X Integrated Layout Editor

PCB Routing

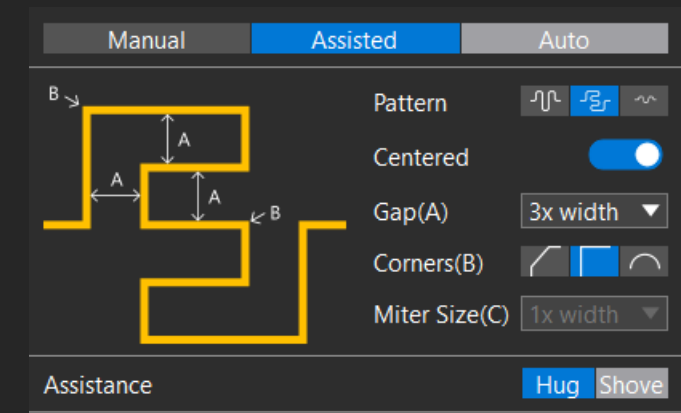
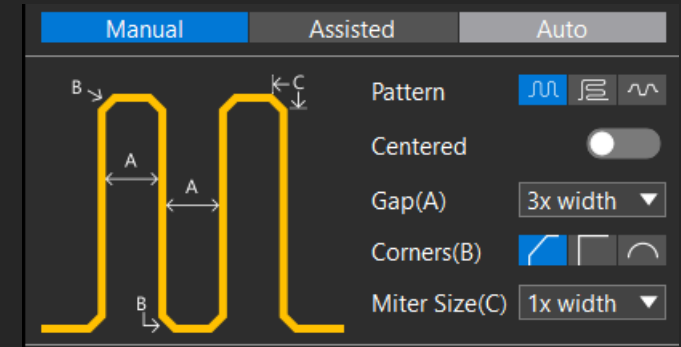
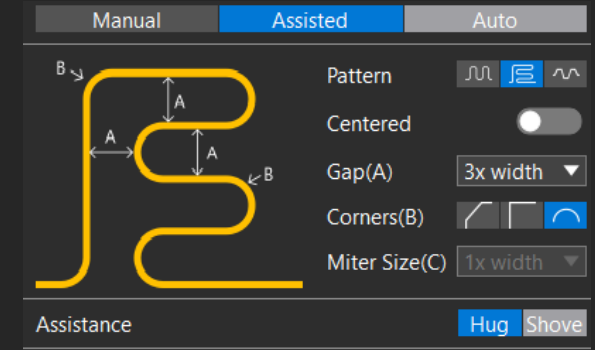
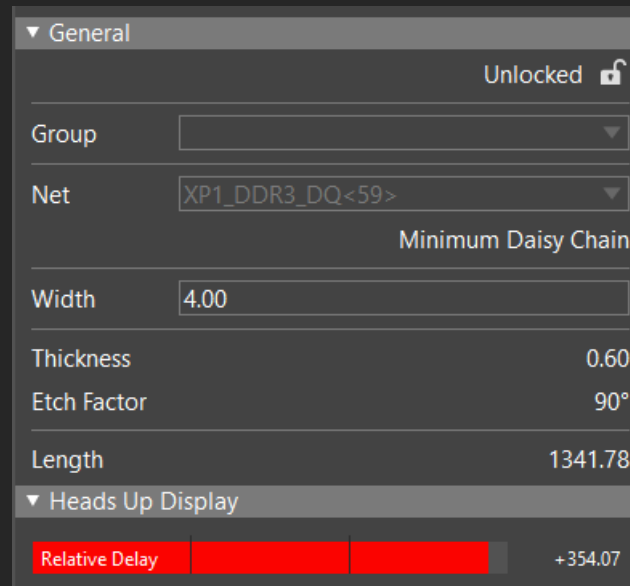
- Easily enable working layer mode for HDI routing
- Trace width can be set to
 - Auto (continue with existing line width)
 - Constraint
 - User entry
- Hug/Shove
- Auto Center
- Integrated contour route for flex
- Display of different visual aids



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PCB Timing – Delay Tuning

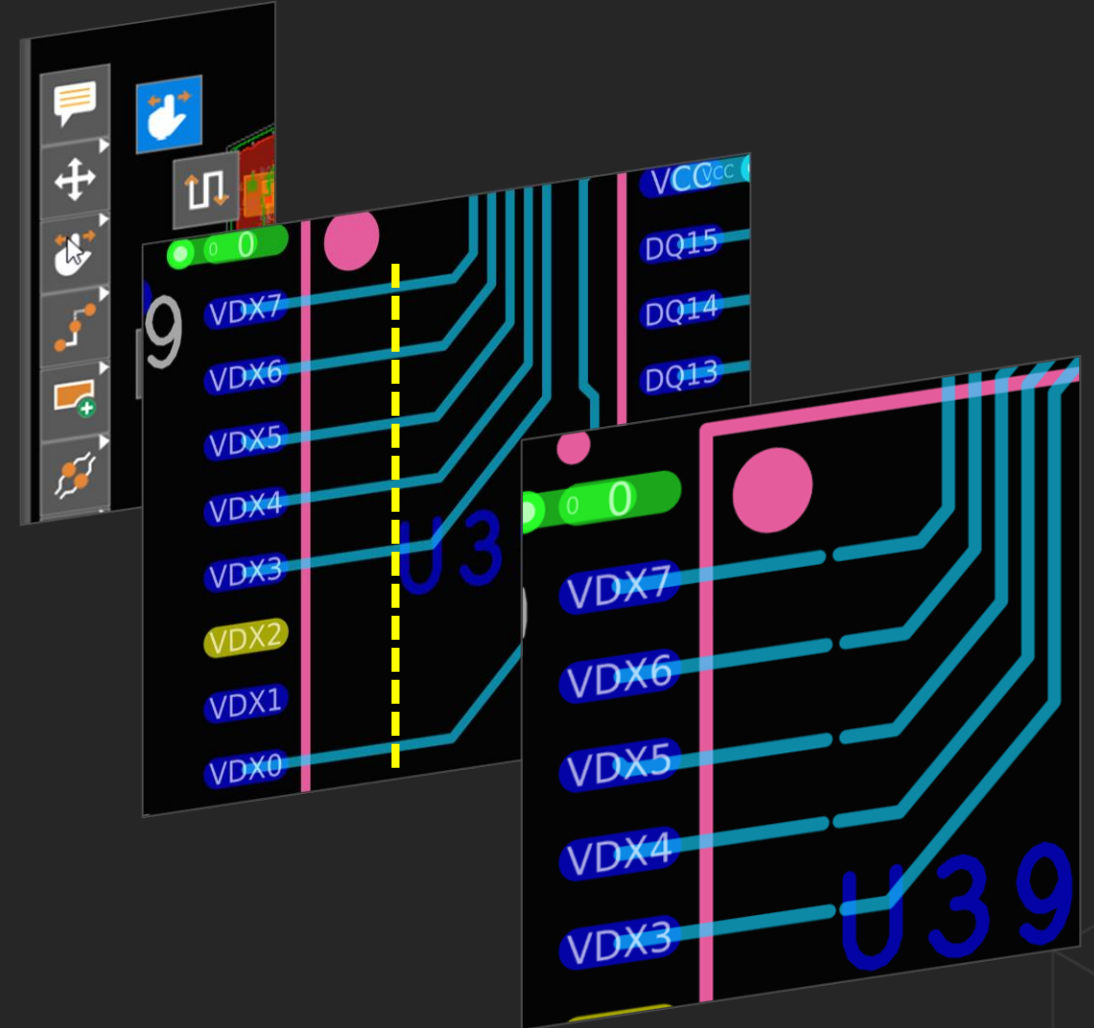
- Modern and easy UX
- 12 different tuning patterns
- Dynamic updating UI WYSIWYG
- Easily toggle Diff pair mode on/off
- Heads Up Display (HUD)



Allegro X Integrated Layout Editor

PCB Engineering Change – Slice

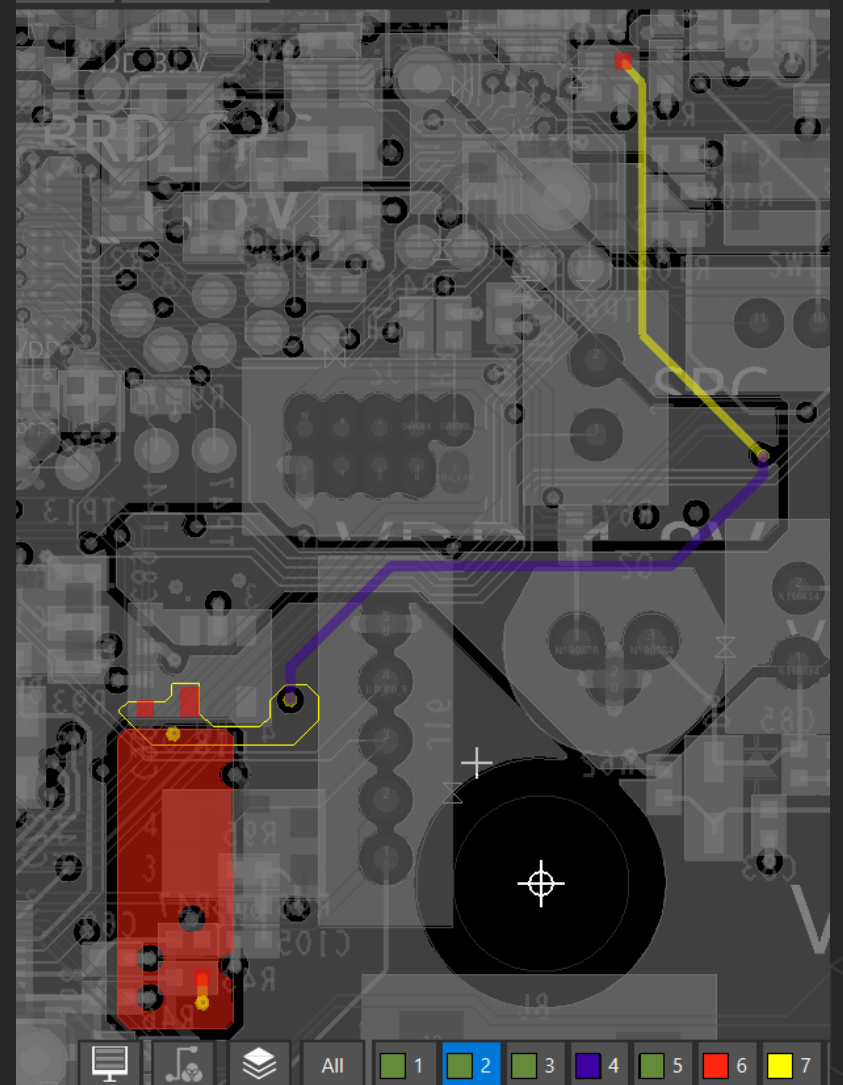
- Slice through existing routes to make it easier to move or edit routed designs or make reuse circuitry
- Benefits
 - Footprint replacements on an already routed board
 - Preserve existing routed area
 - Circuit area replacements
 - Ideal for design rework



Allegro X Integrated Layout Editor

PCB Layout Design Accelerators – Display

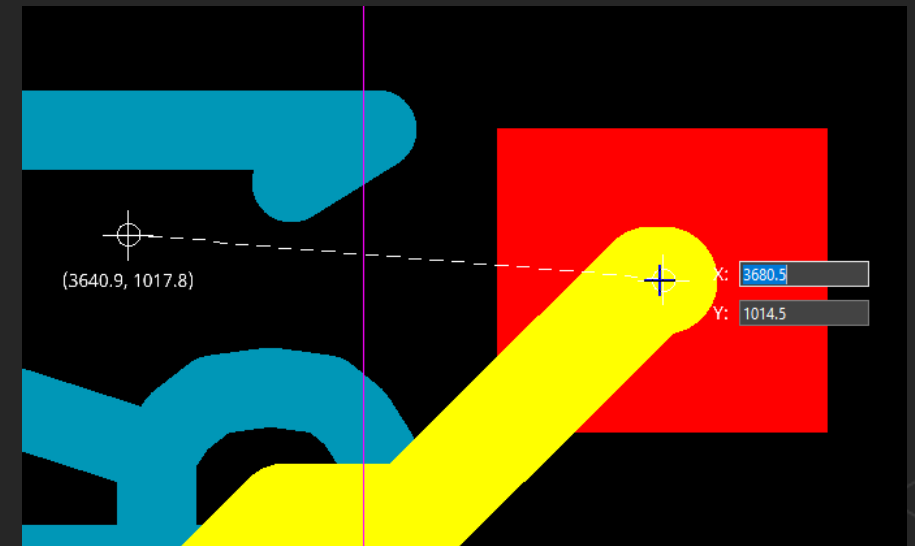
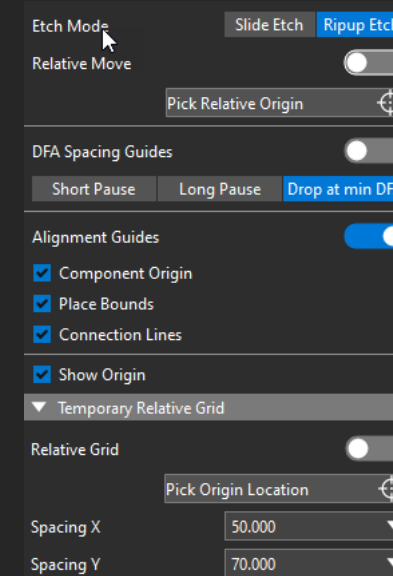
- Enhanced display and navigation of design objects
- Benefits
 - Ultra Shadow Mode
 - Makes selected objects stand out against all other objects making it easy to navigate nets
 - Net Colors On/Off
 - Enable or disable all custom net colors in a single click letting you navigate traces and shapes based on their layer color or their assigned net color
 - Both options are available from the floating visibility toolbar



Allegro X Integrated Layout Editor

PCB Layout Design Accelerators

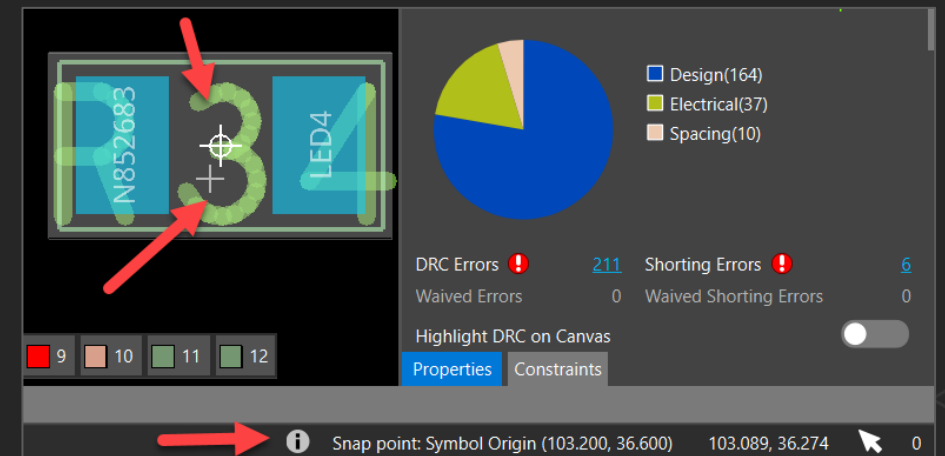
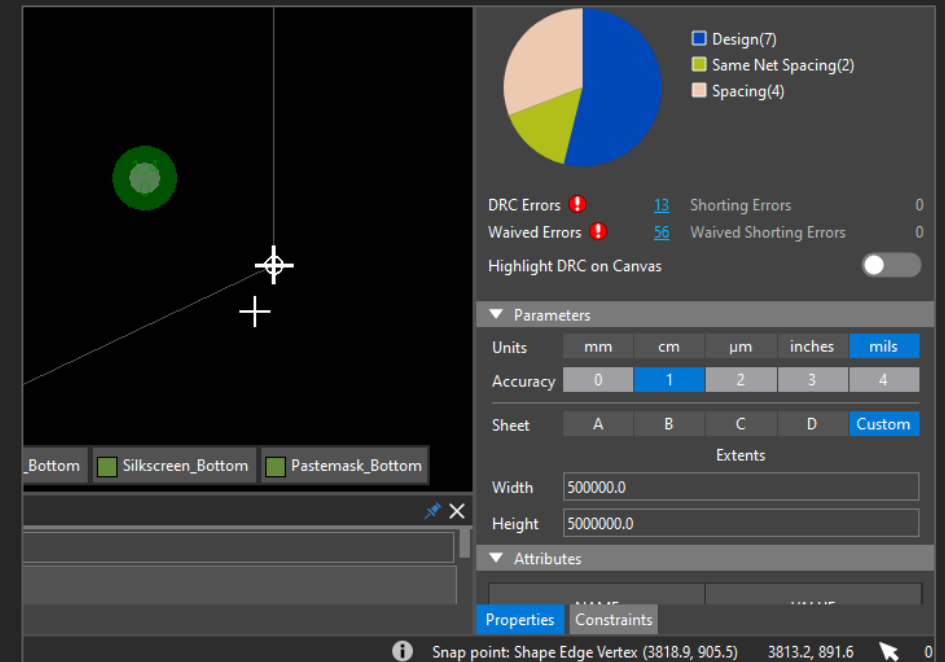
- Significant enhancements to footprint move command
- Benefits
 - Placing and moving parts is the 2nd most time-consuming part of PCB layout
 - Rip up or slide etch
 - Relative move or absolute location
 - Dynamic HUD showing the origin and new location
 - User entry of X Y location
 - Alignment guides and control
 - Temporary relative grid
 - Keyboard support (arrow keys, WASD)



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PCB Layout Design Accelerators

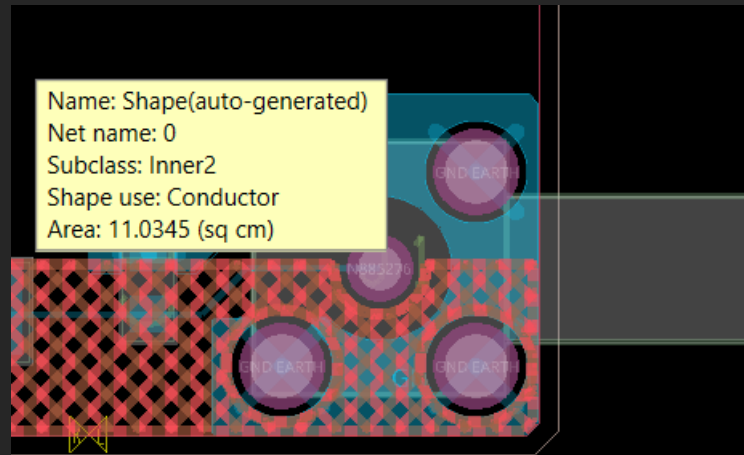
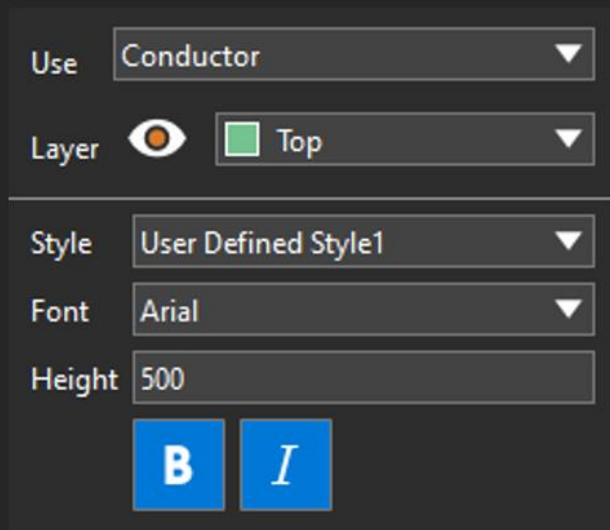
- Visual snap cursor and text readout of snap object
- Ideal for dense design areas with multiple objects
- Benefits
 - Indicates what you're going to pick up before you pick it
 - Snap cursor can be disabled



Allegro X Integrated Layout Editor

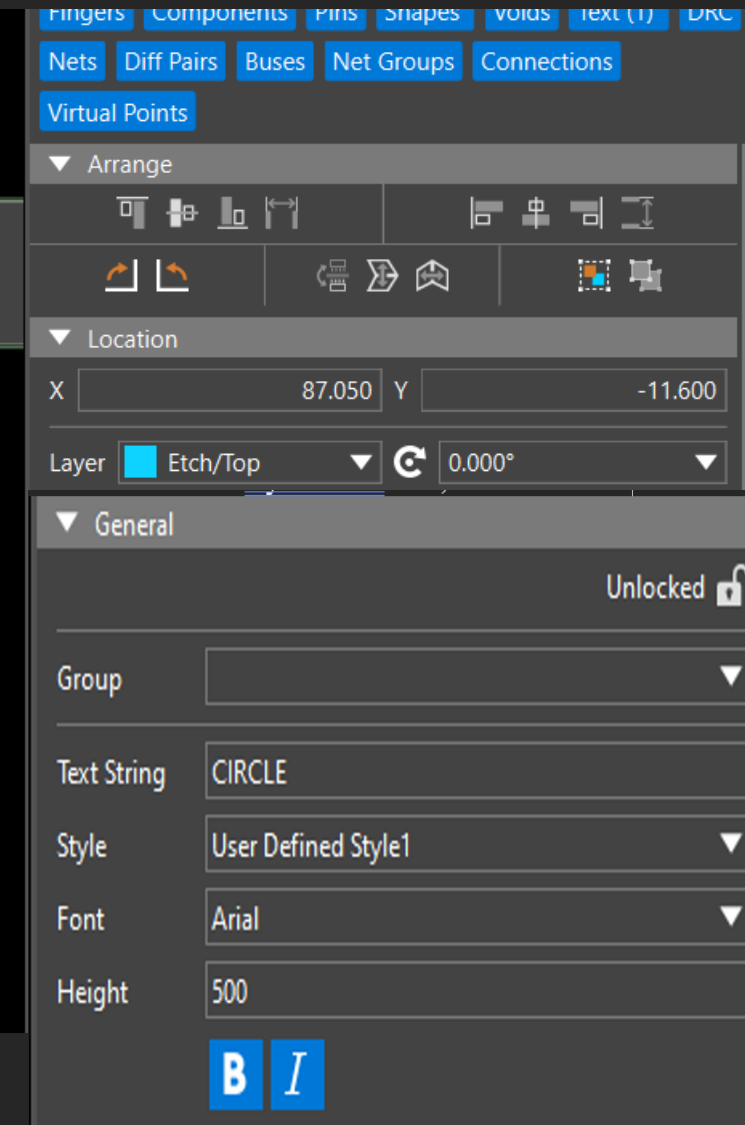
OpenType Font Support

- User can add fonts without any setup
- User can create “Styles” if they want to define certain fonts for specific usage
 - Silkscreen is Arial 10



Real Fonts in
Design

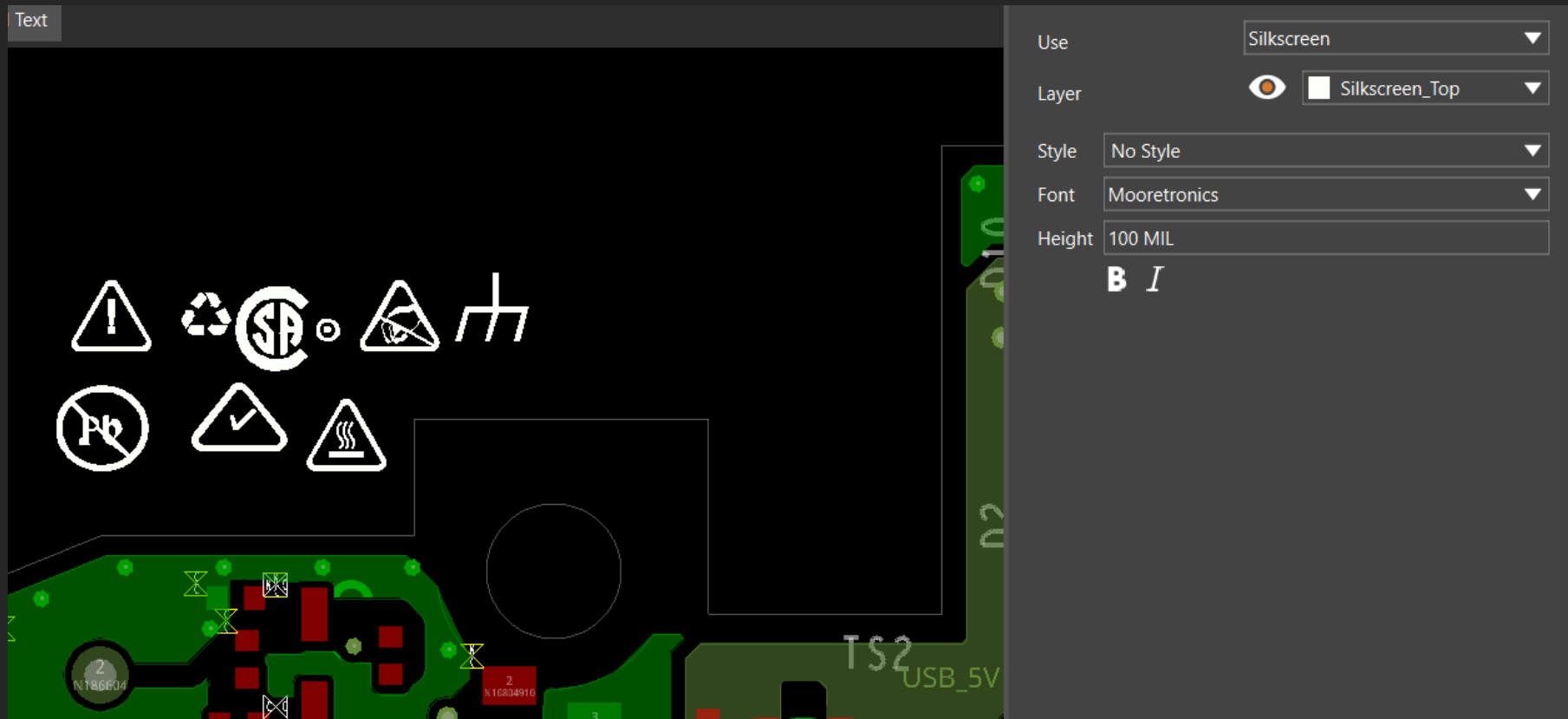
FLEXI_STIFFE



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PCB Symbol Font

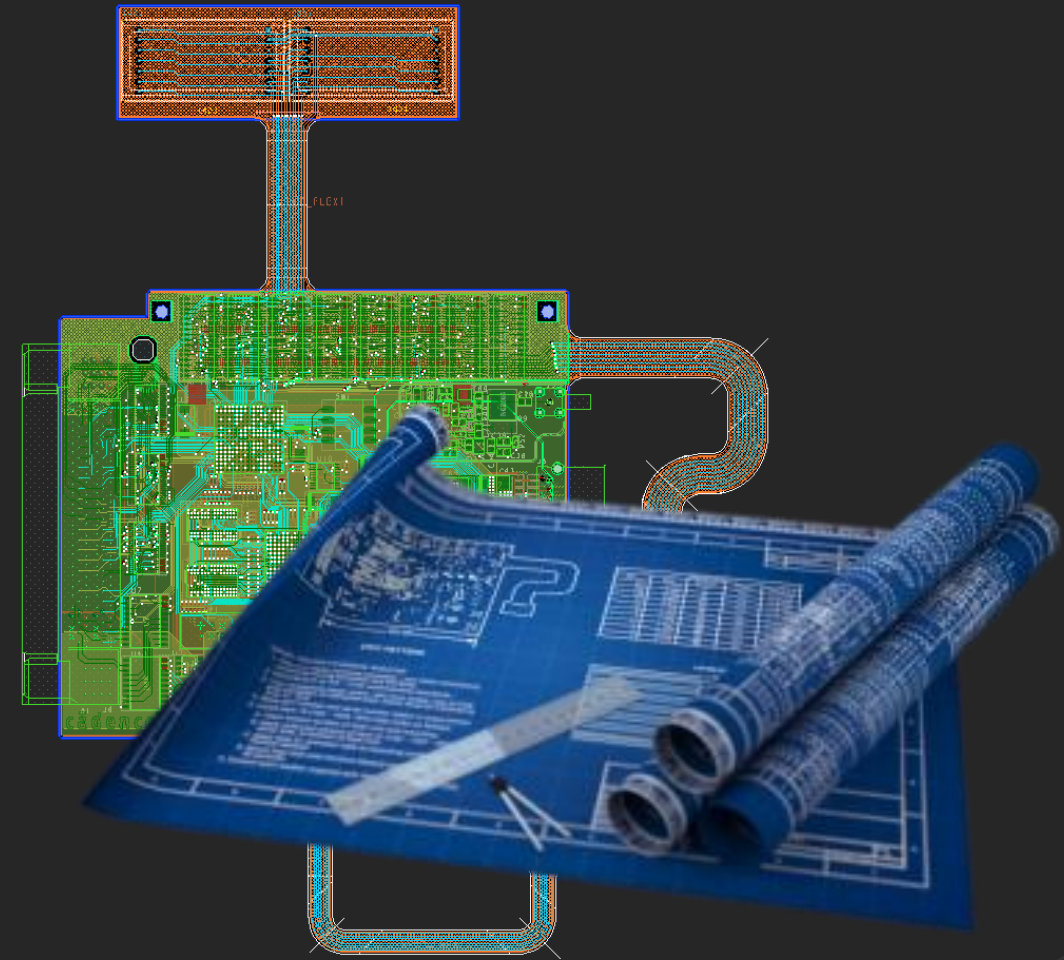
- Easily add common PCB symbols




Allegro X Integrated Layout Editor

LiveDOC

- Next generation fabrication and assembly documentation solution
- Template driven design enables speed & consistency
- Live linked to the PCB design
 - Dynamic updates to the documentation objects – move a component in PCB will automatically update the assembly and fabrication drawings
- Dimensioning, leader, note, and shape drawing capabilities
- Web enabled for future browser support





The background features a dark blue gradient with a faint hexagonal grid. In the upper left, a cluster of small white triangles forms a larger hexagonal shape. Scattered throughout are translucent cubes in various colors (cyan, blue, orange, red) and sizes, some with bright highlights. Mathematical formulas are visible on some of the grid cells: $F(s) = -e^{-sT} \left(\frac{\alpha}{s+\alpha} \right)$ appears on the left and right; $f_{in}(0) = 1 - e^{-\beta t}$ is on the top right; and $\Gamma = m_0 \sqrt{2m - m_0^2}$ is on the bottom right.

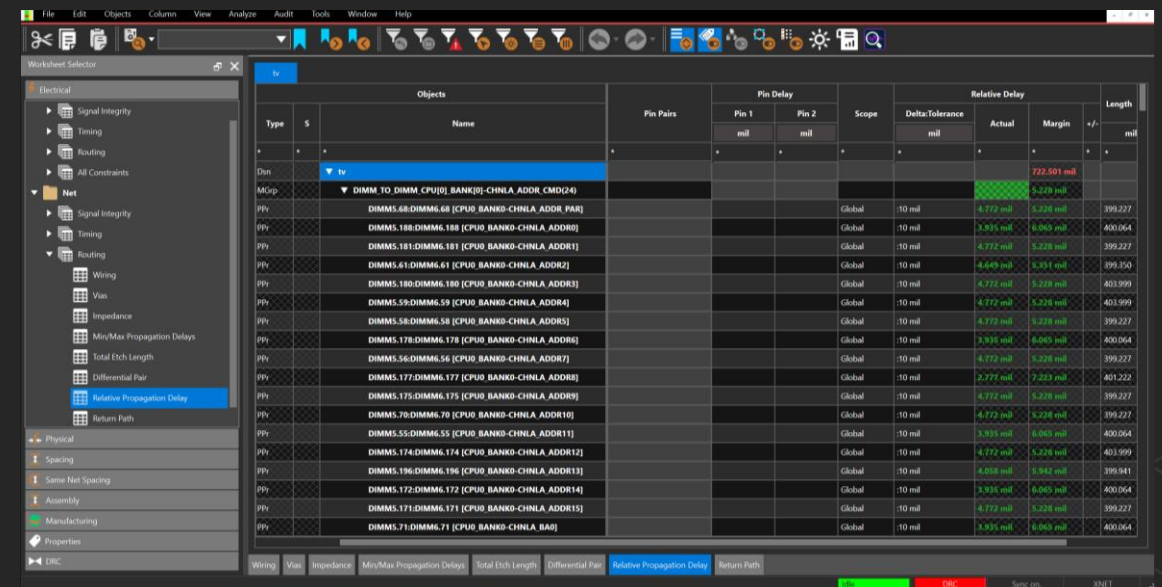
Constraint Panel

Gateway into Constraint Manager

Allegro X Integrated Layout Editor

Managing Constraints Today

- The Constraint Manager is primary “cockpit” for entry/modification/visualization of constraints
 - Covers Physical, Electrical, Spacing, Manufacturing rules, and their application in the design
 - Quite comprehensive and very useful for experienced users
- Adding Constraints is not easy and can be a time-consuming task
- Finding what you need to do/see is not easy or intuitive to start with
- Difficult for many users to know
 - Where to begin, or
 - How to effectively use it



The screenshot shows the Allegro X Constraint Manager interface. On the left is a 'Worksheet Selector' pane with a tree view containing categories like Electrical, Net, Physical, Spacing, Assembly, and Manufacturing. The 'Electrical' category is expanded, showing sub-items like Signal Integrity, Timing, Routing, and All Constraints. The 'Timing' sub-item is further expanded, showing 'Relative Propagation Delay' selected. The main area displays a table of constraints. The table has columns for Type, S, Name, Pin Pairs, Pin Delay (Pin 1, Pin 2), Scope, Delta/Tolerance, Relative Delay (Actual, Margin), and Length. The table lists various constraints related to DIMM signals, such as DIMM5.68: DIMM6.68 [CPU0_BANK0-CHNLA_ADDR_PAR], DIMM5.188: DIMM6.188 [CPU0_BANK0-CHNLA_ADDR0], and DIMM5.181: DIMM6.181 [CPU0_BANK0-CHNLA_ADDR1]. The table shows values for Pin Delay, Scope, Delta/Tolerance, Relative Delay (Actual, Margin), and Length. The bottom of the interface shows a status bar with various indicators and a 'Sync on' button.

Type	S	Name	Pin Pairs	Pin Delay		Scope	Delta/Tolerance	Relative Delay		Length
				Pin 1	Pin 2			Actual	Margin	
				mil	mil		mil			mil
Dn		tv								722.501 mil
Misc		DIMM5.68: DIMM6.68 [CPU0_BANK0-CHNLA_ADDR_PAR]				Global	10 mil	4.772 mil	5.228 mil	399.227
PPV		DIMM5.188: DIMM6.188 [CPU0_BANK0-CHNLA_ADDR0]				Global	10 mil	3.935 mil	6.065 mil	400.064
PPV		DIMM5.181: DIMM6.181 [CPU0_BANK0-CHNLA_ADDR1]				Global	10 mil	4.772 mil	5.228 mil	399.227
PPV		DIMM5.61: DIMM6.61 [CPU0_BANK0-CHNLA_ADDR2]				Global	10 mil	4.649 mil	5.351 mil	399.350
PPV		DIMM5.180: DIMM6.180 [CPU0_BANK0-CHNLA_ADDR3]				Global	10 mil	4.772 mil	5.228 mil	403.999
PPV		DIMM5.59: DIMM6.59 [CPU0_BANK0-CHNLA_ADDR4]				Global	10 mil	4.772 mil	5.228 mil	403.999
PPV		DIMM5.58: DIMM6.58 [CPU0_BANK0-CHNLA_ADDR5]				Global	10 mil	4.772 mil	5.228 mil	399.227
PPV		DIMM5.178: DIMM6.178 [CPU0_BANK0-CHNLA_ADDR6]				Global	10 mil	2.935 mil	6.065 mil	400.064
PPV		DIMM5.56: DIMM6.56 [CPU0_BANK0-CHNLA_ADDR7]				Global	10 mil	4.772 mil	5.228 mil	399.227
PPV		DIMM5.177: DIMM6.177 [CPU0_BANK0-CHNLA_ADDR8]				Global	10 mil	2.777 mil	7.223 mil	401.222
PPV		DIMM5.175: DIMM6.175 [CPU0_BANK0-CHNLA_ADDR9]				Global	10 mil	4.772 mil	5.228 mil	399.227
PPV		DIMM5.70: DIMM6.70 [CPU0_BANK0-CHNLA_ADDR10]				Global	10 mil	4.772 mil	5.228 mil	399.227
PPV		DIMM5.55: DIMM6.55 [CPU0_BANK0-CHNLA_ADDR11]				Global	10 mil	3.935 mil	6.065 mil	400.064
PPV		DIMM5.174: DIMM6.174 [CPU0_BANK0-CHNLA_ADDR12]				Global	10 mil	4.772 mil	5.228 mil	403.999
PPV		DIMM5.136: DIMM6.136 [CPU0_BANK0-CHNLA_ADDR13]				Global	10 mil	4.888 mil	5.112 mil	399.841
PPV		DIMM5.172: DIMM6.172 [CPU0_BANK0-CHNLA_ADDR14]				Global	10 mil	3.935 mil	6.065 mil	400.064
PPV		DIMM5.171: DIMM6.171 [CPU0_BANK0-CHNLA_ADDR15]				Global	10 mil	4.772 mil	5.228 mil	399.227
PPV		DIMM5.71: DIMM6.71 [CPU0_BANK0-CHNLA_ADDR16]				Global	10 mil	3.935 mil	6.065 mil	400.064

Allegro X Integrated Layout Editor

Constraint Panel – Problem Statement

- How do we help the user
 - Quickly define Default Constraint Sets
 - Modify Existing Constraint Sets
 - Assign and Visualize Constraints Sets for design objects
 - Create Abstract associations of objects for constraining (NetGroups, MatchGroups etc.)
 - Ensure constraint resolution is complete and concise.
- These operations can involve a high level of complexity due to the constraint object hierarchy.
- Today, all of this is done through Constraint Manager
 - Visualization of constraints on an object can be “partially” done using Show Element

Table 1-1 Constraint Object Hierarchy

	Electrical	Physical	Spacing (net-to-net / same-net)
	-----	Design	Design
	Net Class	Net Class	Net Class
	Net Group	Net Group	Net Group
	Bus	Bus	Bus
	Differential Pair	Differential Pair	Differential Pair
	Match/Relative Group	-----	-----
	Xnet	Xnet	Xnet
	Net	Net	Net
	Pin Pair	Pin Pair	Pin Pair
	-----	-----	Net Class-Class *
	-----	Region	Region
	-----	Region Class	Region Class
	-----	-----	Region Class-Class *

* Not available in the Same Net Spacing domain

Allegro X Integrated Layout Editor

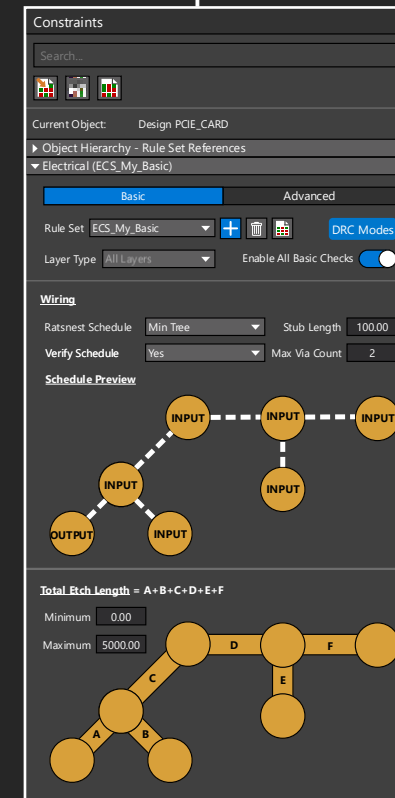
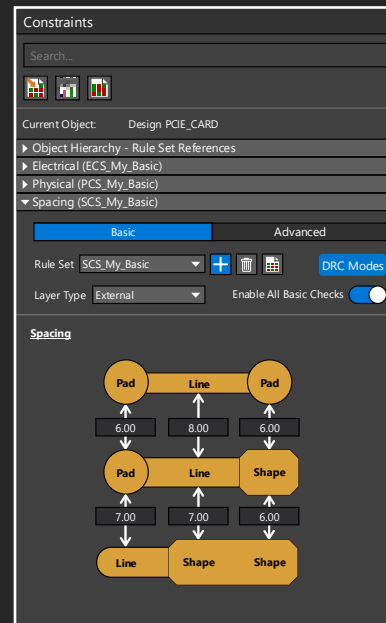
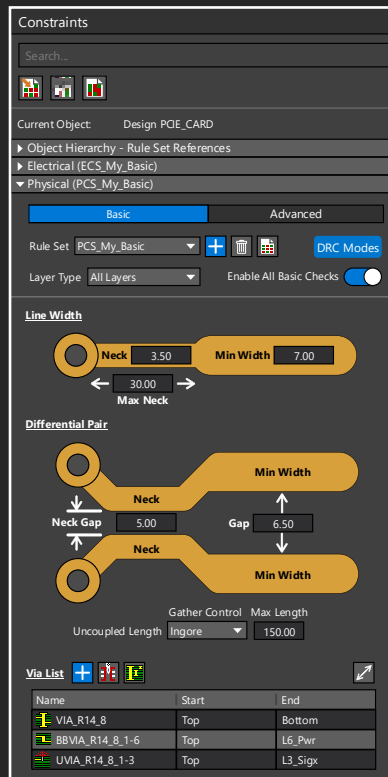
Constraint Panel – Overview

- Goal of Constraint Panel is to provide a gateway to managing Constraints without opening Constraint Manager, it is not a replacement
- Leverage Constraint Manager methodology / functionality but not make any major changes to Constraint Manager itself, but with a couple of exceptions
 - Integration of cross-domain constraints into Physical Rule Set accordion
 - Diff Pair Phase rules in Electrical domain will be available in Physical accordion
 - Integration of Drawing level properties that influence constraints into Spacing Rule Set accordion
 - **BBVIA_SEPARATION** value controls layer separation for **Min BB Via Gap** check
 - The goal is to prevent the user from jumping between different areas of the tool to update related constraints – it should all be in one place
- Constraint reuse interface will be available under Constraint Panel for quick import into design
 - Technology File and Allegro Constraint Compiler Imports

Allegro X Integrated Layout Editor

Constraint Panel – Gateway into Constraint Manager

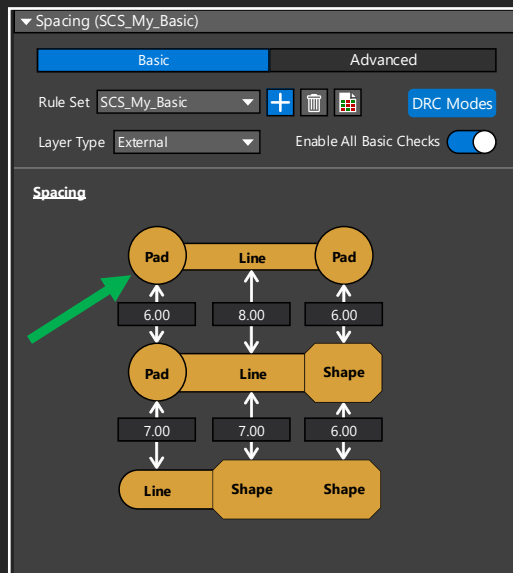
- New Constraint Panel offers a streamlined and intuitive way to manage design constraints directly within layout canvas (Physical, Spacing, Electrical)
 - Access to all existing Constraints Sets with the ability to create new Constraint Set as required



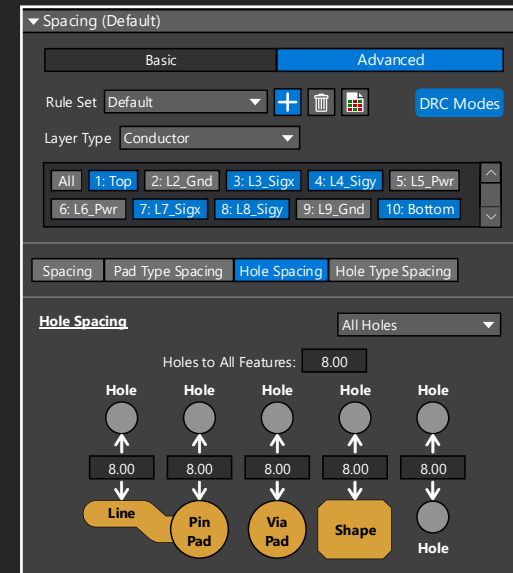
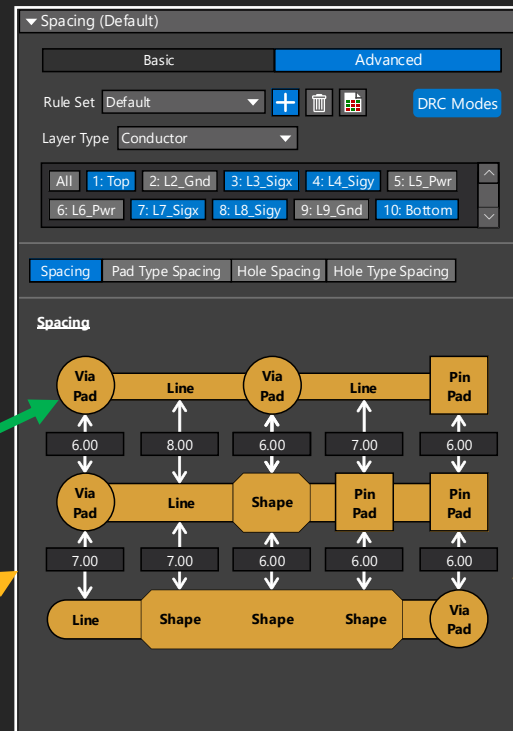
Allegro X Integrated Layout Editor

Constraint Panel – Gateway into Constraint Manager

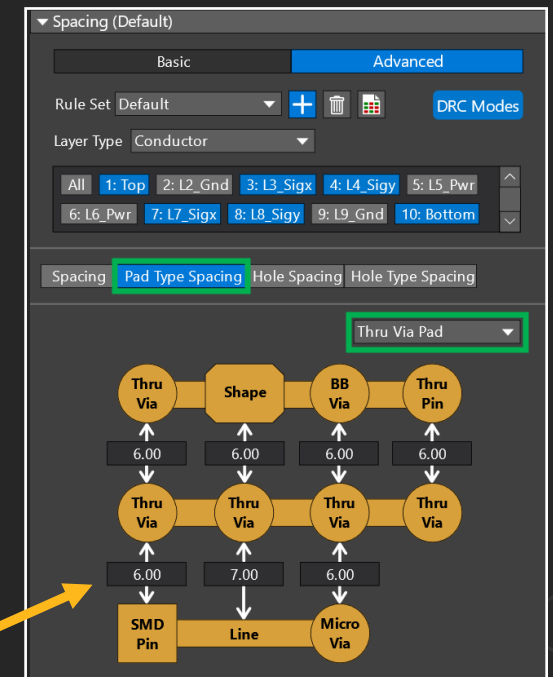
- Enter values on hierarchal object to seed value at lower levels
 - Basic and Advanced slider expands to show more detailed Spacing rules
 - Navigate to lower levels only when exceptions are required



Basic Pad values seeds Advanced Spacing Via Pad and Pin Pad values



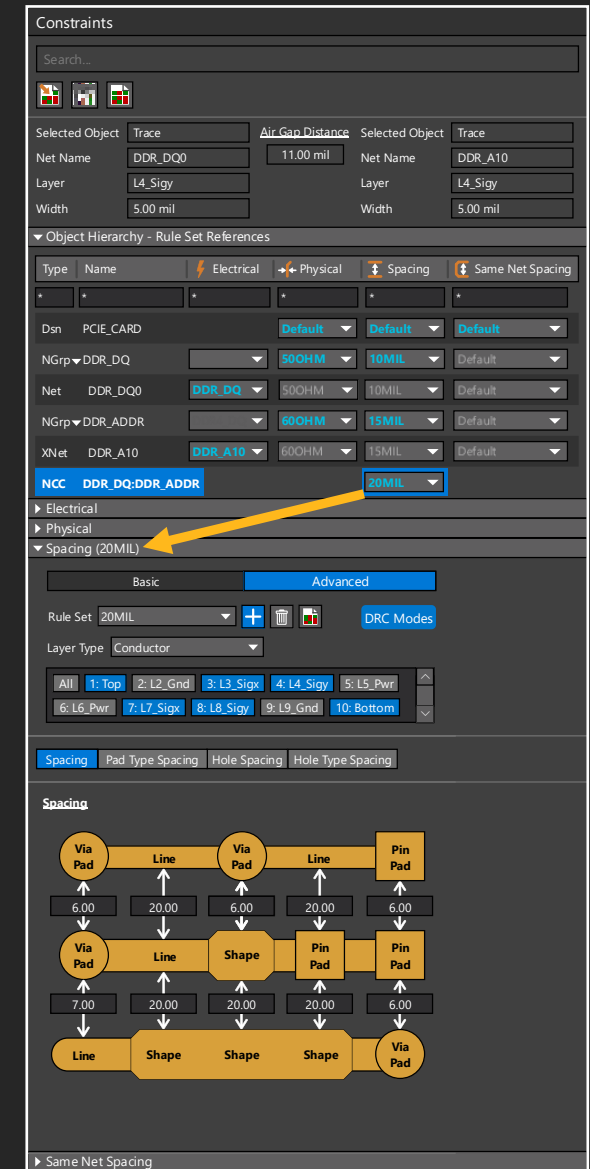
Advanced Spacing Via Pad value seeds Thru Via, BB Via and uVia under Pad Type Spacing to expand value entry



Allegro X Integrated Layout Editor

Constraint Panel – Gateway into Constraint Manager

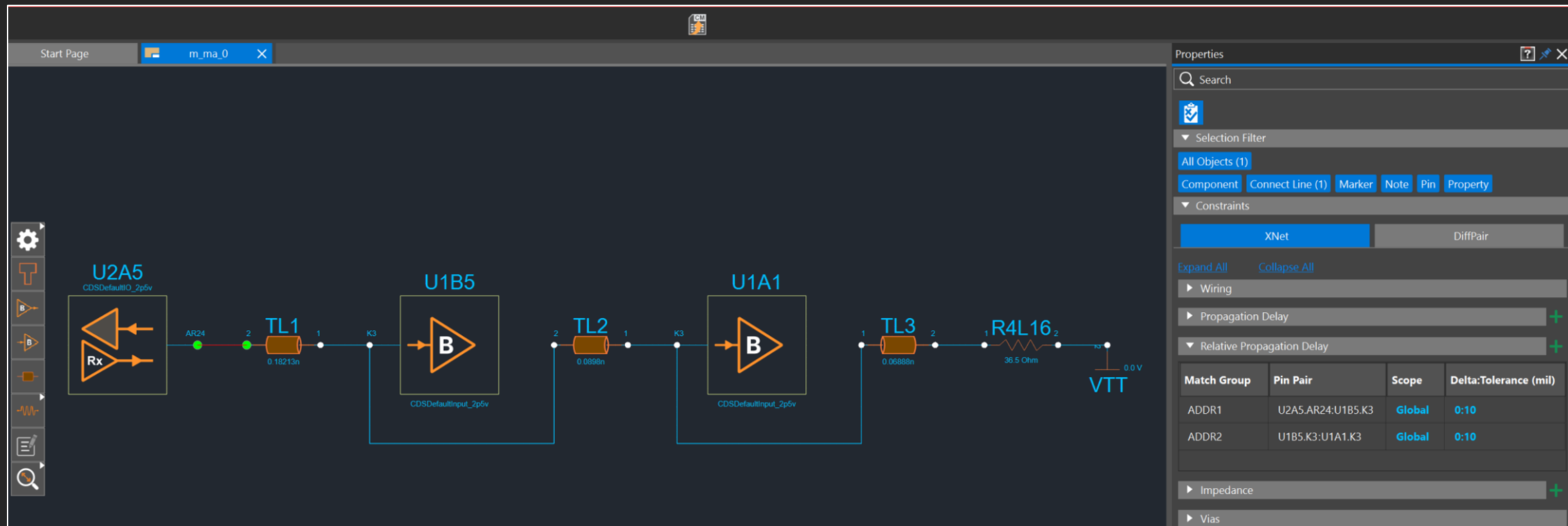
- Select object(s) on canvas to display resolved constraints with associated Constraint Set assignment
 - Constraint Sets can be added at many levels, but it is important to understand the highest level will influence results on canvas
 - Focus on controlling constraints at an abstract level, instead of Net level, by assigning Constraint Sets to hierarchal groups (Net Group, Net Class, Diff Pair)
- Row and Constraint Set will be highlighted indicating resolved constraints with Constraint Sets driving rules activated under each domain for quick reference
 - Adjust Constraint Set or create a new Constraints Set for assignment
- Everything at your fingertips without opening Constraint Manager



Allegro X Integrated Layout Editor

Topology Workbench – Topology-based Constraints

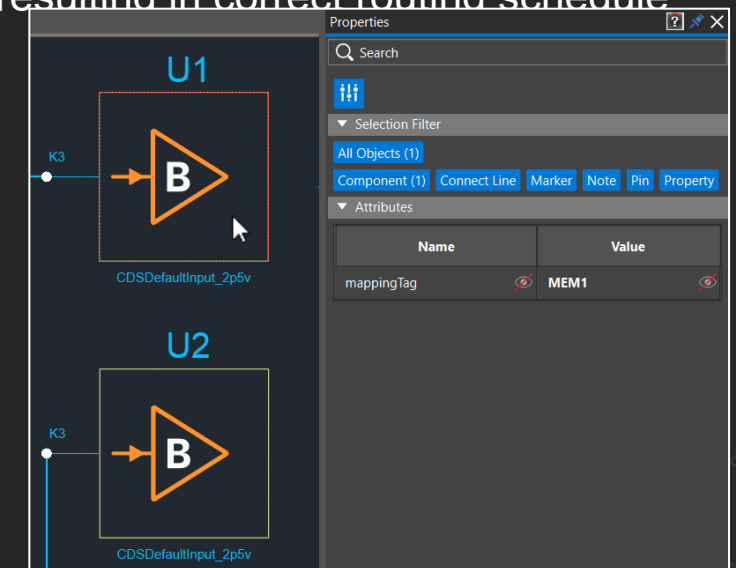
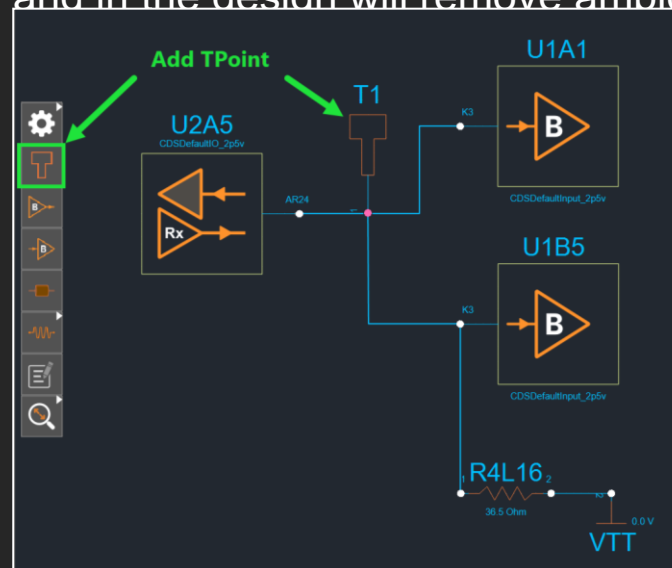
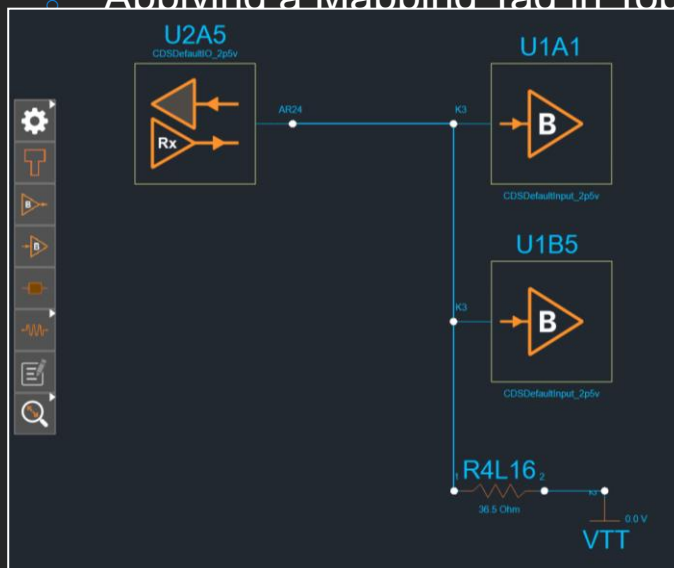
- Signal Explorer (SigXP) has been used to generate topology-based constraints, but we now have a next-generation topology editor called **Topology Workbench**
 - Topology Workbench offers similar functionality to SigXP, with an improved UI and a simpler use model
 - Re-schedule Net, drive constraints globally across the Net or create Pin Pair based constraints



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Topology Workbench – Topology-based Constraints

- Ideal Transmission Lines (TL*) are no longer required for Electrical CSet Topologies
 - **RMB > Delete all Connections** on canvas will delete all T-Lines so pins can be easily rearranged / reconnected
- New T-Point symbol can be placed to form a branch point to split route to different pins
 - Allows matching rules to be applied from T-Point to each component pin.
- Ambiguous pins, pins with same Pin Use, may not produce correct schedule order when applied
 - Applying a Mapping Tag in Topology and in the design will remove ambiguity resulting in correct routing schedule





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