

**Digital DDS–IF–ADC Relationships
In
Polyphase VHF IF Receivers
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Abstract

This paper describes the relationship between the direct-digital-synthesizer (DDS) frequency word, the intermediate-frequency (IF) placement at the analog-to-digital converter (ADC), and the resulting mapping into a polyphase channelizer used in modern digital IF receivers. The DDS tuning word establishes the local-oscillator (LO) frequency, which determines the IF center and the spectral location of incoming signals at the ADC input.

The ADC samples the IF spectrum into a discrete-time representation, and the polyphase channelizer partitions it into uniformly spaced sub-bands suitable for instantaneous-frequency measurement (IFM) and angle-of-arrival (AOA) processing. This paper expands upon the architecture presented in *Polyphase VHF IF Receiver* by detailing the signal-flow mechanics that link DDS tuning to digital frequency estimation and phase-based parameter generation.

1. Introduction

Modern digital IF receivers rely on deterministic signal-flow relationships between the LO tuning source, the IF band, the ADC sampling process, and the polyphase channelizer. The companion paper, *Polyphase VHF IF Receiver*, describes the channelizer and the digital IFM/AOA processor. This document focuses on the preceding stages, explaining how the DDS frequency word defines the IF placement and how that placement propagates through the digital processor.

The goal is to provide a clear, engineering-formal description of the DDS→LO→IF→ADC→polyphase chain that underpins digital IFM and AOA processing.

2. DDS Frequency Word and LO Tuning

The DDS frequency word sets the LO frequency for each RF-to-IF down-conversion path. The LO frequency establishes the center of the IF band, typically 170–310 MHz in the architectures derived from Goodwin's NRL-8005 geometry.

The DDS tuning word provides: deterministic LO frequency placement, fine-tuning resolution, stable phase continuity, and predictable IF center frequency. In the block diagram, the DDS word appears explicitly.

3. IF Placement in the Analog Front End

Each antenna path includes amplification, filtering, and down-conversion to the established IF band. As stated in the companion paper: Each antenna feeds an RF path that includes amplification, filtering, and down-conversion to the established 170 to 310 MHz IF band.

The LO frequency determines where the incoming RF signal lands within this IF band. Any change in the DDS word shifts the IF placement, and therefore shifts the spectral location of the tone at the ADC input. This IF placement is critical because it defines the digital frequency that the channelizer will later resolve.

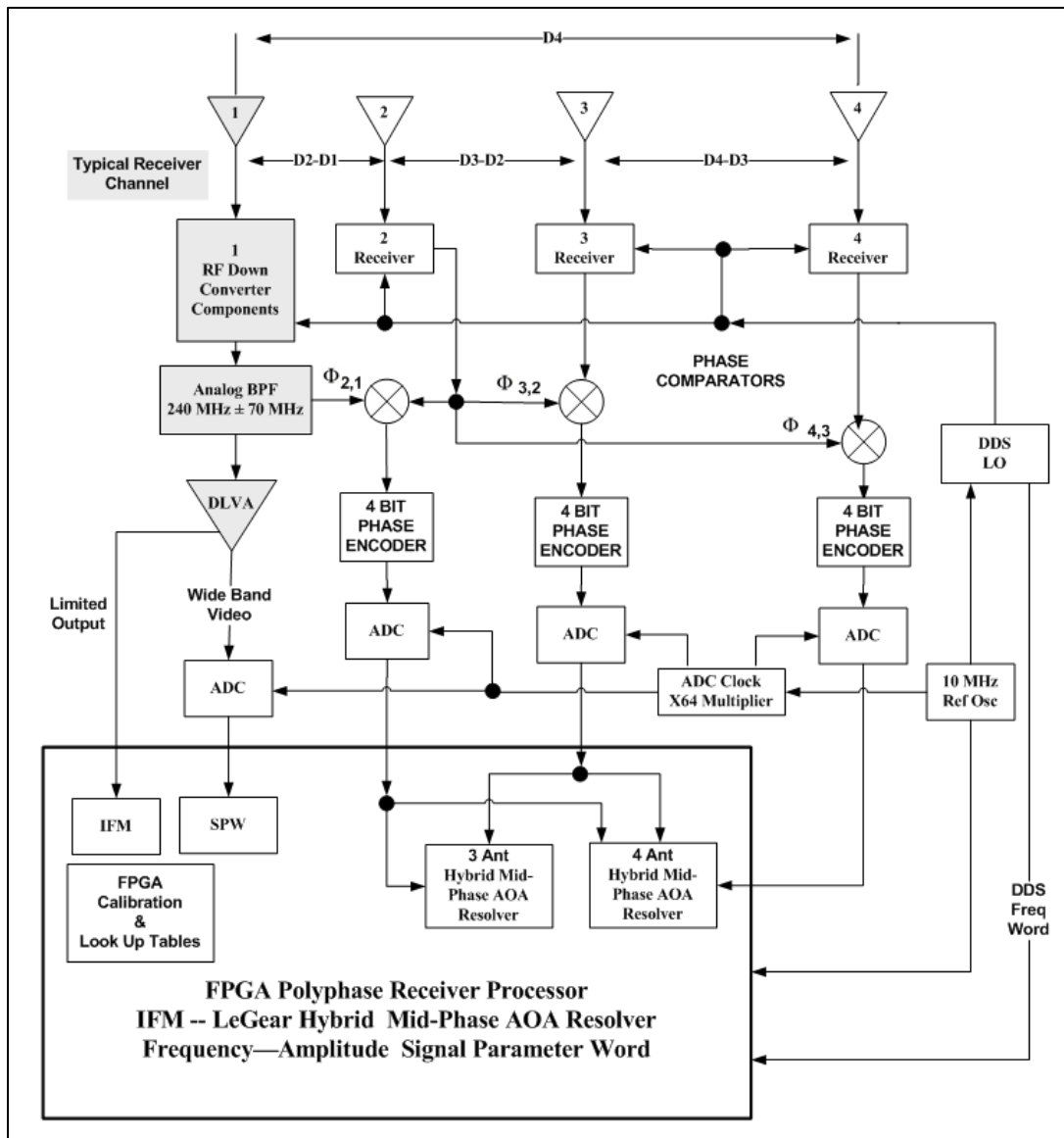


Figure 1. DDS-IF-ADC Signal Path Feeding the Polyphase Channelizer

The DDS frequency word establishes the LO tuning, which defines IF placement at the ADC input. The ADC digitizes the IF spectrum, and the polyphase channelizer partitions it into sub-bands used by the digital IFM/AOA processor. This diagram links the analog front end to the digital architecture described in this paper.

4. ADC Sampling and IF Digitization

After down-conversion, each channel's IF signal is digitized:

Each of the four RF-to-IF channels uses a phase detector whose output is digitized through a 4-bit encoder and delivered to an analog-to-digital converter.

The ADC sampling rate determines: the width of the digital Nyquist band, the mapping of IF frequencies into discrete-time spectral locations, the resolution of the channelizer bins. The ADC converts the analog IF spectrum into a discrete-time sequence that the polyphase channelizer can process deterministically.

5. Polyphase Channelizer Mapping

The polyphase channelizer partitions the ADC spectrum into uniformly spaced sub-bands:

The channelizer front end employs a three-channel polyphase filter bank derived from a prototype FIR design, producing uniformly spaced sub-bands with well-defined passband and stopband characteristics.

The IF tone's location within the ADC spectrum determines: which channelizer bin receives the dominant energy, the magnitude ratios used by the discriminator, the inter-channel phase offsets used by the resolver. Thus, the DDS tuning word indirectly determines the bin index and the magnitude/phase relationships that the digital processor interprets.

6. Relationship to θ -Domain Processing

The companion paper describes how the processor maps channelizer outputs to an internal parameter θ :

Frequency estimation uses a polynomial discriminator that maps channel magnitude ratios to an internal parameter θ . AOA estimation uses a resolver polynomial that maps measured inter-channel phase offsets to the same parameter.

The DDS word anchors this θ -domain interpretation by defining the IF placement that produces the magnitude and phase relationships the channelizer observes.

The chain is: DDS word $\rightarrow$ LO frequency $\rightarrow$ IF placement $\rightarrow$ ADC spectrum $\rightarrow$ channelizer bins $\rightarrow$ θ -domain mapping. This deterministic relationship allows the processor to report frequency and AOA within a unified framework.

Practical Implementation Notes

Several practical considerations influence the DDS→IF→ADC→polyphase chain.

DDS resolution determines LO tuning granularity, **LO stability** affects IF placement accuracy, **ADC clock stability** affects digital frequency mapping, **Channelizer bin spacing** determines frequency resolution, and **deterministic FPGA timing** ensures repeatable processing.

8. Relationship to the First Paper

This document expands the architecture presented in Polyphase VHF IF Receiver by explaining the mechanics that precede the channelizer. The first paper describes the channelizer, discriminator, resolver, and Monte-Carlo behavior. This paper provides the missing link: how the DDS tuning word defines the IF placement that the digital processor ultimately interprets.

9. Conclusion

The DDS frequency word establishes the LO frequency, which determines the IF placement at the ADC input. The ADC sampling process maps that IF placement into a discrete-time spectrum, and the polyphase channelizer partitions that spectrum into uniformly spaced sub-bands. The digital processor interprets these sub-bands through polynomial discriminator and resolver functions that map magnitude and phase relationships to an internal parameter θ . This deterministic DDS→IF→ADC→polyphase→ θ chain underpins modern digital IF receivers and provides the stability, repeatability, and long-term accuracy required for wideband IFM and AOA processing across the entire operating band.

Summary

This paper walked through the complete signal-flow chain linking the DDS tuning word to the digital IFM/AOA processor. The reader has just seen how the DDS establishes the LO frequency, how that LO determines the IF placement, and how the ADC converts that IF spectrum into a stable digital sequence. The polyphase channelizer then organizes that sequence into evenly spaced sub-bands that preserve amplitude and phase relationships across channels. These steps form the deterministic foundation that allows the processor to extract frequency and angle-of-arrival parameters with repeatable behavior.

ADC Slope Adjustment Over Frequency

In modern digital IF receivers, the ADC operates on a fixed, normalized input domain. The hybrid mid-phase values entering the FPGA are dimensionless and digitally normalized, so no frequency-dependent slope adjustment is required. The ADC input range remains constant across the operating band, and the FPGA processes the channelizer outputs directly without applying any analog-derived scale factors. This digital normalization ensures stable behavior across frequency and eliminates the analog slope-protection mechanisms used in earlier architectures.

FPGA Programming Perspective

The FPGA is programmed to carry out the digital operations described in this paper. It applies the required scaling to the ADC data, performs the polyphase channelization, and executes the processing steps that generate the internal parameter used for frequency and angle-of-arrival reporting. These functions are implemented in logic so the system operates continuously and in real time. The specific coding methods used to build these functions are outside the scope of this document, but the FPGA executes them exactly as outlined in the signal-flow description.

Processor Summary (Plain-Language Listing)

- 1. The DDS sets the tuning.** The DDS frequency word tells the local oscillator what frequency to generate, which determines where the incoming RF signal will land in the IF band.
- 2. The analog front end shifts RF into the IF band.** Each antenna path amplifies, filters, and mixes the RF signal down to the 170–310 MHz IF range. The LO frequency set by the DDS defines the exact IF placement.
- 3. The ADC digitizes the IF signal.** The ADC samples the IF waveform at a fixed clock rate, converting the analog IF spectrum into a digital sequence for processing.
- 4. The polyphase channelizer divides the IF into sub-bands.** The channelizer splits the wide IF band into three stable, evenly spaced digital sub-bands while preserving amplitude and phase relationships between channels.
- 5. The processor locates the signal energy.** It examines the channelizer outputs to determine which sub-band contains the dominant energy, giving the initial frequency location.
- 6. The discriminator refines the frequency estimate.** By comparing the magnitudes of the three channelizer outputs, the discriminator maps those ratios to an internal parameter θ , which corresponds to the IF frequency.
- 7. The resolver interprets phase differences.** The resolver uses the inter-channel phase offsets to produce the same internal parameter θ , which corresponds to the angle-of-arrival.
- 8. Both frequency and AOA come from the same parameter.** Because both functions produce θ , the processor reports frequency and angle-of-arrival within a unified, deterministic framework.
- 9. The DDS word anchors the entire chain.** Changing the DDS word shifts the LO, which shifts the IF placement, which shifts the ADC spectrum, which shifts the channelizer bins, which changes θ .

Sidebar: Origin of the Term “LeGear Hybrid Processor”

The term *LeGear Hybrid Processor* acknowledges the concept's historical origin. Earlier work by LeGear showed that magnitude-based frequency information and phase-based angle-of-arrival information could be represented by a single internal parameter. That idea provided the conceptual starting point for architectures that unify these two observables in a single processing chain.

Modern digital receivers implement this unification in FPGA logic, where the magnitude discriminator and phase resolver operate on the same polyphase channelizer outputs and produce the same internal parameter. This combined interpretation is what makes the architecture “hybrid.” The LeGear reference simply recognizes where the idea first appeared; the processor described in this paper is an independent design built around a deterministic $\text{DDS} \rightarrow \text{IF} \rightarrow \text{ADC} \rightarrow \text{polyphase} \rightarrow \theta$ signal-flow chain.