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We are excited to bring to you the launch issue of **Fab Engineering & Operations magazine** – the only magazine for the engineers and managers of the mainstream fabrication plants!

We hope that you will enjoy the first issue of what will become a quarterly digital publication. Remember, this magazine is for you, so any comment is a good comment – we would very much like your feedback and to know what it is that you like and what else you would like us to cover. Our goal is to cover some of the most important day-to-day operational issues that you are facing and hopefully provide you with inspiration and education. **Enjoy!**

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How to Motivate Employees

“Very much like national identity and patriotism, employees look upon their workplace as an entity to identify with.”

Rafi Nave – Tower Semiconductor – **See p19**



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When you wanted a "long term relationship" with a metrology company, we're pretty sure this isn't what you had in mind.

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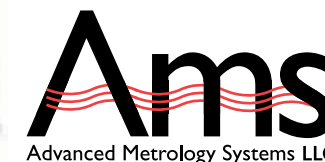
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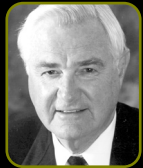
The following pages contain the photos and brief biographies of **FEO's** founding Panel Members. We would like to extend our sincere gratitude for their belief in our idea and their willingness to help us bring this new magazine to fruition. **FEO** magazine would not have become a reality without their support, guidance and wisdom.


Gary Alexander
AMC Intl., LLC. Executive Director - SEC/N®

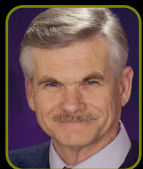
Gary Alexander is Founder/Managing Principal of AMC Intl., LLC, which independently consults on secondary market topics with organizations and government agencies worldwide. He is participating in U.S Department of Commerce/WTO and ANSI-ISO task forces on increasing trade opportunities and developing standards for the global secondary market. He is also Executive Director of SEC/N, the global trade association of the semiconductor industry for secondary market equipment and related services.


Madan Mohan Chakravarthi
Section Manager - IE Systems at Chartered Semiconductor, Singapore

Madan Mohan Chakravarthi is a Section Manager - IE Systems at Chartered Semiconductor, Singapore. Over the years, he has taken the role of a systems evangelist and has successfully led several corporate systems improvement initiatives. Mr. Chakravarthi holds an Industrial Engineering degree and a Master of Technology in software engineering.


C. Richard Deininger
General Partner, Taylor-Deininger Partners

Dick brings 50 years of successful executive management and business experience to the high tech industry. He is one of the general partners in Taylor-Deininger Partners, Inc. (TDP) consultancy and the owner principal of Deininger and Associates, LLC consultancy. He holds a BSEE degree from Newark College of Engineering and is a senior life member of IEEE, Tau Beta Pi and Eta Kappa Nu.


Bill Funsten
Program Manager, Contamination Control at Spansion, Inc.

Bill Funsten has 33 years of experience in semiconductor processing, defect metrology, yield improvement and contamination control. He is currently program manager, contamination control at Spansion, Inc. Mr. Funsten has a B.S. degree in materials engineering from UCLA.


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Senior Etch Line Maintenance Supervisor at Cypress Semiconductor

Kevin Gray is a Senior Etch Line Maintenance Supervisor at Cypress Semiconductor. In 1991, he joined the U.S. Navy, becoming a nuclear electrician aboard the Submarine USS Michigan. Kevin co-authored "Polymer control in a LAM TCP 9600 Aluminum Etch Chamber" at ISSM 2001. He became a Maintenance Supervisor in 2004 and has led the Fab Owners Association LAM 9600 team since March 2007.


Chris Howington
Supply Chain Re-Engineering Manager, Freescale Semiconductor

Chris Howington has over 20 years in the semiconductor industry in manufacturing and supply chain leadership roles. He is currently Supply Chain Re-Engineering manager at Freescale Semiconductor. Previous experience includes management roles at TSMC, National Semiconductor and AMD. Mr. Howington has a B.S. in mathematics from The University of Texas at Austin.


Scott Kramer
Director of International SEMATECH Manufacturing Initiative (ISMI)

Scott Kramer is the director of International SEMATECH Manufacturing Initiative (ISMI), a subsidiary of SEMATECH, overseeing the Equipment Productivity, Fab Productivity, 300mmPrime/450mm, Metrology, and Environment, Safety and Health programs. He joined SEMATECH in 1994 as Fab Manager of the Advanced Technology Development Facility (ATDF). Mr. Kramer holds a B.S. in mechanical engineering from the University of Missouri and an M.B.A. from the University of Utah.


Matthew Nadeau
Director of Manufacturing at NEC Electronics

Matthew Nadeau is the director of manufacturing at NEC Electronics, America in Roseville, Calif. He joined NEC in 1989 and worked as a process engineer in the Dry Etch and Wet Etch areas before starting his work in the manufacturing environment. Matthew received his B.S. in chemical engineering from the University of California at Davis.


Rafi Nave
CTO, Tower Semiconductor

Rafi Nave has been Tower Semiconductor's CTO since 2005. From 2003-2005, he was Tower's VP Customer Services. From 1996-2003 he was VP R&D for NDS Corp. From 1974-1995, at Intel Corp he held the positions of: chip design engineer; general manager of Intel's design center in Israel; director of Corporate Engineering & Corporate DFM. He earned his MSc and BSc EE from Technion, Haifa, Israel.


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Murty Polavarapu is a senior principal engineer at BAE Systems Semiconductor Technology Center in Manassas, Va. Over the last 23 years, he has worked on developing and manufacturing advanced CMOS memory and logic products. His current interests include development of phase change memory technology and application of nanotechnology to meet the needs of the Department of Defense, particularly for space-based applications.


Bill C. Smoak

Vice President of Operations - Intersil Corporation

Bill Smoak is the vice president of operations for Intersil's silicon wafer fab site in Palm Bay, Florida. He has 28 years of semiconductor manufacturing experience in engineering, development, manufacturing systems and operations roles with Harris Semiconductor and Intersil. Primary experience has been in SOI materials and high-performance analog processes. Bill holds a B.S. in materials science and engineering from the University of Florida.


Mario Tellez

Equipment Service Manager, On Semiconductor

Mario Tellez is an equipment service manager with On Semiconductor. He obtained his B.S. in electronic engineering and completed various studies in project management. Mr. Tellez has 20 years of semiconductor-equipment-related experience in photo, implant, diffusion, etch and backgrind. He has held various roles including lead technician, equipment engineer and equipment service management.


Kevin Venor

Manufacturing Development Engineering Manager, Avago Technologies

Kevin Venor is the manufacturing development engineering manager for Avago Technologies in Fort Collins, Colo. He has more than 20 years of experience in the semiconductor industry and has held various positions in R&D, manufacturing and business development at Hewlett Packard, Agilent Technologies, SEMATECH and Avago Technologies.


Mike Weiby

Corporate Environmental, Health and Safety Manager for Integrated Device Technology, Inc. (IDTI)

Mike Weiby has 8+ years managing ISO 14001 and environmental programs, injury/illness prevention, emergency response, business continuity and risk management/loss control plans. He has an M.B.A. from Portland State University, a Master of Industrial Safety degree from the University of Minnesota-Duluth and a Mechanical Engineering degree from the University of Wisconsin.


Greg Westby

Purchasing and Materials Manager, Integrated Device Technology

Greg Westby is the purchasing and materials manager at Integrated Device Technology's 200 mm wafer fabrication facility in Hillsboro, Ore. Mr. Westby earned his M.B.A. from the University of Portland and has over 19 years of semiconductor experience, 12 of which are in procurement and materials management.


Gregory D. Winterton

Process Development Manager for TI's DLP® group

Greg Winterton is the Process Development Manager for TI's DLP group. Greg has responsibility for the development and production of TI's next-generation spatial light modulator MEMS devices. Greg is a 23-year veteran of the semiconductor industry with experience in process engineering, equipment engineering, manufacturing, technology transfer, and quality and reliability assurance on wafer diameters from 125 mm to 300 mm.


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Juergen Woehl is the general manager/VP manufacturing of International Rectifiers Temecula site in Southern California. Previously, he held management positions at IBM, Infineon, Sematech and ON Semiconductor. Juergen has over 25 years in the semiconductor industry, in engineering, manufacturing and R&D. He has a B.S. in chemistry from the Fachhochschule in Aalen, Germany and an M.B.A. from St. Edwards University in Austin, Texas.

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Business Infrastructure & Operations

New Regulations for Everyone's Chemical Security

Julia Bussey - Geomatrix Consultants

How to Motivate Employees

Rafi Nave - Tower Semiconductor

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Bill C. Smoak

Vice President of Operations - Intersil Corporation

This first issue of FEO exemplifies the diverse and complex world of semiconductor fab operations. This section delivers two examples of how multidimensional the issues of maintaining and operating a fab today have become.

These two articles address high-priority concerns in their own right, but are very different in the issues and challenges they present; what a business! You will read about some of the primary concerns and challenges regarding motivating employees and the connection to your fab's performance and culture.

The first article addresses the myriad of details that define conforming to the governmental regulations on raw materials in your fab operations recently enacted via the Department of Homeland Security of the United States. This succinct article distills down this complicated legislation which

enables the reader to assess the impact on their business readily.

The second article illustrates how compensation, although very important, is only one of the many means through which you can motivate and align your workforces with business goals.

In summary, these two articles deliver another message: that there are many common topics and issues among our community which we all address every day.

I am sure you will learn or confirm some ideas that will help you in your own operation from the included articles, and that will maybe encourage you to share your experiences and learning in an upcoming issue of FEO.

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New Regulations for Everyone's Chemical Security

Julia Bussey, Geomatrix Consultants

Background

The Homeland Security Appropriations Act of 2006 gave the Department of Homeland Security (DHS) the authority to identify and regulate high-risk chemical facilities. This act was passed in a response by Congress both to the Oklahoma Federal Center bombing of 1995 and heightened security concerns raised by the attacks of September 11, 2001. The Act required that DHS "establish risk-based performance standards for security of chemical facilities" by April 4, 2007. The Chemical Facility Anti-Terrorism Standards and Appendix A, Chemicals of Interest, April 9, 2007, was met with tremendous response – over 4,300 comments, much of which was due to the low thresholds and the definition of "facility." Particularly concerned were universities, paint and pulp manufacturers, and farmers. Many other industries were unaware of the rule and its broad definition of "chemical facility." Although the regulations are final, the regulatory program is best described as a work in progress. The DHS is releasing the guidance as it is developed, and the criteria by which they will determine high risk is unclear. Several guidances were released or updated as recently as September 2007. Any company with potentially dangerous chemicals, regardless of how common, needs to follow the DHS regulatory process as it evolves and determine if it applies to them. The website for DHS is www.dhs.gov/chemicalsecurity and it is updated frequently.

The Department of Homeland Security (DHS) has adopted new chemical security regulations that require screening by 50,000 to 80,000 chemical facilities. Many of these businesses may not consider themselves to be chemical facilities, because while they possess chemicals as part of their business, they do not produce chemicals. DHS, however, considers any business that uses chemicals as a major part of their operation as subject to these regulations; many companies likely are thus unaware of their obligations and will be unprepared to meet the rules' short time frames. DHS expects ultimately to regulate 5,000 to 8,000 facilities and will require them to meet risk-based performance standards, and conduct security vulnerability assessments (SVAs) and internal and external inspections. Significant penalties could be imposed for missing deadlines: for example, a fine of \$25,000/day plus facility shutdown may accompany a ruling of noncompliance.

A facility is required to complete the online screening process, called "Top Screen," if it has or exceeds quantities of chemicals over the screening threshold quantities ("STQs") in Appendix A of the new Chemical Facility Anti-Terrorism Standards. The final Appendix A is expected to

be published before the end of 2007. After Appendix A is finalized, companies are required to submit the results of their facility-specific Top Screen within 60 days (future exceedance of a specific STQ also will require completion of the Top Screen within 60 days). Calculations of chemical quantities will sometimes be based on the prior 12 months of chemical use on site or will sometimes be based on the maximum expected to be on site at any time in a 12-month period. Appendix A is anticipated to contain a list of 344 chemicals, many of which are common to semiconductor manufacturing, research and development facilities, industrial processes and university campuses. For some examples of the chemicals of interest and their STQs, see Figure 1.

Substantial changes are expected for Appendix A, including increasing the levels of the zero threshold STQs to a specific number, addressing the issue of mixtures, changing the definition of "facility" and

perhaps adding a general "dangerous chemical" definition.

While Appendix A is not final, the regulatory framework that surrounds it, the Chemical Facility Anti-Terrorism Standards, is final as of June 8, 2007 (Fed. Reg. April 9, 2007, p. 171688). Figure 2 provides an overview of the process. The deadlines and substantive requirements are significant, particularly for larger facilities with long chemical lists. Penalties and the risk of unnecessary regulation, coupled with requirements for a wide range of data to complete the Top Screen, suggest that a team-based approach be taken early in the process to provide an accurate response. Information from hazardous materials inventory, locations of materials, toxic release inventory, security, vendor or tenant information, and in some cases, market share information, is required. Team members might include environmental engineers, purchasing, security, vendors/tenants, facilities and sales/marketing.

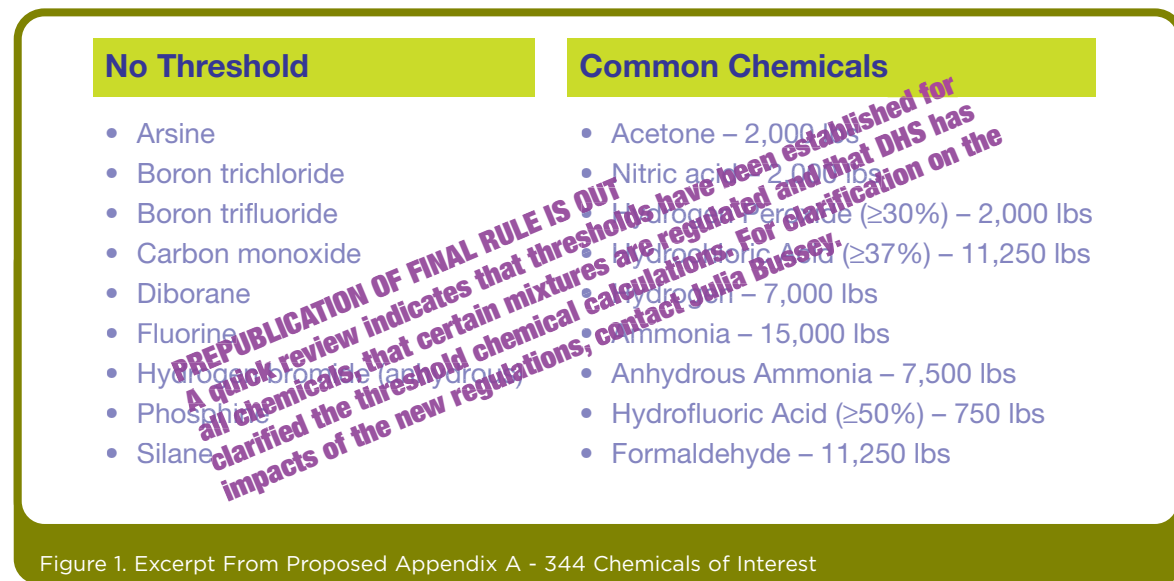


Figure 1. Excerpt From Proposed Appendix A - 344 Chemicals of Interest

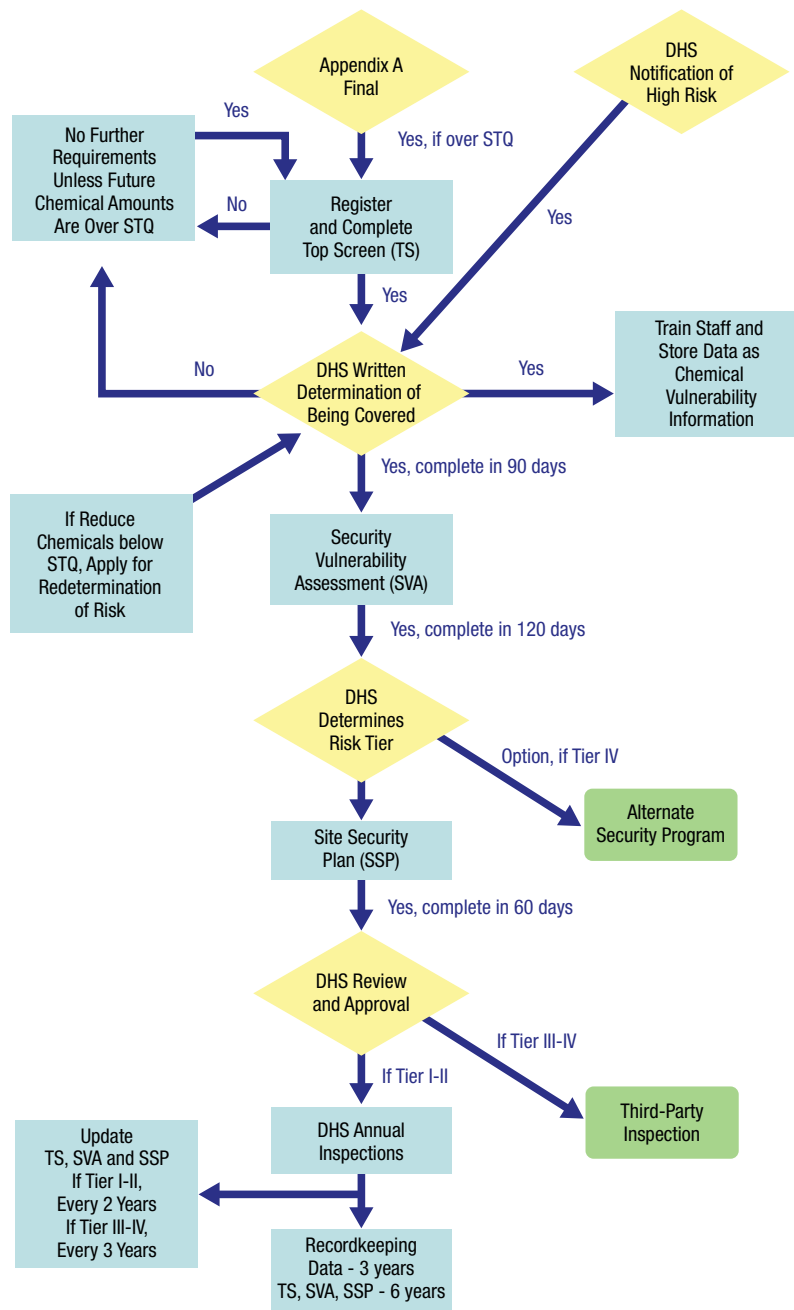


Figure 2. Overview of the Chemical Facility Anti-Terrorism Standards Process

Top Screen will be completed by a company after it first registers and designates to DHS an authorizer (required to be an officer of the company or the officer's designee), a submitter and a preparer who may enter the data into the online program. A separate Top Screen must be submitted for every facility; however, the same individuals in a company may submit Top Screen for more than one of the company's facilities.

Top Screen requires the facility to enter extensive information covering chemical inventory, and relies on the results of an impact analysis using RMPComp to estimate the size of potential areas of concern. Top Screen also prompts the facility to answer questions intended to evaluate potential ways that a chemical may be used by a terrorist. For example, if a chemical were released, would it have the potential for significant adverse consequences for human life or health? Or if it were stolen, could it be used as a weapon? Or if it were mixed with other chemicals, could it be used to create significant adverse consequences to human life or health? There is also concern about whether the threat could be made to significantly harm the nation's economy.

Once the Top Screen is completed online, a screen will appear stating that the facility has been screened out or that the facility may be regulated. If the facility is not screened out, DHS must provide a written notification to the facility regarding whether it is considered high risk and, therefore, regulated as a "covered" facility under the rule. The date of that notification triggers both the date for the SVA, due 90 days later, and the SSP, due 120 days later. The questionnaire and guidance for completing Top Screen are available on the website.

While DHS anticipates that many facilities may be required to submit the Top

Screen, it only plans to regulate a tenth of the facilities that it screens. The facilities subject to screening are not considered regulated. Only high-risk facilities that are screened by the Top Screen or that are designated and identified directly by DHS are "covered facilities." Covered facilities must complete all of the requirements and risk-based standards as required by the rule, including creating a chemical security information (CVI) system to track all the data used to submit the Top Screen, and any of the other requirements, training, drills, incidents and security breaches, maintenance, calibration and testing of security equipment and audits, correspondence, and letters of approval. Staff must be trained to maintain the security safety of CVI records as required by the Act. An online training class is available at the DHS website: www.dhs.gov/chemicalsecurity.

The SVA, required 90 days after notice from DHS, will be used to help DHS determine what final tier the facility should be in - 1 being the most serious risk and 4 being the least. While the SVA (which will also be required to be completed online for this step) is not currently available, DHS has indicated that it will provide both the questionnaire and guidance online prior to the deadlines for completion. The SVA requires a description of the facility's critical assets and existing security measures, assessment of the internal and external threats, identification of potential security vulnerabilities, risk assessment of the potential effect on critical assets, and analysis of countermeasure strategies.

The SSP is required for Tiers 1-3 just 120 days after notice from the DHS. Facilities in Tier 4 have the option of following the same process or completing an Alternative Security Program in lieu of completing the

SVA and the SSP. Any plan or program must include measures that satisfy the 19 performance-based security standards. The standards will apply to different levels of stringency, depending on the tier of the facility. The criteria that DHS will use to determine how to apply the standards based on risk is unclear. The standards include the following types of requirements:

- Perimeter security
- Access control
- Employee and contractor background checks
- Insider sabotage

The DHS Chemical Facility Anti-Terrorism Standards are far-reaching rules that extend throughout the business enterprise and will significantly change the way we manage chemical security.

- Cyber security
- Response planning for sabotage, theft and diversion
- Deterring, detecting and delaying access to assets
- Monitoring, training and reporting

Here's what you can do prior to the finalization of Appendix A:

- Learn about the rule and ensure that your company executives and affected groups understand the requirements.
- Create a team and review data needs and adequacy of chemical tracking systems.
- Prescreen your facilities.
- Ensure that any collocated vendors are aware of the rule and can respond when Appendix A becomes final.
- Complete internal delegations and assign roles for submittal.

The DHS Chemical Facility Anti-Terrorism Standards are far-reaching rules that extend throughout the business enterprise and will significantly change the way we manage chemical security. DHS intentionally has made the Appendix A, list of chemicals of interest and the STQs broad to screen the maximum number of facilities. By approaching compliance with the rule step by step with an internal team, and by working through the calculations carefully, facilities can manage their risks and security profile with the clear understanding that in the majority of cases (9 in 10) they will be screened out from regulation. Those that are

covered will need to follow the DHS process as it unfolds; more guidance and additional online tools are expected to be finalized and provided on the Web over the next year. ■

About the Author

Julia Bussey has over 25 years of experience working in industry, including five years at AMD, Inc., and government to incorporate sustainable compliance practices into operations. As a senior scientist at Geomatrix Consultants, she provides environmental compliance assistance to companies to reduce business risk.

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How to Motivate Employees

Rafi Nave - Tower Semiconductor

Abstract

Employees are the most critical asset of many businesses. Specifically, the success of Semiconductor manufacturing companies hinges on the quality, productivity and effectiveness of their employees. These key variables depend strongly on motivation. Hence, "how to motivate employees" is a vital challenge facing all semiconductor manufacturers.

The Importance of Motivation

Semiconductor manufacturing sites are capital-intensive. The investment in equipment in modern Fabs amounts to multiple billions of dollars. But this costly equipment is useless unless the people operating and maintaining it do their jobs well and the output of the factory - volume, yield, quality and reliability - further hinges on the human resources: researchers, engineers, technicians and operators.

While the equipment is "passive," namely it behaves as built and programmed, and is not subject to moods, stress or the like - people are different. There is a wide swing in employees' performance according to their motivation. Employees who go to work with enthusiasm and drive may attain 10 times higher output than employees who

are demotivated and lack the enthusiasm to get to the job.

Low motivation undermines output, i.e., causes lower production rates, but what is even more dangerous is the impact on yield and quality. If the products produced and shipped lack in quality, the damage to the customers is immense and the long-term damage to the manufacturer's reputation may be nonrecoverable. Hence, it is essential to find ways to motivate employees in all ranks.

What Motivates Employees?

The obvious answer that everybody thinks of is: compensation. This is true, but too simplistic. There are further motivators besides compensation, and within the compensation realm, there are different ways of maximizing the "bang for the buck." Hence, it is important to invest time and effort in correctly architecting employees' motivation efforts and in working in closed loop: measuring the effectiveness and improving with time.

It should be noted that, besides the elements described below, the inherent reputation and success of the company as well as the professional domain and the specific challenges employees face are natural motivators.

The Noncompensation Motivators

The anchor of motivating employees is their manager. There is no substitute for charismatic and inspiring managers. The obvious analogy is to combat units, where good commanders are able to motivate their soldiers to follow them through fire and hail. Similarly, good managers are able to motivate their employees to cope with any challenges they encounter and prevail. So, the No. 1 means of motivating emp-

them and feel good about being associated with a company that commands such values.

Long-term Visibility

Employees like to know where they, and their company, are heading. It is demotivating to work for a company that is perceived as having no future or that the plans are blurred. Outlining a long-term plan is vital for business, but is also critical for motivating employees.

Very much like national identity and patriotism, employees look upon their workplace as an entity to identify with.

loyees is by assigning competent and powerful managers who are natural “leaders of the people.”

Then there are supporting processes and methods that help the management team in motivating the employees. Due to brevity, I'll mention only a few: Values & Culture, Long-term Visibility, Communication and Recognition.

Values & Culture

Very much like national identity and patriotism, employees look upon their workplace as an entity to identify with. If the values that the company stands for are aligned with the person's beliefs and interests, then it is easier for employees to feel that their efforts and contributions are as if they are working for their own self-interest and well-being.

Thus, it is important to crisply articulate the organization's values and to ensure that all employees are familiar with

Furthermore, employees would like to know what's in it for them in the long run, e.g., how they may be able to grow – professionally and in responsibility span – over the years. Hence, a career dialogue that outlines opportunities is a high motivator. Investment in employees' education and training, as a means of professional growth or enrichment, motivates them highly.

Communication

It is essential to nurture open communication with the employees at all times. It should be emphasized that communication is a two-way street. On the one hand, the managers must share with the employees what's going on, to explain why things are done the way they are done and to convey what is expected in unambiguous terms. On the other hand, the managers must listen to the employees. In most cases, the employees, who are closer to the action, have vital information that is essential for

good business decisions, but, more importantly, employees who are listened to are much more highly motivated.

Recognition

Before we turn to the monetary compensation, in many cases the nonmonetary one – recognition – has greater impact than money. Good managers know firsthand what their subordinates do and provide on-the-spot feedback, including words of appreciation, when they accomplish beyond their regular call of duty. Public recognition, in employee gatherings or company publications, goes a long way to instill pride and motivation in recognized employees. Creating opportunities for employees to present their work to senior management is another means of creating satisfaction and morale boost.

How to Leverage Compensation

It is obvious that employees care about their compensation. They do not like to feel

one may leverage compensation by adequate management:

Managing Expectations

I recall a case, some 20 years ago, when both Intel Israel and its neighboring company, Elbit, handed out bonuses in the same month. The Intel employees expected an average bonus of about \$5K each, and in reality, the bonuses handed out were more like \$4K per person. There was an overall disappointment, and the bonuses attained an effect that was opposite to the intent: While the company handed out big money, the employees were demotivated by it.

During the very same week (it was the Hanukkah holiday) – Elbit handed out an average bonus of about \$400 per person (namely, only 10 percent of the Intel bonus). However, this bonus was a total surprise to the Elbit employees, and as a result, each and every one experienced high motivation.

It is obvious that employees care about their compensation. They do not like to feel like suckers who are abused by their employer.

like suckers who are abused by their employer. Still, for the very same level of spending on payroll and benefits, the employer may attain a broad spectrum of resulting motivation based on how the compensation is managed.

The key words for effective compensation management are: Managing Expectations; Meritocracy, Equity & Consistency; and Creativity. Let's take these one by one and show, by examples, how

Thus, if you want to maximize the impact of your compensation elements, carefully manage expectations, and always attempt to exceed the conservative expectations that you generated.

Meritocracy, Equity & Consistency

Employees like to know that their compensation is proportional to their contribution. It is important to put in place processes and methods that will attempt to

adjust the compensation to the person's impact on the company. In most cases, the compensation should include a base pay (the person's salary) that is adjusted over time in a conservative manner (no huge jumps, since it's usually only "upward") and a periodical element – primarily bonuses – and where applicable, stock options, that reflect the person's performance and accomplishments in the given period.

Employees should feel that they were treated fairly, regardless of the absolute value of their pay. If they perceive that their compensation does not reflect their relative contribution – this is source for trouble. One should shy away from tying pay to tenure (how many years out of school, how many years on the job as the primary element). The key is how employees apply their skills and experience to further the company's needs. It all comes down to performance and contribution.

Creativity

This holds true for all elements of the management and compensation system: Try to surprise employees with new, creative methods and approaches. Sometimes it's in the social benefits (e.g., fun days, with families, go a long way to mobilize employees and their loved ones toward feeling positive about the company). Same with the way bonuses are tied to company

goals, or special achievements: Linking high-level awards (e.g., CEO or president) to role modeling and unique accomplishments are also effective motivators.

Summary

There is no single recipe to motivating employees, but there is a long list of elements and tools that may be applied besides sheer pay. What is most important to remember is that we deal with humans, not machines; hence, the human touch can do wonders to improve morale and motivation, thereby driving results. ■

About The Author

Rafi Nave has been Tower Semiconductor's CTO since 2005. From 2003-2005, he was Tower's VP Customer Services. From 1996-2003 he was VP R&D for NDS Corp. From 1974-1995, At Intel Corp he held the positions of: chip design engineer; General Manager of Intel's design center in Israel; Director of Corporate Engineering & Corporate DFM. He earned his MSc and BSc EE from Technion, Haifa, Israel.

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Asset & Resource Utilization

Used Equipment - A Guide to Secondhand Goods

Gary Alexander - AMC Intl., LLC

Facility Assessment for a Fab Wafer Diameter Upgrade

John J. Plata - Texas Instruments

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Gary Alexander
AMC Intl., LLC

Assets are possessions that derive relative value based primarily on their importance to their owner.

Personal assets are probably the easiest for us to identify with, such as our families, houses and that new high-definition TV in the living room.

Businesses and organizations have assets as well. And as company employees, we become trusted custodians of those assets for which we are both directly and indirectly responsible.

There are also several ways to categorize assets, such as fixed/variable; current/long term; personal/public; and people, places and things.

Resources, on the other hand, offer a potential source of support and assistance, but only become assets when actions are taken to capitalize on/acquire their value.

This section of FEO will focus on how to most effectively utilize the assets and resources available relative to semiconductor operations.

For those "engineering types" that just have to have a formula, it goes something like this: "Asset utilization equals the ratio of actual output compared to achievable output if running at maximum capacity while producing 100 percent quality product."

For the rest of us, "Getting the most out of what we have to work with," would probably suffice.

We have chosen in this first edition of FEO to address two topics that are of special interest to mainstream device manufacturing plants: used equipment and fab facility upgrades.

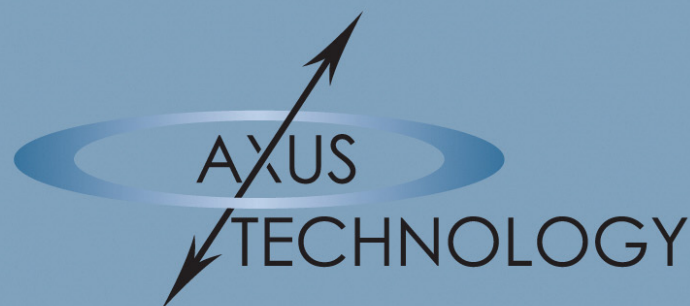
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Used Equipment - A Guide to Secondhand Goods

Gary Alexander, AMC Intl., LLC

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"I'll trade you a Johnny Bench and a Hank Aaron for your Willy Mays."

Sound like a good deal? Well, that all depends on the expertise of the traders and the value placed on the baseball cards involved.

And so it is with the buying and selling of secondhand equipment. The perceived success of any transaction is largely based on the trader's knowledge and understanding of the secondary market, plus the individual value each places on the equipment and related services in question.

The Global Secondary Market

Buying and selling secondhand equipment continues to be one of the most misunderstood and underestimated dimensions of the semiconductor business. The introduction of global ramifications into the equation adds an even more complex third dimension. Today the vast majority of used semiconductor equipment transactions involve multiple market segments across international borders. It has truly become a global market. And while over the past several years China has been the world's

This is the first in a series of FEO articles that is intended to focus on what companies in the semiconductor industry need to know in order to become more successful in sourcing secondhand equipment, as well as disposing of their surplus assets.

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single largest importer of secondhand semiconductor equipment, there is competition on the horizon.

Relatively speaking, the global secondary market continues to evolve both in size and maturity. From a spectrum of garage sales to the resale of planes and ships, the inter-

national market for secondhand goods and related services is generally considered to be the largest business in the world. However, with so many potential buyers and sellers involved, no consensual method has yet been reached on how to objectively quantify either domestic or global market metrics.

address standards for secondhand goods, but I will save that topic for a later discussion as well.

Actually, I have already used three terms in this article which need further clarification before moving on to other secondary market considerations. They are:

Buying and selling secondhand equipment continues to be one of the most misunderstood and underestimated dimensions of the semiconductor business.

The evolutionary keys to the growth and maturity of the semiconductor industry's secondary market hinge on development and acceptance of standards, commensurate with ongoing education and understanding. Our pursuit of education and understanding begins now. We will tackle standards in a future edition.

Terms and Definitions

To improve one's understanding of the secondary market requires at least a minimum knowledge of the market's basic terms, and right away we hit our first snag. Just as there is no universally recognized formula for establishing secondary market metrics, there are no universally recognized definitions for many of the terms used. For example, what is the difference between secondhand equipment that has been "refurbished" as opposed to equipment that has been "remanufactured?" Or what about the terms "recycled," "rebuilt," "operational" and "certified?" And if you think that is ambiguous, try translating these terms into another language.

On a more macro basis, the World Trade Organization and ANSI-ISO task forces are methodically (and politically) working to

- **Secondhand Goods:** "Merchandise, movable assets, wares and commodities that have been in use and that are now reentering the market for resale and/or future use." Technically, this is the internationally and politically correct way to define that which is being returned to the marketplace.
- **Market Segments:** "Participants involved in the buying and selling of secondhand goods and services." Regardless of industry, the market segments include: sellers, buyers, dealers, brokers, recyclers and service providers.
- **Secondary Market:** "All of the activities that market segments employ in the buying and selling of used (second hand) goods and services." Throw in the international dimension and voilà – the "global secondary market."

Secondary Market Considerations

Over my 30-plus years in the semiconductor industry, I have derived a list of secondary market considerations which most companies need to better understand. In alphabetical order they are:

1. Buying Guidelines
2. Contracts and Documentation
3. Decommissioning and Decontamination

4. End of Life
5. Environmental, Health and Safety
6. Equipment Status and Condition
7. Financial Considerations
8. Global and Cultural Considerations
9. Installation and Facilities
10. Intellectual Property
11. Legal Considerations
12. Market Forecast and Future
13. Market Segments
14. Measurement and Metrics
15. Organization Effectiveness
16. Regulations and Regulatory Agencies
17. Selling Guidelines
18. Standards
19. Terms and Definitions
20. Third-Party Resources

As you can see, the list is quite extensive and deserving of multiple subcategories of discussion. If there are additional considerations that your company would like to see addressed in future FEO editions, please forward your suggestions to me at email@amcintl.com.

I have also found that senior management is often no more knowledgeable of the secondary market than are their employees; and in many cases, senior managers understand even less. However, given their usual rise to the top from the more high tech parts of their business, this should probably not have come as any surprise. And since the opportunity to

improve a company's chance of success in the secondary market will most certainly require some "do differentlies" from the top on down, senior management would do well to give knowledgeable consideration to the secondary market components of their company's asset management strategies.

In a presentation to an OEM, I once flippantly said, "A telltale sign of problems to come is when uninformed senior management goes off for a day to develop their company's used equipment strategies." At the end of my presentation, a member of the audience came up to tell me that their senior management was scheduled the following week to go offsite to do just that.

A Concluding Thought

If your company is involved in the secondary equipment market and finding one or more of these topics already to be a challenge, don't wait. Get help from one of the reputable secondary market resources that are available.

In the words of David Starr Jordan, "Wisdom is knowing what to do next, skill is knowing how to do it, and virtue is doing it." ■

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Facility Assessment for a Fab Wafer Diameter Upgrade

John J. Plata, Texas Instruments

Abstract

Changing demands eventually outpace the capability and capacity of even the best-conceived fabs. Refitting a legacy fab to the next wafer diameter to address these issues is often the business solution. However, there is a great deal of analysis and groundwork that must be performed before the first tool is moved, and the trade-offs and costs may be greater than high-level models may suggest.

When designing a new wafer fab, a great deal of effort goes into process flow analysis, production modeling, proximity of

space and production efficiencies through introduction of new technologies, tool set and product mix changes, and incremental fab expansions. In the final stroke, many fabs reach the point where conversion to a larger wafer diameter becomes a financial or technical necessity.

Refitting an existing fab for a larger wafer size can provide a second chance to regain some of the physical optimization lost over time. No less effort needs to go into a wafer diameter retrofit than the original fab planning. For this discussion, assume the desire is a conversion from 150 mm to 200 mm wafers. Rather than try to suggest how to regain optimization, the

Many fabs reach the point where conversion to a larger wafer diameter becomes a financial or technical necessity.

process steps, tool placement, AMHS system design and modeling, etc. The desired result is an efficient design wherein fab space is optimally utilized, product cycle time is minimized and all physical production indices are optimized. Fabs seldom mature per the original design: Time takes its toll on

focus here is on key decisions, issues and actions that must be made if there are to be any opportunities to optimize.

Choosing a Path

There are three basic ways in a wafer diameter change can be implemented:

Incremental

(Soft conversion) replaces 150 mm tools with 200 mm (or bridge tools) on a 1 by 1 basis. Tools are replaced/reshuffled over an extended period of time. This type of conversion has spawned countless fabs running two wafer diameters for years. On the surface, this is the cheapest and least disruptive route, but yields inefficient production at either node, and has the least chance of the end point fab being space- or production-efficient.

Expedited

Once a parallel 200 mm line is running, the 150 mm line is rapidly ramped down and tools either converted or replaced with 200 mm tools in relatively few quarters. An aggressive plan retaining some level of production, this requires intense planning, and carries greater risk of production disruptions. The ability to clear larger areas at a time provides enhanced flexibility in space management, and more opportunity for an efficient end point layout.

Full Conversion

(Hard conversion): Basically rebooting the fab. All tools convert/replace in one coordinated effort, entailing production cessation and major tool rearrangement. This type of conversion is the most costly, but can have the shortest full changeover window, and provides the best opportunity to optimize space and layout and/or automate. Total loss of output during conversion may limit the desirability of this option.

The starting point is key. If the existing fab layout and infrastructure is not a total disaster, retaining tools in their current locations reduces cost and retains production capability through the transition, or a least shortens the shutdown. Seldom does shuffling tools generate the level of

cycle time or efficiency advantages modeling programs might indicate. If there are few or no existing 200 mm tools, or the infrastructure requires significant upgrade, the layout options are more open.

Actions: Making the Assessment

Prior to embarking on a retrofit, a full physical facility assessment is in order. This entails a detailed analysis of the production spaces, current and proposed tool sets, utility systems capacities and specifications, building and environmental codes, building structure, etc., to determine the boundaries and constraints. A fab designed for 150 mm production tools will be deficient in one or more areas with respect to 200 mm tools. The following should be included in the assessment as a starting point, although considerably more detail is warranted.

Physical Facility/Cleanroom:

- All production areas: Space/class/ceiling height/current usage/area constraints
- Structural floor loading: Tools are heavier per unit area; multichamber tools
- Building vibration limits: Smaller geometries/critical photo and metrology tool specs
- Class desired or required: SMIF vs. open cassette
- Site emissions permits and limits: Will the new tools/processes increase emissions beyond the current permit limits? New chemistries?
- Building code review: Will the area meet any new code requirements permitting the retrofit may trigger?

Space:

- Fewer tools will fit with space held constant. Is the fab remaining the same size? Is new space required to accommodate the new tool set? Are

there areas in the current layout that cannot/should not be used?

- Are process areas (tool locations) retaining their original boundaries? Utilities are usually routed only to the areas where needed. Major tool location changes require major distribution changes.
- Tools are larger, use more space and more or perhaps different utilities.
- Tool support equipment is larger/more numerous. Is sufficient subfab support space available?
- Tool move in paths: Width/height; tool elevator size and limits

Layout

- Flow analysis, production modeling, proximity of process steps, tool placement: opportunity to re-optimize the physical flow in the fab
- Automation: If there is any desire for AMHS, it should be planned in from the outset

Tool set

- Availability of tools: Internal vs. external
- SIZE! Tools can be significantly larger
- SMIF vs. non-SMIF: Relates to cleanroom, but can also be a major cost added to the tools and wafer tooling
- Bridge tools require retrofit
- Multiprobe, metrology and test tools must be considered as well

Facilities Systems

- Larger wafers = larger tool chambers/ tanks/tracks = more utility usage
- Utility system capacities and expansion capability: Summary and comparison of existing tool actual usage and new tool requirements
- Mechanical/electrical/chemical/drain+ waste systems/specialty gas/bulk-plant gas/controls systems

- Utility system specifications: do they meet the new process requirements?
 - Cleanroom: temp and humidity; class; ESD
 - DI Water
 - Bulk Gas
 - Chemical systems

Consider not only usage and specifications, but the age and condition of systems in a legacy fab may suggest replacement or upgrade.

Other Issues

If conversion will occur in an operational fab, additional concerns include:

- Contamination control: Particles/ molecular air contamination
- Disruption of utilities/connection & disconnection from live systems
- Physical issues (vibration/odors/temp + humidity excursions, etc.)
- Security and safety

Consider optimizing (reducing) environmental impact.

- **Environmental Impact:** Specify new or upgraded systems that use less energy and produce fewer emissions. Select low VOC coatings and paints. Install energy-efficient lighting. Consider reducing cleanroom airflow and wider temp/humidity specs.
- **Minimization of and recycling of construction waste:** Recycle or reuse construction by products. Separate metals, plastics, wood, etc., at point of generation for ease of recycle. Follow all environmental guidelines when disposing of hazardous materials asbestos/lead/etc.).
- **Energy:** Utility costs are a significant operational expense. The opportunity to select more efficient systems or practices

Example: Purchase energy-efficient vacuum pumps

- > uses less power > eliminates area XFMRs > eliminates substation
- > eliminates space for substation

and

- > generates less heat > reduces building HVAC load > eliminates chiller
- > eliminates chiller substation > eliminates space for substation

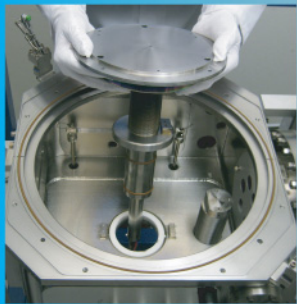
will pay back for the life of the fab, and have a domino effect on facilities' equipment cost.

Summary

A wafer diameter conversion is not simply a matter of replacing one tool with another. In-depth facility and tool set

analysis and planning needs to be performed. The above list is just a seed on which to build the analysis and checklist, but hopefully opens new areas for discussion and consideration. The opportunity to increase environmental stewardship and decrease operating costs should not be missed. ■

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John J. Plata is a member of the International Facilities group at Texas Instruments in Dallas, Texas. He is tasked with strategic facility planning, analysis and layout design for TI projects worldwide. He holds a B.S. in industrial technology from Illinois State University and an M.B.A. in engineering management from the University of Dallas.

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Installation & Maintenance

Support Strategy 200 mm Equipment 2008

Bill Butterfield - Jazz Semiconductor

Using Electrostatic Discharge (ESD) Event Detection as a Predictive Maintenance Tool (Part 1 of 2)

Andrew C. Rudack - SEMATECH North

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Kevin Gray

Senior Etch Line Maintenance Supervisor at Cypress Semiconductor

As 200 mm fabs proceed into the future, they find themselves in the same situation as 4-, 5- and 6-inch fabs before them. Competing with 300 mm fabs has placed cost and technical resource pressure on the 200 mm fabs. OEMs have significantly decreased overall technical resources and concentrated them on 300 mm tool sets. 300 mm fabs are also putting cost pressure on their 200 mm counterparts. The first article, by Bill Butterfield of Jazz Semiconductor, discusses alternate solutions to these issues and addresses cost as well as technical resource solutions.

Predicative maintenance (PdM) - the next step in keeping your maintenance cost down - just got one more technique added to its tool belt: Electrostatic Discharge (ESD) Detection. Andrew Rudack of SEMATECH North describes how and why you would want to use ESD

Event Detection. I found myself wondering where else I could use ESD detection to prevent costly yield loss (plasma tool errors that cause scrap) or throughput issues due to tool stop events (wet benches that have high throughput). This article shows that ESD can be used as a PdM technique, and that there are multiple ways of incorporating it into your fab.

Installation & Maintenance



Mario Tellez

Equipment Service Manager, On Semiconductor

I'm in favor of any tool that can predict a condition that maintenance is required, but I'm not a fan of time-based maintenance routines – potentially a controversial statement. Most factories' preventive maintenance (PM) routines are based on time. PM-based time methodologies are routinely a product of an OEM and similar factories' recommendations; from the factory perspective, this can create added cost. By this method, known working components will be replaced during time-based PM cycles, which is similar to throwing dollars down the drain.

Ideally, if a factory can predicatively determine when a component fails, it will save costs, but more importantly, it can prevent or minimize wafer scrap events or potential yield loss. Factories require manufacturing integrity when a wafer is committed to a semiconductor tool. Implementing monitoring tools to predicatively indicate a potential problem will ensure factory success.

Various monitoring tools are available to factories to help them establish a sound predictive maintenance (PdM) program. Determining which monitors should be pursued can be

a monumental task. The monitor of any semiconductor factories should include such basic items as gas, pressure, RF or DC power, and temperature. Most failures will be detected if these items are routinely monitored.

Accurate failure predictive models need to be in place that graphically output data. This allows monitoring of trends, spike and common excursion points. Control limits should also be implemented with soft and hard shutdown limits. PdM technology has evolved over the years, and on the horizon is a new technology that will interpret data (pattern recognition technology), visually predict a failure and potentially recommend recipe adjustments. It's vital for a factory to stay current with new technology to ensure the longevity of its operation.

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Support Strategy 200 mm Equipment 2008

Bill Butterfield, Jazz Semiconductor

Abstract

The mature 200 mm semiconductor market is faced with unparalleled cost challenges in the wake of 300 mm wafer pricing and the growth of 200 mm wafer production in low-cost regions. The North American and European Fab must transition to a support model that meets these challenges. The foundation of this support strategy is lowest cost with competitive quality. The execution of this strategy includes a flexible workforce, OEM alternative focus and flexible spare/repair part sourcing solutions.

Maintenance Cost Reduction Strategy

The challenges facing the maturing 200 mm wafer Fab continues to mount, particularly in the face of dropping 300 mm (90nm) wafer cost. Initially these challenges begin with the commodity DRAM & CMOS products, but this trend will ultimately drive down to the more specialized AIMS markets. The 200 mm wafer Fab must continue evolving to stay ahead of this curve by transitioning the maintenance support strategy to the optimal cost model. There are three primary factors that influence this strategy, including a high-quality flexible workforce, minimal overhead burden solutions and lowest-possible

inventory costs. The optimal support strategy combines these factors in alignment with the required Fab cycle time and capacity requirements.

Flexible Workforce

The flexible workforce provides a variable cost option to meet the needs of market cycles that challenge all semiconductor Fabs. This includes technician- and engineering-level staff that are traditionally built in to all fixed-cost models. The traditional equipment maintenance model breaks each area into subgroups, including engineers and technicians with knowledge of specific tool set(s). The challenge of hiring, developing and retaining these resources is significant and very geographically dependant. The maturity of the 200 mm wafer Fab changes the level of sustaining versus continuous improvement and new system implementation. As this transition takes place, balancing the proper level of staff engineering and senior technician resources is critical. The flexible workforce can provide a cost-effective solution, including engineering resources for specific challenges or initiatives. As those challenges are met, high cost and highly trained resources are no longer required. The flexible technical workforce model addresses this challenge. The semi-

conductor market has seen many companies transition toward the flex workforce model, including the OEMs. The 200 mm wafer Fab must embrace this solution to optimize their internal versus contract resources. Companies like Global Technical Services and Retronix International have grown successful businesses in North America and Europe using this model.

Reducing Overhead Costs

The common factor that impacts competitive support strategies is the overhead burden still present in various large organizations. In particular, the traditional OEMs have carried significant technical staffs to support product development and have paid for this through large margin business on mature products

capital equipment profits, and the burden has been placed directly on the back of the 200 mm Fab. Breaking this cycle is critical to implementing a cost-effective solution for the mature wafer Fab. Most organizations have begun this process but have yet to completely break the tie from the OEMs by eliminating full-service agreements or outsourcing critical consumables and spares. Through involvement in organizations like the FOA, the engineering managers can collaborate with other Fabs to benchmark their successes and failures with alternative sources.

Virtual Spares Management Solution

The last major topic in a complete maintenance support strategy is spares inventory management. The traditional

The common factor that impacts competitive support strategies is the overhead burden still present in various large organizations.

and services. This places a significant burden on the mature 200 mm Fab that no longer benefits from the OEM infrastructure that is focusing on 300 mm and 65-90nm technology. A more cost-effective solution is moving toward OEM alternatives for spares, consumables and direct labor. Historically the OEM offered a security blanket of service and resources to all customers (small and large), but the transition to 300 mm, corporate streamlining and reorganizations have eliminated a majority of the most effective support. In contrast, the service and spares cost has failed to drop proportionately. This is largely due to margin pressure from declining

model was highest-possible tool availability, minimal waiting time and large spares inventory. As 200 mm equipment has matured, many organizations are faced with large outdated inventories that equal large carrying costs. An alternative that has emerged are companies like NxEdge and OEM Surplus that have amassed large inventories of OEM spares and have set up WEB front ends to facilitate the distribution to the end user. The initial problem with these companies is they face the same challenges as the Fab: outdated nonmoving inventories. A solution that would benefit all parties is a collaboration of mature 200 mm Fabs, along with an organization like

NxEdge. The goal would be to define the optimal inventory for key tool sets and propose a buy-back strategy for NxEdge to purchase this inventory from individual companies for credit towards future purchases. NxEdge would gain the key parts required to generate revenue and turns on their inventory, while individual participating Fabs have access to a larger pool of inventory with no overhead costs. The key would be to get Fabs of similar tool sets and define minimum guidelines for participation to ensure companies are getting an ROI on their involvement. The end result would be maintaining a more extensive inventory, keeping costs down and using the power of multiple Fabs to replace the OEMs' competitive advantage in spare parts inventory and distribution. The implementation would have to take into consideration regional locations, and the same structure could be set up in North America and Europe. There are plenty of spares companies in these locations; the major challenge is pulling in the collaboration of enough Fabs to identify and procure the optimal spares inventory.

Conclusion

A three-part maintenance cost reduction strategy has been outlined to meet the cost challenges of 200 mm wafer Fabs. With maturing equipment sets and pricing pressure from 300 mm Fabs, the use of flexible workforce and alternative sources of labor and parts presents the lowest-cost model. Through the reduction of OEM support, the individual Fab reduces significant sources of overhead burden from the cost model and added flexibility is achieved. Depending on specific geographical challenges, the use of technical contract labor can offer stability

and quality resources with no overhead or relocation burden.

As the consumable and spares market has matured, the use of second-source suppliers can consolidate key consumables like quartz, ceramic, silicon and Vespel to minimize suppliers and take advantage of JIT or consignment inventories. The next advancement in spares management will ideally combine the demand of multiple Fabs and organizations to reduce the burden of obsolescence and nonmoving inventory costs. Several semiconductor spares companies have the potential to expand in this area but require the collaboration of Fabs across major geographical regions. Organizations like the FOA can identify this market and help all 200 mm Fabs move toward this maintenance spares model. ■

About the Author

Bill Butterfield is the manager of Equipment Engineering (Etch & Wet Chemistry) at Jazz Semiconductor in Newport Beach, California. He received his B.S. in mechanical engineering from Cal Poly San Luis Obispo, and his M.B.A. from University of Phoenix. He has 18 years of semiconductor experience as an equipment engineer and engineering manager.

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Using Electrostatic Discharge (ESD) Event Detection as a Predictive Maintenance Tool (Part 1 of 2)

Andrew C. Rudack, SEMATECH North¹

Wikipedia defines **Predictive Maintenance (PdM)** as techniques to help determine the condition of equipment to predict when maintenance should be performed. This approach offers cost savings over routine or time-based preventive maintenance because tasks are performed only when warranted. PdM is used to trend future conditions of equipment and to make decisions about the need to perform maintenance.

Traditional predictive maintenance tools include:

- Vibration monitoring
- Acoustic/ultrasonic monitoring
- Infrared/thermal analysis
- Motor testing/corona detection
- Oil/wear particle analysis
- E-diagnostics/data mining
- Other condition monitoring

Consider adding to the PdM Toolbox:

- Surface charge monitoring
- ESD event detection

An electrostatic discharge (ESD) generates radio waves (electromagnetic Interference - EMI) in the 100 MHz to 2 GHz frequency range. ESD events have been demonstrated to cause lockup issues in semiconductor manufacturing equipment, reducing mean time between failure (MTBF) and decreasing tool productivity. A dampened sinusoid trace is characteristic of all

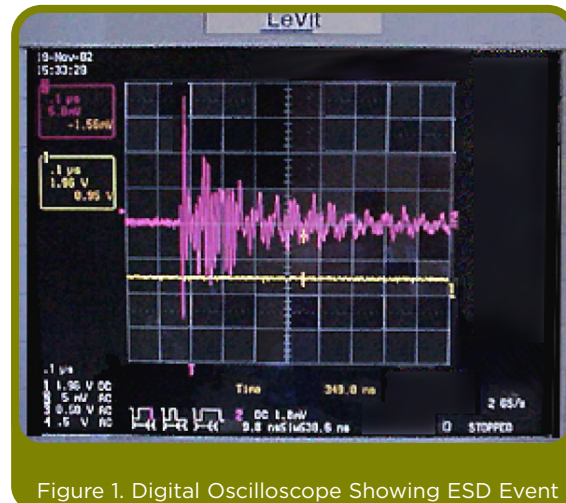
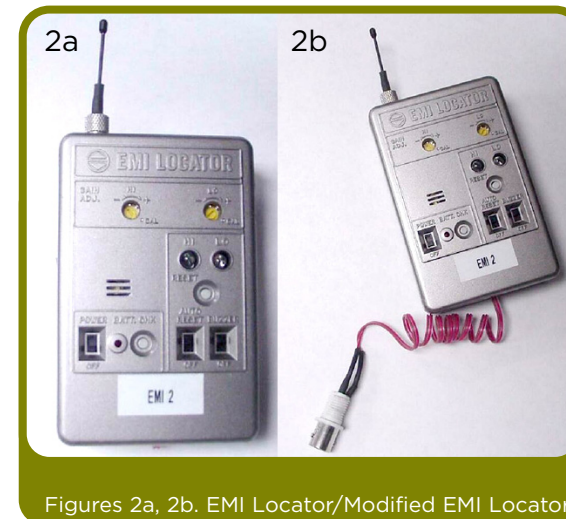


Figure 1. Digital Oscilloscope Showing ESD Event

ESD events (Figure 1). Over in a flash, they are very short in duration and can cause intermittent problems in microprocessor-based hardware. Rarely do the affected tools provide an error message that clearly points to ESD-induced EMI as the culprit. Tools just stop working, and a reboot usually solves the problem. The cycle repeats itself at some time in the future, as the root cause of the ESD-induced lockup has not been resolved.

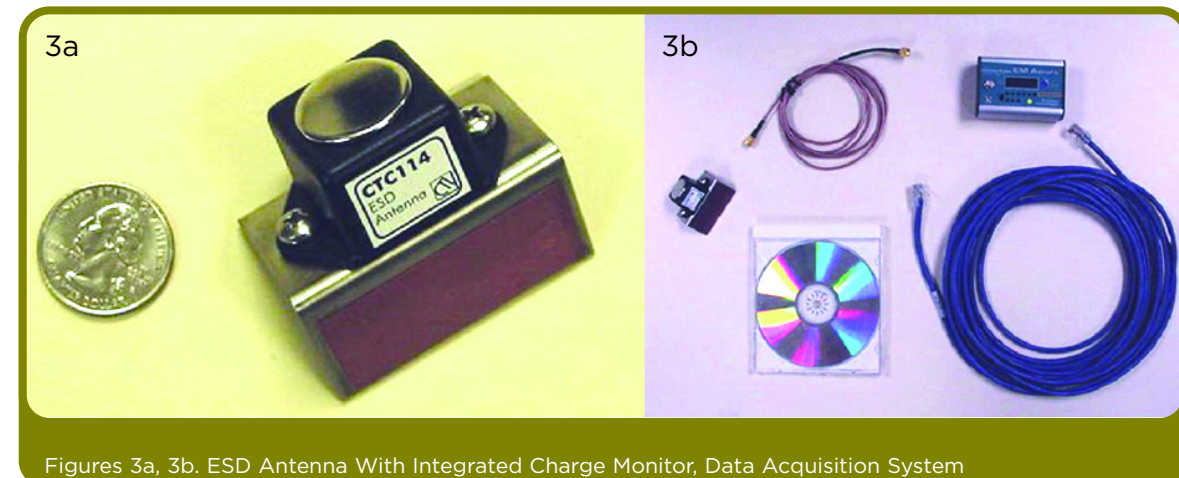


Figures 2a, 2b. EMI Locator/Modified EMI Locator

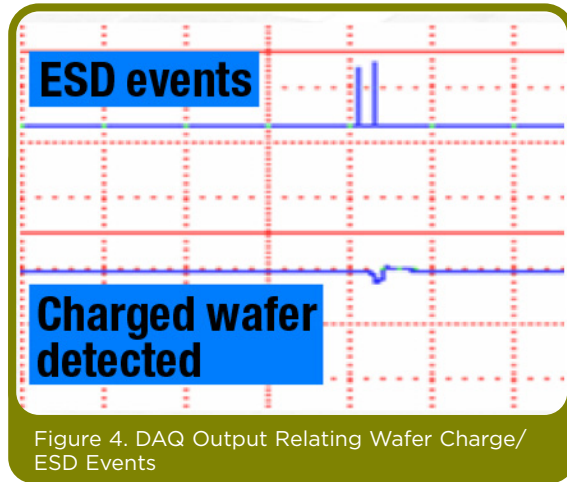
Not every ESD event results in a tool lockup. ESD event monitors can be used to time-stamp ESD as the suspected cause. If an ESD event is found to be synchronous with the tool lockup, it points to ESD as the root cause. A variety of ESD event detection monitors are available to fit most equipment engineers' budgets. Like most things, you get what you pay for as far as ease of use and capability.

A handheld EMI locator (Figure 2a) can be used to "listen" for ESD events. Their best features are portability, ease of use and low cost, but someone must monitor the device in person and wait for a lockup to occur. Boring! Wiring to the locator (Figure 2b) can be easily modified, and the event alarm (red LED lamp, buzzer) can be ported to an external data logger that has been configured to accept and time-stamp the ESD event. If the clocks on the process tool and data logger are synchronized, you will have a record of the ESD-induced EMI if an ESD event causes the tool to lock up.

ESD-event detection is available at a higher cost by using a system of antennas, signal processors/counters, cables, software and laptop PC (Figures 3a, 3b.)



Figures 3a, 3b. ESD Antenna With Integrated Charge Monitor, Data Acquisition System



charge information as well as ESD event detection. Looking at these points simultaneously in the monitoring software can be useful for trending over a longer period of time to see if things change (severity of charging, frequency of occurrence for ESD events). The DAQ can be integrated into monitoring schemes by semiconductor tool OEMs who are concerned about electrostatics and want visibility into wafer charging and ESD events.

As an example, wafers passing from a coat/develop track linked with a photolithography stepper can be measured when they enter the interface charged to -3000



Ethernet-based, this data acquisition system (DAQ) is useful for recording multiple channels of information. One style of ESD antenna also serves a dual purpose as a charge-monitoring device. Its fairly

small size allows it to be positioned closely to an area of interest and provides surface methodology to relate the wafer charge and ESD events is established. This tech-

When it's ESD ... it's too late. Charge-monitoring tools allow an equipment engineer to proactively find and mitigate charged surfaces that can lead to an ESD event.

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nique is referred to as an ESD event timestamp.

One of the most useful, albeit expensive ESD event detection techniques involves a high-speed digital oscilloscope (8-Gig samples/sec) and antenna with multiple channel inputs and a variety of math functions, including histogram techniques for binning peak-peak ESD events. A baseline can be performed to characterize a particular area of interest within the cleanroom, and measurements can be repeated periodically to see how things have changed.

When it's ESD ... it's too late. Charge-monitoring tools allow an equipment engineer to proactively find and mitigate charged surfaces that can lead to an ESD event. There are a variety of small, handheld monitors that can measure surface charge, in addition to smaller, probe-based detectors that can be installed with remote readouts (Figure 5).

Surface charge monitors and ESD event detection have their place in an equipment engineer's toolbox. They might not meet the classical definition of PdM techniques, but they are very handy for surveying suspected charging issues and avoiding ESD-induced EMI lockup. Charging begets discharge, and avoiding both can reduce the conditions in semiconductor manufacturing equipment that contribute to downtime.

Next issue - Part 2 of 2: Case Studies in Photolithography Using ESD Event Detection

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Environmental Stewardship

Impact of Environmental Regulations on Semiconductor Manufacturing

Walter Worth,¹ James Beasley,² Laurie Beu² – ¹SEMATECH, ²ISMI

Meeting the Climate Challenge: Applying Moore's Law to Reduce Greenhouse Gas Emissions From the Electronics Industry

Sébastien Raoux – Transcarbon International

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Mike Weiby

Corporate Environmental, Health and Safety Manager for Integrated Device Technology, Inc. (IDTI)

The global marketplace continues to evolve and change, with market forces and environmental regulations worldwide creating new challenges for the semiconductor industry. Recent changes include promulgation of the Restriction of Hazardous Substance regulations from the European Union (EU) to Asia and the U.S. The impending Registration, Evaluation, and Authorization of Chemicals regulation will directly and indirectly impact semiconductor manufacturers. Greenhouse gas emissions trading markets have also been created, with a net goal of reducing or capping emissions. The Chicago Climate Exchange established voluntary membership agreements to reduce greenhouse gases and establishes a market for Carbon Financial Instruments equivalent to 100 metric tons of CO₂ emissions. The European Union Emission Trading Scheme established carbon allocations for member states and operates in a similar fashion

to the CCX. The recent and impending regulatory and market changes will impact the semiconductor industry.

"Impact of Environmental Regulations on Semiconductor Manufacturing" addresses key regulatory changes facing semiconductor manufacturers. The authors address a broad range of environmental changes, including voluntary PFC reduction efforts supporting the 2010 reduction target set by the World Semiconductor Council (WSC) in 1999 to current U.S. Chemical Facility Anti-Terrorist regulations.

"Meeting the Climate Challenge," provides an assessment of technological and financial challenges the electronics industry faces in reducing greenhouse gas emissions, within the context of voluntary agreements, regulatory changes and market-derived solutions.



Scott Kramer

Director of International SEMATECH Manufacturing Initiative (ISMI)

Sustainability of semiconductor manufacturing operations is a key success factor for the industry as a whole. The Environmental Stewardship section in this edition describes in detail some approaches which have strong potential. First – an outline of several approaches to addressing the climate challenge we all share. There are, in fact, some technology-oriented and sustainable approaches which the electronics industry can use to address this challenge. Second – a description of the current environmental regulation landscape, along with industry initiatives. There are proactive activities in place today, which are being expanded and improved. Not only do these investments avoid future costly liabilities, they are fundamentally the right thing to do.

The environmental challenges faced by semiconductor and electronics manufacturing

industries are similar to those of other manufacturing industries. After all, it is the same environment for us all. But the technology industries bring some unique assets to the effort. Most importantly, these are industries that are defined by rapid change. Corporate survival demands quick decision making and smart risk taking. Successful companies have a track record of consistent success based on those abilities. Also, these industries must be innovative. Every day, they must prove themselves with new products, processes, ideas and innovations. With these attributes baked into the corporate cultures, the technology industries are well-positioned to lead the way in environmental stewardship.

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Impact of Environmental Regulations on Semiconductor Manufacturing

Walter Worth,¹ James Beasley,² Laurie Beu²
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Introduction

Environmental stewardship is a key component of semiconductor manufacturing, not only as a way to keep fab operations in compliance with local, regional and federal regulation, but also as part of ongoing industrywide voluntary agreements and emerging regulatory trends. Environmental stewardship is also embraced by most companies because it is the right thing to do and may avoid costly, future liabilities.

Currently, several global “hot issues” such as climate change and the industrial use of some persistent, bio-accumulative, toxic chemicals are driving the development of many new regulatory initiatives. The efforts to limit emissions of perfluorocompounds (PFCs) to ban the use of perfluorooctyl sulfonates (PFOS), and to register/evaluate and authorize all chemicals (REACH) by the European Commission are prime examples. The U.S. Homeland Security directive on anti-terrorism standards is the latest regulation potentially affecting fab operations.

In the U.S., the industry has proactively addressed many of these environmental issues by voluntary agreements, a concept that has been proliferated throughout the industry through the World Semiconductor Council (WSC), which is made up of high-level industry representatives from the five semiconductor industry associations (SIA, ESIA, JSIA, TSIA and KSIA) and which tries to harmonize the industry’s environmental response to these issues. This paper will discuss details of these regulatory initiatives and their impact on manufacturing.

PFCs

Perfluorinated compounds (PFCs) are long-lived greenhouse gases used in the semiconductor industry for plasma etching and plasma cleaning of chemical vapor deposition (CVD) chambers. In 1999, the semiconductor manufacturing industry became the first industry to coordinate globally and establish a voluntary greenhouse gas emissions reduction goal. The WSC agreement[1] calls on WSC member associations to reduce aggregate

absolute emissions of PFCs by 10 percent or more from baseline levels by 2010. Decommissioning older, higher-PFC-emitting fabs and ramping up newer fabs with lower-PFC-emitting processes have reduced PFC emissions[2]; however, two issues may impede this encouraging progress.

Typically, global warming potentials (GWP₁₀₀) at the 100-year time horizon are used to calculate greenhouse gas emissions. The recently issued 4th Assessment Report from the Intergovernmental Panel on Climate Change (IPCC)[3] contains updated GWP₁₀₀ (see Table 1).

The increased GWP₁₀₀ for all PFCs used by the semiconductor industry will result in higher calculated amounts of greenhouse gas emissions. For example, the increase in GWP₁₀₀ for NF₃ from 10,800 to 17,200 will significantly increase calculated emissions from chamber clean processes using *in situ* NF₃.

The other potential increase in emissions may come from the industry’s move to 3-D

interconnects. One of the technology options considered is a through-silicon via (TSV) etch process that uses large quantities of sulfur hexafluoride, the most potent greenhouse gas measured. The industry must track the development of 3-D interconnect technologies and make plans to mitigate emissions from TSV etch processes.

The PFOS Issue

Until recently, perfluorooctane sulfonate (PFOS) was widely used in photolithography and wet etches. It is a fully fluorinated compound with some unique qualities that are difficult or currently impossible to duplicate in critical applications such as lithography resists and anti-reflective coatings. So far, replacements have been found for only the PFOS-containing surfactants used in developers and wet etch formulations. Unfortunately, the same qualities that give it these unique performance characteristics lead to its persistence in the environment. It has been found that PFOS does not biodegrade, hydrolyze or photolyze[4]; consequently, it biomagnifies along the marine food chain.[5] It has been found in the blood of mammals from the Arctic to the Antarctica, including humans. Therefore, there are initiatives on state, national, regional and international levels to ban the use of PFOS. The U.S. Environmental Protection Agency recently amended the Perfluoroalkylsulfonate (PFAS) Significant New Use Rule (SNUR), adding the remaining 183 PFAS compounds on the Toxic Substances Control Act (TSCA) inventory that are not already on the SNUR, and limits their use in new applications.[6] Europe has undertaken several actions to restrict

| Compound | Lifetime | 3 rd | 4 th |
|---|----------|-----------------------|-----------------------|
| | | AR GWP ₁₀₀ | AR GWP ₁₀₀ |
| Carbon Dioxide | variable | 1 | 1 |
| Methane | 12 | 23 | 25 |
| Nitrous Oxide | 114 | 296 | 298 |
| Select HFC, PFC and SF₆ | | | |
| CHF ₃ | 270 | 12,000 | 14,800 |
| CF ₄ | 50,000 | 5,700 | 7,390 |
| C ₂ F ₆ | 10,000 | 11,900 | 12,200 |
| C ₃ F ₈ | 2,600 | 8,600 | 8,830 |
| c-C ₄ F ₈ | 3,200 | 10,000 | 10,300 |
| NF ₃ | 740 | 10,800 | 17,200 |
| SF ₆ | 3,200 | 22,200 | 22,800 |

Source: IPCC Third Assessment Report / Fourth Assessment Report

Table 1. GWP₁₀₀ for Compounds of Interest to Semiconductor Manufacturers

PFOS use and emissions including adding PFOS to Annex I of the Marketing and Use Restriction Directive 76/769/EC.[7] And the 118 signatories of the Stockholm Convention on Persistent Organic Pollutants (POPs) are evaluating PFOS as a possible addition to the POPs treaty.

REACH

The European Union's Registration, Evaluation and Authorization of Chemicals (REACH) regulation fundamentally changes the way that chemicals are regulated and used in the European Union. REACH places greater responsibility on all actors in the supply chain and, for the first time, requires upstream communications from the downstream users of chemicals (e.g., the IC manufacturers) to their suppliers. REACH requires that all new and existing substances manufactured or imported in quantities greater than 1 ton per year be registered. Registration is phased in over time depending on quantity and hazard. REACH has the potential to disrupt the supply chain, affecting the availability of critical manufacturing chemicals. Fab manufacturing facilities in Europe should ensure that all of their chemical suppliers are aware of REACH requirements and are addressing them. Of immediate importance are the following:

- Existing chemicals must be preregistered June 1–November 30, 2008. By preregistering, suppliers can take advantage of phased-in registration based on hazard and volume. After the preregistration period, chemicals that are not preregistered and are manufactured and/or imported by a supplier in quantities greater than 1 ton/year will require immediate registration.
- Registration requires development of a chemical safety report including an

exposure scenario detailing conditions of use and risk management measures for humans and the environment. The final technical guidance document on conducting a chemical safety assessment and preparing a chemical safety report will be issued on November 21, 2007.[8]

As we have seen in the case of the PFOS issue, new regulations in one region of the world can be quickly adopted by countries in other regions; thus, it is important that all device manufacturers keep abreast of the REACH requirements.

New U.S. Chemical Facility Anti-Terrorism Standards

In the face of the global terrorism threat, the U.S. Department of Homeland Security (DHS) has developed new rules that classify many manufacturing facilities in the U.S. as "Chemical Facilities." These rules became law on June 8, 2007. Under the new regulation, facilities using amounts of chemicals above threshold quantities are required to submit information for review to the DHS using its Chemical Security Assessment Tool. This information will be used to categorize a facility as either low or high risk. High-risk facilities will then be required to perform a Security Vulnerability Assessment following a specific DHS methodology and then prepare a Site Security Plan.

Each facility needs to check its inventory for the maximum quantity on-site at any one time against the thresholds published in Appendix A of the regulation. At the same time, purchasing practices and other methods of bringing materials onto facility property must be reviewed to ensure there are adequate controls and that management practices are being followed.

Failure to register a covered facility may

result in facilities being presumed to possess a high security risk. The consequences of further noncompliance can include significant fines and orders to close and cease operations until the facility is brought into compliance (see: 6 CFR 27.305 & 27.310).

More information on the U.S. Department of Homeland Security's Chemical Facility Anti-Terrorism Standards can be found on the DHS website at http://www.dhs.gov/xprevprot/laws/gc_1166796969417.shtm.

Industry Efforts

The industry has worked for over 15 years on several fronts to reduce emissions of PFCs. Following the familiar hierarchy of process optimization, alternative chemicals, recycle and abatement, the industry has largely moved from low-utilization chemicals like C₂F₆ to C₃F₈ to C₄F₈ to remote plasma NF₃ for chamber cleans. In parallel, the industry has developed some very effective abatement devices with 99.99 percent destruction removal efficiency to treat the remaining emissions. This has allowed the WSC members to commit to a Voluntary Agreement that will reduce semiconductor PFC emissions by greater than 90 percent by 2010 over the "no-action" scenario.[1]

Similarly, the WSC members have voluntarily agreed to minimize emissions of PFOS to the environment by incinerating all resist and anti-reflective coating waste and phasing out PFOS in noncritical applications.[9] The remaining amount of PFOS reaching the environment through aqueous developer waste is minute. In spite of that, the industry is studying technology options for removing PFOS from developer wastewater. For the long term, the industry is actively searching for alternatives to replace PFOS from the critical applications. As a result of this voluntary agreement and active communi-

cation between the SIA and ESIA and their respective regulatory agencies, the industry has been successful in obtaining exemptions for PFOS use for critical lithography applications in the U.S. and the EU.

In the case of the European REACH initiative, the SIA, ESIA and SEMI have mounted a major effort to involve the industry supply chain in proactively preparing for the mandatory registration of all of the chemicals that the industry uses. Eventually, chemicals that are not registered and authorized will not be allowed to be manufactured or imported into Europe. Because of globalization, this could seriously disrupt the industry's supply chain not only in Europe but elsewhere as well.

The anti-terrorism initiative will put an additional administrative burden on semiconductor manufacturing facilities. However, many facilities have already or are in the process of tightening security at their facilities in the face of this latest global threat.

Summary

The semiconductor industry considers environmental stewardship vital to the long-term sustainability of its business and has a history of proactively addressing any new environmental challenge facing the industry. The industry is successfully dealing with the latest global concerns such as PFCs, PFOS, REACH and terrorism. The various industry associations under the umbrella of the WSC are collaborating and coordinating their efforts worldwide to mitigate the impact of existing and emerging regulations on semiconductor manufacturing.

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Meeting the Climate Challenge: Applying Moore's Law to Reduce Greenhouse Gas Emissions From the Electronics Industry

Sébastien Raoux, Transcarbon International

Fluorinated Compound Emissions Reduction: Solutions Are Available Today, But Implementation Can Be Challenging

For the last 15 years, the semiconductor industry has taken a voluntary approach to reduce its carbon footprint. Besides indirect and direct CO₂ emissions from electricity consumption and stationary or mobile combustion sources, the majority of greenhouse gas emissions from semiconductor manufacturing plants originates from fluorinated compounds emissions (FCs[1]). FC molecules have long atmospheric life and high global warming potential (GWP), and they typically represent 50 to 90 percent of a Fab's carbon footprint. In 1999, the World Semiconductor Council (WSC) committed to voluntarily reduce FC emissions by 2010,[2] which spurred the development of cost-effective manufacturing solutions with up to two orders of magnitude lower carbon-equivalent emissions. Such

solutions have been demonstrated in production conditions and can be implemented today for chemical vapor deposition (CVD) chamber cleaning processes, and etch. Solutions range from optimization of processes, implementation of alternative chemistries, abatement or adoption of manufacturing technologies with higher FC utilization efficiencies. Through technology transfer activities, lessons learned in the semiconductor industry can and must be passed on to other sectors of the electronics industry; in particular, flat panel display (FPD) and photovoltaic (PV) devices manufacturing. While FC emissions from electronic products manufacturing only represent a small fraction of total greenhouse gas emissions, they contribute very effectively to carbon footprint reduction. For example, reducing emissions of one kilogram of SF₆ is equivalent to removing 22.8 tons of CO₂.

While most semiconductor manufacturing facilities built over the last five years have adopted the latest tools and processes with reduced emissions, lowering FCs from older Fabs presents a much greater challenge. This is because changing manufacturing processes with lower emissions can require significant R&D expenses, can disrupt production and often mandates costly and lengthy requalification of the final products. Further, older tools and process chambers might simply lack the design features to provide high FC utilization efficiency, and some tools or facilities may not be compatible with the retrofit of advanced technologies. For older Fabs, abatement may be the only feasible option, but such facilities may lack space or have limited amounts of water, electricity or fuel to install control technologies. Other technical and financial barriers may include the limited ability of a facility to treat increased amounts of gaseous and liquid HF waste resulting from the abatement – or the greater utilization efficiency – of FC gases. In brief, the financial and technological barriers to reduce FC emissions from older facilities can be significant.

Advanced Environmental Management Tools Can Be Used to Devise Cost-effective Strategies, and Sustainable Solutions Can Be Implemented

With three years left to achieve the 2010 WSC voluntary goal, operational and EHS managers are faced with implementing effective solutions to reduce the carbon footprint of their facilities, at the lowest possible cost. Naturally, the first step in this endeavor is to identify the largest sources of emissions and to prioritize action. Generally, CVD tools with in-situ CF₄ and C₂F₆ chamber cleaning will be the largest sources of emissions, and consequently

present the greatest opportunity for emissions reduction. CVD chamber cleaning processes using C₃F₈, c-C₄F₈ or C₄F₈O and etch processes typically represent the second-largest sources of emissions. CVD tools equipped with the NF₃ remote clean technology have very low FC emissions (up to 99 percent NF₃ utilization efficiency) and will produce minimal impact on the overall carbon footprint of the facility. The second step before implementing a strategy is to optimize the mix of solutions at the facilities scale. Here, the problem becomes quite complex, due to the large number of factors to be considered (costs, impact on production, natural and human resources, efficiency and productivity...) and the variety of solutions available.

Advanced environmental management systems (EMS) can be used to devise optimal strategies to reduce FC emissions.[3] By using statistical models to calculate costs and quantify the EHS impacts of mitigation solutions, one can analyze various scenarios at the recipe, the tool and ultimately the facility level. The complexity of such analyses arises from the large number of factors and the uncertainty or the variability associated with many input parameters (e.g., capital costs, cost of maintenance, variations in FC flows and recipes, etc). However, Monte Carlo simulations are very effective in dealing with uncertainties, comparing alternatives and assessing risks. Once a manufacturing process is accurately modeled, via Monte Carlo simulations or otherwise, metaheuristic procedures such as Tabu searches, neural network modeling and scatter searches can also be used to find globally optimal solutions to reduce FC emissions, according to criteria and goals set by the Fab manager. For example, such statistical analyses can predict that a solution to reduce FC emissions by 90 percent can be implemented

with a 95 percent probability that the total capital cost will not exceed a certain target, that the total water consumption will not go beyond what is available in the Fab, or that the cost per ton carbon-equivalent saved will be maintained below a certain threshold.

The Policy and Regulatory Landscape Is Changing Fast, But Be Prepared to Trade

Together with technical and cost concerns, policy and regulatory considerations are critical in defining sustainable strategies for addressing climate change. First and foremost, facilities managers should be able to estimate and report their carbon footprint, whether on a voluntary or mandatory basis. Labeling of products with a measure of their impact on climate will also soon become reality. While estimating and reporting emissions is a first and

saved is higher), Fabs can fund implementation of emissions reduction technologies, generate additional revenues and contribute to tackling climate change.

Implementation of emissions trading projects in the electronic industry will require the development of appropriate methodologies to ensure that emission reductions are real, quantifiable, verifiable and additional. In other words, a project developer must demonstrate that the emissions reduction would not have occurred in the absence of the emissions trading project, under a business-as-usual scenario. Such methodologies will also require an accounting accuracy superior to that of existing guidelines to estimate FC emissions from the electronics sector.[4] Adequate monitoring technologies and third-party verification must be adopted

It is crucial that legislators provide long-term and consistent frameworks to build the necessary confidence in the marketplace.

necessary step toward achieving a low carbon footprint, it is real reductions that count. To this effect, many existing or upcoming climate change legislations contain provisions for market-based mechanisms, designed to reduce emissions at the lowest possible cost. In particular, cap and trade regimes, whereby governments mandate an absolute reduction of emissions while relying on trading of credits between emitters to achieve an overall reduction goal, could prove very attractive for the electronics industry. Indeed, by allowing electronic manufacturers to reduce their emissions and sell carbon credits to other industries (where the cost per ton CO₂

to ensure transparency. In developing such market-based mechanism, it is also crucial that legislators provide long-term and consistent frameworks to build the necessary confidence in the marketplace. Finally, economic forces must drive implementation of projects where the cost of reducing emissions is the lowest, and the return on investment attractive for investors. In this respect, reducing emissions from electronics manufacturing could be very attractive, due to the high GWP of fluorinated compounds: At current prices per ton of CO₂, trading emissions credits for SF₆ can generate a monetary value 10 times the price of the chemical itself!

Implementing Moore's Law to Address Climate Change

As many of us have realized, it is critical that we move toward and beyond carbon neutrality. The electronics industry can play an important role in developing and implementing technologies and methodologies to reduce emissions. Imagine applying Moore's Law to climate change: doubling carbon emission credits every 18 months while reducing costs by 50 percent! Such a goal could be achieved in the not-so-distant future, in part if the industry embraces market-based mechanisms to reduce emissions. Already, visionary companies are participating in voluntary – but legally binding – trading markets, such as the Chicago Climate Exchange (CCX). The first Clean Development Mechanism (CDM) projects could be implemented in Asia in the next 18 months, as part of the Kyoto Protocol. Fabs in Europe could participate in Joint Implementation projects and directly contribute to the European Emissions Trading Scheme (ETS) by reducing FC emissions. Whatever business, technical and regulatory path we choose, our industry can pave the way toward technology-oriented and sustainable approaches to address climate change. And when it comes to address serious issues, let's take early action; this industry is not afraid of innovation and change.

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fluorine...). While the vast majority of FC molecules are gaseous at room temperature and atmospheric pressure, some FCs such as C₅F₁₂ and C₆F₁₄ are used as liquids for heat transfer applications.

2. The World Semiconductor Council (WSC) committed in 1999 to reduce PFC emissions 10 percent below regional baselines, by 2010. For Europe, North America and Japan, the baseline year is 1995. For Korea it is 1997 and for Taiwan it is 1998. Estimates indicate that approximately 90 percent of the global integrated circuit manufacturing is currently committed.
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4. 2006 Intergovernmental Panel on Climate Change (IPCC) Guidelines for National Green House Gas inventories – Vol. 3, Chap. 6; <http://www.ipcc-nggip.iges.or.jp/public/2006gl/ppd.htm> ■

About the Author

Dr. Raoux is the president and CEO of Transcarbon International, an independent consulting firm helping clients implement sustainable development practices, and move toward and beyond carbon neutrality. He is a co-author of the 2006 IPCC guidelines on reporting FC emissions from the electronics industry.

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Fab Connectivity

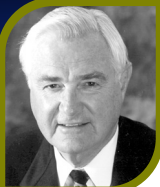
Practical Considerations of Implementing R2R Controllers – Part 1: Basics of Feedback and Feedforward Controllers

Karen Finn¹, Katherine Thorn² and Manish Misra² – ¹K Finn Consulting, Inc. ²University of South Alabama

Recipe Management Challenges for a Mainstream Fab

Don Phillips
Avago Technologies

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C. Richard Deininger

General Partner, Taylor-Deininger Partners, Inc.

Fab productivity may seem like a dull subject, but there is hidden gold buried inside the operations by doing things the way they have always been done. You get the same result every time you do things the same way. There are simple, straightforward, low-cost steps that can be implemented to lower costs and improve the operation, the fab productivity and the profitability at the bottom line. We hope to illustrate what to do to economically mine that gold.

There are two papers in this section for this quarter, which discuss approaches to improving fab productivity. The first deals with "Practical Considerations of Implementing R2R Controllers." The second deals with "Recipe Management Challenges ..." to improve cycle time and yield. Both of these capabilities are so critical to running an efficient, productive fab, that it is hard to

understand why they have not become ubiquitous in fab operations. What is holding the fabs back?

There are commercial offerings to address the capability, and the cost benefit typically is measured in months. The benefits have been well-proven over and over again. The business reward is too compelling to ignore.

There are numerous other straightforward economical steps that can continue to help with productivity improvements with results that fall directly to the bottom line, even in older, well-established fabs. These capabilities will be described in future issues.

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Practical Considerations of Implementing R2R Controllers – Part 1: Basics of Feedback and Feedforward Controllers

Karen Finn¹, Katherine Thorn² and Manish Misra²
¹K Finn Consulting, Inc. ²University of South Alabama

Abstract

Most semiconductor manufacturers consider run-to-run (R2R) control a vital component of high-yielding production. However, many still consider the development and implementation of these controllers as a "black box" process. This article is in two parts, wherein Part 1 primarily presents an overview of common R2R terminology along with the basics of feedback and feedforward controllers, and Part 2 will provide an in-depth analysis of a checklist to aid the reader in developing and implementing R2R controllers and thereby demystify them.

Terminology

As with any technology, part of R2R control's mystique is in its jargon. This section will define some basic R2R terminology.

An R2R controller, as its name implies, provides control on the basis of one run to

the next. A run is any complete single processing on a piece of equipment or the processing of all the wafers in a lot. The complete single processing may include several process steps for a single-wafer process tool. So a run can be a lot, a wafer, a boat, a batch, etc.

In order to control a process, its input and output variables and their relationship must be identified.

- Input variables describe the effect of the external world on the process
 - Manipulated variables can be systematically changed to affect at least one controlled variable
 - Disturbance variables are either measured or unmeasured and are fixed at the controlled process
- Output variables describe the effect of the process on the external world and can be either measured or unmeasured
 - Controlled variables are measured outputs whose value can be affected by at least one manipulated variable

From these variables, a process model is developed by determining the relationship between the inputs and outputs.

A rough measure of the complexity of the R2R controller needed for a process is determined by counting the number of manipulated and controlled variables. If a process has only one manipulated variable

and one controlled variable, it is a Single Input Single Output (SISO) process. If the process has multiple manipulated variables and only a single controlled variable, the process is a Multiple Input Single Output (MISO). (For semiconductor processes, it is typically difficult to develop a successful MISO controller, and the control engineer

will usually be more successful with a SISO controller for this type of process or perhaps a different SISO controller applied to different operating scenarios or regions.) Finally, if the process has multiple manipulated and controlled variables, it is a Multiple Input Multiple Output (MIMO) process.

R2R controllers improve process results by better targeting and reducing the variation of the controlled variable(s) by adjusting the manipulated variable(s). The controller adjusts the manipulated variable(s) on the basis of the process model and the availability of measurements. If the manipulated variable(s) are adjusted based on the controlled variable(s) measurements, the R2R controller is termed as a feedback (FB) controller. An FB controller makes adjustments after the process is affected by a disturbance and is therefore a reactive type of control. If the manipulated variables are adjusted based on disturbance measurements, the

controller is a feed-forward (FF) controller. An FF controller is proactive because it makes adjustments before the system is affected by a known disturbance. These controllers are not mutually exclusive and can be used simultaneously on the same process. If FF & FB are used simultaneously, the FF portion of the controller will adjust for known disturbances to the system and the FB portion will adjust for unknown disturbances. See Table 1 for the pros and cons of each of the three controller types and Figure 1 for a graphic depicting these controller types.

Basic R2R Control Checklist

Reaping the benefits of R2R control requires five basic ingredients:

- Process model
- Reliable measurements
- Equipment automation
- MES connection
- Controller development and implementation

| | Pros | Cons |
|--------------------|---|---|
| FB | Does not require knowledge and measurement of disturbances | Waits until the effect of the disturbance has been felt by the process before taking action |
| | Insensitive to modeling errors | May create instability in the process |
| | Insensitive to parameter changes | Unsatisfactory for slow processes or those with significant dead time |
| FF | Acts before the effect of known and measured disturbances are felt by the process | Requires identification and measurement of all disturbances which are to be compensated for |
| | Does not introduce instability | Is sensitive to process model inaccuracies |
| FF & FB | Acts before the effect of known and measured disturbances are felt by the process | May create instability in the process |
| | Does not require knowledge and measurement of disturbances | |
| | Insensitive to modeling errors | |
| | Insensitive to parameter changes | |

Table 1. Pros and Cons of FB and FF Controllers

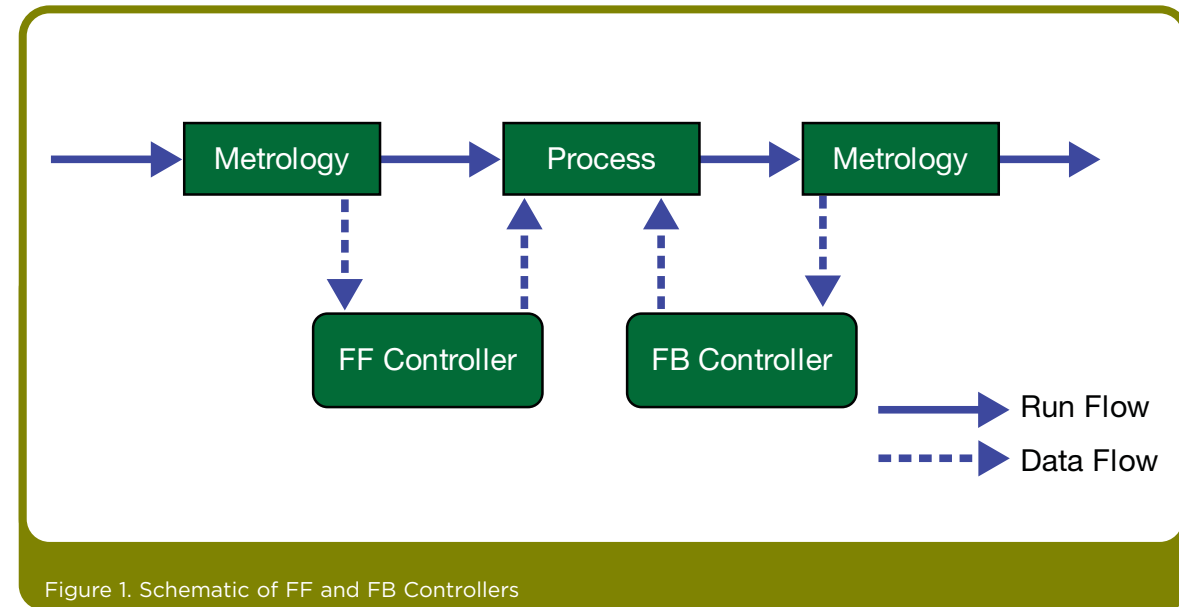


Figure 1. Schematic of FF and FB Controllers

| PROCESS MODEL | | |
|--|---|---|
| Understand the Process | What is happening in the process? | |
| | What is the operating region? | |
| | What are the constraints on the process? | |
| | What are the assumptions about the process? | |
| | How and why are the recipe parameters chosen and set? | |
| | How does the recipe relate to the process to be controlled? | |
| | What are the concerns and constraints the engineers, technicians and operators have with respect to the process? | |
| Gather Process Data | What are the process recipe parameter settings? | |
| | What input data is available? | |
| | What output data is available? | |
| | Are there enough historical data to build a model or is a design of experiments (DOE) required? | |
| | Are the data valid? | |
| Fit a Model to the Data | What model granularity is needed? | |
| | <ul style="list-style-type: none"> • Process • Recipe • Part • Chamber • Process Tool • Metrology Tool • Reticle • Consumable Batch • Etc. | |
| | What is the tolerance for a good fit? | |
| | RELIABLE MEASUREMENTS | |
| | Validity | Are the stand-alone metrology tools matched? |
| | | How are data checked for outliers? |
| | | Is this level of validity appropriate for the controller? |
| Availability | When are the measurements available? | |
| | How will this affect the controller? | |
| | What business rules must be in place to accommodate the availability of measurements? | |
| | How will the measurements get to the controller? | |
| EQUIPMENT AUTOMATION | | |
| | Is data collection automated? | |
| | Is recipe selection automated? | |
| | Is recipe download automated? | |
| | Is the recipe parameterized? | |
| | When can the control move be implemented? | |
| MES CONNECTION | | |
| | How can context information be made available to the controller? | |
| | How do lots get routed to tools? | |
| | When can the control move be implemented? | |
| CONTROLLER DEVELOPMENT AND IMPLEMENTATION | | |
| Controller Development | What is the controller objective? | |
| | What is the simplest controller to meet the control objective? | |
| | Do the control moves need to be dampened? | |
| | Is the controller tuned? | |
| | Can the controller be retuned after installation? | |
| | Is a user interface required? | |
| | What are the data storage requirements? | |
| Controller Installation | What is the path of installation? | |
| | <ul style="list-style-type: none"> • Manual control • Suggestion control • Monitored control • Automatic control | |
| | What training is needed for the fab personnel? | |
| | What controller reliability is needed? | |
| Controller Use | How is the controller being monitored? | |
| | How are new models created? | |

Table 2. Basic R2R Control Checklist

Table 2 presents a basic R2R control checklist which is organized by these ingredients. The checklist is presented in the form of questions to emphasize the need to gather information and to stimulate the reader to develop other questions more specific to their control development situation.

Summary and Conclusions

This article has presented some basic terminology and an analysis on feedback and feedforward controllers to help demystify R2R controllers. While the essentials of the R2R checklist were introduced in this paper, Part 2 of this paper will provide a detailed analysis on the major sections of the R2R checklist.

Resources

Finn, Karen and Manish Misra, AEC/APC 2005 Tutorial: "An Introduction to APC for New Process Control Engineers and Managers." ■

About the Authors

Dr. Karen Finn

Dr. Karen Finn has over 10 years' experience in managing the development, deployment and maintenance of APC systems for a variety of semiconductor manufacturing environments. She was a senior manager of corporate development at Micron Technology, Inc., and an APC manager at Motorola's

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Dr. Manish Misra

Dr. Manish Misra performs systems engineering research in developing real-time fault prediction systems and run-to-run controllers. He was a professor of chemical engineering at the University of South Alabama and has several years of work experience in APC for semiconductor manufacturing fabs. Dr. Misra holds a doctorate in chemical engineering from The University of Texas at Austin.

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Recipe Management Challenges for a Mainstream Fab

Don Phillips, Avago Technologies

Abstract

In order to improve cycle time and increase yield in a mainstream fab, automated recipe management is essential. There are challenges to overcome in order to successfully implement a recipe management system, but they are not insurmountable. The business reward for accomplishing such a project is too compelling to ignore.

Fab organizations worldwide have one thing in common: All fabs continually strive to reduce cycle time and increase yield. To improve performance in both of those areas, it is essential to put automation in place to simplify and bulletproof the process. A solid process ensures that the odds of correctly processing any given lot are weighted in favor of the fab operator. In a large fab with a low product mix where each process can be given a dedicated set of tools, the challenges center more around the correct setup and regular maintenance of a particular tool, as well as ensuring that lots are processed on an appropriate tool at a given point in the process. In a fab with a higher product mix where a single tool may not be dedicated to a particular process, an additional challenge is added. In that type of an environment you must not only ensure

that the lot is at an appropriate tool at any given time and that the tool is in an appropriate state to run, but you also must ensure the correct recipe is run for that lot. With a high product mix in a fab, recipes can and do change from lot to lot all day long. Successful management of that change is absolutely essential if the goal of higher yield is to be obtained.

Recipe management can be subdivided into two areas: recipe name management and recipe body management. Recipe name management involves making sure that for a given lot, the correct recipe on the tool is used. Recipe body management involves making sure that when a particular recipe is selected, the contents of the recipe have not been corrupted accidentally or changed intentionally from the series of instructions that are intended for the lot that is about to be run.

Both areas of recipe management face challenges in mainstream fabs where existing tools are often leveraged and effectively used. There are tools in operation that have embedded, vendor-specific operating systems, tools running on various Windows varieties from 3.11 to XP, tools on various UNIX varieties and even some that run OS/2. This issue is somewhat mitigated by the presence of the GEM, SECS and HSMS standards and protocols. As long as the tool supports at least the GEM and

SECS protocols, automated recipe selection can be implemented in a fairly straightforward, though sometimes elbow-grease intensive manner. If the tool does not support those standards, things get tougher. Recipe name management can still be achieved to a certain extent by using equipment such as programmable logic controllers or other means of creating an interface with the tool, and then using that interface to control which recipe is selected on the tool.

Achieving recipe body management requires overcoming additional hurdles and is a much less straightforward problem. One of the challenges that complicate the issue is the failure of the SECS communication standard to define something that would allow for retrieving information about a recipe without actually retrieving the entire recipe. Something along the lines of a checksum or the ability to check the recipe size and last modified date would greatly simplify things, but in the absence of that, a different approach is required.

Fortunately the issue of recipe uploads and downloads is addressed in the standard. That functionality is far more crucial than the recipe information retrieval but it comes with its own set of problems. Here the issue of the differing tool interfaces crops up again. Some tools make use of text recipes and other use binary recipes. Some require that you select an appropriate directory prior to uploading or downloading a recipe, and others keep all the recipes in a single directory. This issue is by no means a showstopper, but it does add a level of complexity to implementation of recipe body management.

Since recipe body verification is not addressed in the SECS standard, use of the recipe upload and download functionality is necessary in order to verify the contents of the

recipe are correct. The next issue that crops up then is the issue of the time required to either send the recipe to the tool or retrieve the recipe from the tool. If the recipe is too large, the amount of time necessary to perform that action may result in loss of operator attention, and could potentially result in a negative impact on cycle time. There are various ways that this can be overcome or mitigated for tools that take too long to accomplish recipe upload or download. The most foolproof way to deal with this issue is to utilize HSMS communication for tools that support it. Plenty of older tools have no support for that standard, however, so more creative approaches may be necessary for tools with large recipes but with slow communication speeds. Depending on the tools used in a particular fab, it may be the case that some tools which can achieve recipe name management cannot achieve recipe body management.

Recipe management in a mainstream fab is not an easy, slam-dunk type of project. There are challenges to overcome in order to successfully implement recipe name management and recipe body management, but they are not insurmountable. The business reward for accomplishing such a project in a mainstream fab is too compelling to ignore. ■

About the Author

Don Phillips has been an engineer with Agilent Technologies, Inc. and Avago Technologies. He has seven years of experience in the software industry, with the last three focused in the area of fab automation as a manufacturing engineer.

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Supply Chain Management

No Middle Ground

Carl Johnson - Infrastructure

ERP for Dummies

Chris Howington and Chris Welch - Freescale Semiconductor

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Greg Westby

Purchasing and Materials Manager, Integrated Device Technology

The need for Y2K compliance introduced any of the rest of us to the idea of a "suite" of software that could be deployed across multiple functions of a company providing an interdisciplinary solution to the then "stand-alone" systems. The acronyms for these systems have changed over time and today are commonly known as ERP or Enterprise Resource Planning systems.

In "ERP for Dummies," an ERP system is defined in a very simplistic but spot-on way. The key to the system indeed begins with the understanding of demand. Unfortunately, this can be the exact same place where these systems can cause trouble - remember the term "garbage in garbage out?" To understand demand, you introduce an element that is not automated. Demand is forecasted and then judged to account for an array of validation, all in the name of

protecting market share. This then is what is loaded into the ERP system and from here is where these systems add value. However, feed a bad number into an ERP system and it will respond accordingly.

In "No Middle Ground," we are reminded again of the cyclical nature of the semiconductor business. Partly to blame is our own propensity to overbuild based on the forecasted demand. The author more specifically addresses the silicon markets consolidation. I'm reminded of this daily when I look across our parking lot and see a new business taking over what was once a silicon grower that never went into full production before shutting down. If you're wondering what took its place ... a solar wafer producer.



Chris Howington

Supply Chain Re-Engineering Manager, Freescale Semiconductor

The definition of understatement: "The supply chain activity in the semiconductor industry is very dynamic." Thanks for the information, Mr. Obvious.

We all commiserate around the facts that we cannot achieve stable demand; are continually challenged with technical hurdles; and pray that we do not get hit with that next catastrophic event. If you have any time under your belt in this industry, you know of three sure things: death, taxes and that your supply chain plans will change tomorrow.

In Carl Johnson's article, he points out some results of our industry business that many of us have experienced: consolidation of players and diversification of product lines. This leads to constant questions of the viability of our older fabs and technologies and how we can best utilize them (or not). These market dynamics impact not just at the

fab level, but also direct material and equipment providers.

As a part of supply chain management, Enterprise Resource Planning systems are supposed to help. While the systems themselves are no panacea for solving the wild swings in business, and certainly have their critics, they are designed to be able to react to the changes in a systematic way. In the semiconductor industry, fabs themselves are the lion's share of resources for most companies. Whether you use SAP or Oracle or any number of other applications available, fab management teams need to be aware of their part in the bigger picture of company resource planning.



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No Middle Ground

Carl Johnson, Infrastructure

Everyone knows the semiconductor business is inherently cyclical. That cyclicity reaches all the way down to the silicon producers. During the late '90s and the early years of the current decade, silicon producers have seen wild profit vacillations due to capacity/supply demand imbalances.

When we take a brief look at the recent history of the silicon business, we can see how attitudes and strategies have evolved. Prior to 1990, people believed that wafers were just that: just wafers. When the industry moved to < 1 micron feature

first half of '04. The silicon shortage in '04 was followed by an inventory correction in the semiconductor business.

Following the semiconductor inventory correction, the move to < 90nm prompted a change in thinking – wafers were a critical element. Flatness specifications became very important, the use of strained silicon became prevalent and, of course, came the migration by leading-edge manufacturers to larger diameter, 300 mm wafers.

The move to < 65nm device production has ushered in an era that requires new silicon substrates – polished and epitaxial,

Right after the burst of the '00 technology bubble, there was a large drop in silicon wafer production/utilization - almost a 50 percent drop from Q1 '00 to Q1 '02.

sizes, the silicon players started paying attention. Money was made in the early '90s but, per usual, an overcapacity situation was reached in the latter years of that decade.

Right after the burst of the '00 technology bubble, there was a large drop in silicon wafer production/utilization – almost a 50 percent drop from Q1 '00 to Q1 '02. The collapse forced silicon-producing companies to underinvest, and a shortage appeared in the

annealed, strained and SOI. This trend of enhancing wafer substrates should continue through 2010. Every manufacturer requires wafers that are a bit different. By the end of the decade, it is estimated that over 3K specifications will be required. The number of specifications stood at 1K just a few years ago.

Most recently, the use of polysilicon by the solar industry has the silicon community racing to add capacity. This emergence of

solar cell production as a viable sales channel is wreaking havoc with those manufacturers that process smaller diameter wafers.

What Happens Next?

Those that have been looking for a consolidation or, shakeout, in the semiconductor manufacturing community, the equipment industry and the materials supply chain, should not be surprised by the changes taking place in the silicon wafer business. The trend is clear: The number of suppliers is contracting. Today there are six major players and there may

large markets – often larger than \$1 billion in size – before they even start to recoup what they have invested in initial design. And, to top it off, the costs associated with the development of the next product generation should be considered, because most companies do not want to be one-hit wonders.

Semiconductor capital equipment companies are diversifying their product lines to address other markets (solar and flat panel display) because their customer base for the most advanced semiconductor equipment is narrowing. The subsystem supply chain that supports the OEMs has not gone unscathed. A number of firms

What we are seeing take place in the silicon business dovetails with trends that will soon take hold in other parts of the semiconductor supply chain.

be less than four in the near future. At one time there were over 20.

What we are seeing take place in the silicon business dovetails with trends that will soon take hold in other parts of the semiconductor supply chain. IC makers that cannot afford to stay in step with Moore's Law are outsourcing advanced production to foundries (Texas Instruments and Advanced Micro Devices are two of the largest names in this category). Many of the "traditional" semiconductor markets (DRAM, MPU, FPGA, Graphics) are closed to new entrants. Nonrecurring engineering (NRE) costs, meaning the cost to design a chip and get it taped out and ready for production, are going higher – particularly as we move to smaller and smaller dimensions. By some estimates, NRE costs to produce one leading-edge device exceed \$200 million. This means these devices must address very

have dropped completely out of the market because they cannot compete with the R&D requirements. Others have made it blatantly clear that they want to diversify their product lines away from semiconductor manufacturing and into the medical, biotechnology, solar and flat panel display industries.

Right along with the silicon market, specialty materials companies are faced with R&D challenges that are pushing decision makers to question whether or not they want to be part of the supply chain. This chain includes the business of delivering and developing process materials, including CMP consumables, bulk and specialty gases, graphite, quartz, sputtering targets, masks and reticles, photoresists, lithography ancillaries, silicon carbide, wet chemicals, advanced dielectrics, advanced metallization, and packaging.

Longer Term

The majority of this paper has been focused on the changes that have gripped the silicon business. Longer term, there are some difficult challenges to be addressed by the semiconductor device manufacturers and the OEMs that supply the equipment for the fabs. Clearly, in the case of the newer leading-edge factories, the focus is on capital expenditures and return on investment (ROI). In the case of the more mature fabs, the focus moves to the operating expense line.

This creates a set of questions that the industry must soon address:

Given the narrowing of the industry and the intense focus by larger companies on the most advanced process technologies, can we expect to see more collaboration at the less-advanced levels of the semiconductor food chain? Will that collaboration between the OEM/subsystem/materials supplier and the customer result in

solutions that are well-matched to the needs of companies that manufacture devices with larger geometries, on smaller wafers? ■

About the Author

Carl Johnson is director of research for Infrastructure (www.infras.com). He has editorial responsibility for all content. His Wall Street experience includes seven years with Merrill Lynch and three years with Piper Jaffray, Inc. As an analyst with Infrastructure, Carl has studied the semiconductor, semiconductor equipment and materials industries.

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ERP for Dummies

Chris Howington and Chris Welch, Freescale Semiconductor

Enterprise resource planning (ERP) systems are designed to integrate most business data and processes of a company into a unified system. In the semiconductor manufacturing industry, wafer fab manufacturing comprises a large portion of resource requirements for most companies, from both human and equipment capital standpoints. With this large investment, it is incumbent upon the fab management team to understand how the fab fits into the overall ERP picture, and how it can positively impact corporate financial performance and overall customer satisfaction.

Enterprise resource planning represents the latest evolution in business management

make timely and accurate decisions. Functions ERP is designed to manage include manufacturing, distribution, invoicing, inventory and accounting aspects of a company, as well as other support functions. The ERP term evolved from manufacturing resource planning (MRPII) as the cost and complexities of capacity planning increased – especially for semiconductor manufacturing companies.

Two major components of supply chain planning within an ERP system are resource planning and master production scheduling.

As a part of resource planning, sales & operations planning (S&OP) is a key process that aligns the sales plan, the production plan, the research and development plan

Two major components of supply chain planning within an ERP system are resource planning and master production scheduling.

concepts. As competitive pressures to improve cost and speed increase, the need to integrate a company's systems and processes increases as well. This integration is aimed at supplying each functional area in the company the information needed to

and the financial plan for companies. It facilitates managing critical resources (i.e., capacity, inventory and cash) based on how each of those items impact the sales/demand plan. Usually, this is a monthly process, but may be more or less frequent,

depending on the demand volatility and capacity complexity of a given company.

The S&OP process begins with understanding demand – the force that drives activity, inventory and cost for any business. A demand plan stated in terms of product groupings or families is the beginning of the process. This plan is a product of forecasts through collaboration with customers combined with “judgment” from the overall market and economic perspectives. Furthermore, current inventory levels must be understood and the need for increases or decreases determined, in line with service strategy and inventory cost plans.

To determine the feasibility of supporting the demand plan, each company must understand both its capacity and inventory position. Capacity plans are another critical component to the S&OP process, and are typically managed at aggregate levels or “families”: Wafer Technology families, assembly package families and product testing families. Each manufacturing site publishes a monthly update to the capacity statement at the appropriate “family” level, for comparison to each new monthly demand plan. It is important to remember external capacity – whether foundry or subcontract – and that it must be included in the overall capacity plans.

The demand plan and capacity plans are then compiled and analyzed using rough-cut capacity planning (RCCP) to understand how much of the demand plan can be supported with current capacity. Two important results are derived from this comparison: 1) disconnects between demand and capacity plans are identified and considered for capacity development in line with the corporate manufacturing strategy; and 2) there is a creation of a

production plan that becomes the commitment of manufacturing resources along with the identified products from the demand plan supported from the RCCP process.

The production plan provides the capacity and inventory boundary conditions for the master planning process. The master production schedule (MPS) is maintained by the master planner at the finished goods device level in weekly buckets, typically as far out as 26-39 weeks from the current week. The job of the master planner is to keep inventory, demand and capacity effectively balanced – decisions are made daily to stay in alignment with actual orders and demand changes, including those that differ from the original demand plan. While the production plan is usually the baseline plan for master production schedules, these schedules must be closely managed and modified in reaction to actual demand (customer orders, as opposed to customer forecasts).

The master production schedule also provides the initial information to the order acceptance process. The MPS dictates available to promise (ATP) for use in committing delivery to customers. ATP is a future projection of the availability of finished goods for shipment to the customer taking into consideration the MPS quantity minus what has already been committed to customers. Thus, delivery commitments can be made when a new customer order is received – an important customer responsiveness benefit.

For fab manufacturing in a semiconductor company, there are at least four key elements that must be managed well in order to support effective ERP processes: capacity statements, schedule validation, planning attributes and performance to schedules.

Capacity management must simply, but effectively represent capacity for ERP. The most common form is to have capacity as wafers per week by wafer technology with trade-offs amongst technologies. While this statement cannot perfectly represent Fab capacity, static and dynamic capacity modeling processes are important to provide the best possible statement for ERP.

Schedule Validation allows the opportunity to validate that the capacity statement is correct by reviewing the wafer starts schedule from the MPS process versus capacity models. The goal of most planning within ERP is to provide the best possible capacity feasible schedules; however, it is normal to have an intervention process to modify a schedule if the schedule violates current capacity constraints.

Planning Attributes include cycle time and yields. These attributes are an input into the ERP engine that helps drive proper schedules. A solid statistical view of recent actual performance, plus consideration of current activity, should be reviewed on a regular schedule with attributes adjusted accordingly. Standards must be set for each planning attribute in accordance with inventory and delivery goals.

Finally, **Performance to Schedules** is a crucial measurement for fab manufacturing. On-time delivery in the proper mix and volume are standard metrics for fabs. Performing well in these metrics drives delivery satisfaction for customers and allows for good inventory control.

Enterprise resource planning is commonplace in semiconductor manufacturing companies. The fab management team that is actively engaged in the company ERP processes will gain better understanding of how their factory resources are planned in the overall company resource picture. ■

About the Author

Chris Welch has worked in the supply chain management field for 21 years – all in semiconductor manufacturing. He joined Motorola Semiconductor in 1986 after graduating Cum Laude from Arizona State University with a B.A. in materials management. He has held management positions in master planning and customer service manager and currently is the planning manager in the Freescale Chandler, Arizona wafer fab.

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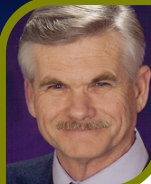
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Dan Cowles, Scott Anderson and Hugh Gotts - Balazs Analytical Services, a Division of Air Liquide Electronics U.S. LP

Recent Developments in Airborne Molecular Contamination Control

Andreas Neuber - M+W Zander FE GmbH

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Bill Funsten

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Keeping an Eye on the Invisible

Particle control is probably the first thing that comes to mind when we think of contamination control. However, molecules in the air, even in low ppb concentrations, beyond our sense of smell, can also be detrimental to device yield. While we know to control smaller and smaller particle sizes as technologies progress, our awareness of the impact and ability to control corrosives and condensable contaminants in the air has lagged behind.

Chlorine from nearby swimming pools and cooling towers, to sulfur from bird droppings on air-intake louvers could be contaminating sources. Fabs that had a clean bill of health at one point in time are in jeopardy of unexplained yield excursions unless continually monitored.

Process and facility engineers may not be aware of device sensitivities and whether or not air-handling units have effective chemical filtration. Chemical filters in older fabs, even if part of the original installation, may have been pulled out or neglected as part of cost reduction efforts.

The good news is that, although there are dozens of potentially contaminating molecules in the air, chemical filtration works! Another piece of good news is that monitoring equipment sensitive enough to measure critical AMC levels is becoming more affordable, easier to operate and maintain, and is providing more real-time feedback.

The articles included in this FEO edition give a good overview of AMC concerns and the monitoring techniques with the sensitivity required for peace of mind. Have you seen what's in your fab's air lately?

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Advances in Real-Time Airborne Molecular Contamination Monitoring

Dan Cowles, Scott Anderson and Hugh Gotts
Balazs Analytical Services, a Division of Air Liquide Electronics U.S. LP

Abstract

The semiconductor industry is moving toward data on demand to monitor the levels of cleanroom contaminants. No single (or simple combination of) instrument(s) is available today that is sufficiently sensitive, absolutely selective and reliable to meet the requirements and provide the required on-line monitoring of all desired airborne molecular contamination (AMC) present in semiconductor fabs. However, on-line monitors are rapidly improving, and we present here a review of the monitoring requirements and the tools that can address these requirements.

Airborne molecular contaminants (AMCs) at critical levels cause yield issues at all technology nodes in the semiconductor industry. Semiconductor fabs have long had monitoring programs that have taken advantage of grab or point sampling to understand the environmental load of these critical contaminants. While these sampling programs have been useful for determining the target levels of AMCs (see Table 1) and have been able to provide the ultimate in

required sensitivity, this type of monitoring only provides a snapshot of the diurnal or weekly changes in contaminant levels.

A large variety of techniques exist which may be utilized to provide continuous monitoring of AMC levels. These analytical tools need to be cost-effective, compact, require little operator intervention, be self-calibrating, and offer multipoint testing, which is a very tall list of requirements. The following provides a list of techniques that may begin to meet some of these requirements.

Surface Acoustic Wave (SAW)

Acoustic wave sensors were used in the '50s as quartz crystal microbalances. Later, in the '70s, surface acoustic wave sensors were applied toward chemical sensing, and the latest SAW technologies can measure mass changes of less than 0.02ng/cm²/Hz with a 1-minute sampling interval. One advantage that SAW technology holds is its ability to provide data that is directly relatable to how AMC affects the surface of interest. SAW devices can be fabricated from SiO₂ or copper and thus can be directly related to what is happening on the surface of the semiconductor product or

photolithography optical components. This technique measures the gas-phase contamination which accumulates on a surface, but cannot identify the adsorbing molecular species. SAW sensors provide a measurement of surface molecular contaminants (SMCs) and are utilized as a gross (although sensitive) measure of contaminant levels.

Chemiluminescence (CL)

Chemiluminescence has been promoted by several analytical companies as a sensitive and mature method for the *in-situ* analysis of NOx and many molecular bases (MB: NH₃, NMP, amines). Indeed, this technique has been shown to provide low ppb DLs for these nitrogen-containing compounds by reacting their nitrogen into NO and then converting the nitric oxide with ozone into the "excited" NO₂* followed by collecting the subsequent luminescence radiation. The method is destructive and potentially generates ozone, which is undesirable in the cleanroom environment. This technique is restricted to nitrogen-containing molecules, and cannot be applied to most of the MC and MA compounds on

the SEMI list, significantly diminishing the usefulness of CL techniques for real-time AMC monitoring.

Ion Mobility Spectrometry (IMS)

Ion mobility spectrometry is widely utilized, and its acceptance is growing as a portable analytical technique. In IMS, analyte vapors are ionized and the resulting ions are characterized using a drift tube at atmospheric pressure in the presence of a drift gas, typically air or nitrogen. One of the significant advantages of IMS is its capacity to operate at atmospheric pressure with no moving parts. This is unlike traditional mass spectrometry, which operates at reduced pressure and requires bulky and expensive vacuum pumps. As is the case in traditional mass spectrometry, the direct analysis of analyte mixtures using IMS leads to complex spectra which may be challenging to interpret either quantitatively or qualitatively. Some manufacturers have used mathematical algorithms and chemometric data-treatment methods to deconvolve mixture mass-spectra in real time. Other approaches involve the forfeit of real-time data in favor of "near-real-time"

| Material Category | 1 ppt | 10 ppt | 100 ppt | 1,000 ppt | 10,000 ppt |
|---------------------|-------|--------|---------|-----------|------------|
| Acids | MA-1 | MA-10 | MA-100 | MA-1,000 | MA-10,000 |
| Bases | MB-1 | MB-10 | MB-100 | MB-1,000 | MB-10,000 |
| Condensables | MC-1 | MC-10 | MC-100 | MC-1,000 | MC-10,000 |
| Dopants | MD-1 | MD-10 | MD-100 | MD-1,000 | MD-10,000 |

Table 1. SEMI F21-95 AMC Classification of Semiconductor Cleanroom Environments and Measurement Equipment Performance

data by using “fast-GC” or by simply adding a GC to pre-fractionate the sample mixture and deliver analyte constituents individually to the ion mobility spectrometer. Thus, the fast-GC option for IMS serves to simplify the complexity of the resulting ion mobility spectral data at the cost of increased analysis time and instrumental complexity.

Unfortunately, even though sensitive enough, this analytical technique is not selective for most of the tabulated

FTIR systems to be sensitive to the low ppb level, sufficient for continuous AMC monitoring. These sensitive measurements typically require cryogenic or thermo-mechanical cooling of the detector. Several manufacturers (MIDAC, Thermo Nicolet, MKS, Horiba, Bruker, Varian) offer instruments that could deliver real-time performance sufficient for the individual on-line analysis of many MA, MB and MC compounds.

Among the major disadvantages of FTIR, besides the low sensitivity to a limited number of compounds, is the difficulty of quantification of similar compounds

molecules and is known to often generate spurious ghost signals, especially in the cases of complex mixtures. There have also been reported problems with analytical windows not sufficiently narrow to discriminate the signal from an overlapping compound. This technique has found a niche application for the analysis of ppb levels of ammonia in lithography areas.

Fourier Transform Infrared Spectroscopy (FTIR)

The majority of the molecular airborne compounds of interest exhibit large infrared absorption cross sections, and this technique is one of the most commonly used real-time monitoring techniques for molecular air pollutants with abundant commercial equipment available. The high quality of modern multipass closed cells (ranging in path length from 10 to 100 m), along with substantial progress in the design of low-noise near and mid-IR detectors, allows many of the cutting-edge

Among the major disadvantages of FTIR, besides the low sensitivity to a limited number of compounds, is the difficulty of quantification of similar compounds (e.g., amines), because of their similar IR spectra. In a real-world air matrix, overlapping bands from different species produce interferences in various spectral intervals. In order to identify the compound, extensive and reliable reference spectral libraries and specialized software are required to deconvolute the spectra.

Open-path FTIR (OP-FTIR) leverages massive path lengths to achieve high sensitivity, and is mainly utilized for fenceline analysis of airborne pollutants around plants and factories. The use of OP-FTIR for AMC analysis in the cleanroom does not appear to yield a significant advantage over the state-of-the-art closed-cell instruments. OP-FTIR use in cleanrooms is hampered by the fab layout itself (closed mini-environments with limited path

lengths), moving optical obstructions, ceiling-to-floor airflow and air recirculation, high humidity and instrument calibration challenges.

Resonance-Enhanced (Multiphoton) Ionization Combined with Time-of-Flight Mass Spectrometry REI-TOF

REI-TOF is another potentially extremely sensitive technique to measure various volatile organics in air. It adds the high-efficiency resonant photo-ionization, with an appropriately tuned laser source, to the mass discrimination of TOF MS. Trace aromatic and chlorinated polycyclic air

pollutants have been monitored *in-situ* at sub-ppb (and low ppt) range by several groups. However, much work needs to be done to utilize this technique as a rugged, portable on-line monitoring technique, and the very high equipment costs may inhibit widespread adoption.

Atmospheric Pressure (Chemical) Ionization Mass Spectrometry

(AP(C)I-MS) has been the most sensitive and advanced analytical technique used by Air Liquide Electronics US (ALEUS) for on-line analysis of bulk and inert gases. ALEUS, in collaboration with VG (currently a part of Thermo Electron Corporation) has

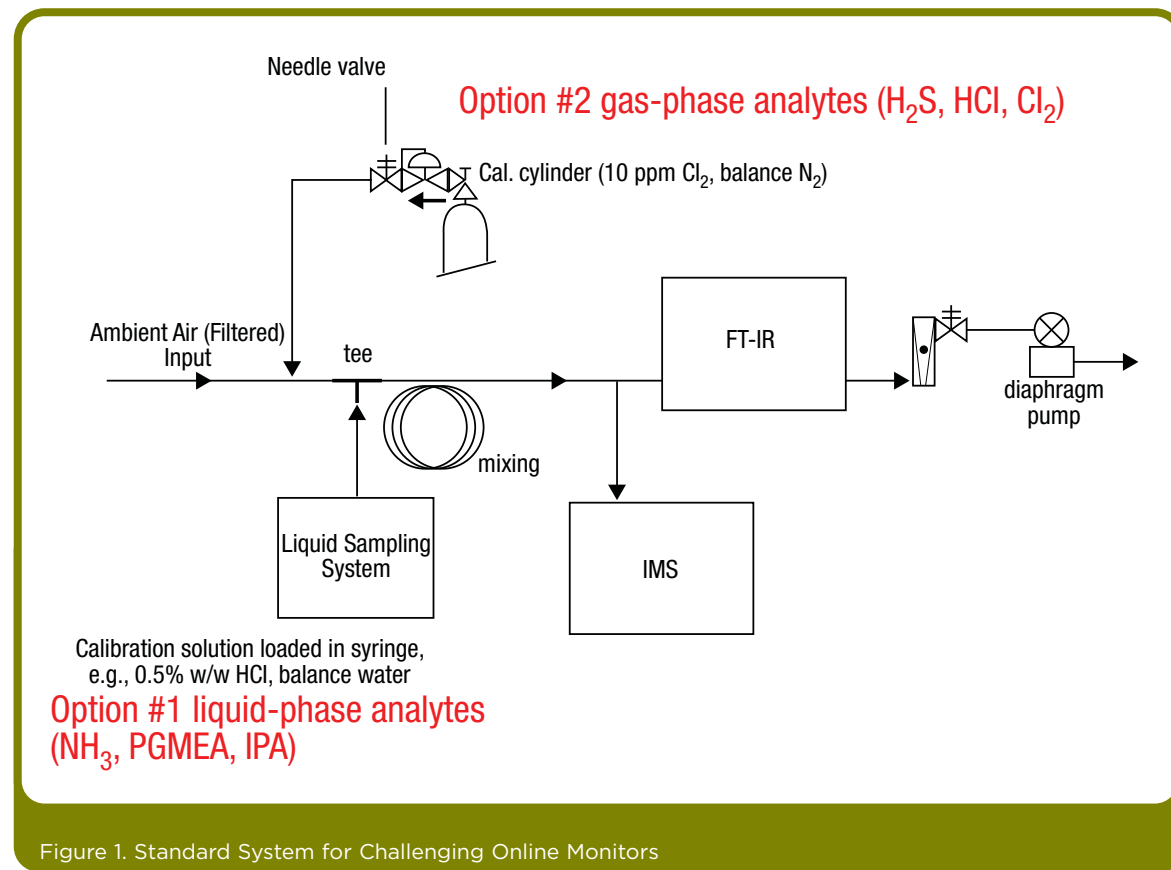


Figure 1. Standard System for Challenging Online Monitors

successfully developed commercial products (Trace+™, APIX™) allowing automatic continuous monitoring of such critical impurities as CH₄, CO₂, H₂O, etc., down to single ppt limits of detection, in different UHP matrixes: N, Ar, He and H. As early as 1980, AP(C)I-MS techniques were applied to ambient analysis for sub-ppb detection of inorganic and organic acids and volatile organic solvents (including amines). These results, along with the fact

heated in a relatively short amount of time and purged with an inert gas, so that the analytes are de-sorbed onto the head of the GC column. Analyte separation occurs on the GC column and is detected by flame ionization, mass spectrometry or other means, including a detection method called mini argon ionization detection (MAID) that incorporates argon as a carrier gas and a tritium source for ionization. This method works with most organic analytes because

Each system installed at semiconductor fabs should be challenged with a series of MA, MB, MC and MD compounds at a concentration at the lower limits of the operating levels.

that the first ionization potential of most of the targeted molecules is lower than that of N and O, suggest AP(C)I-MS methods could be considered for the on-line AMC monitoring in the cleanroom. The major foreseeable difficulties, such as mass interference ensuing from the potential complex composition of AMC mixtures or various competing charge-transfer reactions, could be resolved by such standard remedies as switchblade multichamber ionization sources with appropriate inlet membranes, and makeup reactants. Current APIMS technology is mechanically complex and quite expensive.

Thermal-Desorption Gas Chromatography (TDGC)

TDGC is often the preferred method for environmental samples, where high sensitivity is desired. In the context of AMCs, TDGC requires that a metered volume of air is impinged and concentrated directly onto an adsorbent trap. The trap is subsequently

their ionization potential falls below that of argon.

Guaranteeing System Calibration

Each system installed at semiconductor fabs should be challenged with a series of MA, MB, MC and MD compounds at a concentration at the lower limits of the operating levels. A typical system for challenging online instrumentation is shown in Figure 1.

Conclusions/Recommendations

Acids/oxidizers:

- FT-IR appears best to achieve targets for HF, HCl, HBr, Acetic acid and ozone.
- Cl₂ must be done by IMS or other dedicated monitor.
- Other acids (HNO₃, H₂SO₄, H₃PO₄ and organic acids) are best done by IC (grab sampling for now with on-line IC being developed).

Bases:

- FT-IR appears to provide same or better sensitivity in comparison with IMS.
- Must use IC (via grab sampling) to achieve sub-ppb DLs.

Molecular Condensables:

- FT-IR appears to provide sensitivities comparable to IMS. However, FT-IR calibration stability and speciation ability are generally far superior to IMS. Either method will detect low-molecular-wt organics, and will complement TD-GC-MS.
- Must use TD-GC-MS (off-site) to achieve 0.1 ng/liter-air DLs, or to provide speciation of similar compounds.

Refractories:

- FT-IR appears to provide same or better sensitivity in comparison with IMS.
- Must use TD-GC-MS-based method (via grab sampling) to achieve sub-ppb DLs. ■

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Recent Developments in Airborne Molecular Contamination Control

Andreas Neuber, M+W Zander FE GmbH

Abstract

Airborne molecular contamination (AMC) is a relevant yield concern for many fabs not only with regard to the most advanced technologies, where certainly the problems multiply. The paper intends to provide a short overview about the most relevant sources and contamination mechanisms. It also provides an overview about recent developments in contamination control both with regard to chemical filtration as well as other protection strategies.

Although particles remain a major contamination source in the semiconductor manufacturing process, a wealth of knowledge has been accumulated over the past few years with regard to the effects of airborne molecular contamination (AMC) and how to protect the wafer from such contamination. Actually, these contamination problems are often closely related since it has been demonstrated that gas (chemical) to particle reactions already occur even at very low concentrations.[1] These are partially triggered by the powerful laser radiation used in litho

exposure and metrology tools, but can also occur directly.

The sources of airborne molecular contamination can be identified internally as well as externally, which often makes their correct identification and elimination a difficult task. Typical internal sources include:

- Fugitive emissions from equipment, e.g., ammonia from chemical mechanical polishing (CMP), vapors from wet benches, HCl during epitaxial reactor maintenance, etc.
- Outgassing from materials, e.g., ammonia from concrete or insulation materials, organics and refractories (organics which also contain other elements, such as Si, S, P, N, F, etc., or inorganic compounds, that are normally not present in air) from coatings, gloves, polymers
- Dopants (B, P, etc.,) from tool maintenance activities, flame retardants and chemical reactions of fugitive HF emissions in the air with borosilicate fibers
- Contamination released during maintenance activities or accidental spillages, such as IPA and other organics from cleaning, or fluorocarbons used in chillers and vacuum pumps

Typical external sources can consist of:

- Traffic and other environmental pollution, e.g., power plants, refineries and other industrial sources
- Agriculture, e.g., ammonia, organics
- The fab's own exhaust systems, as well as from adjacent fabs, since they can contain relatively large amounts of dopants and corrosive vapors, even after exhaust treatment

However, the overall complexity of the problem remains immense as depicted in Figure 1, which provides an overview of the most frequently observed contamination mechanisms and what can be done to reduce their impact on a wafer.

Figure 1's list is certainly not exhaustive. Organics can cause peeling off of subsequent layers, and ozone and other gases can cause unwanted oxidation reactions.

| Sensitive Layer | Effect | Active Protection | Passive Protection |
|---|--|---|---|
| Metal and metal compounds (Al, Cu, silicides) | Corrosion | Prevent release of corrosive substances in cleanroom air | Chemical filtration to remove acids (ion exchange or chemically impregnated surfaces) |
| Resist (chemically amplified resists) | PAC (photo active compounds) react with bases in air [2] | Protective TARC (Top antireflecting coating) layer | Chemical filtration to remove bases (ion exchange or chemically impregnated surfaces) |
| Dopants in sensitive areas (pre-diffusion clean) | Dopants deposit after cleaning and impact layer resistivity [3] | Eliminate Boron or Phosphorous sources (Boron-free Hepa filter, flame retardants, etc.). Improve maintenance procedures for dopant sources. | Chemical filtration to remove Boron compounds and other harmful substances |
| Laser and chemical vapour-exposed volumes and surfaces | Nanoparticle generation (gas to particle conversion) [4] | Increase exhaust flow rates in wet benches, encapsulate critical laser-exposed volumes and use nitrogen purge | Chemical filtration to remove acids and bases (ion exchange or chemically impregnated surfaces). Chemical filtration to remove organics (adsorption). |
| Insulators (SiO ₂ , Si ₃ N ₄) | Incorporation of Carbon atoms in grid structure and change of electrical characteristics [5] | Hot baking before deposition or drive-in steps | Chemical filtration to remove organics (adsorption) |

Figure 1. Typical AMC Sources and Treatment Methods

It is important to understand that not all contaminants of a certain class are equally critical. Well-known examples are organics and refractories. Not all of them arrive at the wafer's critical surface, or do not remain long enough, if present, since they are displaced by less volatile substances. Therefore, it is certainly important to understand the deposition and reaction processes well to determine which contaminant levels are critical.

Chemical filters apply different mechanisms to reduce AMC, such as adsorption, chemisorption and/or ion exchange.

Besides achieving low contamination levels, operational costs are a major economic consideration with chemical filters. In comparison to Hepa filters, which practically only improve performance over time and do not need to be replaced, a chemical filter's limited useful lifetime is primarily dependant on the level of incoming contaminants. Also, the pressure drop is often not negligible, and increases by the usage of more media mass within a filter to reach higher capacities, thereby increasing the power consumption of the recirculation air system in the cleanroom.

Several companies have recently announced improvements in these fields. One solution is to utilize a cross-flow adsorption system, which reduces the pressure drop substantially compared to conventional pleated filter/adsorber media. Another strategy to improve the system's cost of ownership is to regenerate the filter/adsorber media. The possibility of frequently regenerating the media also allows capturing the organics with higher volatility, such as isopropanol, in the future.

Regenerable filters/adsorbers have been introduced for both ion exchangers as well as adsorption media. They reduce the operational (filter replacement) costs remarkably in the long term, as well as reduce the amount of solid waste. Figure 2 illustrates possible locations for chemical filters, but also the complexity of the problem, since, e.g., FOUF cross-contamination cannot be prevented by chemical filtration.

Monitoring often presents a real headache. Today impingers and monitoring wafers are typically used in addition to continuous monitoring methods for critical impurities, such as acids and bases. The selected monitoring program should be cost-efficient, but also should include the capability to perform regular background checks to enable faster troubleshooting if a process problem actually occurs. In particular, organics are difficult to monitor and achieve an adequate identification of any harmful substances. Furthermore, traditional monitoring techniques, such as thermal desorption GC-MS, utilize adsorption tubes which cannot detect substances that do not adhere to their surface.

Smelling issues also sometimes indicate an AMC problem, but such events typically occur at much lower levels than currently detectable.

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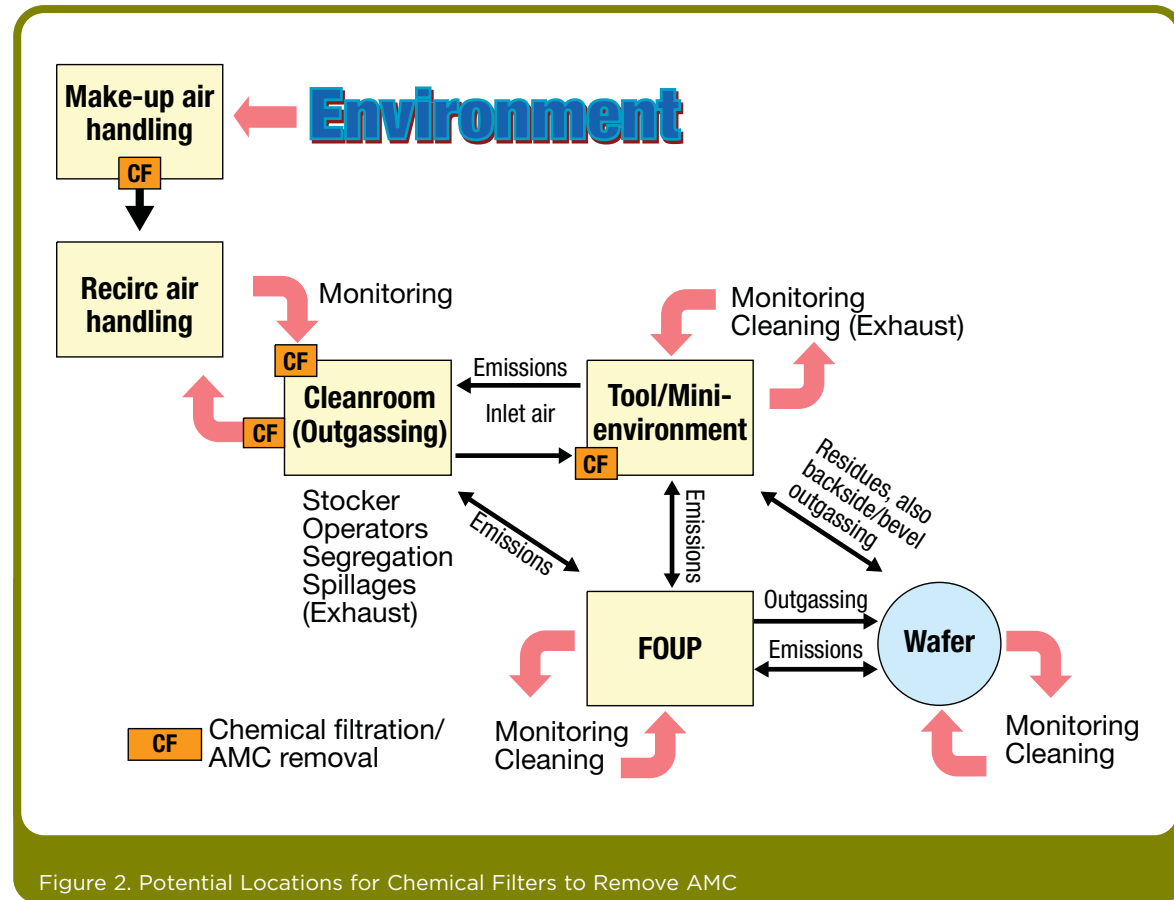


Figure 2. Potential Locations for Chemical Filters to Remove AMC

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Yield & Efficiency

Challenges in Automated Real-Time Dispatching

Brandon Lee, Ung Tin Tin, Lim Kian Wee – Chartered Semiconductor Manufacturing Ltd.

A Broadband Approach to Constraint Optimization

Kevin Funk – Avago Technologies

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Gregory D. Winterton

Process Development Manager for TI's DLP® group

Welcome to the inaugural issue of FEO. This project promises to bring some useful information at the working level to the individuals whose livelihoods are the fabrications of the most complex devices in the world. It is my belief that working-level “how to” information is far more valuable to the operations of an existing facility than a paper on some esoteric barrier which may be applied a decade into the future.

The papers in this section by Funk of Avago Technologies, and Lee, Tin and Wee of Chartered Semiconductor, address some of the real-world issues involved in constraint optimization and automated real-time dispatching. Both papers address a similar subject - that being how to get the most out of your factory.

The Funk paper discusses the use of cross-functional teams to resolve real-time

production constraints that occur in almost every semiconductor factory. I advocate this approach, as I have seen it used very effectively in a variety of situations.

The Lee et al paper discusses aspects and challenges in implementing dispatching rules to maximize factory output, as well as highlighting some of the constraints which are placed on these types of systems. Each factory manager must determine which elements are most important to the success of their specific facility and then reduce these items to an automated system to maximize their output and profit.

I trust you will benefit from these authors' work; I know I did.



Murty S. Polavarapu

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Yield enhancement and continual factory efficiency improvements are essential to the economic survival of any semiconductor facility, considering the large investments required and the quick technology obsolescence. In the area of yield enhancement, there needs to be a systematic approach to diagnosis of loss mechanisms and rapid execution of corrective actions. Improvement of factory efficiency demands focus on hard metrics such as cycle time and equipment utilization as well as on “soft” issues such as maximizing the people side of the equation. In this volume on Yield and Efficiency, we are pleased to present two papers that address both these aspects.

The team from Chartered Semiconductor highlights real-time dispatching issues in a fully automated fabrication facility where decisions need to be made by the manufacturing execution system with a higher degree of

granularity. The paper from Avago Technologies focuses on maximizing the output of cross-functional teams in a high-mix specialized fab. Please share your thoughts on these papers and suggest topics for future contributions.

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Challenges in Automated Real-Time Dispatching

Brandon Lee, Ung Tin Tin and Lim Kian Wee
Chartered Semiconductor Manufacturing Ltd.

Abstract

As the semiconductor industry shifts from 200mm toward 300mm wafer production, the level of complexity with regards to lot sequencing and dispatching has increased accordingly. This article analyzes the additional challenges faced in the implementation of Real Time Dispatching (RTD) in a fully-automated fab environment.

In today's competitive industry, semiconductor manufacturers are driven toward 300mm wafer production in order to achieve economies of scale and drive down the cost per die. The increased level of automation associated with 300mm manufacturing, coupled with the latest 90nm-and-below technologies requiring over 700 processing steps, has added

Establishing robust business rules and following them is still a necessity for effective production control.

complexity to fab management, and real-time dispatching (RTD) has become a critical automated decision support tool to manage inventory movement in the fab.

In 200mm operations, dispatch rules would only need to consider lot ranking

based on some predefined scheduling criteria, e.g., earliest due date (EDD), first-in first-out (FIFO), shortest processing time (SPT) or critical ratio (CR). The final decision on whether to follow the recommended sequencing would lie with the production operators, who would assess the local conditions at the time and reserve the lots accordingly. Typically, to prevent excessive overriding of the global scheduling criteria, reports would be developed to measure compliance to dispatch rules (Chik et al, 2002; Chakravarthi et al, 2005). The level of compliance would serve as a measure of the effectiveness of the dispatch rules and aid in continuous improvement.

The concept of RTD compliance does not change in 300mm manufacturing. Establishing robust business rules and following them is still a necessity for effective production control. However, as

production shifts from a manual mode to an automated mode, all the factors that would normally be considered by the operator in lot dispatching must be programmed into the dispatch rules. The dispatch rules must evolve from just the "What" perspective, i.e.,

lot ranking, to include the "Where" (which is the best equipment to process the lot?) and "When" (is this the right time to dispatch the lot?) considerations. Compliance would by default be 100 percent for optimized rules, as the system would be responsible for making all dispatching decisions based on the programmed dispatch rules. It is therefore critical in such an environment

2. WIP Conditions

At the local equipment level, the optimal dispatching policy may be affected by the WIP conditions at the time. When WIP is low, the emphasis may be on equipment monitoring and preventive maintenance to minimize disruption during critical high WIP periods. This implies the need for seamless integration with the

In the over 700 processing steps required for advanced technologies (90nm and below), the same sets of equipment will be utilized throughout the entire process flow.

that all requirements are gathered and analyzed in order to optimize the dispatch rules. Failure to consider all requirements may result in inefficient dispatching or even quality issues.

Some of the key considerations for automated real-time dispatching are summarized below. This is not an exhaustive list, but rather, highlights the complexity of the dispatch rules required for fully automated operations.

1. Dispatching Validity

As lot reservation is now done automatically, the RTD rule must ensure that the dispatch list submitted to the MES contains only valid lots. Nonvalid lots would include those that are on hold, or not in the AMHS system. Failure to filter away these nonvalid lots would cause reservation failures, as the MES would reject the reservation request. If these lots happen to be at the top of the dispatch listing, the operator would just keep attempting to reserve these lots, causing valid lots lower down the list to jam up.

preventive maintenance planning system. Under high WIP conditions, the emphasis may be in reducing WIP to acceptable levels and effectively feed downstream operations through setup reduction by increasing batch sizes and lot training. This implies not just rule optimality but also rule robustness. The dispatch rule must be able to switch automatically with the changing WIP levels in real time for full hands-off operation.

On a global level, the dispatch rules have to consider the overall WIP profile of the entire fab. In the over 700 processing steps required for advanced technologies (90nm and below), the same sets of equipment will be utilized throughout the entire process flow. Furthermore, in a foundry environment where multiple (possibly conflicting) process flows coexist, the task becomes increasingly complex. Regardless, linearizing the WIP profile of the fab is necessary to achieve continuous and even arrivals to minimize the previously mentioned extreme high/low WIP conditions.

3. Equipment Conditions

Dispatching rules must also consider the amount of equipment available for processing. The rules must be programmed to optimally utilize available resources. If Eqp A is already processing one lot while Eqp B is idle, it would be desirable to dispatch to Eqp B to balance the loading. Or, if Lot A can be processed in Eqp 1 and Eqp 2, while Lot B can only be processed in Eqp 1, dispatching Lot A

RCA should stop when Gate or Poly are not available (e.g., down for preventive maintenance) to minimize the risk of exceeding the queue-time limits.

Each equipment or process may also have its own specific quality requirements. For critical processes, the requirement may be to process few wafers out of a lot (known as sendaheads or pilot wafers) and pending metrology feedback, make the decision on whether to commit the rest of

From optimizing incoming WIP, to reducing setups through batching and lot training, dispatch rules must be in place to maximize the throughput from these machines.

to Eqp 1 would have no value, as this would cause Lot B to queue with no equipment available to process. Meanwhile, Eqp 2 remains idle. It would be better to dispatch Lot A to Eqp 2 and Lot B to Eqp 1, so that both lots can be processed simultaneously, reducing total flow time. These are key “Where” conditions that would be under the control of the operator in 200mm manufacturing.

4. Quality Requirements

Queue-time restrictions between key process steps are common in most process flows. These links define critical quality requirements for two process steps to be completed within a certain time frame (e.g., RCA-Gate-Poly) for yield purposes. The dispatch rules must consider the WIP, equipment and process conditions within these critical zones and act accordingly. In the previous example, dispatching from

the lot, or alert the engineer for attention. Another requirement might be to dispatch nonproduction wafers to “season” or warm up equipment before any production lot can be dispatched. These requirements must be programmed into the dispatch rules for automated control.

5. Bottleneck Management

As the throughput rate of the entire fab is constrained by the throughput from bottleneck machines, it is critical to ensure that these bottlenecks are sufficiently fed to avoid equipment idling. A minute wasted at a bottleneck is a minute lost for the entire fab (Goldratt & Cox, 1992). From optimizing incoming WIP (considering not just quantity but also the type of WIP arriving), to reducing setups through batching and lot training, dispatch rules must be in place to maximize the throughput from these machines.

The opposite aspect of bottleneck management can result from temporary bottlenecks due to equipment or process issues. In this case, it would add no value to continue feeding the bottleneck, as the lots would just end up queuing when they reach the bottleneck. Instead, preference should be on avoiding the high WIP pileups caused by these temporary bottlenecks and prioritizing lots feeding other areas. In extreme cases, it may even be beneficial to stop dispatching entirely and instead, use the time available for equipment monitoring and preventive maintenance activities. The intelligence on the best course of action must be programmed in for automatic execution.

The shift toward 300mm manufacturing has added additional complexity to the requirements of RTD. Successful RTD implementation requires dispatch rules that exhibit artificial intelligence to mimic the actions of production operators in running the fab. This article summarized some of these details. Of course, it must not be forgotten that RTD rules are evolutionary, and continuous improvement is required to ensure that the rules are optimized to meet ever-changing demands.

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A Broadband Approach to Constraint Optimization

Kevin Funk, Avago Technologies

Abstract

Enthusiastic, highly motivated cross-functional teams can provide a powerful resource in the resolution of production line throughput constraints ... particularly in limited-volume, high-mix, specialized product manufacturing lines. Team member/team leader selection represents a critical management decision with very significant bottom-line implications.

Manufacturing lines producing limited-volume, high-mix, specialized products inherently exist on the impoverished side of the economies-of-scale curve. Nowhere is this more evident than when attempting to optimize the throughput performance of constraint tool sets, which are often those most highly customized, most expensive or most limited in number while often servicing multiple process steps and utilizing multiple process recipes.

It is typically straightforward to determine when such a tool set constitutes a constraint to the operation of the production line, but mounting an effective assault on the problem can be a considerably more difficult issue. In most cases, transforming the throughput performance of such tools to a significantly higher level requires careful consideration of many aspects of their multifaceted production

environment. Intrinsic recipe times, operational efficiency, information management, monitoring/qualification procedures, machine maintenance protocols/schedules, as well as a host of other considerations, all come into play simultaneously and interactively.

It can generally be assumed that the skills exist within the overall manufacturing organization to study and improve any individual variable affecting throughput performance. However, given the unique multirole/multiprocess/multi-operation nature of the tool sets in question, it is typically not possible to make a sufficiently large shift in performance by solving any one individual problem. The challenge often becomes one of developing and managing the implementation of multiple improvements involving multiple disciplines and requiring resources from multiple portions of the overall organization.

A rigidly delineated organizational structure (Operations/Maintenance/Engineering/IT) does not readily lend itself to the effective grappling of such problems. In such a structure, one specific entity is typically charged with improving the situation ... bringing to bear all available skills and tools at their disposal. The result is often the optimization of a single aspect (e.g., intrinsic recipe time), but it often lacks aggressive and comprehensive

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consideration of multiple other opportunities which would likely in their summation have had a significantly larger overall effect on the problem at hand.

Under these production conditions, it becomes exceptionally important to employ a broadband approach to the management of constraint throughput improvement projects.

The long-proven strength of cross-functional teams has been repeatedly demonstrated to provide an excellent framework under which to launch a multifront attack on a throughput constraint. Key elements to success have been found to pivot around the selection of an appropriate set of team members and the provision of effective team leadership.

Experience in this arena has indicated conclusively that self-motivation and enthusiasm are by far the most important selection criteria for team members, and that the team can be effectively led and coordinated by a highly engaged man-

Highly motivated team members with strong basic skills will bring the full benefit of their own specific talents to bear and (critically) will actively seek out and acquire expertise, information and resources which they personally lack. The roles of the team leader then become primarily those of actively assuring that the various facets of the production environment are being robustly addressed, and of assuring that information flows freely throughout the team.

Enthusiasm and self-motivation are unfortunately not assignable characteristics. A specific process expert or an individual with exceptional tool knowledge may or may not be an effective team player. If they are not, they are of little practical use to a cross-functional team regardless of their credentials. In fact, assignment of such a resource to a critical role in a cross-functional team will almost certainly be obstructive and ultimately counterproductive. Conversely, the

significant improvements to production constraints ... a fundamental limiter to the bottom line of the entire organization.

An alternative approach is to apply industrial engineering resources in an attempt to grapple with various aspects of a production constraint problem. While it is the inherent nature of the industrial engineering role to examine multiple aspects of the production environment and to apply multiple disciplines to solutions, in this scenario, the ultimate responsibility for providing a significant performance improvement lies in a more concentrated area of the organization. Depending upon specific organizational structures and upon the size and skill sets of the industrial engineering team, this approach can also be quite successful ... although probably on a significantly longer time frame than that provided by an aggressive cross-functional team.

When addressing a production constraint issue, speed of resolution is in fact a very important consideration. By definition, the existing constrained production situation is limiting revenue generation on a day-by-day basis. This economic fact of life also coordinates well with the advantages of highly motivated cross-functional teams. The resolution of any particular problem ultimately relies on the performance of observations, analysis of data and the determination and implementation of machine, process and operational environment changes. Given that a comprehensive solution will almost certainly involve the resolution of numerous such problems, a well-coordinated multiperson, multitalented assault will typically provide the shortest route to a practical and effective implementation.

In summary, the application of cross-functional teams to constraint optimization

can be a powerful tool with significant bottom-line implications to the manufacturing organization. Team member selection should be viewed as a very critical management decision process ... one which will have a very direct impact on the overall quality, extent and speed of implementation of the resulting improvements. ■

About the Author

Kevin Funk has been a manufacturing development engineer for Avago Technologies (and its progenitors Agilent Technologies and Hewlett-Packard) since 1980. His areas of concentration are cycle time reduction and factory information data collection/analysis.

When addressing a production constraint issue, speed of resolution is in fact a very important consideration.

agement representative from within either technical/tool-based section of the organization (Maintenance or Engineering). Motivation and enthusiasm on the part of the team leader have proven to be every bit as important as the mind-sets of the team members. The strength of the relationship between team selection and the ultimate level of success in effectively reining in a production constraint cannot be overstated. As such, the construction of a cross-functional team must be approached with considerable care and forethought.

inclusion of highly skilled “nonexperts” to the team can often provide insights into system-level improvements which are not obvious to those closely tied to the existing processes.

From a management perspective, the creation and effective utilization of cross-functional teams can provide a means of demonstrating and recognizing the contributions of these enthusiastic team-oriented individuals. This recognition is altogether appropriate with respect to their enhanced capability to implement

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Capacity, Utilization & Cycle Time

Assets Optimization

Lim Kian Wee, Mohd Azizi Chik and Lim Lip Hong - Chartered Semiconductor Manufacturing Ltd.

The Economics of Speed

Robert C. Leachman - Leachman & Associates LLC

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Kevin Venor

Manufacturing Development Engineering Manager, Avago Technologies

We all know that shorter cycle time leads to improved inventory control, shorter lead times and higher on-time delivery performance. What is many times missed is just how critically important cycle time is to both top-line and bottom-line financial performance. While metrics such as yield are focused on and scrutinized with large teams of engineers and a plethora of diagnostic tools, cycle time often takes a backseat in terms of the amount of resources brought to bear for improvement. With a similar focused effort, significant reductions in cycle time are achievable. These lead not only to higher output rates, but also a significant increase in the rate of learning. This increased rate of learning improves the ability to rapidly improve yields and to respond quickly to any excursions. In addition, the ability to shorten the release time for new technologies and new products is in direct

proportion to the gain realized in cycle time. Fortunately there are many tools available to enable a structured approach to cycle time improvement. Significant improvements in queuing methods and shop floor control are widely available. What is also often overlooked is that significant improvement can be realized when management focus is directed to this area, as well as incremental resources applied in constraint areas, resulting in high payback for very little investment. The articles in this section touch on how to better measure the impact of cycle time improvements, as well as ways to improve the utilization of existing tool sets. It is clear that with minimal effort, large gains can be realized if cycle time is elevated to a "top" metric for your organization to focus on.



Madan Chakravarthi

Section Manager - IE Systems at Chartered Semiconductor, Singapore

Over the past decades, the semiconductor industry has been moving at a frantic pace in terms of technology. With added complexities and wafer sizes increasing, fab cycle times are perennially going up, worsening the bullwhip effect. It is imperative that the industry looks at operational improvements more critically to counter this. That Moore's Law is going to last only for the next 10-15 years is predicted by none other than Dr. Gordon Moore. Perhaps it is time we have a Moore's Law equivalent to set the direction for semiconductor supply chain speed/velocity? In the meanwhile, we need new perspectives to approach cycle-time improvements. At the macro level, there is a need to quantify cycle-time improvements in monetary terms so that fab managers prioritize them better. At the micro level, we need a paradigm shift in

the use of real-time decision support systems to optimize asset utilization by reducing "white space" to near-zero levels. The article on Economics of Speed from Dr. Robert Leachman illustrates an approach to assign an economic value to cycle time. Such an approach will stimulate fab managers to pursue cycle-time improvement with renewed vigor. The white space reduction journey outlined in the article from Lim et al kills two birds with one stone - asset optimization by reducing the white space (idle time between lots) and cycle-time reduction.

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Assets Optimization

Lim Kian Wee, Mohd Azizi Chik and Lim Lip Hong
Chartered Semiconductor Manufacturing Ltd.

As with any company, the main objective of the business is to improve the stakeholder value. It can be accomplished through revenue growth and productivity strategies. Since 2004, Fab 7 has embarked on the journey of assets optimization in pursuing efficiency to improve stakeholder value. Figure 1 illustrates an improvement strategy for stakeholder value (Kaplan and Norton, 2004).

Fab 7's assets optimization effort started with copy smart systems from a strategic business partner. Divergence from polling to an event-based solution was made with the acquisition of an event-based solution, "Activity Manager," from Applied Materials (formerly Brooks Software) at the end of 2004. Forty-three days after deployment kickoff in February 2005, the first tool-to-tool move was accomplished (in April

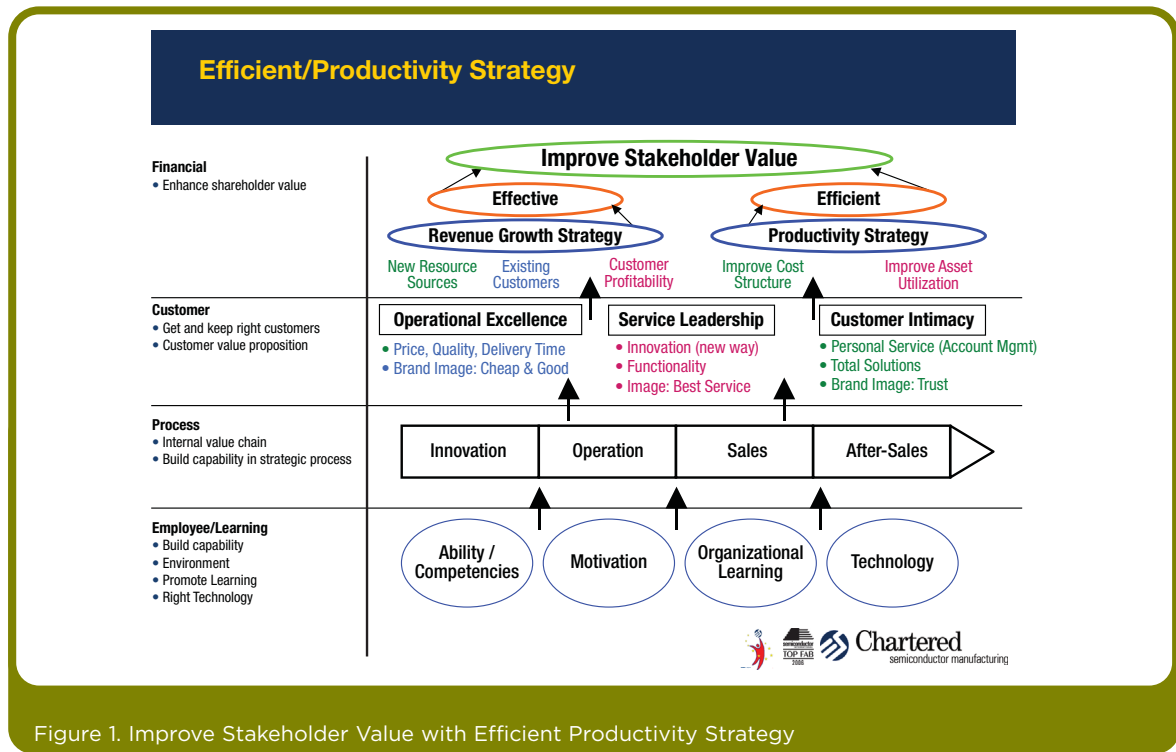


Figure 1. Improve Stakeholder Value with Efficient Productivity Strategy

2005). Since March 2006, all tools in Fab 7 are now under event-based control AUTO3 (automatic lot selection, delivery/pickup and track in/out). Figure 2 shows Fab 7's assets optimization roadmap.

Today many wafer fabs of the world (200mm and 300mm alike) are largely on polling-based solutions (Maxim, 2006; Burda, 2006; Ignizio, 2006). The difference between event-based versus polling-based is real time versus lag time, respectively. Lag time means predetermined schedule (every X mins), whereas real time means detection, as when it occurs and triggers appropriate work flow and actions. This is the crucial role for cost rationalization in a multibillion-dollar facility (Ignizio, 2006; Parunak, 2000).

The business rules (37 local and 1 global) in Fab 7's manufacturing decision system

emphasized that "Quality, Output, Cycle Time" is important to operations. In order of sequence, every move is a quality move, which consists of yield, output objective and cycle time to meet customer's demand. Through event-based, the intelligent manufacturing decision system was further enhanced with "tool-to-tool," "preemptive dispatching," "white space reduction" and eventually "real-time scheduling," with the objective of assets optimization. Figure 3 shows Fab 7's vision for optimizing white space to "near zero."

White space is the time clock between when a completed lot departs and the next lot arrives for processing on the same load port. The same measurement is applicable across all fabs (200mm and less, plus 300mm wafer fab). The target is < 1 min or "near zero"

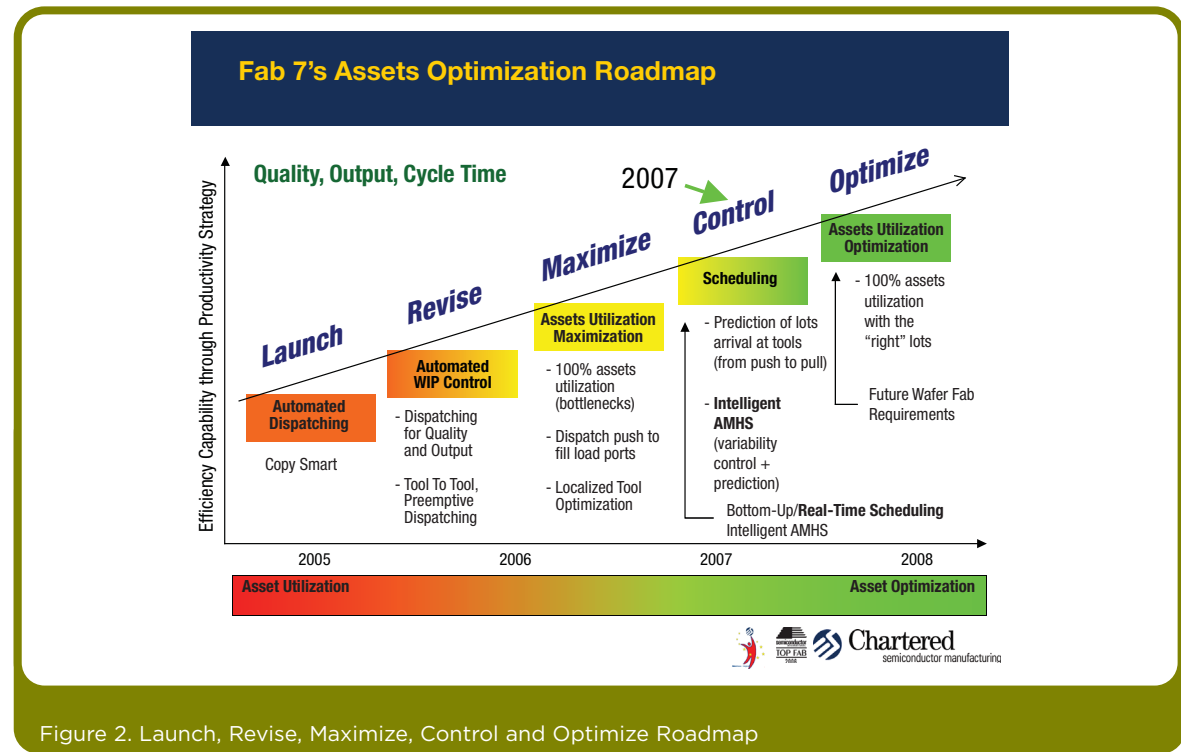


Figure 2. Launch, Revise, Maximize, Control and Optimize Roadmap

white space. Since October 2006, “near zero” capability was demonstrated in Fab 7. The “near zero” white space solution hardening effort is ongoing through collaboration, with AMAT and Daifuku scheduled to be ready by October 2007. There’s also effort toward “real-time scheduling,” which will be the focus for 2008 and beyond. Illustrations regarding optimized real-time scheduling are shown in Figure 4.

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Mohd Azizi Chik

Mohd Azizi Chik joined Chartered Semiconductor Manufacturing, 300mm FAB 7 in 2005 as an E-Manufacturing Integrated Solutions principal engineer. Prior to joining the company, he was the lead for overall APF product, real-time dispatching rule, FAB capital analysis, equipment capacity analysis

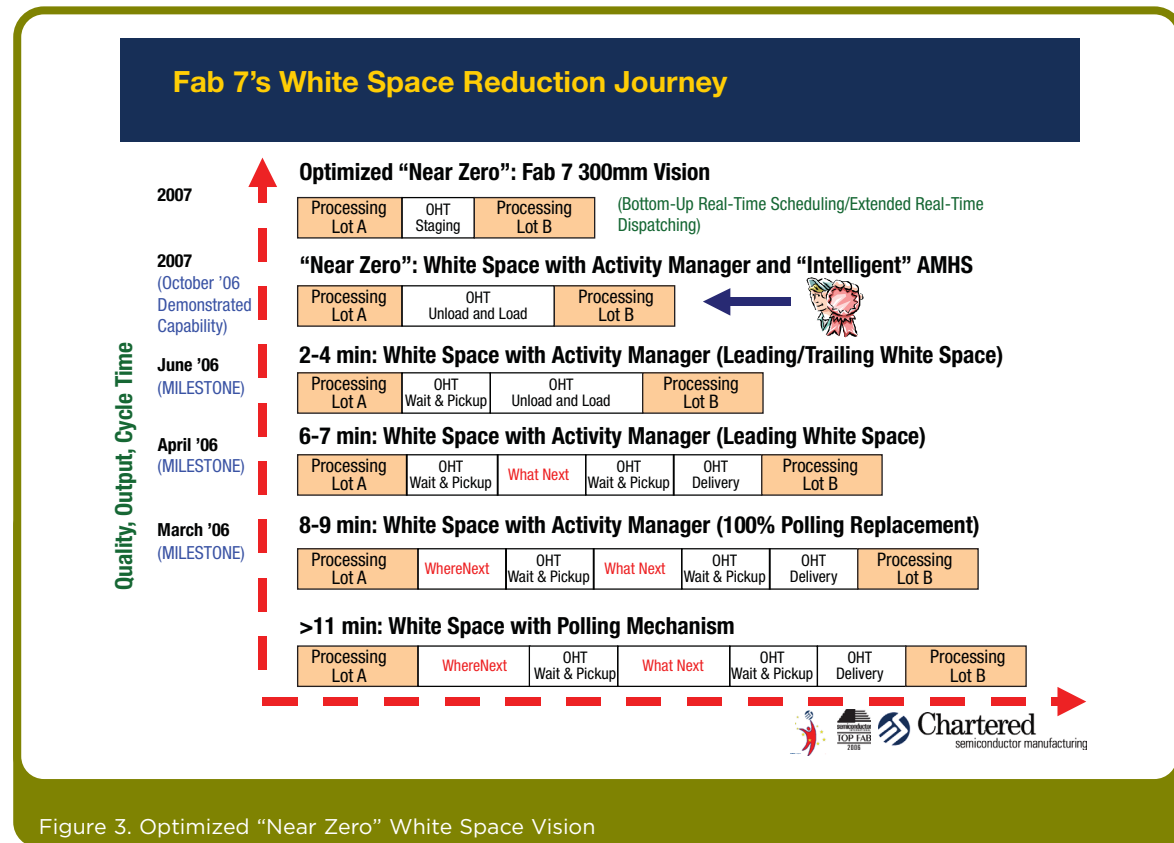


Figure 3. Optimized “Near Zero” White Space Vision

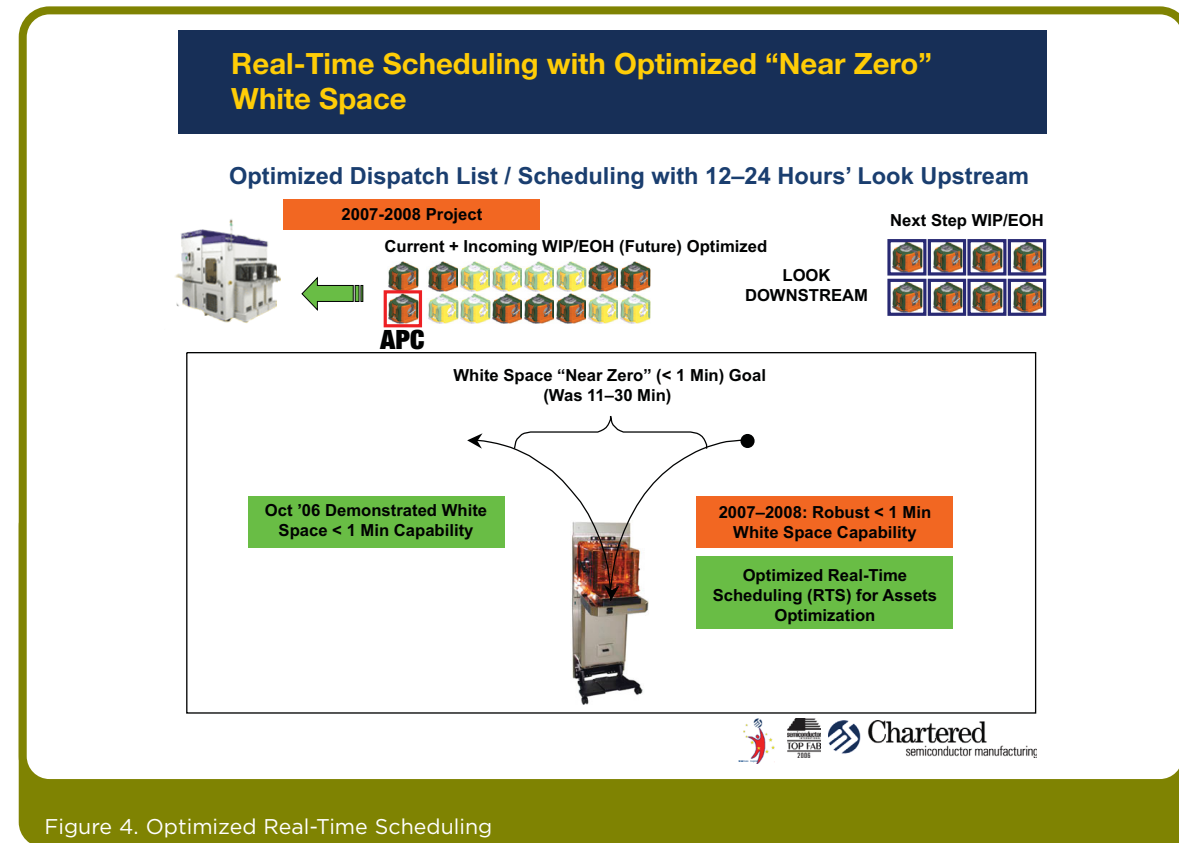


Figure 4. Optimized Real-Time Scheduling

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...Assets Optimization

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Lim Lip Hong

Lim Lip Hong has been the senior principal engineer for E-Manufacturing Integrated Solutions in Fab7 300mm Operations at Chartered Semiconductor Manufacturing since 2004. His current focus is on real-time dispatch rules optimization to increase Fabwide throughput and reduce cycle time variability. He started his career as a manufacturing engineer in 1995 at Chartered's 200mm Fab 2, where he was instrumental in the start-up and ramp of the diffusion and implant manufacturing modules. His experience in 200mm manufacturing scheduling, work flow organization and equipment throughput improvement laid the foundations for pragmatic RTD implementation. He graduated with a degree in mechanical and production engineering from Nanyang Technological University (Singapore) in 1995. He jointly holds two patents pending.

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SECTION 9 - Capacity, Utilization & Cycle Time

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The Economics of Speed

Robert C. Leachman, Leachman & Associates LLC

Since the industrial revolution, a basic principle guiding all manufacturing corporations is to evaluate two sides of their organizations quite differently. One side, encompassing sales and marketing activities, is judged primarily on the basis of the revenues they bring in. The other side, encompassing manufacturing and the supply chain, is judged primarily on the basis of expenditures, i.e., on the basis of product costs. Product development and technology development most often belongs to the supply side of the organization and is also judged on the basis of costs.

This principle worked pretty well for two centuries. But in a world of rapid technological obsolescence, it has become less effective. Driven by Moore's Law, prices for many semiconductors, and prices for end products incorporating them, decline rapidly. For example, in the first year or two of life, selling prices for commodity memory and microprocessors decline 50 percent a year, or even more. And those products are completely obsolete within a few years. The speed of technology development and the speed of the supply chain matter enormously.

"Cycle time" is semiconductor industry jargon for the elapsed time to pass

manufacturing lots through the manufacturing process, from lot creation until lot completion. The term is also applied to individual manufacturing steps, measuring the elapsed time from completion of the preceding step until completion of the step in question, or to a series of manufacturing steps (the sum of the cycle times of the subject steps). The term also is applied to developmental activities, such as the "cycle time" to develop and qualify a new product or process technology.

In produce-to-order businesses, the manufacturing cycle time is part of the product/service apparent to the customer and is therefore an important competitive issue. It is also a competitive issue for bringing new products to market. Suppliers able to offer shorter cycle times will be preferred. But there is another aspect. Even for commodity semiconductor products, cycle time has a very strong influence on the realized average selling prices. Firms with shorter cycle times are able to make sales at earlier times when prevailing prices are higher. And by making those sales, they tend to drive prices down and thereby diminish revenue available to competitors.

This is not to say that managements in our industry do not recognize the crucial importance of speed. We hear expressions

like “time is money” as managements strive to shorten the “time to market.” But seldom is the economic value of speed quantified, and hardly ever is that value added to the cost figures used to evaluate specific engineering projects, engineering staff or operational staff. Instead, the economic metrics for the supply side of the organization primarily or exclusively concern costs. And it needn’t be this way.

I would like to propose a different general managerial strategy with respect to cycle time as follows:

- (1) Management should impute an economic value to cycle time, considering revenue gain as well as product costs, and declare this value to the engineering and operations organizations. Management should require that any proposals for changes to the manufacturing process or to operational policies that would change cycle times must be justified by quantifying the overall economic impact, including the gain or loss in value associated with changes in cycle time.
- (2) *Entitlement cycle times* should be calculated by the engineering organizations for every product and every manufacturing process. Entitlement cycle time is the result of an analytical queuing model calculation or a discrete-event simulation determining what cycle time the manufacturing process is capable of, considering the process specifications, the equipment released, statistics on process times, and statistics on process and equipment trouble. Practical tools must be distributed to the engineering and manufacturing organizations enabling them to measure entitlement cycle times, not only for the current situation, but also for any proposed changes to process, production volume or opera-

tional policy. One can think of the entitlement cycle time as engineering’s endowment to the manufacturing department. If entitlement cycle time is not competitive, it is engineering’s job to fix that; no amount of manufacturing finesse can make up for an inadequate entitlement. And even if it is competitive, engineering should be rewarded for making changes to reduce cycle time, because reduction has real economic value to the corporation.

- (3) The gap between actual cycle time and entitlement cycle time is manufacturing’s problem. Where there is a significant gap, the manufacturing organization needs to improve execution. Improved execution tools may be required; e.g., more advanced planning and scheduling systems. Again, improvement in policies, tools and performance should be justified and evaluated on the basis of the real economic value of cycle time reduction.

Imputing the Economic Value of Cycle Time

The notion of assigning an economic value reflecting the corporate revenue gain afforded by small, local cycle-time reduction efforts is so new to the industry that I would like to provide some practical engineering mathematics for doing this. Consider a product currently in production. The number of good die per wafer start is Y (considering line yield, die yield and the number of die printed on the wafer). The product continues in production with yield Y until time H , at which time it will become totally obsolete and will be withdrawn.

The current average selling price per die is P_0 , but this price is eroding rapidly with time. If the rate of price erosion is constant, then t days from now, the average selling

price may be modeled as

$$P(t) = P_0 e^{-\alpha t}$$

For example, if prices are eroding 50 percent per year, then we should set $\alpha = 0.0019$.

Now suppose the manufacturing cycle time for wafers started on day t is $CT(t)$, and suppose the wafer start volume per day at time t is $W(t)$. Then the total lifetime revenue for the product may be expressed as

$$R = \int_0^H W(t)YP(t + CT(t))dt = \int_0^H W(t)YP_0 e^{-\alpha(t+CT(t))} dt.$$

Let’s consider the special simple case where the wafer starts and cycle time are constant over the remaining life of the product, i.e., $W(t) = W$ and $CT(t) = CT$. Then the lifetime revenue integral may be simplified as

$$\int_0^H WYP_0 e^{-\alpha(t+CT)} dt = WYP_0 e^{-\alpha CT} \int_0^H e^{-\alpha t} dt = WYP_0 e^{-\alpha CT} \left(\frac{1 - e^{-\alpha H}}{\alpha} \right).$$

Now suppose cycle time is permanently shortened by one day, i.e., $CT \rightarrow CT - 1$. Then the remaining lifetime revenue becomes

$$WYP_0 e^{-\alpha(CT-1)} \left(\frac{1 - e^{-\alpha H}}{\alpha} \right).$$

The revenue gain from reducing cycle time by one day is therefore

$$\Delta R = WYP_0 e^{-\alpha(CT-1)} \left(\frac{1 - e^{-\alpha H}}{\alpha} \right) - WYP_0 e^{-\alpha CT} \left(\frac{1 - e^{-\alpha H}}{\alpha} \right)$$

or

$$\Delta R = (e^{\alpha} - 1) WYP_0 e^{-\alpha CT} \left(\frac{1 - e^{-\alpha H}}{\alpha} \right).$$

To illustrate, suppose a fab makes 13,000 wafer starts per week of a product that yields 420 good die per wafer. The cycle time is 50 days. The current selling price is \$4.50 per die and is declining 50 percent per year. The remaining product life is two years.

Plugging these values into the equation immediately above, the revenue gain from a permanent, one-day reduction in manufacturing cycle time made today is then

$$\Delta R = \$2,391,768$$

i.e., the revenue gain to the corporation from cycle-time reduction in this fab is worth about \$2.4 million per day. Every engineer and operations manager associated with this fab ought to know this: Changing the process or operation in a way that permanently reduces cycle time by just one day (while still maintaining current volume and yield) is worth \$2.4 million, just in added revenue to the company.

Not included in the above analysis is the reduction in product costs associated with reducing cycle time. The most important element of such cost reduction in semiconductor manufacturing concerns the positive impact on yield from cycle-time reduction. This occurs for two reasons: 1) Certain yield-loss mechanisms involve equipment or process “excursions” in which the process or equipment shifts out of control, but this excursion is not detected until the first lot processed after the excursion is tested at the end of the production line. All lots that had passed the out-of-control point also will have poor yield. When cycle time is reduced, the work in process is reduced, and therefore the number of lots with exposure to excursion loss is reduced; and 2) A process change that will improve yield must be justified on the basis of an in-line experiment. Typically, some wafers from a selected manufacturing lot are processed the old way, while others from the same lot are processed the new way. The lot then must travel through the rest of the fabrication process to the end of the line where all wafers are tested so as to confirm statistically that the process change

indeed improves yield. The shorter the cycle time, the less time is required to implement process changes, and therefore the yield learning curve is improved.

If statistics are available about excursion frequencies and magnitudes, then we can quantify the yield gain from cycle-time reduction, whereupon we can quantify the cost reduction afforded by cycle-time reduction and add it to the revenue gains as computed above.

Example Gains From Improving Supply Chain Speed

During the period 1996–2000, Leachman and Associates LLC worked with Samsung Electronics, Ltd. to reduce semiconductor manufacturing cycle times. Cycle times to manufacture DRAMs were reduced from 80 days to 30 days. Just during the project, the revenue gains afforded to Samsung by this cycle-time reduction tallied in excess of \$1 billion.[1] The revenue gains subsequent to the project amounted to untold billions more. Samsung’s market share and profits in DRAMs soared. Meanwhile, other Korean, Japanese and American memory companies suffered tremendously or were driven out of the business entirely. Samsung subsequently ported their DRAM cycle-time reduction methodology to their LCD business with comparable effectiveness.

Summary

Across the electronics industry, leading companies have one thing in common: They are faster than the competition. They bring new products and technologies to market sooner, they fulfill customer needs more quickly, and they enjoy higher selling prices and drive down the selling prices available to competitors. The revenue gains afforded by faster speeds through the supply chains of semiconductor manufacturers are

profound. Yet quantitative metrics and practical tools for speed management by the industry’s engineering and manufacturing organizations are lacking. This can and should be changed.

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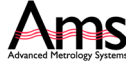









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Rob C. Leachman is President and CEO of Leachman and Associates LLC, a firm providing consulting and software for operations management to semiconductor manufacturers and other corporations. He also is a Professor of Industrial Engineering and Operations Research at the University of California at Berkeley. In 1995, Dr. Leachman won the Franz Edelman Award Competition sponsored by the Institute for Operations Research and the Management Sciences, recognizing his work in designing and implementing automated production planning systems in the semiconductor industry.

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