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WELCOME...

to the sixth issue of Fab Engineering & Operations.

No, your eyes do not deceive you. This is a particularly thin issue because unless you've been: a) living in a cave in an effort to return to nature b) kidnapped by aliens for experimental purposes and then returned as a spy, or c) something more reasonable as an excuse for not paying attention for the last 12 months – then you'll know that the industry is in turmoil. As of this writing, there are two manufacturers facing the ugly specter of Chapter 11, and cash has suddenly become the rarest commodity in any market – everyone is being affected by this and we're no different. The first thing that is traditionally cut is marketing, and if, like us, you rely on marketing dollars/euros/yen, etc., to exist, then something's got to give. In our case, it has meant we've had to cut back on production, meaning fewer pages – but fear not; we're working on a new business model for this year that we hope will change things. For now, enjoy what we have, and go out and buy something – because that's the best way to kick-start the economy ...

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"Automation, intelligently applied, reduces human error and the effects of human error on a working wafer fab. When a task cannot be taken over, but can be monitored by automation, the effects of human error can be eliminated."

Mark Crabtree et al. – NEC Electronics America, Inc. ***See p17***

"We have found common themes in the fabs we visit: Firstly, there is a loss category called "unknown" that is typically one of the largest, if not the largest, category of yield loss."

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"Regular removal of residuals has to be done to obtain stable and repeatable deposition results with uniform surfaces at acceptable particle levels in all PECVD equipment."

Marcello Riva et al. – Solvay Fluor GmbH ***See p35***

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The following pages contain the photos and brief biographies of ***FEO's*** Panel Members. We would like to extend our sincere gratitude for their belief in our idea and their willingness to help us bring this magazine to fruition. ***FEO*** magazine would not have become a reality without their support, guidance and wisdom.

Gary Alexander

Managing Principal, AMC Intl., LLC; Executive Director, SEC/N®

Gary Alexander is Founder/Managing Principal of AMC Intl., LLC, which independently consults on secondary market topics with organizations and government agencies worldwide. He is participating in U.S Department of Commerce/WTO and ANSI-ISO task forces on increasing trade opportunities and developing standards for the global secondary market. He is also Executive Director of SEC/N, the global trade association of the semiconductor industry for secondary market equipment and related services.

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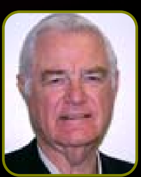
Senior Scientist, AMEC Geomatrix, Inc.

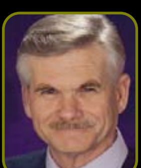
Julia Bussey helps companies develop sustainable business practices to reduce their costs and footprints, as well as to improve their efficiency. She has the unique experience of having been in their shoes and also having been in government, focusing on air and waste issues, so she brings 25 years of experience to the table for creative and practical solutions.



C. Richard Deininger

General Partner, Taylor-Deininger Partners, Inc.

Dick brings 50 years of successful executive management and business experience to the high tech industry. He is one of the general partners in Taylor-Deininger Partners, Inc. (TDP) consultancy and the owner principal of Deininger and Associates, LLC consultancy. He holds a BSEE degree from Newark College of Engineering and is a senior life member of IEEE, Tau Beta Pi and Eta Kappa Nu.



Bill Funsten

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Bill Funsten has 33 years of experience in semiconductor processing, defect metrology, yield improvement and contamination control. He is currently program manager, contamination control at Spansion, Inc. Mr. Funsten has a B.S. degree in materials engineering from UCLA.

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Kevin Gray is a Senior Etch Line Maintenance Supervisor at Cypress Semiconductor. In 1991, he joined the U.S. Navy, becoming a nuclear electrician aboard the Submarine USS Michigan. Kevin co-authored "Polymer control in a LAM TCP 9600 Aluminum Etch Chamber" at ISSM 2001. He became a Maintenance Supervisor in 2004 and has led the Fab Owners Association LAM 9600 team since March 2007.

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Executive Director, Fab Owners Association;
President, FOA Purchasing Partners, Inc.

L.T. is the executive director of the Fab Owners Association (FOA), a not-for-profit, mutual benefit corporation, providing a forum for fab owners and associates to discuss/act on common manufacturing issues, and president of FOA Purchasing Partners, Inc. (PPI) a group purchasing organization (GPO) for the semiconductor industry. L.T. is a graduate of Columbia Pacific University.

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Site Statistician, Samsung Austin Semiconductor

Bob Henderson is a site statistician at Samsung Austin Semiconductor. He holds a Ph.D. and an M.S. in mathematical statistics from Southern Methodist University, as well as an M.B.A. from the University of Delaware. Bob has authored or co-authored approximately 20 articles and two books on the use of statistical methods or approaches in semiconductor and other industrial settings.

Chris Howington

Supply Chain Re-Engineering Manager, Freescale Semiconductor

Chris Howington has over 20 years in the semiconductor industry in manufacturing and supply chain leadership roles. He is currently Supply Chain Re-Engineering manager at Freescale Semiconductor. Previous experience includes management roles at TSMC, National Semiconductor and AMD. Mr. Howington has a B.S. in mathematics from The University of Texas at Austin.

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Scott Kramer is vice president, Manufacturing Technology at SEMATECH, overseeing the ISMI subsidiary as well as business development and strategic planning for manufacturing productivity programs. He joined SEMATECH in 1994 as Fab Manager of the Advanced Technology Development Facility (ATDF). Mr. Kramer holds a B.S. in mechanical engineering from the University of Missouri and an M.B.A. from the University of Utah.

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EDITORIAL PANEL

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Director of Manufacturing, NEC Electronics America, Inc.

Matthew Nadeau is the director of manufacturing at NEC Electronics, America, Inc., in Roseville, Calif. He joined NEC in 1989 and worked as a process engineer in the Dry Etch and Wet Etch areas before starting his work in the manufacturing environment. Matthew received his B.S. in chemical engineering from the University of California at Davis.

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Senior Principal Engineer, BAE Systems Semiconductor Technology Center; Manassas, Va.

Murty Polavarapu is a senior principal engineer at BAE Systems Semiconductor Technology Center in Manassas, Va. Over the last 23 years, he has worked on developing and manufacturing advanced CMOS memory and logic products. His current interests include development of phase change memory technology and application of nanotechnology to meet the needs of the Department of Defense, particularly for space-based applications.

Bill C. Smoak

Vice President of Operations, Intersil Corporation

Bill Smoak is the vice president of operations for Intersil's silicon wafer fab site in Palm Bay, Florida. He has 28 years of semiconductor manufacturing experience in engineering, development, manufacturing systems and operations roles with Harris Semiconductor and Intersil. Primary experience has been in SOI materials and high-performance analog processes. Bill holds a B.S. in materials science and engineering from the University of Florida.

Christopher Tan

Deputy Director, Business Systems and Processes; Chartered Semiconductor

Christopher Tan joined Chartered Semiconductor in 1996, and is currently leading its supply chain integration and reengineering initiatives from the customer service, planning, industrial engineering, purchasing and logistics functions. He has a B.S. in economics from UOL from the Singapore Institute of Management.

Mario Tellez

Equipment Service Manager, ON Semiconductor

Mario Tellez is an equipment service manager with ON Semiconductor. He obtained his B.S. in electronic engineering and completed various studies in project management. Mr. Tellez has 20 years of semiconductor-equipment-related experience in photo, implant, diffusion, etch and backgrind. He has held various roles including lead technician, equipment engineer and equipment service management.

Kevin Venor

Manufacturing Development Engineering Manager, Avago Technologies

Kevin Venor is the manufacturing development engineering manager for Avago Technologies in Fort Collins, Colo. He has more than 20 years of experience in the semiconductor industry and has held various positions in R&D, manufacturing and business development at Hewlett Packard, Agilent Technologies, SEMATECH and Avago Technologies.

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Yonathan Wand is Numonyx Manufacturing Vice President and Numonyx Israel General Manager, in charge of Fab1. In his 28 years in the semiconductor industry, he has lead Fab18 to achieve world-class LY, DY and cost, and lead a factory to achieve single-digit DPM defects levels for automotive products. He holds a B.Sc. in chemistry from Tel-Aviv University and an MSc. in applied chemistry from the Hebrew University in Jerusalem.

Mike Weiby

Corporate Environmental, Health and Safety Manager; Integrated Device Technology, Inc. (IDTI)

Mike Weiby has 8+ years managing ISO 14001 and environmental programs, injury/illness prevention, emergency response, business continuity and risk management/loss control plans. He has an M.B.A. from Portland State University, a Master of Industrial Safety degree from the University of Minnesota-Duluth and a Mechanical Engineering degree from the University of Wisconsin.

Greg Westby

Purchasing and Materials Manager, Integrated Device Technology

Greg Westby is the purchasing and materials manager at Integrated Device Technology's 200 mm wafer fabrication facility in Hillsboro, Ore. Mr. Westby earned his M.B.A. from the University of Portland and has over 19 years of semiconductor experience, 12 of which are in procurement and materials management.

Gregory D. Winterton

Process Development Manager, TI's DLP® group

Greg Winterton is the Process Development Manager for TI's DLP group. Greg has responsibility for the development and production of TI's next-generation spatial light modulator MEMS devices. Greg is a 23-year veteran of the semiconductor industry with experience in process engineering, equipment engineering, manufacturing, technology transfer, and quality and reliability assurance on wafer diameters from 125 mm to 300 mm.

Juergen Woehl

General Manager/VP Manufacturing, International Rectifier; Temecula, CA

Juergen Woehl is the general manager/VP manufacturing of International Rectifier Temecula site in Southern California. Previously, he held management positions at IBM, Infineon, SEMATECH and ON Semiconductor. Juergen has over 25 years in the semiconductor industry, in engineering, manufacturing and R&D. He has a B.S. in chemistry from the Fachhochschule in Aalen, Germany, and an M.B.A. from St. Edwards University in Austin, Texas.

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Matthew Nadeau
Director of Manufacturing, NEC Electronics America, Inc.

An Unprecedented Look at the Recovery of the Semiconductor Industry

When my teenage son recently asked me how things were going at work, I found myself caught off guard. Although he has a good understanding of what his dad does for a living, he hasn't expressed a great deal of interest in my company's well-being before now. After probing a little, I came to realize that his question was rooted in his (over)exposure to the many stories of companies going bankrupt, people losing their homes and employees getting laid off. Even for a 13-year-old, it's hard to avoid the constant presence of negative news reports related to the financial crisis that we're enduring.

What's most frustrating for many is the fact that there are so many unknowns attached to this economic turmoil. I'm not sure if anyone has been keeping a count, but I would not be surprised if the usage of the word "unprecedented" reached record levels in the media as the stock market registered losses not seen since the dot-com bubble burst or the post-9/11 drops. The frightening element of the word "unprecedented" is the notion that since we haven't seen market conditions like these in the past, we don't know what to expect going forward. There are no historical references for us to study to indicate what the recovery of the banks, the automotive manufacturers and the housing market will look like or when it will occur.

While all of the businesses related to semiconductor manufacturing have been uniquely impacted by the current state of our economy, there is undoubtedly one common theme for all: Now is the time to strengthen the core systems and processes. Inventory correction, supply chain reinforcement and yield enhancement are a few examples of the improvements that fabs should be implementing. This form of business optimization will allow companies to respond rapidly to signs of recovery and should enable them to return as stronger organizations. Although 2008 and the first part of 2009 have been treacherous, this is an unprecedented opportunity for semiconductor companies to take the necessary steps to prepare for the future.

The articles in Volume 6 of Fab Engineering & Operations provide a few examples of activities geared toward improving core operations. Expense and scrap reduction, process optimization and fostering healthy employee morale are topics presented as important reminders to look forward and prepare for better days to come.

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Keeping Your Sanity in Difficult Times: Staying Competitive While Making Hard Choices

Jennifer Kalmbach – agileTCP

Abstract

The current global economic crisis has even the most seasoned executives at a loss for how their companies should plan for the future. The financial crisis, combined with unprecedented reduction of average selling prices, revenue and savings among some chip makers and suppliers, has even the experts disagreeing on what should be done to survive. This article is not about how to run your business but how to best keep your sanity while making exceedingly painful decisions in positioning your company for the future. A fully engaged and committed workforce will ensure you and your company come through this time as high-performing as possible.

Recognize the Situation

Not all companies are large enough to house their own internal team of analysts to prognosticate the future. But you know what type of situation you are in judging from your bookings, billings and sales pipeline. If you are having trouble making heads or tails of your situation, rely on other executives and analysts in your field to help sort things out. If you are not already in a professional networking group – which may feel more like a support group these days – then get in one. Your networks, industry associations or online communities can help. Many are going through the same or similar struggles. Make certain the contacts you lean on are leaders – positive in their thinking and decisive in their action; and make yourself available to others as well.

Be a Leader

Your company needs you to lead. Your family and friends need you to lead. This is no time to shirk. Your own strength of leadership is hopefully what provided the open door to your current level of employment. Recognize that no one knows the perfect answer in these times. Well-thought-through, decisive action not only exudes leadership, but improves morale. Being a leader involves maintaining your integrity. Tried and true principles of integrity are timeless: honesty, trustworthiness, fairness. Don't be tempted to waver from your high standards: Hold the trust of those who depend on you and maintain a clear conscience.

Understand Your Options

Understand the implications of all of your decisions: ethical, legal, financial, cultural and personal. The law and culture varies by region. Our global market may cause you to take this for granted, but you wouldn't be the first to be caught off guard by a regional difference. Other impacts will be specific to your company as well, and we can't pretend to know the extent of issues we will be forced to balance. Keep your work and family life in balance. Don't forget your life's priorities and purpose; write them down. Your vision keeps you, your family and your company strong. Without a clear vision, your staff may lose their way.

Understand the Value of Investing in Your Company Morale

Increasing your corporate revenue requires the building up of your people. Without your leadership, the people will be distracted by the dreadful rumor mill. Valuable energy necessary for productivity can easily be stolen through uncertainty. But with your direction, the workforce will gain steady confidence. Investing in your people shows that you sincerely value them. While some managers set team building as a priority, others feel that during a layoff, one should feel lucky to have a job and choose to ignore the emotional impact that ripples down through the company. Keeping morale high isn't just good for the employees, it's essential for the good of the entire organization. Make your company an

employer of choice in preparation for economic recovery, allowing employees more opportunities.

In a study of 24 publically traded companies, those with high morale outperformed similar companies in their same industries by almost 2.5 to 1, while the stock prices of companies with medium or low morale lagged behind their industry peers by more than 1.5 to 1.[1]

2005 Stock Gains

Likewise, in a similar study of 50 global companies, those with highly engaged employees increased operating income 19 percent and earnings per share almost 28 percent over one year, while companies with low employee engagement levels showed declines of 32 percent in operating income and 11 percent in earnings per share.

Strategies for Keeping Morale Up: Continuous Learning

In keeping with the theme of learning from your networks, I've asked a number of experts from ours and other industries for in-depth perspective on the key values of their operation in today's economic climate.

Here are their comments:

"Great leaders create morale positively or negatively from the top down. This is the time leaders have to take control and let their people know that this is a team effort, and together we will survive. Remember to generate your own positive morale by not worrying about things you cannot control, but plan and take action on what you can control. Ensure you are giving every day your best. Stay away from negative people and attitudes. Take control of your own expenditures and get lean; there is no better feeling than knowing you've made sound decisions related to personal finance. Debt only adds more pressure. Finally, stay busy; there is nothing worse than just sitting idle; if you don't have anything to do, then find something to do that will be constructive for you, the company and your community."

... automotive general manager

"Don't forget what keeps the whole business alive in the first place – your customers. Remember your customers are hurting as well. Value is more critical now than ever before. You will sell more today and raise your chances of keeping their loyalty when the sun comes back out."

"Reinforce the meaning of 'integrity' within yourself and your team."

"Use the lesser loading as an opportunity to educate, and where needed, reeducate your team. It's a good time for training."

"Rewards are essential. Publicly reward the people who are over-delivering. More than ever, they need and deserve it."

... VP chip maker taken from Jack Welch, 2009

"Layoffs are always an emotional roller coaster. The key is not to be stuck in the upside-down position without your safety harness securely fastened.

"Packages can be an opportunity to assess what you really want to do; try a different path, or challenge yourself greater in your current industry.

"Above all, do what you believe is right, seek wise counsel and try not to hurt anyone along the way."

... equipment manufacturer director of marketing

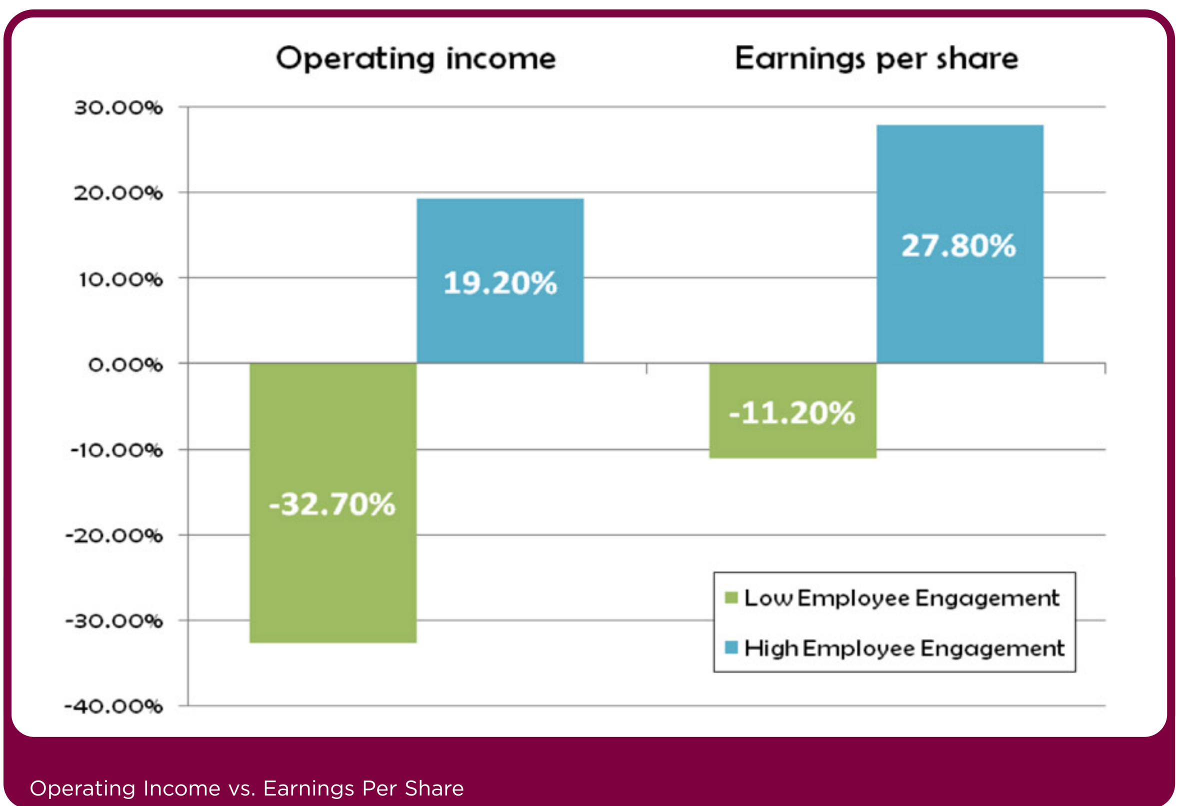
"Leadership needs to be visible and hands-on. To minimize damage to business in bad times, the leaders need to be active and communicate at all times. The leaders need to get out of the office and communicate directly. No slides, no fancy plans – talk to the people!"

"Morale, loyalty to companies and personal ambitions vary in many ways: by country, by industry, by age; understand this before concluding anything."

"Tell the truth! Lie just once and morale drops instantly."

"Keep regular meeting sessions, with fixed agendas."

"Work with the unions – not against them. Laws in this area are different in the U.S. and

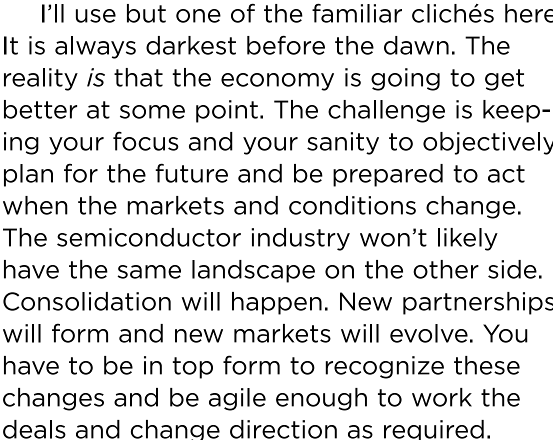


Operating Income vs. Earnings Per Share

Europe, making labor a critical component to success."

"Make sure you do everything you can for the people who have to leave"
... aerospace scientist

Reality Check



I'll use but one of the familiar clichés here: It is always darkest before the dawn. The reality *is* that the economy is going to get better at some point. The challenge is keeping your focus and your sanity to objectively plan for the future and be prepared to act when the markets and conditions change. The semiconductor industry won't likely have the same landscape on the other side. Consolidation will happen. New partnerships will form and new markets will evolve. You have to be in top form to recognize these changes and be agile enough to work the deals and change direction as required.

Though the strategies of the past may not apply right now, good principles and practice do, particularly when it comes to your employees. By keeping your employees' morale as high as possible, you'll not only have better performance from your existing workforce, but be better prepared and more efficient for the evitable upturn.

Absolute Must-Dos

Examine all options beyond the typical reactionary approach. Seek to lose less. Needless waste still haunts the halls of most every fab today. Gain competitive advantage by seeking counsel from experts who know how to assess, analyze and implement practices and methodologies to stop the bleeding. Doing so will help you succeed in maintaining and improving your workforce, keep your doors open and gain market share as the economic climate improves.

Endnotes

1. "High Morale Again Pays Off In Stock Market Gains," Sirota Survey Intelligence, 2006.
2. "Closing the Engagement Gap: A Road Map for Driving Superior Business Performance," Towers Perrin Global Workforce Study, 2008, p. 5. ■

About the Author

Jennifer Kalmbach

Jennifer Kalmbach, agileTCP's global engagement manager, is a published author on such topics as manufacturing cycle time reductions. She has also been an invited speaker for ISMI, SEMI, AFSME and Nanoscience member events, panels and think tanks. Proficient in predictive and preventative maintenance standards and fab-centric goals and achievement, Ms. Kalmbach serves agileTCP customers as a skilled team member of the factory cost-reduction tiger team.

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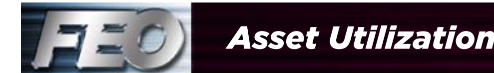

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Photoresist Bar Code Monitor

Mark Crabtree,[1] Dan Landry[2] – [1]NEC Electronics America, Inc. [2]Landry Engineering Development, LLC

Abstract

Automation, intelligently applied, reduces human error and the effects of human error on a working wafer fab. When a task cannot be taken over, but can be monitored by automation, the effects of human error can be eliminated.

This article describes the automated system implemented by NEC Electronics America semiconductor fab to monitor photoresist bottle changes on coaters. The system prevents installation of the wrong resist type, an error that could have costly results. Two generations of resist monitoring systems are discussed.

The first system was created in the 1990s, when the potential problem was identified and the consequences considered. That system has been in place, successfully, for nearly 12 years. More than a decade later, when a new set of coaters was being installed as part of an expansion, NEC Electronics America extended protection to the new coaters by working with the designer of the original system. That designer, now with Landry Engineering Development, a custom equipment manufacturer, designed a second-generation system that today provides improved protection with a simpler design.

Even in the hyper-automated manufacturing environment of a modern wafer fab, there remain many operations that defy automation. Replacing spent photoresist bottles is one of those tasks likely to be performed by operators well into the foreseeable future. In such a case (of a mission-critical task that can't be performed automatically), the best option is to monitor the task via an automated system.

This is the approach that NEC Electronics America has used in the past – with proven success. Over a decade ago, using the wrong bottle to replace an empty resist was a real possibility – with real potential for serious consequences. To prevent this possibility, equipment engineers at NEC Electronics America developed and implemented a networked, photoresist-monitoring system. Since that system was installed, there have been zero incidents of misset resists.

Recently, as part of an ongoing expansion and conversion to 8-inch equipment, several additional coaters were installed and put into production. It was clear that the additional coaters would have to be monitored too. The question facing NEC Electronics America was, "How can we dig into a 10-year-old, one-of-a-kind system

with antiquated hardware, unsupported software and orphaned programming without risking its continued operation?"

History

In 1996, NEC Electronics America became increasingly concerned about potential losses of product due to misset photoresists at its wafer fab in Roseville, Calif. A misset photoresist event can occur if a technician mistakenly replaces an empty bottle with a bottle of a different resist type, and then the coater resumes processing of the wafers with a resist not suited to the next process step.

It is not hard to understand how this could happen. At any point, a wafer fab can have upward of a dozen resists in use, on different coaters. Each coater would have three or four different resists on board, each selectable by different recipes for different processes. Commonly, the only indication the technician has (as to which photoresist to bring to the coater) is a brief glance at the empty bottle before heading off to retrieve its replacement. All resists from a particular supplier can have the same label style; the same colors, layout and logo – the only difference being the resist name printed on the label. In the production environment, with multiple demands on a technician's attention, it is easy to see how a mistake could be made.

The impact of a misset resist could be anywhere from bad to very bad. In the best-case scenario – where a mistake is caught before wafers are etched – the affected wafers could be reworked and the coater taken off-line while the resist circuit is purged, cleaned and set up with the intended resist. In the worst-case scenario, the replacement resist would be too similar to the intended one; so similar that it would not be caught at inspection, and the wafers would be etched. In cases of anti-reflective coatings, detection of an error would be even more difficult. The loss calculation in these situations would include the loss of product, the loss of fab time already invested in that product and the loss of the affected lots. Since the empty bottle is the main indicator of which replacement to retrieve, the potential exists to dispense more than one bottle of the wrong resist.

Once the NEC Electronics America team identified this potential problem in 1996, it determined that the situation was unacceptable. It was investigated and a number of process controls were considered. There was a strong feeling that such a simple problem should be simple to overcome. Check sheets, buddy system checks, oversized tags dangling over the bottle position, and daily meetings and reminders were all considered by production managers at that time, but no one option offered 100% protection.

Engineers at the NEC Electronics America wafer fab in Roseville determined that the only foolproof system would be a mandatory, interlocked system; in other words, a bottle of resist could not be changed without using the system, and the coater could not run unless the system was satisfied. The goal was complete elimination of the potential problem, so the system had to be 100% self-enforcing.

Approval and budget was given for a server-based, networked, photoresist bar code verification system. A DeviceNet network line was run under the floor with branches running to I/O cards mounted in the coaters. Existing sensors in the coaters were monitored and additional sensors were installed. Wireless bar code scanners were networked to the host system. The system functionality was designed to be self-enforcing and foolproof, but still easy to use, so that no one was encouraged to find a way around it.

Success

That system went live in June 1997, and has been working nearly 12 years without a

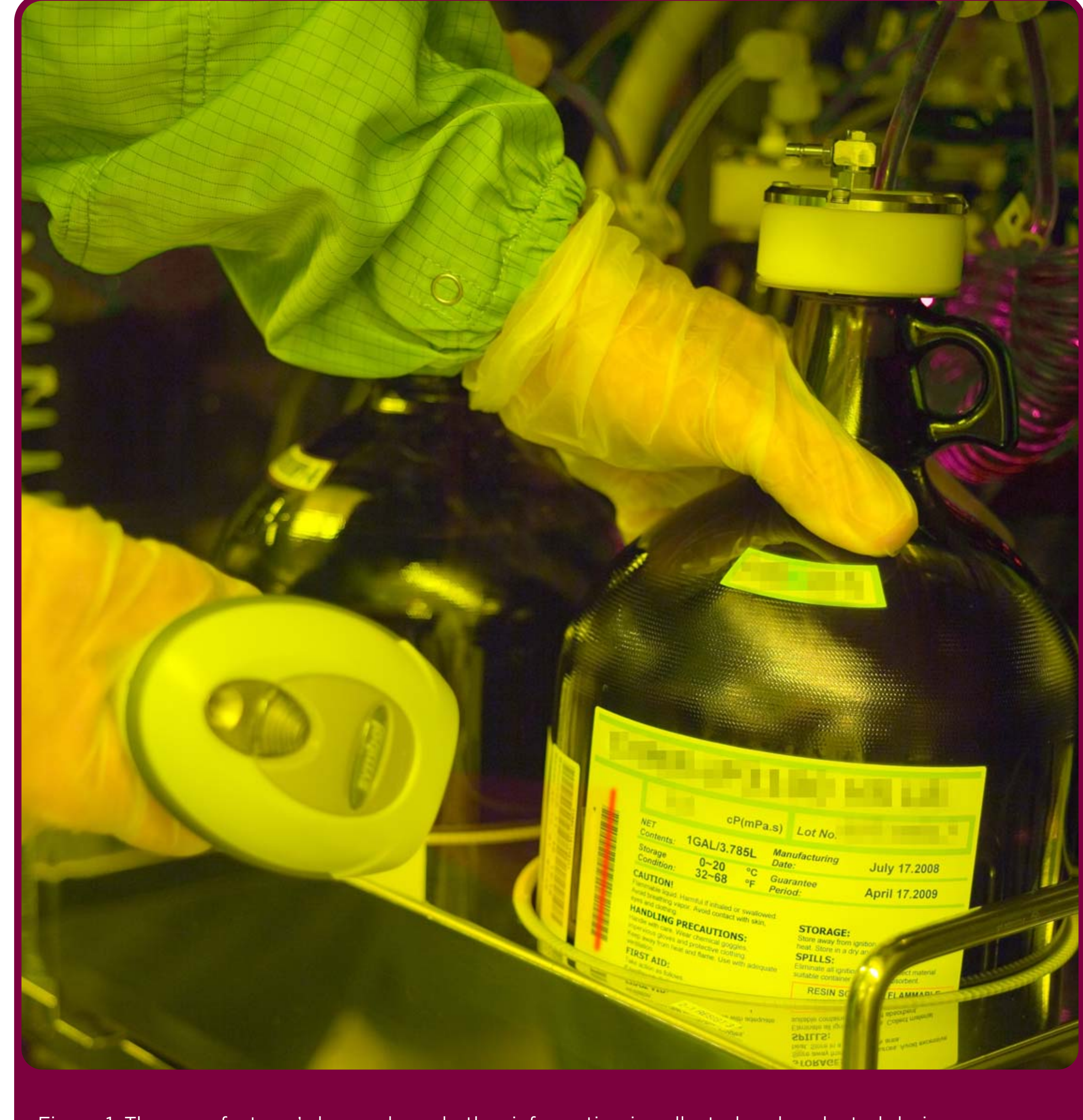

Figure 1. The manufacturer's bar code and other information is collected and evaluated during a resist change.

problem, or the threat of a problem. Exact savings are unknown, but, assuming a mistake would have been made during that time, the company has reaped savings of wafers lots not scrapped, production deadlines not missed, chemicals not wasted in purging and morale not lost due to a simple mistake with huge repercussions. The potential drawback was that the additional steps required of the chem techs would be seen as a burden, and cause complaints. But, according to the techs, the relief from stress overshadowed any additional steps in the bottle change procedure. The system has, more or less, become invisible and continues to work.

How to Protect Additional Coaters

Recently, over a decade later, as part of its ongoing 8-inch expansion, NEC Electronics America installed and put into service additional coaters. It was obvious that these new coaters should be protected, but it was not clear whether to try to expand the original system or replicate it.

Second-Generation Protection

The NEC Electronics America team consulted with Landry Engineering Development, a custom equipment manufacturing company, and selected a modular, serverless system. The modular system would be self-enforcing, interlocked and easy to use.

Figure 2. The system's user interface was designed to fit within existing panel cutouts.

Eliminating the central database, the network backbone and the networked wireless scanner system reduced the company's costs significantly.

Improved Success

Working closely with NEC Electronics America to ensure all needs were addressed, Landry Engineering Development developed a system that monitors the same criteria as the original system. When a replacement resist is brought to the coater (Figure 1), the coater remains interlocked until it is verified that:

- The new resist is the correct type
- The resist is placed in the correct position in the coater
- The thaw time for that resist type has elapsed, and

Figure 3. Utility and setup operations are performed at the user interface.

- The bottle being scanned is, in fact, new to that coater

In addition, the new system ensures that the new resist has not passed its expiration date, and also monitors all resists continuously to prevent the coater from running with an expired resist.

The system uses a dedicated, Bluetooth scanner at each coater. The controllers were installed in the coater's chemical cabinets so it was not necessary to find space on the coaters or add to their footprint. The user interface was customized to fit into the standard cutouts in the coater's instrument panels (Figure 2).

As with the original system, functionality was designed to minimize the impact to the bottle change procedure. The user interface is only used for utility and setup functions (Figure 3) or if a new user needs to be prompted through the bottle change steps. A trained tech, however, will not use the interface except as audio confirmation of the bar code scans.

Conclusion

Any opportunity to remove the potential effects of human error is a benefit to a wafer fab. The ideal case is when a task can be automated to remove human error altogether. If the task cannot be automated, it is possible that mistakes will be made. Automated monitoring is the best way to catch those mistakes and prevent losses.

Photoresist bottle changes are a good opportunity to catch mistakes and eliminate their effects through automated monitoring. A successful system must be self-enforcing and easy to use. NEC Electronics America was in need of a second-generation system to monitor recently installed coaters and was able to have it developed by the architect of their proven, first-generation system. ■

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Dan Landry

Dan Landry is a partner and co-owner of Landry Engineering Development, LLC. He received a B.S. degree in mechanical engineering and materials science from the University of California at Davis. Dan's first patent was initiated as a student intern at IBM. He joined NEC Electronics America in 1990. As equipment engineering group leader over masking, he created the company's original photoresist bar code system. Dan subsequently started Landry Engineering Development, which has been providing custom equipment and modifications to the semiconductor, biomedical and pharmaceuticals industries since 2000.

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DoE Method for Stress Optimization of PECVD Dielectric Thin Films Used in Microelectronics: Part II

Valerio Magazu – Numonyx

Abstract

Fixing dielectric film parameters in the development phase and keeping them repeatable during production is fundamental in microelectronics process flow. Interconnection and final passivation CVD dielectric properties layer can affect die attach (DA) cohesion in wire-bonded electronic packages. This work deals with the definition and application of design of experiment (DoE) for PECVD thin dielectric films, and specifically in this part II, used at the final passivation level, in order to optimize the intrinsic stress.

Passivation Nitride Layer

Si3N4 films deposited by plasma-enhanced chemical vapor deposition (PECVD) have been analyzed in literature by a variety of analytical techniques, including Fourier Transform Infrared Spectroscopy (FTIR), X-ray reflectivity (XRR) and Rutherford Backscattering Spectrometry/Elastic Recoil Detection Analysis (RBS/ERDA) to collect data on bonding, density and chemical composition, respectively.[1]

It has been generally found that the amount of bonded hydrogen as [N-H] detected by FTIR is higher for compressive Si_3N_4 films compared to that of tensile ones. The amount of bonded hydrogen in a film is well-correlated with tensile stress. Moreover, final exposure of Si_3N_4 films to elevated temperature (> 400°C) of final thermal treatments after deposition leads to film tension increase toward compressive stress with possible consequent electrical I-V characteristic shifts.

Stress components may generally be controlled in a repeatable way to realize tensile or compressive stresses (in-plane longitudinal) and positive or negative stress gradients (out-of-plane), by varying the RF deposition power.[2] But in our case (compressive stress 3–10 times higher than reference), only RF deposition power isn't sufficient to reach extreme stress values, so the gas ratio was also modified.

The aim of our trials was to develop (beyond the reference one), three final passivation silicon nitride layers that were more and more compressive.

For the process window definition, the original 80 MPa compressive stress has been enhanced up to 10 times. A three-level full factorial design on four factors was constructed for the experiments. Four repetitions of the center point were included. The factors were SiH_4 gas flow, RF power, pressure and gas shower to wafer holder spacing. The Si_3N_4 deposition runs were randomized. All films were deposited at 380°C. The N_2/NH_3 gas flow and process temperature were held constant during the experiments.

All the Si_3N_4 films were prepared on 300 mm Si from gas mixtures of SiH_4, NH_3, N_2 on a commercial, parallel plate PECVD system, using a 13.56 MHz RF power source to generate the plasma.

The measured DoE output responses were refractive index, deposition rate, thickness nonuniformity/range and stress. In studying DoE output, two main conclusions have been drawn:

- Low pressure values and high SiH_4 flow are mandatory to maintain RI values under control.
- HF RF and spacing have an influence, but are not a constraint with regard to RI.

In Figure 1, an overlay plot for an optimized high stress Si_3N_4:H process is displayed. The nonshaded area shows the optimized process regime. The point in the middle denotes the center point of the design of experiment.

Passivation PECVD Nitride Layer	Stress
Si_3N_4 600nm (used as reference standard)	-80 MPa
Si_3N_4 600nm “high” stress	-200 MPa
Si_3N_4 600nm “medium high” stress	-400 MPa
Si_3N_4 600nm “very high” stress	-800 MPa

Table 1. Nitride Film Definition According to Stress Values

Factor	LOW	HIGH
SiH_4	710 sccm	1070 sccm
HF RF	1200W (Delta std process = 0W)	2000W (Delta std process = 800W)
Pressure	3.7 torr	4.9 torr
Spacing	330 mils	530 mils

Table 2. Nitride Film Process Conditions

Following these preliminary considerations, a follow-up design of experiment table has been drawn (Table 3).

Contrary to what Martin and Evert[4] affirmed, the different conditions that we tested for dual frequency process were not promising. In fact, in testing dual frequency on a wide range of values, a high compressive stress of about -600 MPa was achieved, but with too high a range (more than 150nm for 600nm film thickness) and unacceptable values for NU%; thus double frequency approach was not pursued.

In Figure 2, the general response trends from the analyzed DOE are summarized. The up and down arrows indicate the directional change in the response resulting from an increase in a process factor. Double and single arrows respectively indicate a strong or weak dependence of a response on a factor over the range investigated.

In conclusion, it has been stated that it is possible to tune high stressed (-800 Mpa) single-layer silicon nitride film by manipulating the process chamber pressure, the composition of the deposition source gas adding He flow and a process window with higher single frequency HFRF (1380+/-40W) plasma power and cathode to gas shower spacing (1.2954+/-0.0508 cm).

A different experimental design, closer to standard deposition conditions, has been carried out to achieve passivation layer with -200 MPa and -400 MPa optimizing experimental variables. In this case, the use of Doehlert’s designs makes it possible to create sequential designs, and enables the use of blocks and the detection of lack of fit

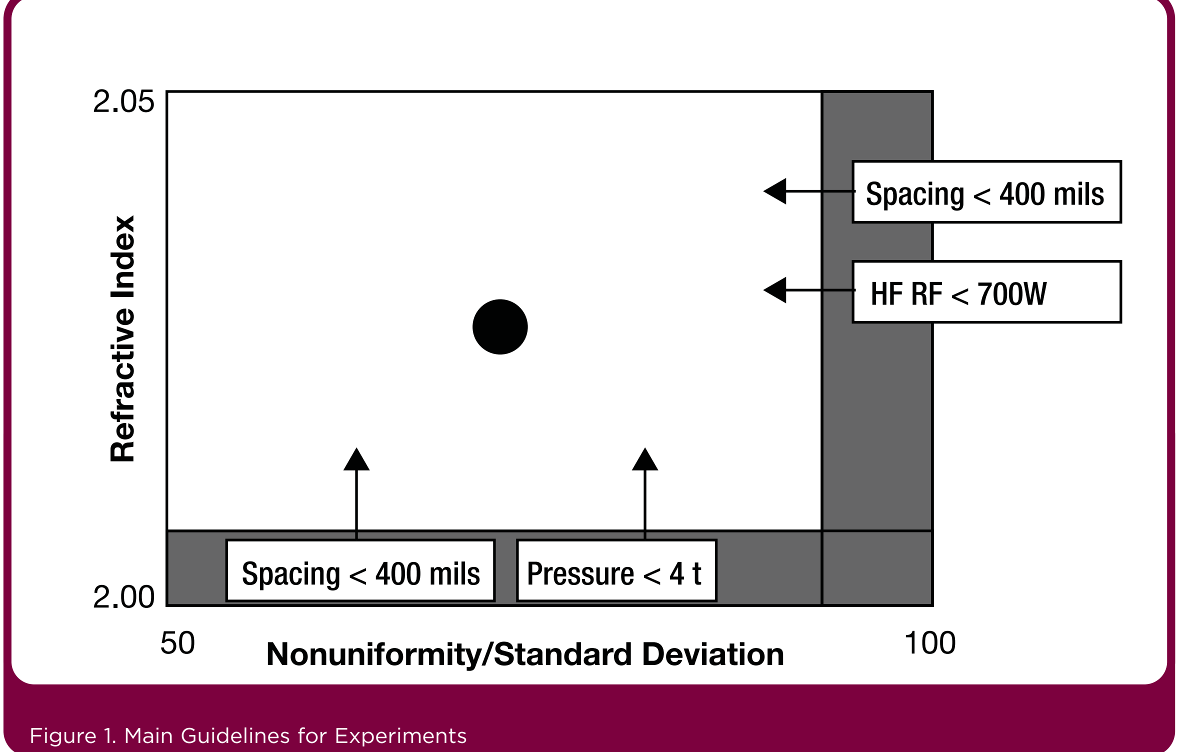

Figure 1. Main Guidelines for Experiments

in the calculated model by making replicates of the central point.

The plot of metrology results versus the experimental variables selected gives three response surfaces that allow the optimum conditions to be identified for the definition of the production process window. On completion of the DOE matrix and its analysis, a set of confirmation runs has been carried out around the optimum parameter set to validate the optimization.

Without going into myriad detail about all the performed trials, the matrix of influence for the main parameters in the whole experimented area is the same, and reported in Figure 3.

Process Window Comparison

The fundamental objective for a process window fixing is to ensure that the deposition process is suitable for production. Beyond considerations such as maintaining cost per wafer and of ownership, production suitability is mainly dominated by three concerns: deposition quality, process stability and throughput. The primary concern is that the characteristics of the deposition layer on the blanket wafer match the requirements process release (RPR) criteria. After that, the process variance must be estimated, and making a comparison between the different process windows is an essential requisite to evaluate the best process. For USG films, optimal conditions that achieved the desired performance and property goals for USG films were represented by a simple shift of standard condition to higher power RF and lower gas shower-to-heater spacing.

For passivation film, although the stress target was perfectly centered for all recipes, the other RPR criteria weren't completely met. To outline the Gaussian process repeatability distribution, three datum sets have been distinguished:

The first one is composed by high stress USG with high stress and medium high stress nitride passivation. The second group is the standard process flow with standard USG and passivation. The third datum set is composed by very high stress nitride passivation. The box plot of repeatability tests within these defined process windows for

PROCESS PARAMETER	RANGE	COMMENT
Pressure	3-4 Torr	Decrease pressure
HF RF	2400 +/- 100W	More narrow process window
Spacing	480-540	Increased spacing
SiH_4	890 sccm	Fixed
NH_3	455-655 sccm	
He	100-1000 sccm	Loboda and Seifferly[3] inferred from residual gas analysis that He enhances the creation of N+ species in the plasma resulting in increased incorporation of N bonding in the Si_3N_4 film. This results in compressive stress due to the volume expansion of the Si_3N_4 film.
Temperature	380°C	Fixed
Dual Frequency RF	350-550W	For Si_3N_4, a common technique allowing much more control of the stress in a conventional 13.56 MHz parallel plate PECVD reactor is the addition of low-frequency power (usually 450 kHz). The added low-frequency component results in high-energy ion bombardment of the growing Si_3N_4 film and this results in a more compressive stress state.[4]

Table 3. DoE Table Planning

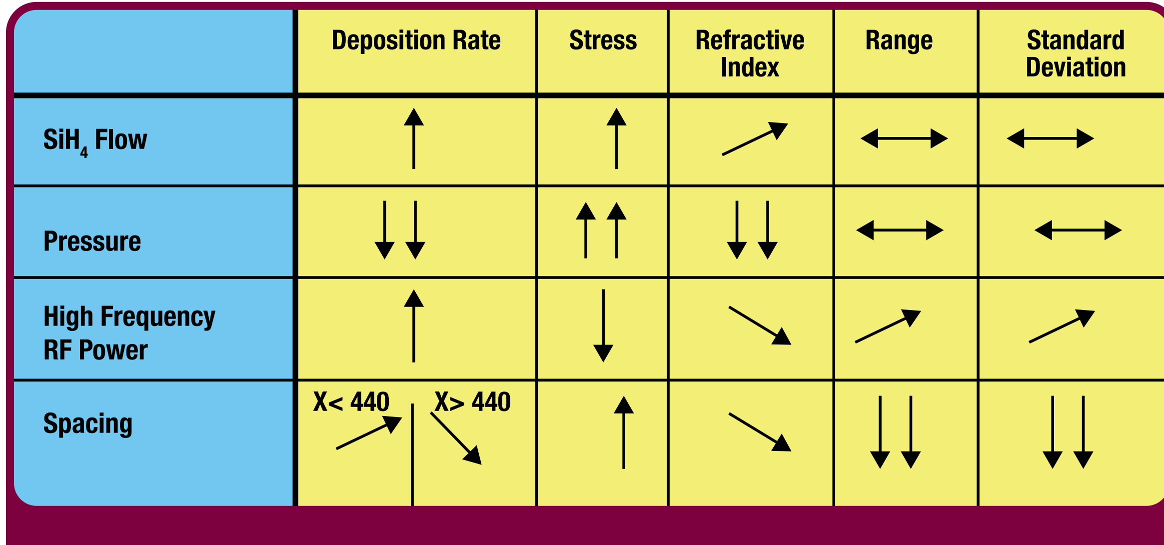

Figure 2. General Response Trends From Passivation DOE

	Deposition Rate	Stress	Refractive Index	Range	Non-uniformity %
Spacing	↓↓	↑↑	↘	↓↓	↓↓
High Frequency RF Power	↗	↓	↘	↑	↑

Figure 3. Passivation Nitride Matrix of Influence for Stress Up to -400MPa

the three groups is shown in Figure 4.

Every process, with the exception of Si_3N_4 VHS, meets the requirements, even if the processes of group No. 1 have a shrink factor lower than the processes of group No. 2, and considering that for Si_3N_4 non-standard deposition the High Frequency RF window is half the standard recipe (consequently more difficult to control), this suggests adopting a larger control chart gap. In the case of very high stress passivation nitride, it is only possible to establish an acceptable process window as a defined subregion inside the process space that is large enough to accommodate the natural variation of the process, but that is very sensitive at each tool parameter shift and doesn't perfectly match the target.

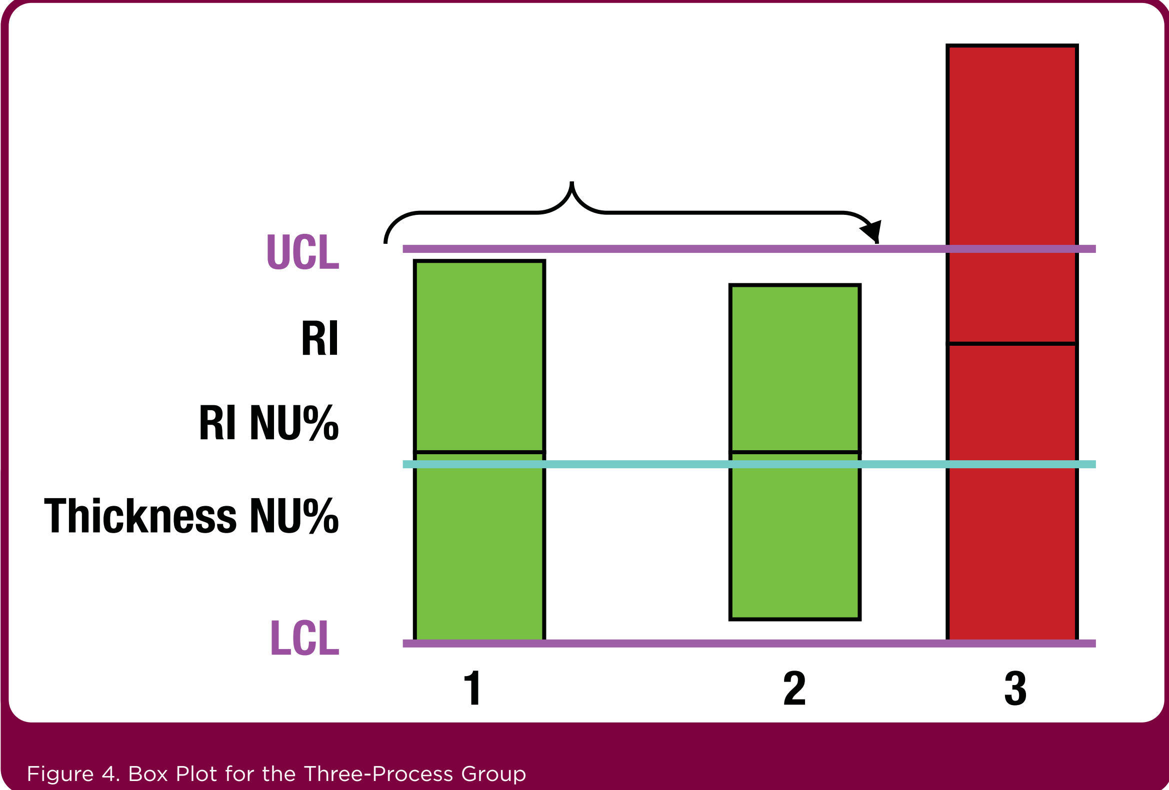

Figure 4. Box Plot for the Three-Process Group

Conclusions

This paper has described a methodology for ensuring adequate process robustness and developing high compressive stress layer following end-user requirements and achieving flat patterned wafers at the end of the process flow. We used well-known experimental methods and rigorous mathematical techniques. The application of different designed experiments permitted optimum conditions to be identified from a limited set of test runs, obviating the need for a full test matrix that would entail hundreds of deposition tests. Optimization of the process was carried out achieving three important goals:

- To define a deposition process that would achieve the desired film electrical performances and mechanical properties.
- To establish manufacturing robustness and the process window for a reliable process.
- To understand the process and trends that give an indication of, and can later be used as, a troubleshooting guide; when parameters are identified as significant, these variables will be the first areas of investigation in problem solving.

Acknowledgments

The author wishes to express his gratitude to Luca Zanotti for his very useful support.

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Variability Is the Root of Many Evils in Manufacturing

Rebecca Taylor, C. Richard Deininger – Taylor-Deininger Partners, Inc.

Every fab manufacturing operation has extreme pressure to cut costs and increase productivity. This paper focuses on reducing/eliminating the largest category of loss, to aid fab management in reducing costs in 2009 and beyond. This is critical to your bottom line.

We have found common themes in the fabs we visit: Firstly, there is a loss category called "unknown" that is typically one of the largest, if not the largest, category of yield loss. Secondly, there is absolute denial in many Fabs that facilities-supplied parameters such as water, gasses, etc., are experiencing any variability that could contribute to losses in yield or performance; that is, until they dynamically measure and monitor those parameters. Surprise! When dynamically measured, variation is found to be much worse than expected. Conclusion: These variables need to be monitored and controlled much more aggressively than is possible using techniques we have observed in most fabs.

We investigated further and base this paper on this subject, discussing how to address these issues. Up to now, they have been largely ignored. Read on for what we have found, and for recommendations on how to continually reduce (or even eliminate) this pernicious source of yield loss.

Variability is the root of many evils in a fab, causing a high percentage of unexplained wafer and die losses. Rooting out variability nets benefits in ways that accrue to substantially all of the wafer losses in a fab. We thus focus this paper on the "Ghost of the Unknown Failure," and how to remove it from your fab.

Following are three situations we have observed. They each affect a different part of the fab, and each is related to failures caused by variability. To repeat: The typical situation in many fabs is that they consistently experience 10 percent or more of wafer losses in an "unknown" category. This category is usually in the top three of wafer loss causes.

Therefore, the question to ask is, "What, given its prominence, can be done to eliminate the "unknown" from the pareto, and what is the value in so doing?"

The following situations involve wafers being lost due to out-of-spec chilled water temperatures, irregular DI water flows and gas/air flows dipping unpredictably. All of these scenarios also contribute to die yield losses, as well as equipment failure, downtime and cost increases.

The following examples will make the point that costs can be saved by using common-sense approaches to avoid many "unknown" problems.

1. Process Cooling Water Temperature and Flow Variability

In a number of fabs, we have seen problems caused by variation in these parameters. In all cases, there was no dynamic monitoring of these parameters. Without data to pinpoint timing of temperature changes, it is difficult to correlate the variation to specific losses. Until the cause is determined and corrected, wafers continue to be lost. Three specific examples:

- ***Fab 1:*** Chilled water flow and temperature variation caused chuck overheating and related yield/performance problems with the etch tools. Once the variation problem was identified and fixed, the etch issue disappeared.
- ***Fab 2:*** Variability in water flow and temperature was an issue in diffusion. Water flow and temperature should be considered as high impact opportunities that affect die yield and performance, and should be considered a high impact opportunity for remote gauge reading.
- ***Fab 3:*** IRIDIA tool problems appear to be affected by water temperature variation, which can cause poor control of RF/temperature and affect wafer film deposition.

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Figure 1. Wireless Gauge Reader 'Facemask'

There is a definite need for dynamic chilled water flow monitoring capability. Monitoring confirms that chilled water is: 1) flowing, and 2) the temperature is not varying in/out of limits. Variation affects die yield and does not show up in any other way. It is an example of a subtle failure with large implications to profitability.

Effective cooling water management requires targeted, remote dynamic wireless monitoring and alarming of gauge readings. There are thousands of static gauges already installed in most fabs that can be inexpensively updated with remote, wireless gauge readers. The cost of this approach is much less than it was even three years ago. This is due to the confluence of low-power processors, wireless communications and advanced optics that can convert an analog reading into a digital number. Cypress Envirosystems' wireless gauge reader is a good example of this capability (see Figure 1).

To measure the benefits in an objective manner, and to help determine which gauges are most important to monitor, TD Partners created a series of simple modeling tools. This modeling shows break-even payback by monitoring the cooling water in less than three months.

2. Compressed Air/Gas Pressure Variability

We have also seen significant pressure variation issues relating to compressed air and process gas. Many fabs have no monitoring of these supplies. Without real-time data to pinpoint timing of pressure changes, it is difficult to correlate the gas and air pressure variation to specific losses. Until the cause is determined and cor-

rected, time elapses and wafers continue to be lost.

- Using quarterly ops review figures from an operating fab as illustration, some specific tool issues with process gas and compressed air variation are as follows:
  - Chuck "clutch" issue – lost seven wafers/week
  - Wafer handling – lost six wafers/week
  - Chamber pressure manometer – lost four wafers/week

- Fabs typically rely on the MFCs within a tool to control and track gas usage. There are two–three events per year caused by a gas outage, which affects an entire lot. Monitoring gas bottle pressure directly, by dynamically monitoring the gauge reading on the bottles, will reduce this situation.

Our modeling shows a break-even payback in 3 months, sometimes less.

3. Tool Internal Variability

A third type of variability emanates from within a tool. This failure is not visible without remote monitoring due to enclosed gauges inside a tool, or otherwise housed to make the data infeasible to collect.

At a contract pilot line company, CMP slurry filters were clogging at unpredictable intervals, requiring one–two wafers to be scrapped before the clog was identified and the filter changed. This event occurred every seven–14 days. The financial impact of this situation, given that it happens toward the end of the wafer manufacturing process, is that the wafers are nearly fully loaded with cost. The market value was estimated at $1,650 each for this fab.

There were two approaches under consideration in this situation: 1) change the filters more frequently, or 2) monitor pressure across the filter and send an alarm to operators when the filter is nearing its operating limit. A third alternative is to do nothing, and take the hit when a wafer is scrapped. Let's look at the cost of these three approaches.

Changing the filters twice as often reduces but does not eliminate the problem. This solution requires at least 26 additional filters/year at a cost of $4,160/year and involves unnecessary tool downtime that significantly impacts throughput of the CMP area. It does not eliminate the potential for an actual filter clog event and resultant $1,650 wafer scrap.

The most common-sense approach involves monitoring the filter pressure, tracking it and alarming when the filter is nearing its operating limit. This maximizes tool production availability and eliminates associated wafer scrap. The one-time cost of this approach: $1,250 per filter.

With a wafer cost of $1,125, the ROI is a bit more than one week. When factoring in lost revenue of $1,650 – more appropriate given that CMP is typically done toward the end of a wafer's processing life the ROI is less than one week.

As a test, a wireless gauge reader (WGR) from Cypress Envirosystems was installed on a CMP tool. After WGR was in use for one week, the filters were found to clog from three hours to 15 days after installation. The fab derived a strategy for dealing with the clogging filters that included setting alarms for filter replacement.

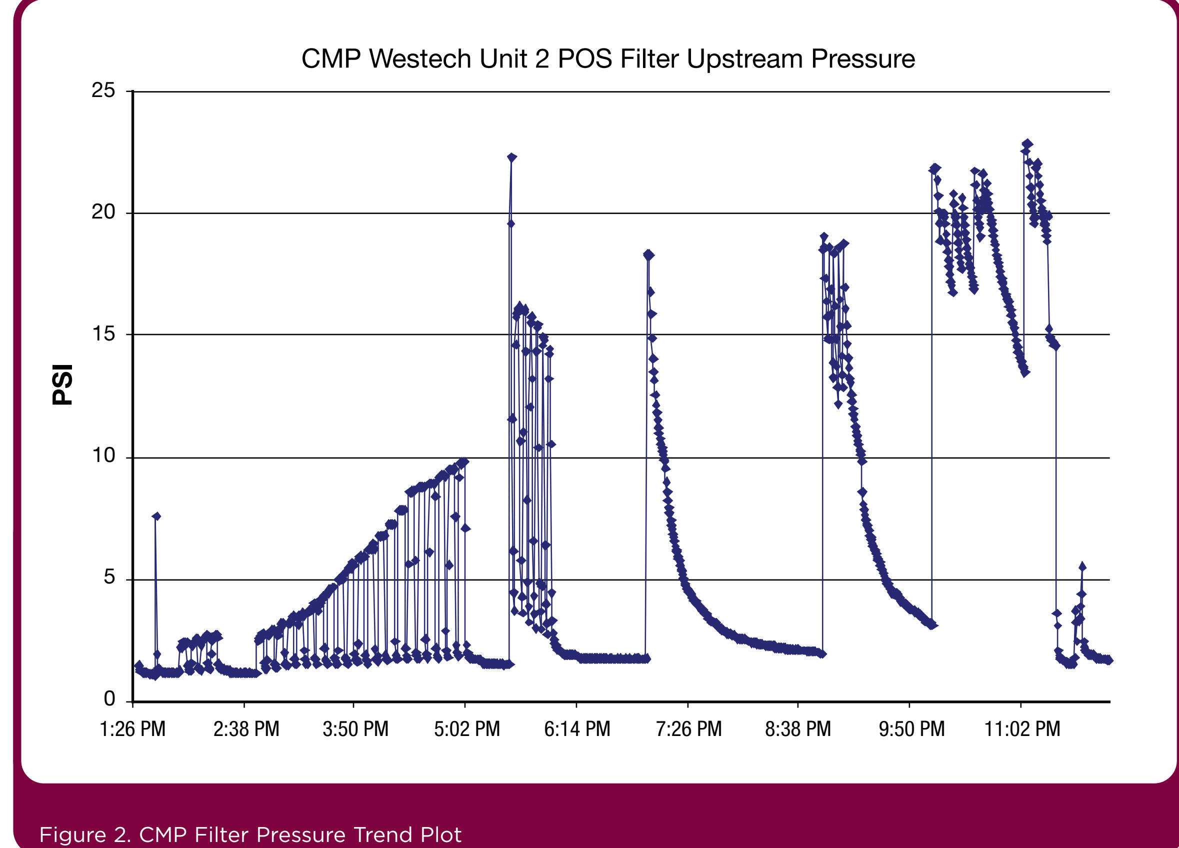

Figure 2. CMP Filter Pressure Trend Plot

Halftime Summary

Facilities parameter dynamic monitoring is essential to get on top of these problems. That does not mean every one of the thousands of gauges needs to be monitored, only those where a cause and effect can be identified.

We have illustrated where some of the opportunities lie with these examples.

Now, we move to the really big idea, that we derived based on our observations at multiple fabs.

Advanced Process Control Opportunity

Dynamic real-time data monitoring further increases the opportunity for implementing advanced process control (APC) applications, extending the reach and results of APC further into fab operations. The additional key enabling technology that raises the bar is, once again, the inexpensive ability to do dynamic wireless parameter monitoring. APC applications have been accepted as a normal practice within and between tools to increase processing precision, to increase yields and reduce losses/costs. It also accommodates chamber and other differences between tools, eliminating the need to dedicate tools for sensitive processes.

We ask the following question: Why hasn't that concept been adopted around the infrastructure and facilities to minimize and eliminate the effect of abnormal facilities supply variations? This includes temperature, pressure, flow, energy, water and gas variations – all of which can and do affect the end product and cost.

The first answer is that variation in facilities-supplied parameters were not consid-

ered significant at the time the fab was built. These variables are thus not dynamically measured. Most are metered with statically read analog gauges. Most are hidden from normal view. No one looks at them unless there is a problem, and then they get only static readings after the loss or damage has occurred. There is thus no ability to correlate product loss events with facilities variations.

The second answer relates to significant new capabilities and an equally significant cost reduction relating to remote monitoring, available as of about two years ago. Inexpensive wireless gauge reader adapters make it possible to inexpensively dynamically monitor these gauges for abnormal variation. This enables alerts for immediate corrective action before product is adversely affected. In addition, it will identify areas where abnormally high gas, water or energy usage is occurring, thus allowing corrective action to be taken to reduce waste and save cost. It enables the development of applications to address supply and infrastructure variation issues. It is an opportunity to bring APC applications to the facility, particularly for companies that have already implemented APC technology.

Any parameter that is monitored can then be controlled. Most fabs start by establishing simple SPC charts and then by alarming the out-of-limits deviations of that parameter. A next step is to correlate out of limit deviations with product and die yield losses. The following step is to implement the feedback loop to automatically adjust the pressure, temperature or the flow for the given parameter.

Remote dynamic monitoring enables the data collection for potential "dynamic closed loop control" of numerous facilities-based parameters that affect chip yield and chip performance. These APC applications are similar in many ways to those currently used in other portions of the Fab to improve yield, productivity and save money.

The final conclusion: Dynamic parameter monitoring is a proven approach to reducing costs with rapid payback. Using APC approaches, based on accurate real-time data collection, have been found to be effective in all applications where they have been implemented, and should be implemented for facilities applications to reduce variability. This brings the fab to a new level of control. The benefits of control such as this provide very rapid payback. ■

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High Performance and Zero GWP Fluorine-Based Chamber Cleaning Recipe

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Abstract

In this work, a new F_2 gas mixture was tested. This novel $Ar/N_2/F_2$ recipe has been evaluated as a candidate to replace conventional cleaning gases, like NF_3, C_2F_6 and CF_4 in an industrial AMAT P5000 tool, which shows complete compatibility with the new gas. The tested $Ar/N_2/F_2$ mixture shows remarkable performance, both in terms of etching rate and in terms of gas consumption.

Introduction

Regular removal of residuals has to be done to obtain stable and repeatable deposition results with uniform surfaces at acceptable particle levels[1] in all PECVD equipment. For a long time, chamber cleaning gases like Tetrafluoromethane (CF_4) and Hexafluoroethane (C_2F_6) have been used.[2-4] Nitrogen trifluoride (NF_3) has emerged as the main cleaning gas for 300 mm tools equipped with remote plasma source (RPS) systems, which show significantly shorter clean times compared to C_xF_y-based cleans.[5-6] All mentioned cleaning gases have a high GWP value.

The work presented here investigates argon/nitrogen diluted fluorine ($Ar/N_2/F_2$), delivered from conventional gas cylinders. 20% F_2 mixtures are easily available on the market and are already delivered in bulk quantities to the automotive industry for the fluorination process of plastic gasoline tanks and to the semiconductor industry for "thermal cleaning." Our approach – using the classical stainless steel gas cylinders – differs from the on-site fluorine generation, that utilizes hydrogen fluoride (HF) as feed material.[7-9]

It is important to underline the good environmental properties of the mixture $Ar/N_2/F_2$, due to the fact that its global warming potential (GWP) is zero.

Experimental

Gas mixtures in stainless steel cylinders containing 20% F_2 were used; this F_2 concentration conforms to the standard used in the automotive and semiconductor industries, so that all necessary system parts can be easily procured on the market.

The tests were performed in an Applied Materials PECVD reactor on a P5000 mainframe.

The wafer size for all experiments was 200 mm. The F_2-containing gas cylinder was installed inside a gas cabinet close to the CVD reactor.

For the safe, clean and dry handling of the fluorine gases, a three-way purging unit is part of the gas supply. The gas line was connected in the form of a T-connection to the existing standard CF_4 gas line, which is used as the standard Applied Materials chamber cleaning gas for this reactor. For the precise gas flow control, a metal sealed MFC was applied. Two F_2 resistant O-rings (Isolast 9675) from Trelleborg Sealing Solution Germany GmbH were installed; one for the chamber lid outer seal and one for the gas feed-through.

The CF_4 gas line was passivated according to the procedure of Solvay.

The best mixture and the best working parameters were selected calculating three L9-Taguchi matrices; the best mixture was identified with the following composition: 10% Ar/ 70% N_2/ 20%F_2.

In order to investigate the etching gas performance (etching rate and etching nonuniformity), SiO_2 and Si_3N_4 layers were used. For this purpose, blank 200 mm-Si-wafers were deposited with a 1µm thick oxide layer (silane-based PECVD); additionally, Si wafers were deposited with a 550nm thick Si_3N_4 film.

Three repeatability runs with the selected 10%Ar/70%N_2/20%F_2 mixture were carried out by using a batch of 25 wafers per run. The wafers in slots 1, 12 and 25 were monitored for particle contamination. The particle performance behavior of the cleaning gas mixture was measured on particle monitor wafers by a Tencor Surfscan 6400. The minimal particle size measured was 0.25µm.

Results

The first plasma ignition of the F_2/N_2 mixture could be achieved without observing arcing or other unknown effects, with the following parameters: chamber pressure: 5 torr; N_2/F_2 gas flow rate of 1 slm, temperature of 400 °C and 570 mils spacing.

The effects of the parameter variation on the performance of the F_2/N_2 plasma were evaluated through a first L-9 Taguchi matrix on SiO_2 as well as on Si_3N_4.

The addition of Ar to the mixture improves the uniformity of the process. It is possible to achieve etching rates > 1300nm/min even maintaining nonuniformity values < 5%, far below the value of 20%, which is generally considered the highest acceptable. These results are encouraging, in consideration of the fact that the addition of Ar dilutes the concentration of the active specie F_2, which is not desirable.

As a consequence of the described test results, the mixture 10% Ar/70% N_2/20% F_2 was chosen for the following parts of this study. The mixture was premixed by Solvay Fluor and delivered in a cylinder, so as to avoid any F_2 dilution effect by adding Ar during operation.

In order to test the repeatability within-wafer, wafer-to-wafer and batch-to-batch of the $Ar/N_2/F_2$ etching and particle performance, three runs with 25 wafers each were performed. Processing the wafer batch was done in full automatic mode, by the deposition of a 1µm SiO_2 film for 35 sec and a subsequent 60 sec plasma chamber clean in $Ar/N_2/F_2$ gas. The particle monitor wafers were placed in slot 1, 12 and 25, respectively. Immediately after SiO_2 deposition, the wafers left the CVD reaction chamber.

The cleaning recipe was chosen as follows: a gas flow rate of 900 sccm $Ar/N_2/F_2$

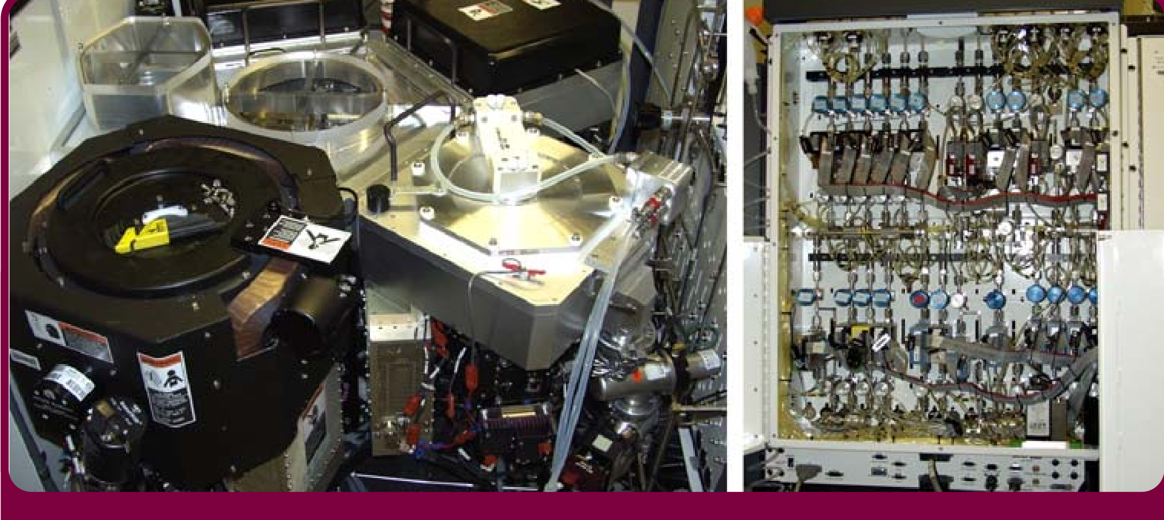

Figure 1. View of the AMAT P5000 which has been used for the experiment. On the right, the gas cabinet where the F_2 mixture has been flown in the existing CF_4 line, after passivation.

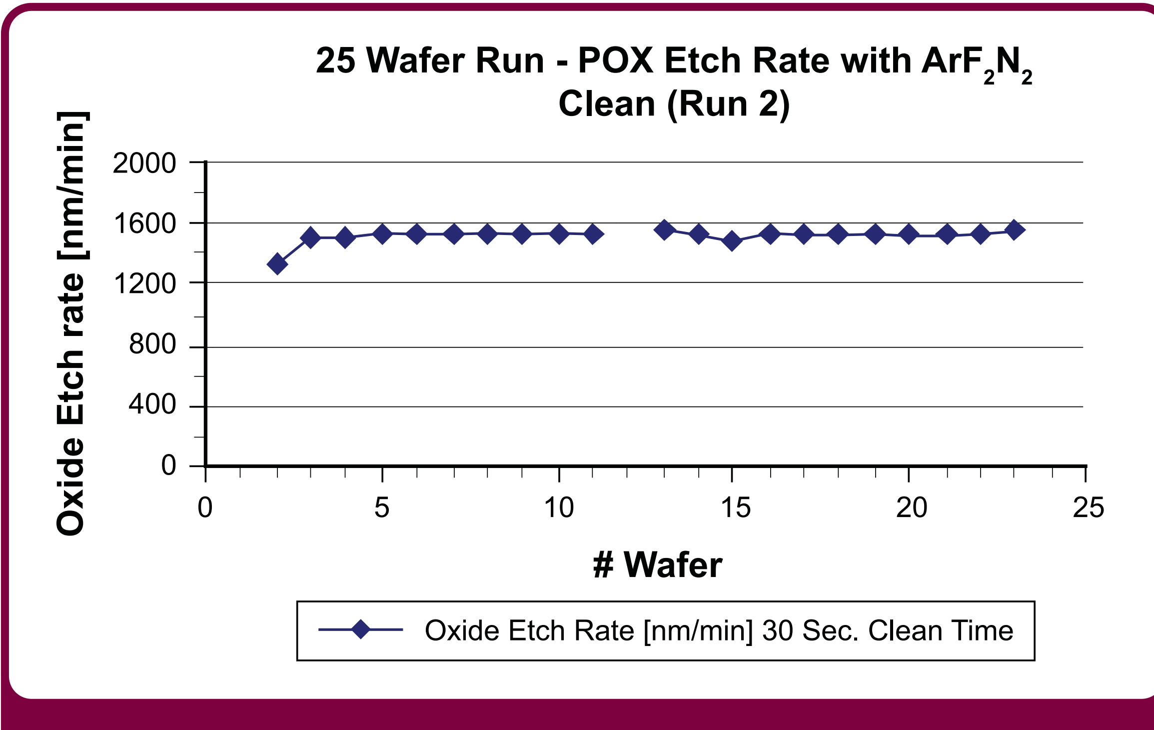

Figure 2. Repeatability (within-wafer and wafer-to-wafer) runs of SiO_2 etching rate [nm/min] of $Ar/N_2/F_2$ for 30 sec. as a function of wafer position (total of 25 wafers).

and a chamber pressure of 2.1 torr. The RF power was 800 W and the susceptor temperature was 400°C with 540 mils spacing (maximum spacing value on the silane-based oxide/nitride CVD chamber). The total cleaning time of 60 sec included an over-cleaning of about 30% in order to verify that any previously deposited oxide at the chamber walls, pumping plates, susceptor edges and on the shower head would be completely removed.

The deposition recipe to deposit 1μm of SiO_2 was the standard BKM recipe of Applied Materials with SiH_4 and N_2O as the main process gas.

A SiO_2 deposition of about 1034nm was achieved for all 25 wafers. The oxide deposition nonuniformity was measured within-wafer as well as wafer-to-wafer. The within-wafer oxide deposition nonuniformity was about ±1.4% (1 sigma) and wafer-to-wafer nonuniformity was ±0.8% (1 sigma), demonstrating a very stable oxide deposition.

In order to verify the repeatability of the SiO_2 oxide etching rate for 25 wafers, the previously deposited wafers were run again and partially etched by $Ar/N_2/F_2$ for 30 sec. After measuring the remaining oxide thickness, the cleaning rate was calculated.

Figure 2 shows the results of SiO_2 etching rate of $Ar/N_2/F_2$ as a function of wafer position (run No. 2). For the first wafer, the etching rate was about 1280nm/min and significantly lower compared to the rest of the 24-wafer batch, indicating the "first wafer effect." From the second wafer on, the oxide etching rate was, on average, about 1525nm/min for all wafers with a corresponding within-wafer oxide etch nonuniformity of ±7.1% (1 sigma). This shows, within the wafer as well as wafer-to-wafer, a very repeatable and stable oxide etching rate.

In order to verify $Ar/N_2/F_2$ etch rate nonuniformity on SiO_2 from batch-to-batch, three wafer runs (75 wafers) were carried out. Table 1 displays the result of all three runs. An average SiO_2 deposition thickness of 1036nm was achieved for all three wafer batches. For all three runs, the within-wafer oxide deposition nonuniformity was, on average, ±1.3% (1 sigma) and the wafer-to-wafer nonuniformity was, on average, ±0.7% (1 sigma), demonstrating a very constant oxide deposition across all three batches.

The $Ar/N_2/F_2$ etching rate on SiO_2 was batch-to-batch, on average, (mean) 1522nm/min with a corresponding within-wafer oxide etch nonuniformity of ±8.0% (1 sigma). For all wafer runs, this demonstrates a very repeatable and stable oxide etching rate of the $Ar/N_2/F_2$ gas mixture.

To obtain information about the particle performance behavior of the $Ar/N_2/F_2$ etching gas mixture on the wafer surface, three particle monitor wafers (located in slots 1, 12 and 25) were measured before (reference) and after the wafer run. With a Tencor Surfscan 6400, the minimal particle size measured was 0.25μm. The virgin reference wafer showed a particle contamination of about 20 particles (0.25Qm). The results of the particle measurements are shown in Table 2.

On average (mean), just 14 particle adders were generated from run-to-run. The data indicates that no significant particle contamination was induced by the process, and $Ar/N_2/F_2$ can be used as a highly clean etching gas.

It must be pointed out that all the obtained oxide etch rates and oxide etch nonuniformities of the $Ar/N_2/F_2$ cleaning gas mixture on SiO_2 are equal to or better than the standard CF_4-based BKM chamber clean of Applied Materials.

The achieved cleaning time with $Ar/N_2/F_2$ gas mixture was approximately 30% shorter than the CF_4-based BKM Applied Materials clean time. The particle values were < 50 adders, which is well within specification for the AMAT P5000 process based on CF_4 cleaning chemistry.

The chamber was opened after processing the first 25-wafer run as well as after the final run (run 3) and visually inspected. For both inspections, the surface of the showerhead, shadow ring, pumping plate and chamber lid O-rings were clean and showed no signs of wear or residue.

Si-pieces with a thin SiO_2 layer were placed on the pumping ring, in order to check the cleaning efficiency outside the

Run #	Depo Nonuniformity			Clean Nonuniformity		Reference CF_4 BKM	
	SiO_2 Thick.	Within Waf	Waf - Waf	Clean Rate	Within Waf	Clean Rate	Within Waf
	nm	1% sigma	1% sigma	nm/min	1% sigma	nm/min	1% sigma
1	1040	1.2	0.6	n/m	n/m	850	2
2	1034	1.4	0.8	1525	7.1		
3	1035	1.3	0.6	1518	8.8		
Mean	**1036**	**1.3**	**0.7**	**1522**	**8.0**	**–**	**–**

Table 1. Summary of the three repeatability runs of 1μm- SiO_2 deposition for 35 sec, followed by an $Ar/N_2/F_2$ chamber clean etching for about 60 sec. The data showing the average values of SiO_2 layer deposition thickness [nm], oxide deposition nonuniformity (within wafer/wafer-to-wafer) in [1 sigma] and $Ar/N_2/F_2$ oxide etching rate [nm/min] nonuniformity (within wafer) in [1 sigma] for three wafer runs (total 75 wafers). The average (mean) values of the batch-to-batch uniformity are shown as well. For the first run, the etch rate was not measured (n/m).

Run #	**# Adders (particle size > 25μm)**			
	Slot	Slot	Slot	Average
	1	12	25	
1	38	7	21	22
2	5	5	32	14
3	11	2	6	6
Mean				**14**

Table 2. The number of particle adders with a particle size ≥ 0.25μm on 200 mm (slots 1, 12 and 25). The SiO_2 deposition (1036nm for 35 sec.) was followed by a subsequent $Ar/N_2/F_2$ oxide etch (> 1500nm for 60 sec.) for three wafer runs (total 75 wafers).

susceptor area. The complete oxide layer on the Si-pieces was removed throughout the three repeatability runs. This verifies that the $Ar/N_2/F_2$ gas mixture cleaned all important CVD chamber areas very well.

A further article on these experiments will appear in the next issue of FEO.

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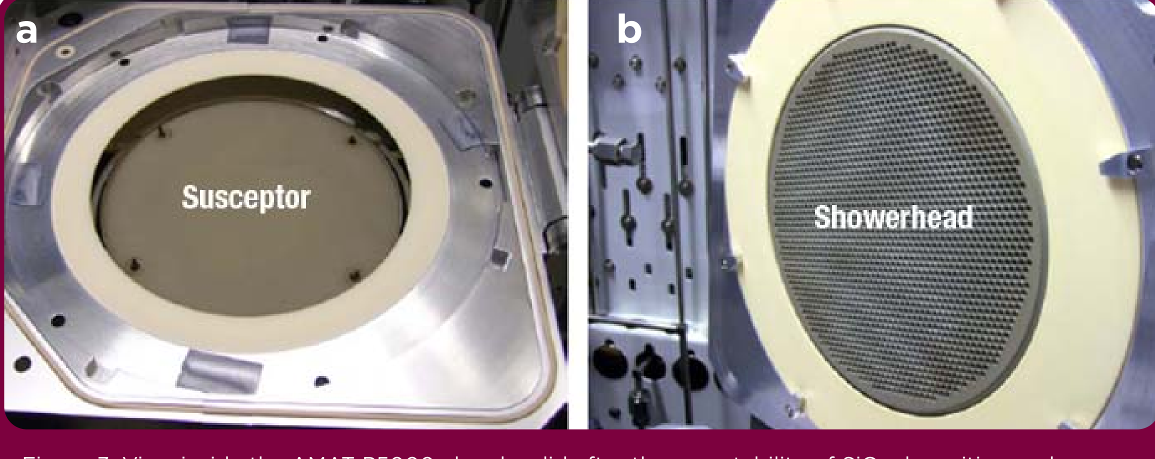

Figure 3. View inside the AMAT P5000 chamber lid after the repeatability of SiO_2 deposition and $Ar/N_2/F_2$ gas cleaning runs (total 75 wafers) with the susceptor and cream-colored large and small O-rings (a) as well as the showerhead (b).

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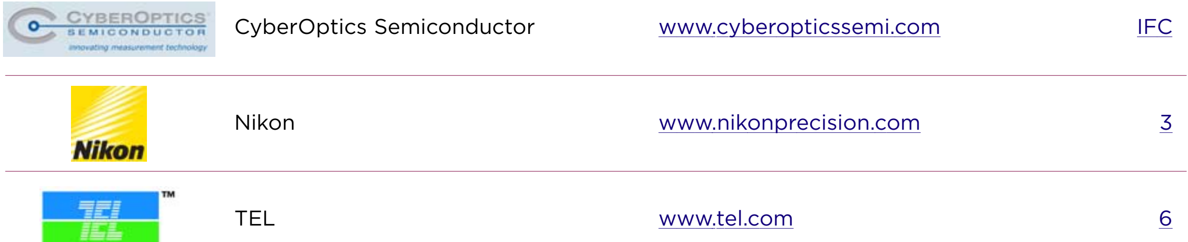

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