# Future Fab

## INTERNATIONAL

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**WELCOME** to the first-ever April edition of Future Fab International. As part of our quest to improve and develop the magazine, we needed to not only modernize and expand, with our switch to the digital platform and the expanded coverage of Design-Manufacture-Package, but also to increase our frequency, as readership surveys showed people wanted more regular updates. It's certainly been an interesting process, with the shorter deadlines, but we're happy to have made the change. As we move further into 2008 with a recession looming over all our heads, timely information in a regular format becomes more important then ever, so we're pleased to give you this – the first FFI April edition.

In this issue we are pleased to welcome and introduce you to the following new FFI panel members:

***Stephen Buffat*** – Nantero – Manager, Jordan Valley Innovation Center

***Janice Golda*** – Intel Corp – Director, Lithography Capital Equipment Development

***Lode Lauwers*** – IMEC – Director, Strategic Program Partnerships

***Davide Lodi*** – Numonyx – Manager, Wet Processes & Metrology Engineering

***Kazu Yamada*** – NEC Electronics America – VP, Custom SoC Solutions Strategic Business Unit

***John Warlaumont*** - SEMATECH North – Site Executive

Your comments and suggestions are always welcome and very much appreciated!

**Enjoy!**

**The Future Fab team**

## FUTURE VISIONS & CURRENT CONCERNS



## NEW TECHNOLOGIES & DEVICE STRUCTURES



## DESIGN IMPLEMENTATION & PROCESS INTEGRATION



## MANUFACTURING, SYSTEMS & SOFTWARE



## FRONT END OF LINE

## BACK END OF LINE



## METROLOGY, INSPECTION & FAILURE ANALYSIS



## WAFER FAB & PACKAGING INTEGRATION



## ASSEMBLY, TEST & PACKAGING TECHNOLOGIES





Biographies of Future Fab's Panel Members

For the full version of the following biographies please click here.

## Paolo A. Gargini

### Director of Technology Strategy for Intel Corporation

Dr. Paolo Gargini is the director of Technology Strategy for Intel Corporation in Santa Clara, Calif. He is also responsible for worldwide research activities conducted outside Intel for the Technology and Manufacturing Group by consortia, institutes and universities. Dr. Gargini received doctorates in electrical engineering and physics from the Universita di Bologna, Italy.

## Alain Charles Diebold

### Empire Innovation Professor of Nanoscale Science; AVS Fellow; Senior Member of IEEE

Alain's research focuses on the impact of nanoscale dimensions on the physical properties of materials. He also works in the area of nanoelectronics metrology. Alain is a member of the International Metrology Technical Working Group, founder and co-chair of the U.S. Metrology Technical Working Group for the 2007 International Technology Roadmap for Semiconductors, and chair of the Manufacturing Science and Technology Group of the American Vacuum Society.

## Daniel J. C. Herr

### Director of Nanomanufacturing Science Research, Semiconductor Research Corporation; SPIE Fellow

Dr. Herr leads a team that provides vision, guidance and leveraged support for collaborative university research in emerging nanoelectronics-related materials and assembly methods, environmentally benign high-performance manufacturing and future factory technologies. He is an adjunct associate professor in materials science and engineering at North Carolina State University, where he also serves as a graduate thesis advisor.

## Janice M. Golda

### Director, Lithography Capital Equipment Development; Intel

Janice Golda manages an organization responsible for creating strategies and working with Intel's lithography, mask and metrology suppliers and subsuppliers to deliver equipment meeting Intel's roadmap technology, capacity and cost requirements. She is a member of the Berkeley CXRO Advisory committee, is Chairman of the Board for the EUV LLC and holds one U.S. patent. She earned her B.S. in electrical engineering from Cornell University.

## Steve Greathouse

### Global Microelectronics Technology Manager; Plexus Corporation, Nampa, Idaho

Steve Greathouse is the Global Microelectronics Process Technology manager at Plexus Corporation, in Nampa, Idaho, responsible for the development and deployment of microelectronic devices worldwide for Plexus. He has published many articles on technical topics related to semiconductor packaging, failure analysis and lead-free packaging. Steve has a B.S. in electronic physics from Weber State University with advanced studies in material science and computer science.

## Christian Boit

### Head of Semiconductor Devices at Berlin University of Technology, Germany

The Berlin University of Technology is an institution for research and development in the areas of device simulation, technology, characterization and reliability. Christian Boit received a diploma in physics and a Ph.D. in electrical engineering on power devices, then joined Siemens AG's Research Laboratories for Semiconductor Electronics in Munich and has been a pioneer on photoemission.

## Alan Weber

### President, Alan Weber & Associates

Alan's consulting company specializes in semiconductor advanced process control, e-diagnostics and other related manufacturing systems technologies. He was previously the VP/GM of the KLA-Tencor Control Solutions division, acquired from ObjectSpace in March 2000. Prior to that, he spent eight years at SEMATECH and 16 years at TI. He has a bachelor's and a master's degree in electrical engineering from Rice University.

## Peter Rabkin

### Director of Device and Process Technology, Sandisk Corp.

Dr. Peter Rabkin is director of Device and Process Technology at Sandisk Corp., focusing on development of novel 3D memory technologies and products. Previously, he served as program director for Advanced Technology Development at Xilinx, Inc., responsible for process-to-design integration and DFM. Dr. Rabkin holds a master's degree in physics from Tartu University and a Ph.D. in physics of semiconductors from the St. Petersburg Institute of Physics and Technology.

## Kazuyoshi "Kazu" Yamada

### VP & General Manager, Custom SoC Solutions Strategic Business Unit, NEC Electronics America, Inc.

Kazu Yamada oversees the company's custom ASIC-related business as well as engineering and system memory and power management business. In his 25-plus years with NEC companies, he has held several key positions in marketing and engineering. Mr. Yamada holds bachelor's and master's degrees in electrical engineering from the Musashi Institute of Technology in Tokyo and holds 20 patents in Japan for bipolar-related designs.

### Giuseppe Fazio

**Advanced Process and Equipment Control Sr. Engineer, Numonyx**

With a laurea degree in applied physics from Milan University, Giuseppe has working experience in several sectors, from research to industry, and vast experience in industrial and scientific instrumentation, as well as in the sector of components for industrial automation. After many years with ST Microelectronics, he is now in the R&D division of Numonyx. Giuseppe has authored and co-authored numerous articles, is an avid contributor at conferences and holds several patents in the semiconductor field.

### Klaus-Dieter Rinnen

**Director/Chief Analyst, Dataquest**

Klaus-Dieter Rinnen is director for Dataquest's semiconductor and electronics manufacturing group, which covers trends and competitive positioning in semiconductor capital equipment, materials, contract manufacturing (foundry and SATS), and electronics manufacturing services. He received a diploma degree in physics with minors in physical chemistry and mechanical engineering in Germany, and a Ph.D. in applied physics from Stanford University.

### Gilbert J. Declerck

**President and CEO, IMEC**

Gilbert Declerck is president and CEO of IMEC, Europe's largest independent research center in the field of microelectronics, nanotechnology, enabling design methods and technologies for ICT systems. He has authored and co-authored over 200 papers and conference contributions. Declerck received his Ph.D. in electrical engineering at the University of Leuven in 1972 and became a professor there in 1983.

### John Schmitz

**Vice President, NXP Semiconductors Research**

Prior to working with NXP, John Schmitz served as VP and COO for manufacturing technology of SEMATECH from April 2002 to December 2005. There he launched the Advanced Technology Development Facility (ADTF) for-profit subsidiary as well as the International SEMATECH Manufacturing Initiative (ISMI) subsidiary. Schmitz holds a master's degree in chemistry from Radboud University of Nijmegen, Netherlands, and a doctorate in physical chemistry from Radboud University Nijmegen.

### Lode Lauwers

**Director, Strategic Program Partnerships for Silicon Process and Device Technology, IMEC**

Lode Lauwers has an M.S. in Electronics Engineering and a Ph.D. in Applied Sciences. He joined IMEC in 1985 as a researcher. In 1992, he became scientific advisor at IWT, and in 2000 general manager at Easics NV. He is currently Director Strategic Program Partnerships for Silicon Process and Device Technology at IMEC, managing IMEC's core partner research program on sub-32nm CMOS technologies.

## Ernst Richter

### Technology Transfer Manager, Inotera Memories/Qimonda

Inotera Memories is a joint venture between Qimonda (previously Infineon Technologies) and Nanya Technologies in Taiwan. Richter joined Inotera at its startup in 2003 as Infineon delegate for DRAM technology transfers. He holds a Ph.D. and an M.Sc. in chemistry from the University of Regensburg and an M.Sc. in materials science from the University of Kent at Canterbury.

## Ehrenfried Zschech

### Sr. Manager, Center for Complex Analysis; AMD Saxony LLC & Co KG

Zschech has held this position in Dresden since joining in 1997, responsible for the analytical support for process control and technology development, as well as physical failure analysis. He received his diploma degree in solid-state physics and his Dr. rer. Nat. degree from Dresden University of Technology. He is an honorary professor for nanomaterials at the Brandenburg University of Technology in Cottbus, Germany.

## Steven E. Schulz

### President and CEO, Silicon Integration Initiative, Inc.

Since 2002, Steve Schulz has served as president and CEO of Si2, the leading worldwide consortium of semiconductor and software companies chartered to develop EDA standards. Steve was previously employed by Texas Instruments for 19 years. He has a B.S. in electrical engineering from the University of Maryland at College Park, and an M.B.A. from the University of Texas at Dallas.

## Raj N. Master

### Senior AMD Fellow, Chief Technologist, Advanced Micro Devices

Master manages the advanced packaging group involved in developing strategic enabling technologies and is also manager of the lead-free program of AMD. He joined AMD after spending 21 years at IBM, where he was a senior technical staff member. Master has 36 U.S. patents issued to him and has published more than 70 technical papers.

## Stephen J. Buffat

### Manager, JVIC Center, Nantero, Inc.

Stephen J. Buffat is the operations manager of the Jordan Valley Innovation Center for Nantero, Inc, Springfield, Mo. He is also an adjunct faculty member at the Center of Applied Science and Engineering/JVIC Center at Missouri State University. Stephen has more than 33 years experience in the semiconductor industry, and has authored or co-authored numerous articles on various subjects of photolithography and 300 mm surface preparation process technologies.

## Davide A. Lodi

### Wet Processes & Metrology Engineering Manager, Numonyx

Davide Lodi graduated from Milan University in 1997, having studied solid state physics, with a thesis on shape memory alloys. Soon after, he joined STMicroelectronics, where he started as a process engineer; after becoming the manager of Wet Processes and Metrology Engineering at the NVM R&D site in Agrate, Italy, he moved to Numonyx, where he holds the same position. He has authored and co-authored several papers in both fields.

## John Caffall

### Director of Operations, Submicron Development Center (SDC); Spansion Inc

John Caffall is director of operations for the Submicron Development Center (SDC) at Spansion, the world's largest pure-play provider of Flash memory solutions. He is responsible for overseeing engineering, manufacturing and maintenance activities for the company's R&D center for advanced technologies for Flash memory. He holds an M.B.A. from San Jose State University and a B.S. in electronics engineering technology from the University of Houston.

## Jeff Wetzel

### Senior Member of the Technical Staff, SVTC, LLC

Dr. Jeffrey (Jeff) T. Wetzel was recently appointed to the role of senior member of the Technical Staff of SVTC, LLC/ATDF in Austin, Texas. His previous experience includes material characterization, tool, process and device integration at IBM, Motorola, SEMATECH, and Tokyo Electron in engineering and management roles in silicon microelectronics R&D since 1983.

## Peter Ramm

### Head of Dept. Si Technology and VSI, Fraunhofer IZM, Munich

Peter Ramm received the physics and Dr. rer. nat. degrees from the University of Regensburg. He worked for Siemens in the DRAM facility and joined Fraunhofer in 1988 focusing on 3D integration technologies. Dr. Ramm is head of the Silicon Technology and VSI department at Fraunhofer IZM, Munich. He has authored over 50 papers and 20 patents, and is editor of the *Handbook of 3D Integration* (Wiley-VCH).

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# FUTURE VISIONS AND CURRENT CONCERNS

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**Stephen J. Buffat**
Manager, JVIC Center, Nantero, Inc.

To maintain the growth and profitability of our industry, miniaturization through technological advances and increasing wafer size are necessary to continue to reduce fabrication costs.

For the last several years, the emergence of nanotechnology has provided the industry with various types of micro devices. The fundamental nature of nanotechnology is the ability to work at the molecular level, to create various size structures or devices. A natural offshoot of this technology is bionanotechnology, manufacturing extremely small structures which are made up of as little as one molecule. The interfaces between biological systems and molecules and/or materials are the essence of bionanotechnology. The technology accomplishes many goals that are impossible to achieve by other means. DNA, for example, may serve as a basis for the next-generation devices: bionano-circuits and bionano-structures.

In Part 1 of his article, Rob Meagley of ONE Nanotechnologies, LLC, reviews how new opportunities are emerging to harness chip-based technology for biochemical and medicine as well as other applications with increasing levels of integration. There are three subsystems discussed that relate to various biochip technologies: sample containment, fluidics and cantilevers. In Part 2 of his article, he will discuss electronic and photonic subsystems as well as current and potential applications.

The IC industry continues to struggle with some aspects of the transition to 300 mm wafers, and even 450 mm wafers are now being considered. A transition is necessary to keep up with Moore's law. Moving to 450 mm wafers sometime during the next decade will be a very challenging transition. The move will certainly increase chip manufacturing complexity.

In the second article in this section, Daren Dance and David Jimenez of Wright Williams & Kelly, Inc., review some of the challenges that 300 mm manufacturing has overcome and some of the anticipated challenges that 450 mm manufacturing will need to address.

We hope this issue is enjoyable and informative.

FUTURE VISIONS AND CURRENT CONCERNS

# The Emergence of Bionanotechnology, Part I

**Rob Meagley**
ONE Nanotechnologies, LLC

## Introduction

As the nanoelectronics industry has executed aggressively to the International Technology Roadmap for Semiconductors device dimensions have shrunk below those of cells, bacteria and viruses, and reached the size of larger biological molecules.[1,2] Concom-itant with this structural trend, biology and medicine have begun to integrate the technologies and techniques of micro- and nanofabrication into new instruments, devices and perhaps most intriguing, chip-based diagnostic techniques. Such developments as subminiature cameras, probes and implanted RFID use CMOS and MEMS chips systems for medical applications.[3] However, in biochips, novel systems and materials are emerging that directly interact with biochemistry, and as devices approach the size of biomolecules themselves, new opportunities are emerging to harness chip-based technology for biochemistry and medicine and other applications with dramatically increasing levels of integration.

## Containment

The field of biotechnology integrated with nanofabrication – "bionano technology" – had its origins in the miniaturization of biochemical testing. As analysis improved, testing volumes became dramatically smaller and test tubes gave way to microwell plates, now common for genetic analysis. Affymetrix began making a microlithographically printed chip containing genetic sequences for fluorescent detection in 1993 (the first prototype of what became the GeneChip was disclosed in 1989). The size of the nucleic acid-containing features advanced from the 100 micron to the 18 micron scale between 1994 and 2002 (Figure 1). Such microfabricated arrays serve as convenient platforms upon which to contain and perform massively parallel chemical testing, and have been extended to many types of biomolecules, including DNA, RNA, protein, oligosaccharide and many types of detection, including photonic, plasmonic, mass spectrometry and electronic detection.[4]

For higher levels of integration, additional subsystems have been developed to enable more complex, powered biochips. These include: fluidics; cantilevers; electronics (capacitive, inductive, transistor); photonics; and the list keeps growing. The remainder of this article will explore the development of fluidic and cantilever device technology.

## Fluidics

A key to the manipulation of molecules has traditionally been chemistry in solvent. Techniques pioneered by Merrifield enabled solution chemistry to operate on the surface of glass beads, and thus later glass microscope slides and subsequently, chips. However, moving the entire chip from solution to solution uses relatively large volumes of sample and reagents; therefore systems have been created to move the solvent (usually water) around on the chip surface. Thus, with control of the motion of solvent, complex chemical manipulations are enabled with dramatical-

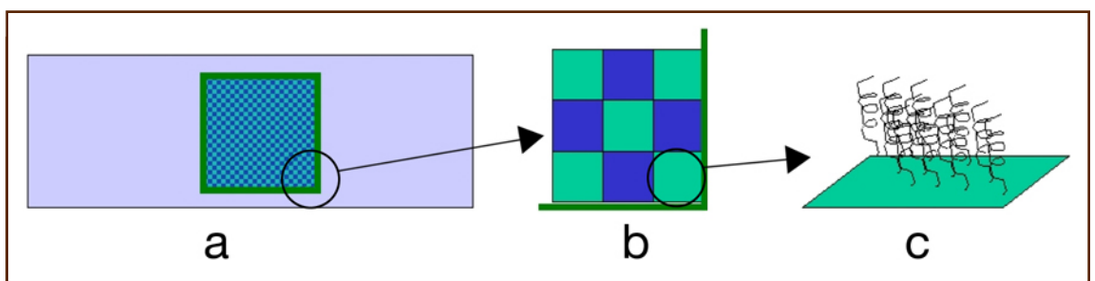


Figure 1. Nucleic Acid Array: glass slide (a) with gasket surrounding regions (b) functionalized with single-stranded RNA (c).[4]

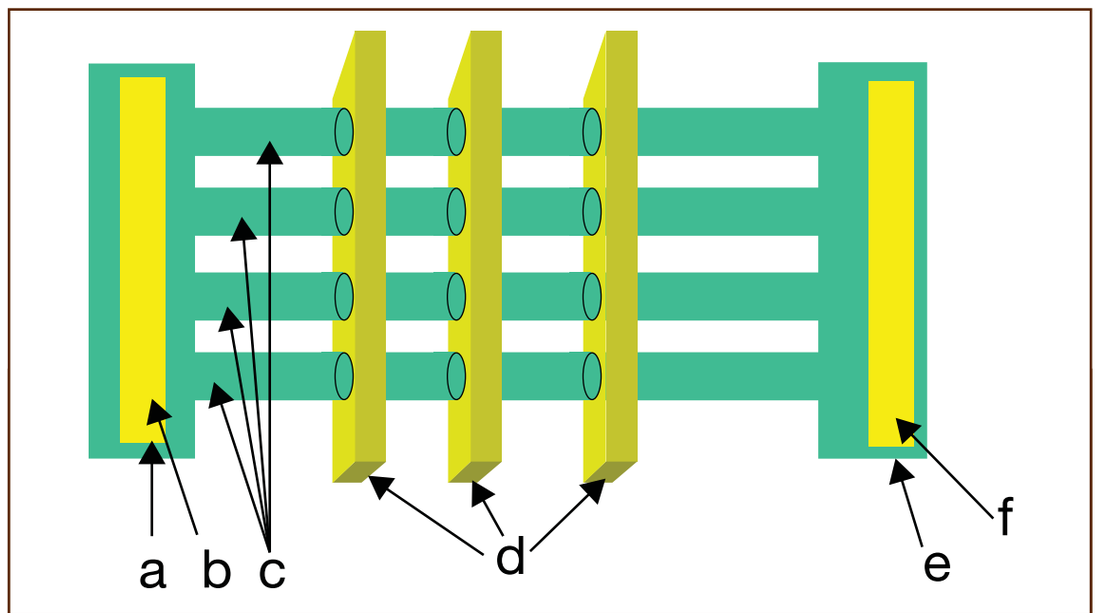


Figure 2. Electrokinetic valve "FET": microchannel supplying electrolyte (a, e) in contact with source/drain (b, f) and 35nm nanochannels (c) surrounded by gates (d).[6]

ly smaller volumes, and sample may be delivered precisely to specific sensors or other regions on the chip. Chips have been demonstrated with submicron channels in silicon as well as other materials including various polymers such as polydimethylsiloxane (PDMS), a material related to spin on glass.[5]

Fluid is moved within the chip due to pressure differential generated externally or internally. The electrokinetic (electro-osmotic) effect can be used to generate pressure differentials. Here, an imposed electric field acts upon ions in solution to create pressure and is frequently employed in micro- and nano-fluidic chips. Another application with this effect is flow regulation through a very small (i.e., 35nm, Figure 2) channel with an imposed field analogous to a FET.[6] MEMS-pumping designs as well as systems relying on flow control by pneumatics have also been described, and PDMS-based fabrication by soft lithography can facilitate the incorporation of valves. One example of the power of this technology is the success of massively parallel chips to grow protein crystals and chips to synthesize proteins and other biological molecules.[7]

## Cantilevers

A cantilever is a bar anchored at only one end that vibrates. The resonance properties of a nanoscale cantilever are profoundly sensitive to minute changes. This is a key biosensor approach. Individual cells, bacteria and viruses have been detected through their impact on cantilever resonance. Molecular events too are detectable with this approach; for example, single-stranded DNA attached to a cantilever will bind uniquely to its complementary strand in solution resulting in a change in frequency response (Figure 3). This method can also use antibody-antigen response as well as a host of other molecular recognition events.[8]

Arrays of cantilevers have been employed to investigate sets of species (cells, viruses, proteins, particles and small molecules) and have been developed for biomedical, military and security applications. Signal may be read optically from the vibrating cantilever; however, perturbations of a cantilever's electronic properties are information-rich data as well.[9]

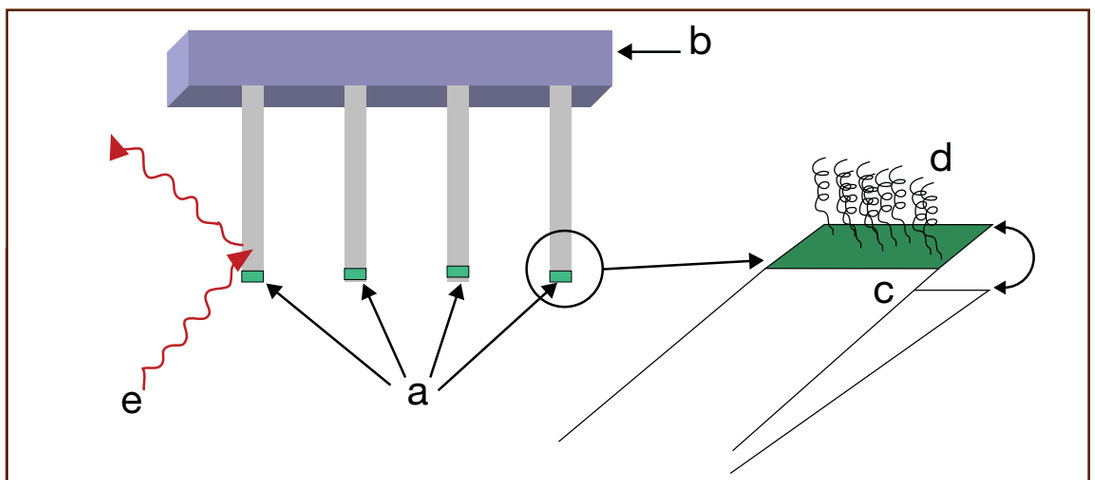


Figure 3. Cantilever: flexible beams (a) affixed to substrate (b) containing regions (c) functionalized with single-stranded RNA (d) and read with laser (e).[8] Note that many other geometries have been demonstrated. This "diving board" structure is for illustrative purposes.

## Conclusion for Part 1

With three subsystems – sample containment, fluidics and cantilevers – a vast number of biochip technologies can be derived. Applications of these three systems include cell, bacterial, virus, nucleic acid, protein and small molecule sensors. Genetic characterization and amplification as well as protein synthesis has been demonstrated with chips based on these three simple subsystems. Fabrication has been accomplished using photolithography; however, the techniques of soft lithography have been exploited in many cases to enable both biocompatible materials fabrication as well as cost-effective miniaturization. Moore's Law-like trends to decreasing sizes and increasing densities and levels of integration are clear. These trends point the way toward very high levels of integration including sample acquisition, processing and response, with applications not only in analysis, diagnostics and synthesis, but also therapeutics. Net-worked autonomous implanted devices are but one direction in which such work may lead.[10] In Part 2, electronic and photonic subsystems will be discussed as well as current and potential applications.

## References

1. http://www.intel.com/pressroom/archive/releases/20070918corp_a.htm?iid=tech_arch_32nm+body_pressrelease;
2. Proc Natl Acad Sci U S A. 2001 May 8; 98 (10): 5904–5909 http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=33311
3. http://www.masternewmedia.org/news/2007/01/06/medical_imaging_technologies_20_portable.htm; http://ieeexplore.ieee.org/Xplore/login.jsp?url=/iel5/11194/36055/01708315.pdf?temp=x; http://www.verichipcorp.com/news/1195161153
4. http://www.genomicsolutions.com/instruments/higro.aspx; http://www.affymetrix.com/corporate/history/index.affx; http://pubs.acs.org/cgi-bin/abstract.cgi/ancham/asap/abs/ac800226k.html; http://sciencelinks.jp/j-east/article/200614/000020061406A0434562.php; http://www.proteomesci.com/content/5/1/7/abstract/;http://www.sciencemag.org/products/ddbt_51404.dtl; http://www.nsti.org/Nanotech2008/showabstract.html?absno=284; http://www.lshtm.ac.uk/itd/grf/microarrayoverview.htm)
5. http://nobelprize.org/nobel_prizes/chemistry/laureates/1984/merrifield-lecture.pdf; http://www.trnmag.com/Stories/2002/100202/Integrated_biochips_debut_100202.html; http://ieeexplore.ieee.org/Xplore/login.jsp?url=/iel5/9801/30909/01434211.pdf?arnumber=1434211; http://thebigone.stanford.edu/foundry/about/publications/ICNMM-2007.pdf
6. http://www.sciencedirect.com/ science?_ob=ArticleURL&_udi=B6WHR45B63BW3C&_user=10&_rdoc=1&_fmt=&_orig=search&_sort=d&view=c&_acct=C000050221&_version=1&_urlVersion=0&_userid=10&md5=59c5f6089a3a0c9c2db1961a091a9d44; http://www.comsol.com/ showroom/gallery/259.php;http://cat.inist.fr/?aModele=afficheN&cpsidt=17907597; http://books.google.com/books?id=JRSYpC8OwsgC; http://link.aps.org/abstract/PRE/v74/e066311;

http://www.sciencedaily.com/releases/-2005/07/050703231541.htm; http://dx.doi.org/10.1021/nl050493b
7. http://www.springerlink.com/content/21784g3455646482/; http://www.ece.cmu.edu/~mems/pubs/show.php; http://www.mtbeurope.info/news/2007/705001.htm; http://thebigone.stanford.edu/foundry/technology/valve.html; http://www.jstage.jst.go.jp/article/analsci/24/2/24_243/_article; http://www.sciencedirect.com/science?_ob=ArticleURL&_udi=B6X1J4DHWP99Y&_user=10&_rdoc=1&_fmt=&_orig=search&_sort=d&view=c&_acct=C000050221&_version=1&_urlVersion=0&_userid=10&md5=52ccb1d2f92624e52c4292275c169147; http://www.aseanbiotechnology.info/scripts/count_article.asp?Article_code=21022564; http://www.nature.com/nature/journal/v442/n7101/full/nature05058.html; http://pubs.acs.org/subscribe/journals/ancham/78/i21/pdf/1106feature_mukhopadhyay.pdf; http://thebigone.stanford.edu/quake/publications/nature-biotechsep2003.pdf; http://www.sciencemag.org/cgi/content/abstract/288/5464/316
8. http://www.future-drugs.com/doi/abs/10.1586/14737159.4.6.859?cookieSet=1&journalCode=erm; http://jjap.ipap.jp/link?JJAP/45/2301/; http://www.rsc.org/publishing/journals/LC/article.asp?doi=b410905h; http://ieeexplore.ieee.org/Xplore/login.jsp?url=/iel5/7361/29088/01310333.pdf?arnumber=1310333; http://ttp.northwestern.edu/abstracts/viewabs.php?id=204&cat=87; http://news.uns.purdue.edu/html4ever/2004/040204.Bashir.virus.html ; http://www.veeco.com/pdfs.php/156/%3fshowPDF=true;
9. http%3a//www.phantomsnet.net/Docs/PosterLAASNaPaBarcelona.pdf; http://www.ornl.gov/sci/engineering_science_technology/sms/Hardy%20Fact%20Sheets/CMOS%20Centilever.pdf; http%3a//www.iop.org/EJ/article/1742-6596/34/1/059/jpconf6_34_059.pdf; http://www.mdpi.org/sensors/papers/s7091834.pdf; http://www.cfse.purdue.edu/includefile/rapidmethodworkshop/bashir.pdf
10. http://www.ncbi.nlm.nih.gov/pubmed/10941095; http://portal.acm.org/citation.cfm?id=1219476; http://www.ncbi.nlm.nih.gov/pubmed/17945924; http://www.medicaldevicestoday.com/2007/11/body-computing-.html

## About the Author

***Rob Meagley***

Rob Meagley is CEO and CTO of ONE Nanotechnologies, LLC, which develops and markets photonic nanodevices and device arrays for biomarker characterization and related technology. He received his Ph.D. from the University of Delaware in 1996. Rob holds 23 patents with many more pending, and has published and lectured extensively on materials science chemistry and nanotechnology. ■

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# Contemplating 450 mm

**Daren Dance and David Jimenez**
Wright Williams & Kelly, Inc.

## Abstract

The semiconductor industry's introduction of 300 mm wafers required addressing some significant manufacturing challenges. The industry is now contemplating 450 mm wafers. Respondents to a survey conducted by Wright Williams & Kelly, Inc. (WWK) in April of 2007 suggested that the challenges to 450 mm wafer introduction may be economically insurmountable. WWK followed up on the survey results by using economic models to compare profitability of 300 mm and 450 mm wafer fabs based on current manufacturing and economic trends. This article will look at some of the challenges that 300 mm manufacturing overcame and some of the anticipated challenges that 450 mm manufacturing must address.

## Survey

In April of 2007, WWK conducted a survey of semiconductor industry professionals. Table 1 shows the survey results of the following question: "Please indicate the year that you expect to see 450 mm wafers in production manufacturing."

The most common answer was 2013 or later. However, WWK was surprised to find that nearly 40 percent answered that 450 mm wafer would never happen. Subsequently, WWK has looked more closely at 450 mm wafers and the impacts on semiconductor manufacturing economics.

## 300 mm Challenges

The semiconductor industry has produced the International Technology Roadmap for Semiconductors (ITRS) and its predecessors since 1992. Not only are these roadmaps useful for anticipating technology needs, they are also useful as historical documents. From past roadmaps, we better understand critical semiconductor issues at any point in time.

In 1999, the industry was preparing for the anticipated arrival of high-volume 300 mm wafer processing in 2001. From the

| Expected Date | % of Respondents |
|---|---|
| 2012 or earlier | 5% |
| 2013 or later | 56% |
| Never | 39% |
| **Total** | **100%** |

Table 1. Year in which surveyed semiconductor industry professionals believe 450 mm wafers will be in production manufacturing.

| TWG | Difficult Challenge | Comments |
|---|---|---|
| Test | Full wafer test | |
| Test | Power and thermal management problems, especially with 300 mm wafers and increasing parallel test sites | |
| Process Integration | Cost-effective process integration of many functions on a single chip | |
| Front-End Processes | Etch CD control and selectivity | |
| Front-End Processes | CoO of large wafers (>300 mm): epi, SOI, Si:Ge | The 1999 ITRS anticipated 450 mm wafers in use in 2014 |
| Litho | Achieving constant/improved throughput with larger wafers | |
| Litho | Achieving ROI for industry (chip makers, equipment and material suppliers, and infrastructure) on large investments necessary for Roadmap acceleration | |
| Interconnect | Multidimensional control of interconnect features is necessary for circuit performance and reliability. Multiple levels, new materials, reduced feature size and pattern-dependent processes create this challenge. | |
| Factory Integration | Larger wafers and carriers driving ergonomic solutions – increasing expectations for material handling automation systems | Factory integration did not separate near and long-term challenges |
| Factory Integration | Reuse of building, production and support equipment, and factory systems<br>• Across multiple technology nodes<br>• Across a wafer size conversion | |
| ESH | *Reduce Energy Use of Process Equipment* – Need to design energy-efficient larger wafer size processing equipment. | Italics are from the 1999 ITRS |
| Defect Reduction | *Escalating Inspection Costs* – Equipment must effectively utilize real-time process and contamination control through integrated *in situ* process and product metrology | |

Table 2. ITRS Grand Challenges Facing 300 mm Wafer Fabrication: The View From 1999

1999 ITRS,[1] WWK has extracted some of the difficult challenges that were anticipated for the new wafer size. Not all technical working groups (TWGs) anticipated difficult challenges with 300 mm wafers. The Design, Assembly & Packaging, Metrology, and Modeling & Simulation TWGs expressed other challenges but none related to 300 mm wafer processing.

The items in Table 2 should sound familiar because many remain issues today. These challenges did not prevent the introduction of 300 mm processing. 300 mm was delayed by an even greater challenge – economics.

After a record-breaking year in 2000, the semiconductor industry collapsed in 2001–2002. Capital equipment purchases dropped to an industry record low percentage of revenue. Even though some cost of ownership studies showed that 300 mm was more cost-effective than 200 mm processing, most companies could not afford or risk capital investment in 300 mm.

In addition, economic trends made 200 mm processing more economical. Raw 200 mm silicon wafer costs dropped and wafer fab closures made pre-owned 200 mm equipment widely available if capacity expansion was needed. Faced with declining revenue, companies had to decide between the lower cost expansion of 200 mm capacity and the higher costs, but potentially more productive investment in 300 mm manufacturing. Most companies initially chose 200 mm.

As capacity needs and revenues grew to support continued investment, many 300 mm wafer fabs were built and more are being constructed today – but only as capacities and technologies require and revenues allow. In fact, 200 mm remains the wafer size of choice for many products.

## 450 mm Challenges

Today the semiconductor industry is in a similar position as in 2001. Companies are faced with declining revenues and tough choices for investing their R&D funds. However, there are also differences. Some of the challenges faced today are similar to the challenges faced by 300 mm investment. Following are some of the key challenges facing those who may invest in 450 mm manufacturing:

- **Full Wafer Testing** – Test costs continue to increase, and complexity increases mean that test times continue to grow. Testing all the devices on a wafer at the same time is one path to increased test productivity. Full wafer test is currently achievable for 200 mm wafers, within reach for 300 mm, but not currently achievable for the number of devices on a 450 mm wafer.
- **Lithography** – Achieving state-of-the-art resolution and high productivity for lithography remains challenging. The patterning technology of choice for the first 450 mm wafer technology node has not yet been determined. Moore's law may hang in the balance – does the industry invest in new technologies or 450 mm wafers?
- **Interconnect** – The need for multilevels, high-aspect ratio structures, and the continued introduction of new materials continue the interconnect challenge into 450 mm wafer processing.
- **Factory Integration** – Can 450 mm wafer fabs reuse the buildings, production and support equipment from 300 mm manufacturing? How does a company maximize return on investment from their current manufacturing infrastructure? Not many companies chose to reuse 200 mm wafer fabs for 300 mm expansion. Most built totally new facilities. It is too early to tell if 450 mm can reuse some of the extensive 300 mm infrastructure.

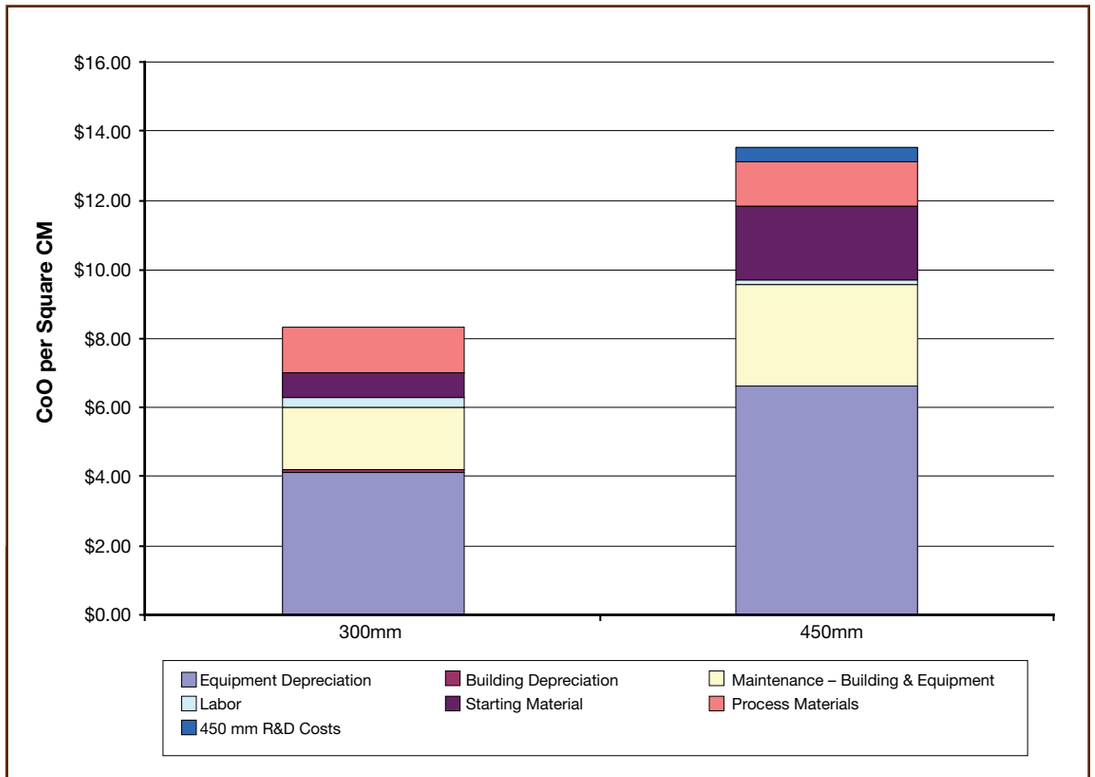


Figure 1. Comparison of Factory Commander® Financial Modeling Results of 300 mm and 450 mm Manufacturing Simulations

These are a few of the 300 mm challenges that continue into next generations of integrated circuit manufacturing. There are some new challenges as well. Following are some of the challenges from the 2007 ITRS:[2]

- **Scaling Planar CMOS** – Conventional scaling by reducing gate thickness, gate length, and increasing channel doping might no longer meet performance and power requirements.
- **Lithography Masks** – Mask cost has escalated each generation. Increased mask resolution and larger mask error enhancement factors make critical dimension uniformity and placement accuracy more difficult.
- **3D Integration** – The industry is implementing 3D integration technologies to fill the gap created by the physical limits of Moore's law scaling. Thermal management, thin die handling, signal integrity and test are near-term critical challenges.
- **Metrology** – Measurement of complex stacks, front-end processes and measurement uncertainty are examples of the many metrology challenges.

## Economic Projection

WWK used semiconductor manufacturing cost models to compare the relative costs of a 300 mm wafer and an expected 450 mm wafer for the same process. The selected process is typical of the processes anticipated by the ITRS for 2014–2015. In this comparison, we considered:

- Equipment cost differences
- Building costs, including automated materials handling
- Wafer, materials and consumables cost, including the R&D cost of qualifying the first 450 mm process.

For other wafer fab processing materials, WWK is assuming the same cost per $cm^2$ for 450 mm as for 300 mm. Material requirements should be the same – just the area differs.

Figure 1 compares the Factory Commander® financial modeling results of both 300 mm and 450 mm manufacturing simulations.[3] All results are expressed in terms of cost per $cm^2$ to normalize the difference in wafer size.

***Would you like to participate in WWK's 2008 semiconductor manufacturing survey? The survey is a list of semiconductor manufacturing technologies and equipment capabilities. Respondents are asked to indicate the expected year that each technology will enter production manufacturing. Each person completing a survey will receive a summary of the final results if desired. Individual surveys will remain anonymous. To participate, see the WWK website: http://www.wwk.com/2008survey.pdf.***

The lower costs of 450 mm wafer manufacturing for labor and process materials show some of the productivity improvement promise of 450 mm. Higher maintenance costs for 450 mm are driven by the higher equipment costs. The much higher costs for equipment and starting materials illustrate the challenges to be overcome before 450 mm becomes a viable option. Thus, even if the R&D costs associated with 450 mm were free, our economic models show that 450 mm could be as much as 36 percent more expensive than 300 mm manufacturing at the same advanced technology node.

WWK's analysis and economic comparison of two comparable fabs of about 30nm to 35nm processing technology suggests the following conclusions:

- Die size is no longer driving increases in wafer size;
- Continued expansion of 200 mm wafer capacity in a 300 mm technology environment show that smaller wafer sizes remain economically viable for some semiconductor products; and
- Just as 300 mm equipment had a price premium over 200 mm equipment, WWK expects 450 mm equipment will have a price premium over 300 mm equipment.

As a result of the WWK economic analysis, we expect that the largest challenge for 450 mm may be showing the productivity benefit that is expected with larger wafers sizes.

## References

1. "Difficult Challenges Tables," International Technology Roadmap for Semiconductors: 1999 Edition, Semiconductor Industry Association, San Jose, Calif., pp 11–20. Note: The

1999 edition was the first international roadmap.
2. "Grand Challenges," International Technology Roadmap for Semiconductors: 2007 Edition, Semiconductor Industry Association, San Jose, Calif., pp 11–18.
3. Additional details are found in "An Economic Comparison of 450mm and 300mm Wafer Fabs," Wright Williams & Kelly, Inc., 2008, http://www.wwk.com/pr450.html.

## About the Author

***Daren Dance***

Daren Dance is VP of technology at WWK. Previously, he was a senior member of the technical staff at SEMATECH and a staff engineer with American Microsystems. His career has focused heavily on yield modeling, manufacturing capacity simulation and cost modeling.

***David Jimenez***

David Jimenez is president of WWK. He was responsible for the design of the industry's standard in cost of ownership, TWO COOL®. For the past 17 years, he has been a facilitator in the SEMI-sponsored workshop, "Understanding and Using Cost of Ownership." ■

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**Paolo Gargini**
Director of Technology Strategy for Intel Corporation

In this issue of Future Fab International, you will find some exciting reports on innovative ways of producing nanophotonics and also new results on organic-based electronics.

Researchers from Ghent University-IMEC and CEA-LETI have fully demonstrated the potential of nanophotonics following two approaches. In the first case, they have developed a silicon-based process capable of producing state-of-the-art photonics wires, WDM lattice filters and WDM demux based on a diffraction grating. Silicon and silicon dioxide represent an excellent combination to guide light due to the difference in index of refraction between the two materials. By taking advantage of the high-resolution exposure tools developed for the production of today's integrated circuits, it is possible to produce nanophotonics integrated circuits with densities of up to six orders of magnitude larger than that of glass-based components. In the second case, they have developed heterogeneously integrated circuits comprehensive of SiGe and also III-V materials. Integration of active and also nonlinear materials enables the realization of complex all-optical signal processing integrated circuits capable of performing sophisticated functions such as wavelength conversion, switching and optical buffering. Stay tuned for the follow-up article on how to bridge between research and commercialization.

Researchers from the University of Texas at Dallas report on recent results obtained in their laboratory on organic semiconductor-based devices and circuits. It is well-known that from a processing point of view, it is of paramount importance to maintain the maximum processing temperature as low as possible to preserve the integrity of the organic film. In this work, the maximum temperature used in the fabrication remained below 120°C. Schottky diodes were fabricated by using copper phthalocyanine while OTFT were fabricated by using pentacene. The Schottky diodes demonstrated an impressive $I_{on}/I_{off}$ ratio of $6x10^3$ at 5V and sustained a forward current density of 29.3 A/cm$^2$ at 5V. An organic-based rectifier circuit demonstrated a DC output voltage of 2V at 14MHz.

Furthermore, OTFT transistors produced in this laboratory demonstrated a threshold variation of less than 200mV across a 4-inch wafer! This is the best result ever reported with this kind of transistors.

In summary, different combinations of these organic devices offer a cost-effective solution for several applications, such as RFID tags, flexible electronics and flexible displays.

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**Lode Lauwers**
Director, Strategic Program Partnerships for Silicon Process and Device Technology, IMEC

Research on new technologies concentrates on more than just finding new processes and materials for the sub-32nm nodes. The two papers in this section bear witness to an intense interest in alternative devices, using, for example, light; or in alternative materials, as used in, for example, organic electronics. The rationale behind this research is not only traditional scaling, but finding low-cost, manufacturable solutions for specific needs and applications.

In the first article, researchers from IMEC's associated INTEC lab (Ghent University, Belgium) and CEA-LETI review the progress in silicon nanophotonics. They describe how state-of-the-art process technology allows building silicon-based nanophotonic electronics that outperform photonic components made from other materials (e.g., glass, Ge). Moreover, silicon nanophotonics tremendously profits from the existing IC manufacturing infrastructure and research. First products are entering the market, targeting data communication (e.g., fiber to the home). The article also reports on research for using light and waveguide circuits for sensing, showing the concept of a label-free biosensor based on optical resonators. And what makes silicon particularly attractive as a material is the possibility to integrate it with devices in other materials, such as SiGe or III-V materials, needed for light detection at telecom wavelengths.

The second paper, from the University of Texas, reviews recent results on organic semiconductor devices and circuits, made with photolithography-based fabrication techniques. Organic devices promise large-area, cost-effective manufacturing, for applications such as RFID tags and flexible circuits for clothing. But they also present important challenges, such as low carrier mobility and sensitivity to environment conditions. The article reports on the fabrication of Schottky diodes using copper phthalocyanine (CuPc) and on pentacene-based organic thin-film transistors. The results for the diodes fabricated with conventional photolithography techniques demonstrate a rectifying functionality at frequencies useful for commercial applications, such as in radio frequency identification (RFID) tags.





# Silicon Nanophotonics

**Pieter Dumon,[1] Wim Bogaerts,[1] Alexei Tchelnokov,[2] J-M. Fedeli,[2] Roel Baets[1]**
[1]Ghent University – IMEC, [2]CEA-LETI

## Abstract

Silicon photonics builds on the momentum of silicon electronics to deliver to photonic integration what was lacking: a generic integration platform. Silicon-based nanophotonic ICs tremendously increase the integration scale, and the functionality per chip, compared with their counterparts in other material systems (glass, III-V semiconductor, etc.). This will drive adoption of photonic integration by a wide range of volume applications with increasing requirements in size, weight and power consumption.

## Photonic ICs in Silicon-on-Insulator

Today photonic integration suffers from an extreme diversity in materials, processes and integration approaches. Convergence on a generic platform with a select set of processes and industry-standard tools can overcome this bottleneck.[1] As silicon is an excellent material for passive optics in the infrared, the use of CMOS processes for photonic ICs is obviously attractive.

Industrial "off-the-shelf" CMOS processes can be used for a variety of photonic devices, as young companies such as Luxtera and Lightwire have been

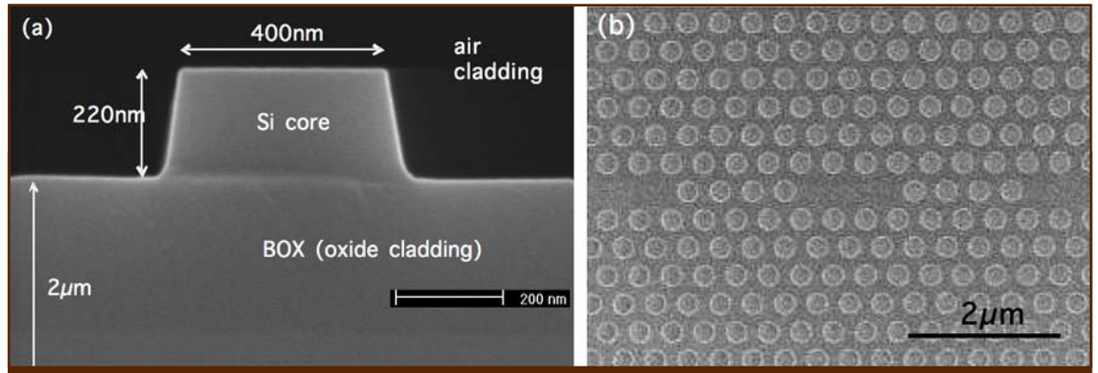


Figure 1. (a) high-index contrast strip waveguide in SOI
(b) photonic crystal (pitch 440nm) with cavity confining the optical mode in a 2 x 0.5μm² area.

demonstrating in the U.S. Their multi-channel transceivers for optical interconnect and datacom are made with CMOS foundry processes applied in a clever way. Meanwhile, IMEC and CEA-LETI have been developing processes to support a wider range of photonic circuits: To meet the stringent alignment requirements of photonic circuits, both the isolated and very dense structures in nanophotonic circuits have to be patterned simultaneously.[2]

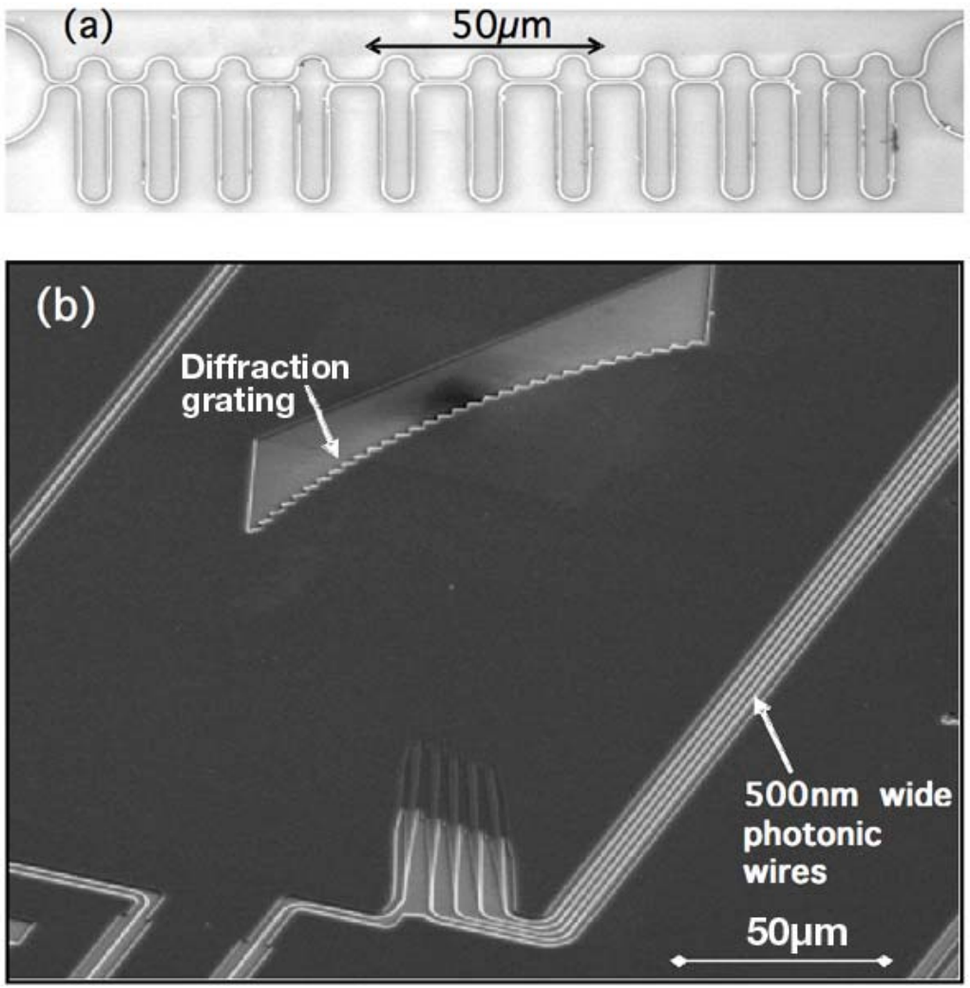


Figure 2. Compact wavelength-selective devices in SOI
(a) WDM channel selector based on a lattice filter with a 0.02 mm² footprint [3]
(b) WDM demux based on a diffraction grating [4]

## Strong Light Confinement

To create a dielectric waveguide for light, a core is defined in a high refractive index material surrounded by cladding with a lower index. With semiconductor for the core (n≈3.5) and an oxide or air (n≈1-1.5) as the cladding, light can be bound to a submicron strip waveguide, as shown in Figure 1. The optical mode is strongly confined in a cross section comparable to the light's wavelength in the material. Because of this, the optical path can be steered on a much smaller footprint compared with other material systems. Bends of just a few micron radius, compact splitters, wavelength-scale cavities with high-quality resonances (Figure 1) and strong nonlinear effects enable very compact circuits. The integration scale can be up to six orders larger than that of glass-based components. As an example, a WDM channel selector with a 0.01mm² footprint is shown in Figure 2, together with a wavelength demultiplexer smaller than 0.02mm².

## The Need for Extreme Accuracy

The typical critical dimensions (CD) of the silicon waveguides are in the 100–500nm range. However, nanometer-scale deviations can limit the device performance due to losses, reflections and crosstalk. The alignment tolerance between waveguide elements is of the order of a few nanometers at best, so most patterns within a single circuit layer need to be printed in the same lithographic step. To complicate matters, waveguide circuits consist of diverse features, from (semi-) isolated lines all the way to ultradense arrays of holes. The generic processes needed to support this wide range of features have been developed on CMOS tools at institutes like IMEC over the last decade. As the layer-to-layer alignment accuracy of scanners is improving towards the 5nm-level, double exposure techniques now start to reach the tolerance requirement of a number of photonic devices, opening opportunities to further optimize the fabrication processes.

One of the most striking requirements of silicon photonics is the extreme accuracy on the critical dimensions: While 100–500nm feature sizes are fairly large for today's high-end CMOS tools, an accuracy of 1 percent or better is needed. In fact, within a single wavelength-selective device, CD control of even 1nm or better is needed. While CD variations can be compensated for by thermo-optic or electro-optic tuning, an accurate base technology is needed to keep the power consumption low and the compensation algorithms simple. IMEC is now at a stage where wafer-level uniformity is controlled within less than 1 percent (1σ) for 450nm-wide waveguides, with even better uniformity within a single die. This accuracy requirement also poses significant metrology challenges. Still, sub-nm deviations which are impossible to measure with SEM can be assessed accurately through optical device characterization.

## Recycling Old Fabs and Processes?

The accuracy requirements show that silicon photonics cannot just "recycle an old fab," but need cutting-edge technology. Additionally, the smaller the allowed minimum CD, the wider the range of possible devices and applications. Still, technology from the 0.18μm or 0.13μm CMOS nodes already deliver many possibilities for silicon photonic circuit designers, with standard 193nm DUV lithography being the key necessity. While existing tools and fabs

can be used, novel processes are needed to support the diversity of features, and to ensure a sufficient scalability both in technology and in applications.

## Applications

First products are entering the market now with waveguide mode sizes smaller than 1μm². For the data communication market, Luxtera has developed multichannel transceivers, in the process setting up a complete tool chain from CMOS-compatible design libraries all the way to packaging and testing. They integrate photonic circuits with electronics for control, tuning and drivers, and run the processing through a fab from Freescale. Elsewhere, basic and applied research is targeting communication applications such as fiber-to-the-home, short-range interconnects/datacom and all-optical signal processing. Within two years, other companies can be expected to develop prototypes and enter the market with products based on even smaller mode sizes, with corresponding larger-scale integration. Key in driving these developments is the integration of silicon photonic ICs with SiGe for detection and modulation, and with III-Vs for light generation and signal processing.

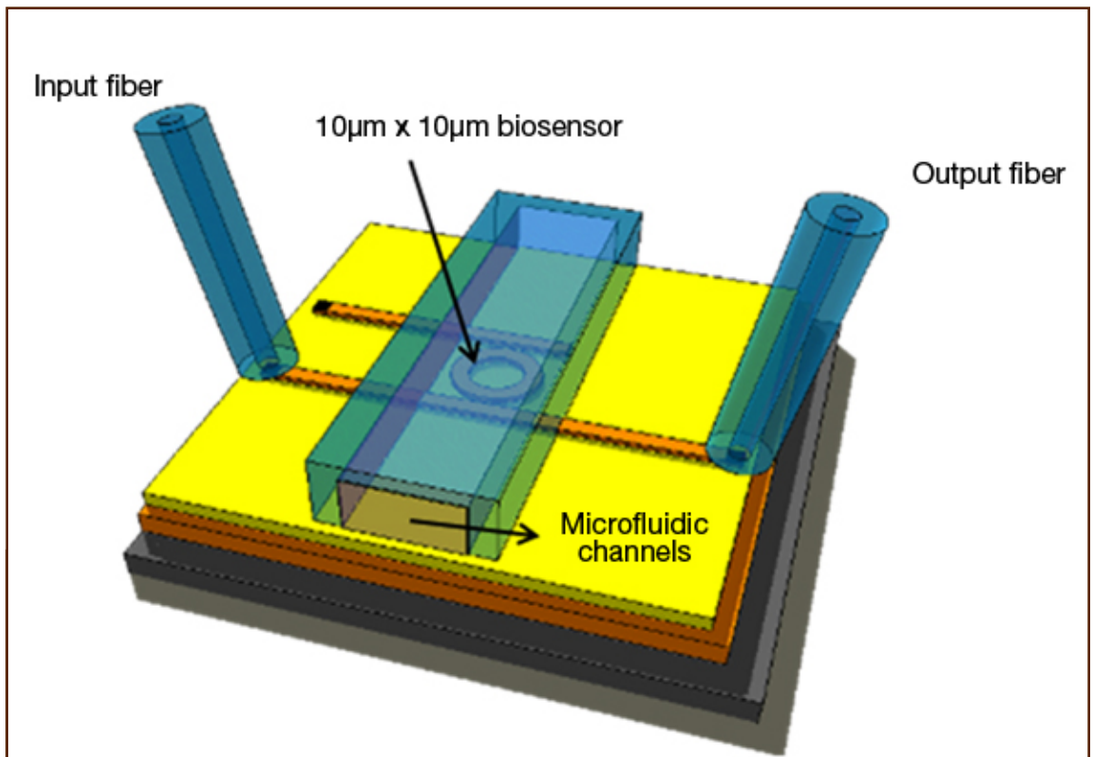


Figure 3. Label-free biosensor concept based on optical resonators. Thousands of functionalized biosensors can be integrated on a single chip.

Light can also be used as a sensing instrument, either directly or indirectly, and waveguide circuits for this purpose are the focus of many research teams. For instance, a highly integrated silicon photonic IC could serve as a multiparameter sensor for infrastructure monitoring, even equipped with on-chip logic for data processing. Ultracompact label-free biosensor chips, as illustrated in Figure 3, can easily contain hundreds of sensors for different substances or sensitivity ranges. Throw in on-chip communication capabilities and data processing logic and you have a very powerful mix.

## Active-Passive Integration

As in electronics, silicon is not the holy grail of materials, but it offers an immensely attractive integration platform. For light

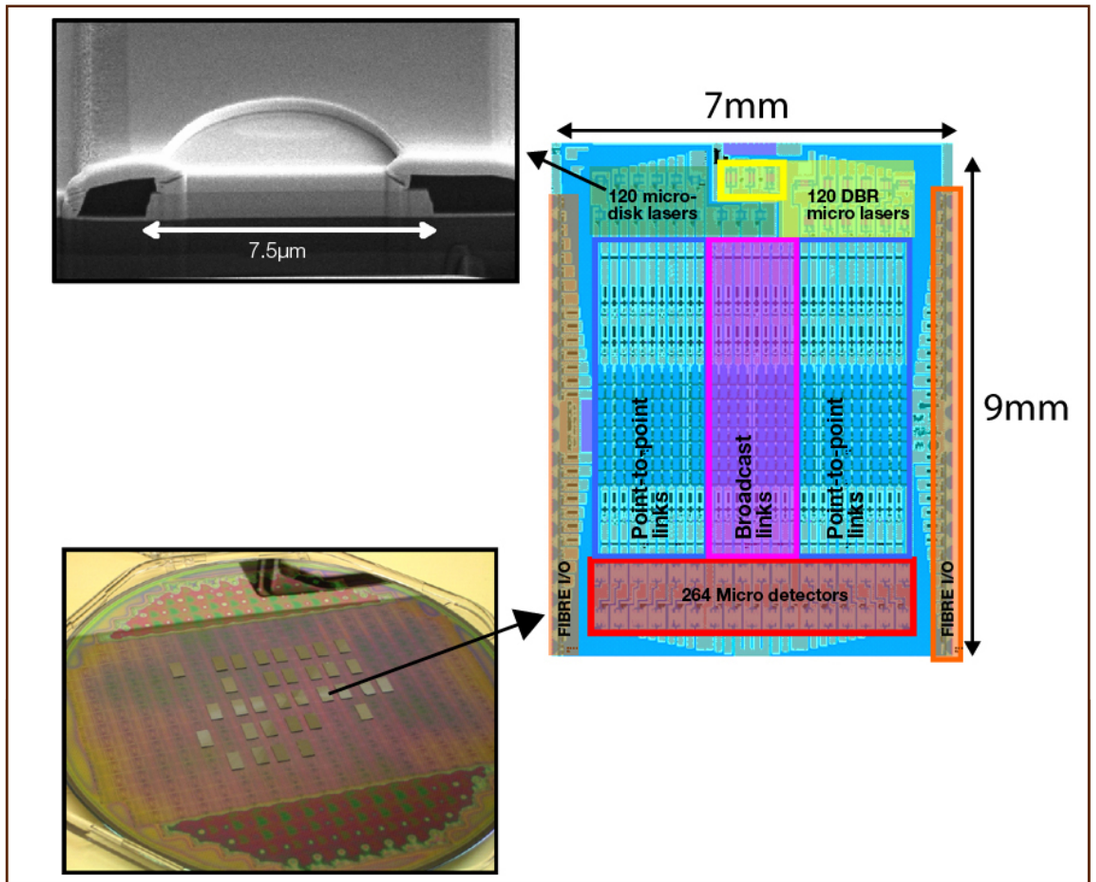


Figure 4. On-chip optical interconnects with Si photonic circuits form the EC-funded FP6 PICMOS project [5] III-V microsources and microdetectors. Sources and detectors are integrated by die-to-wafer bonding. The demonstrator contains point-to-point as well as broadcast links. Microdisk lasers, DBR microlasers and microdetectors are processed in the thin-film III-V after bonding and III-V substrate removal.

detection at telecom wavelengths, SiGe or III-V materials need to be integrated,[6,7] either monolithically or heterogeneously. Similar integration efforts are needed for light amplification and generation. Die-to-wafer bonding approaches for heterogeneous integration of III-V sources and detectors with silicon circuits have been extensively studied over the last years, and significant research efforts are directed towards wafer-scale processing of III-V bonded material in CMOS lines. Pioneering work of IMEC and CEA-LETI has already shown that these can be viable technologies.[5,6]

Hundreds of multi-Gbit/s transceivers can be integrated on a single chip, e.g., for use in access networks and high-performance computing. Integration with active and nonlinear materials enables complex all-optical signal processing, such as wavelength conversion, switching and optical buffering. A possible route towards this is the sandwiched waveguide technology developed by CEA-LETI. Dramatically improved high-speed interconnect solutions will be needed in the next decade for box-to-box down to on-chip data communication, to address the ever-growing memory and processor bandwidth requirements. Both Intel and IBM have projects on multicore processors with terabit/s on-chip bandwidth requirements, which can be powered by silicon photonics. An example of such on-chip optical interconnects from the PICMOS project [5] is shown in Figure 4.

## Integration With CMOS

As silicon photonics is working on the same platform as CMOS, why not integrate with CMOS? Transmitters and detectors can then be directly integrated with their driver circuits and logic. Or labs-on-a-chip can have the optical sensors, ADC, logic and external connectivity all on board. Of course, the most direct application of integration with CMOS is for optical interconnects as previously described.

However, it is currently unclear which of the many integration approaches is best for each application. The impact of manufacturability, yield, thermal properties and raw device performance is either unknown today or depends very much on the application. The possible approaches can mainly be classified in front-end, back-end and 3D integration (separate electronic and photonic ICs). In the industrial examples, Luxtera integrates photonics and electronics on the same chip in the front end, while Lightwire keeps them on separate chips, though both make clever use of CMOS technology. In contrast, both IMEC and CEA-LETI have developed low-loss amorphous silicon films deposited with (low-temperature) PECVD, compatible with back-end integration.[8,9] Interesting times are ahead.

## Part II: From Research to the Market

The first start-ups in silicon are delivering their first products. However, a tremendous amount of research is bringing in new applications and better-performing devices. In the next issue, we will discuss how the gap between the research and the market can be bridged, as well as how the ePIXnet silicon photonics platform organizes affordable prototyping for this purpose.

## References


1. ePIXnet Vision Document on Photonics Foundry Model, http://www.epixnet.org/index.php?id=392.
2. W. Bogaerts, R. Baets, P. Dumon, V. Wiaux, S. Beckx, D. Taillaert, B. Luyssaert, J. Van Campenhout, P. Bienstman, D. Van Thourhout, "Nanophotonic Waveguides in Silicon-on-Insulator Fabricated with CMOS Technology," Journal of Lightwave Technology (invited), 23(1), pp 401-412 (2005).
3. W. Bogaerts, P. Dumon, D. Van Thourhout, D. Taillaert, P. Jaenen, J. Wouters, S. Beckx, R. Baets, "Compact Wavelength-Selective Functions in Silicon-on-Insulator Photonic Wires," J. Selected Topics in Quantum Electronics, 12(6), pp 1394-1401 (2006).
4. J. Brouckaert, W. Bogaerts, S. Selvaraja, P. Dumon, R. Baets, D. Van Thourhout, "Planar Concave Grating Demultiplexer with High Reflective Bragg Reflector Facets," Photonics Technology Letters, 20(4), pp 309-311 (2008).
5. D. Van Thourhout, J. Van Campenhout, P. Rojo-Romeo, P. Regreny, C. Seassal, P. Binetti, X.J.M. Leijtens, R. Nötzel, M.K. Smit, L. Di Cioccio, C. Lagahe, J.-M. Fedeli, R. Baets, "A Photonic Interconnect Layer on CMOS," ECOC (2007).
6. M. Rouviere, L. Vivien, X. Le Roux, J. Mangeney, P. Crozat, C. Hoarau, E. Cassan, D. Pascal, S. Laval, JM Fedeli, JF Damlencourt, JM Hartmann, S. Kolev, "Ultrahigh speed germanium-on-silicon-on-insulator photodetectors for 1.31 and 1.55 Qm operation," Applied Physics Letters, 87(23) (2005).
7. J. Brouckaert, G. Roelkens, D. Van Thourhout, R. Baets, "Thin-Film III–V Photodetectors Integrated on Silicon-on-Insulator Photonic ICs," Journal of Lightwave Technology, 25(4), pp 1053–1060 (2007).
8. S. Jeannot, V. Jousseaume, JM Fedeli, S. Martin, R. Orobtchouk, P. Mur, P. Maury, T. Benyattou, A. Kazmierzack, "Different technological platforms for optical functions above integrated circuits," ECIO April 2005, Grenoble.
9. S. Selvaraja, D. Van Thourhout, R. Baets, E. Sleeckx, M. Schaekers, "Deposited silicon-on-insulator material technology for photonic integrated circuitry," 12th IEEE/LEOS Benelux Annual Symposium 2007, Belgium, pp 15–18 (2007).


## About the Authors


***Pieter Dumon***

Pieter Dumon obtained his Master in Electrical Engineering degree from Ghent University in 2002. He obtained his Doctorate in Electrical Engineering degree in 2007, also from Ghent University. Pieter now coordinates the ePIXnet silicon photonics platform at IMEC, Dept. of Information Technology, in the Photonics Research Group, which gives access to the CMOS facilities at IMEC (B) and CEA-LETI (F) for wafer-scale research and prototyping of silicon photonic components. He is a member of the IEEE and the OSA.

***Wim Bogaerts***

Wim Bogaerts started in silicon photonics at Ghent University-IMEC in 1999. He developed CMOS-compatible processes for nanophotonic circuits, with a Ph.D. in 2004. He is currently a postdoctoral fellow of the Flemish Research Foundation, and member of IEEE-LEOS and OSA.

***Alexei Tchelnokov***

Alexei Tchelnokov heads the Optoelectronic Devices Laboratory at CEA-LETI. He worked successively at A.F. Ioffe Physico-Technical Institute (Russia), In-t d'Electronique Fondamentale CNRS (France), Corning SA (France) and CEA-

LETI. Has vast experience in III-V opto-electronics, photonic crystals, nano-optics and silicon photonics.

***Jean-Marc Fedeli***

Jean-Marc Fedeli acts at CEA-LETI since 2002 as coordinator of silicon photonic projects with a focus on 200 mm fabrication technology. He has been working on different European projects (PICMOS, PHOLOGIC, MNTE, ePIXnet) for the development of photonic layer on top of an electronic integrated circuit.

***Roel Baets***

Roel Baets received the degree in electrical engineering from Ghent University, Belgium (1980), M.Sc. in electrical engineering from Stanford University (1981) and his Ph.D. degree from Ghent University in 1984. He leads the Photonics Research Group at Ghent University-INTEC (associated lab of IMEC), which focuses on new concepts for photonic components and circuits. Currently he coordinates the European Network of Excellence ePIXnet. Roel is a Fellow of the IEEE and from 2003 to 2005 was an elected member of the Board of Governors of IEEE-LEOS. ■

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# Organic-Based Electronic Devices and Circuits

**H. N. Alshareef, M. Quevedo-Lopez, S. Gowrisanker, Y. Ai, B. Gnade**
University of Texas at Dallas

## Abstract

In this article, we review recent results obtained in our laboratory on organic semiconductor-based devices and circuits. Manufacturable photolithography-based fabrication techniques were implemented to fabricate capacitors, Schottky diodes, organic thin film transistors (OTFTs), and several analog and logic circuits. All processes were performed below 120°C, which makes these integrated devices suitable for low-temperature flexible circuit applications. Specifically, our devices have been integrated to fabricate rectifiers, amplifiers, ring oscillators, current mirrors, matched pairs, and other circuits. Good performance is obtained for the single-stage rectifiers, and acceptable performance is obtained for integrated amplifiers, matching pairs and ring oscillators. The OTFTs are all based on pentacene as organic semiconductor, while the Schottky diodes are based on copper phthalocyanine (CuPc).

## Introduction

Organic-based electronic devices and circuits are being actively investigated for a variety of applications. These applications include RFID tags, flexible displays and flexible circuits. The interest in organic semiconductors stems from the fact that they have the potential for large-area, cost-effective manufacturing, as well as the potential to fine-tune their properties and performance using structural modification at the molecular level.[1] However, there are still several limitations that must be addressed for such materials to enter the mainstream. For example, carrier mobility in organics is very low when compared with inorganic semiconductor materials, which restricts their use to applications requiring low mobility. Furthermore, the moisture sensitivity of some organic materials poses a significant challenge to their long-term reliability. For this reason, proper encapsulation methods are needed, particularly in the case of organic light-emitting diodes. The interest in organic electronics actually dates back to the late 1960s, when the electronic properties of phthalocyanine and chloranil were investigated.[2] The first thin-film transistor based on an organic semiconductor was reported in 1986 by Tsumura et al. [3] Since then, there has a been a tremendous growth in the number of materials and publications dealing with devices based on organic thin films. A number of recent reviews have been published on the topic.[4,5] In this article, we present

a brief review of our research activities in the area of organic electronics, and highlight the advantages and challenges of using such devices.

The Schottky diodes were fabricated using photolithographic processes to make it possible to integrate them with organic thin-film transistors and other components on flexible substrates.[6] The organic semiconductors pentacene and copper phthalocyanine (CuPc) were both used to fabricate Schottky diode devices. However, this article reviews mainly the CuPc results since it gave a better performance. Figure 1 shows the molecular structure of CuPc and a schematic of the cross section of our CuPc Schottky diodes. Aluminum thin films (the Schottky contacts) were typically used as the bottom electrodes, as this resulted in better CuPc diode characteristics. Gold thin films (the Ohmic contacts) were used as the top electrode. The room temperature I-V characteristics are also shown in Figure 1 of the Au/CuPc/Al diode. The diode exhibited a current density of approximately 29.3 A/cm$^2$ at a forward bias voltage of 5V, and an $I_{on}/I_{off}$ ratio of approximately 6x10$^3$ at 5 V. Under forward bias conditions, the *I-V* curves, plotted on a log-log scale (not shown here), showed four regions: (1) Ohmic region supported by thermal carrier generation; (2) shallow trap space-charge-limited current region; (3) trap-filled limited region; and (4) trap-free space charge. The rectification performance and circuit of these diodes is shown in Figure 2(a) and 2(b), respectively. The organic-based rectifier circuit generated a dc output voltage of approximately 2 V at 14 MHz from an input ac signal with a zero-to-peak voltage amplitude of 5 V. This demonstrates the rectifying functionality of the organic diodes fabricated using conventional photolithographic methods at frequencies that are useful for commercial applications, such as radio frequency identification tags.

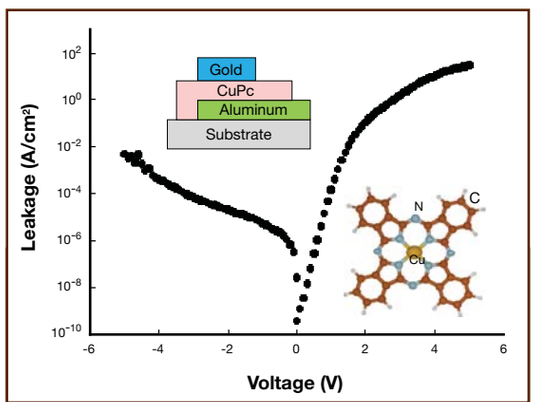


Figure 1. Forward and reverse bias I-V characteristics of a CuPc-based Schottky diode. The insets show the molecular structure of copper phthalocyanine (CuPc) and a schematic of the cross section of the CuPc-based Schottky diodes.

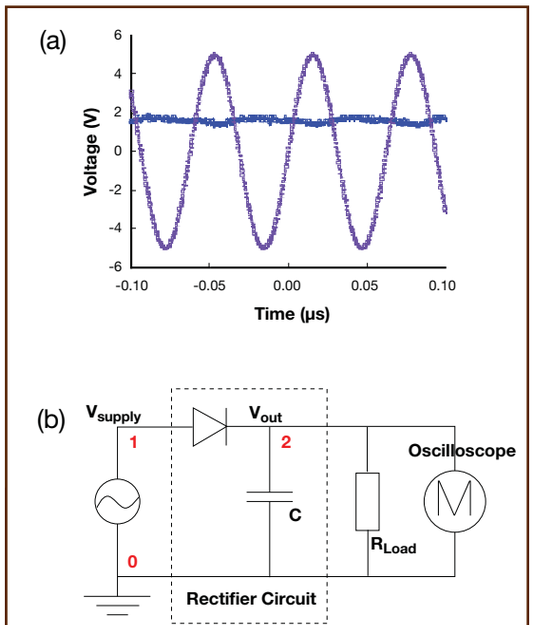


Figure 2. (a) Rectification behavior of a single-stage CuPc-based rectifier (5 V ac input, 2 V dc output), and (b) schematic showing the single-stage rectifier circuit.

Pentacene-based organic thin-film transistors (OTFTs) were fabricated using a gate-last approach that has been described elsewhere.[7] Several unit processes had to be developed and optimized to obtain good OTFT devices. For example, in pentacene-based transistors, the device performance is strongly dependent on the pentacene/dielectric interface and pentacene film morphology. Both of these properties can be affected by pentacene deposition conditions and surface quality of the gate dielectric.[8] Figure 3 shows the pentacene molecular structure and the cross section of our typical OTFT. The transistor layout is also shown in Figure 3(c) with the source (S), drain (D) and gate clearly labeled. This bottom-gate configuration was found to give good within-wafer uniformity and to give flexibility for integration with other devices. Figure 4(a) shows the $I_D$-$V_D$ characteristics of pentacene transistors fabricated using the gate-last flow. The figure shows the curve-family where drain-source

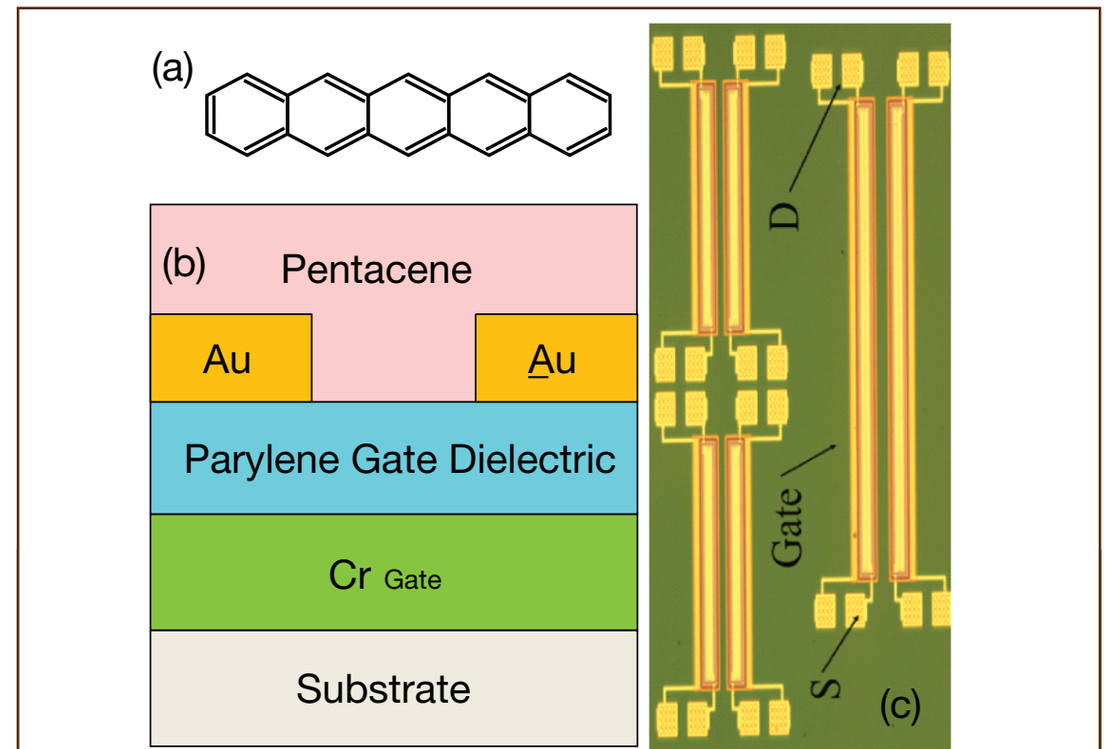


Figure 3. (a) Molecular structure of the organic semiconductor pentacene (b) schematic showing the cross section of the pentacene-based organic thin film transistors (OTFTs), and (c) optical image of the OTFT layout.

voltage ($V_{DS}$) is swept from 0 V to -35 V for different gate voltages ($V_{GS}$). The measured device mobility is around 0.2 $cm^2$/V-s and the threshold voltage variation is <200mV over a 4-inch wafer. Such small variation in threshold voltage has not been reported for pentacene-based transistors. In fact, our matched pair test structures had threshold voltages of -2.8 V and -2.7 V, which is an excellent result for OTFTs. Figure 4(b) shows the input-output characteristics of an enhancement load inverter fabricated using the gate-last process. The inset shows the schematic of the inverter circuit. The maximum gain achieved with this process was 6.5.

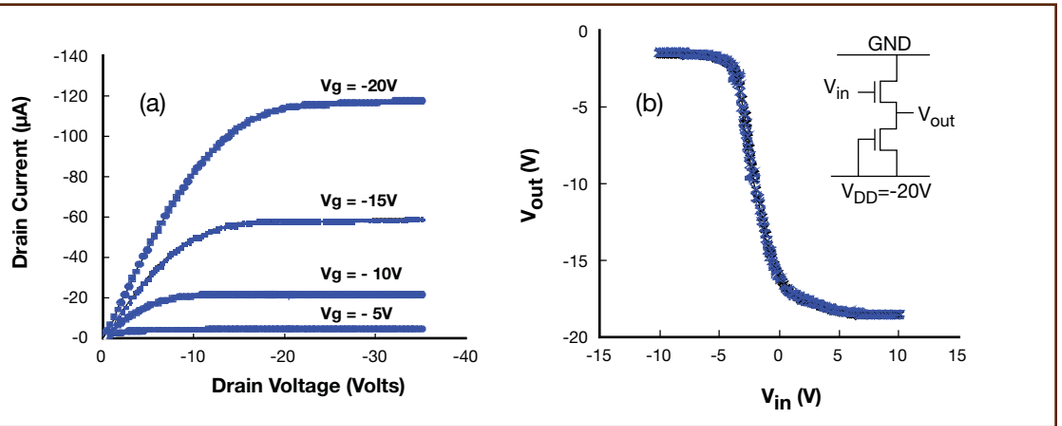


Figure 4. (a) $I_d$-$V_d$ characteristics of a single pentacene-based organic thin film transistor and (b) input-output characteristics of an enhancement load inverter. A maximum gain of 6.5 was achieved.

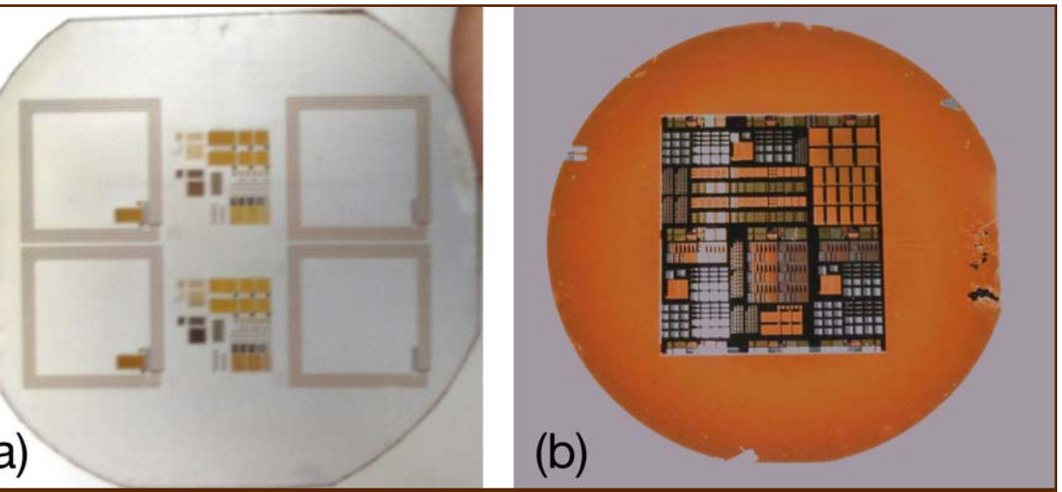


Figure 5. (a) Organic-based rectifier test chip fabricated on plastic substrate and (b) organic-based multicircuit test chip fabricated on silicon substrate.

Finally, Figure 5 shows two test chips fabricated using organic semiconductor-based devices and circuits. Figure 5(a) shows a rectifier tag test chip fabricated on a flexible substrate. In comparison, Figure 5(b) shows a 7-mask test chip incorporating several organic-based devices and circuits including analog, logic and discrete devices. Testing and optimization of many circuit types is ongoing.

## Conclusion

Organic semiconductor-based devices have been fabricated and successfully integrated to demonstrate a variety of electrical circuit types. These circuits include rectifiers, amplifiers, current mirrors and ring oscillators. These devices could offer a cost-effective solution for several applications, including RFID tags, flexible electronics and flexible displays.

## References

1. G. Malliaras and R. Friend, *Physics Today*, May 2005, pp. 53-57
2. D. F. Barbe and C. R. Westgate, *J. Phys. Chem. Solids* 31, 2679(1970).
3. A. Tsumura, K. Kurokawa and S. Nara, *J. Appl. Phys.* 54, 3255(1983).
4. G. Horowitz, *J. Mater. Res.* 19 (7), 1946 (2004).
5. J. Zaumseil and H. Sirringhaus, *Chem. Rev.* 107, 1296 (2007).
6. Yuming Ai et al. *Appl. Phys. Lett.* 90, 262105 (2007).
7. S. Gowrisanker, presented at the Materials Research Society Meeting, San Francisco, March 25, 2007.
8. D. Knipp, R.A. Street, A. Volkel and J. Ho, *J. Appl. Phys.* 93, 1 (2003).

## About the Authors

***H. N. Alshareef***

Dr. Husam Alshareef received his Ph.D. from NC State University in 1996. He is currently working with the University of Texas at Dallas (UTD). His research interests include organic electronics and energy harvesting materials and devices. The holder of 49 issued patents, he has authored 110 articles and three book chapters.

***M. Quevedo-Lopez***

Dr. Manuel Quevedo-Lopez received his Ph.D. from the University of North Texas. He is currently at UTD working on organic devices for flexible displays, photovoltaics and sensors.

***S. Gowrisanker***

Srinivas Gowrisanker is a Ph.D. candidate in physics and a research assistant in the Materials Science Department. His research includes physical and electrical characterization of novel materials for applications in the field of flexible electronics.

***Y. Ai***

Yuming Ai is a Ph.D. student in electrical engineering at UTD. His research interest is in organic semiconductor device fabrication and circuit integation.

***B. Gnade***

Bruce Gnade received his Ph.D. in nuclear chemistry from the Georgia Institute of Technology in 1982. He is currently the vice president for Research and the Distinguished Chair in Microelectronics at UTD. ■

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**Kazu Yamada**
Vice President and General Manager, Custom SoC Solutions Strategic Business Unit, NEC Electronics America, Inc.

***Problem***

As old-timers know, mask making used to be a "no-brainer" and a straightforward process in IC manufacturing, up until 130nm. This last stage of design used to take no longer than a few days and cost a fraction of overall design and manufacturing expenses. However, when engineers began attempting to design geometries smaller than 100nm on silicon – with a 248 or 193nm wavelength – making masks became the equivalent of using an axe to craft fine pieces of woodwork! Another limitation for Moore's law!

***Solution***

Thanks to the creativity and diligence of many very bright engineers, the industry has been dodging the limitation by (1) using new lithography technologies such as immersion lithography to achieve higher resolution, (2) using smart-shape processing technologies such as OPC and RET, and (3) using new design flows that take parameter variations into account as statistical data. These technological achievements have made it possible for companies to manufacture 35nm chips using 193nm lithography methods.

***Paradox!***

Although technology has pushed the limits of Moore's law, the new solutions are very, very costly. In fact, costs are so high that the whole industry might need to find new ways of doing business to survive. The use of immersion lithography methods is not helping to slow the pace of rising investment costs, while the use of complex mask processing methods has increased mask costs to millions of dollars. These increases have created a climate in which it only makes sense for companies to produce ICs that can be mass-produced in large volumes. Even so, IC manufacturers have been moving in the opposite direction by accepting designs that have relatively small volumes, very short life cycles and lots of customization. Consequently, this paradox is poised to hurt the industry by stifling innovation and putting growth at risk.

The two articles presented here illustrate some recent attempts to formulate "real solutions" from the paradox. For both approaches, it is mandatory that IC engineers work together and be brave enough to let others cross into "their territories." After all, if economically viable solutions are not discovered, and soon, there will be no territories left for engineers to protect.





# It Takes a Village to Reduce Mask Costs

**Mitchell Heins,[1] Christopher Progler,[2] Venu Vellanki[3]**
[1]Pyxis Technology, Inc.; [2]Photronics Inc.; [3]KLA-Tencor Corporation

## Abstract

There is an old proverb that says, "It takes a village to raise a child." The gist is that it takes a collaborative effort among different players to make a difference. Three very different companies from the design, photo-mask and equipment spaces are applying the proverb to create a virtual village to tackle costs.

## Introduction

Over the last three decades, the semiconductor industry has gone through a disaggregating process that fractured the industry into stand-alone islands of specialization. While each step became more efficient through specialization, the industry lost much of its ability to optimize across the design-through-manufacturing flow. At the same time, the industry continued its push along Moore's Law, doubling integrated circuit (IC) transistor counts by 2X every 18 months. Mask making for today's state-of-the-art 45nm technologies has accelerated well past the basic assumptions in place when specialization occurred. Even with productivity boosts from specialization, the costs as shown in Figure 1 to create a set of photo-masks have continued to skyrocket, driven by the increases in complexity and associated technologies required to deliver the smaller geometries on silicon. So what does it take to reduce or at least maintain these costs? KLA-Tencor, Photronics and Pyxis Technology have set out to see if they can bridge the traditional boundaries set up almost three decades ago to attack these costs.

## Photo-Mask Making in Retrospect

The photo-mask (mask) is probably one of the most misunderstood, undervalued and maligned elements of the semiconductor process. For the first several decades of semiconductor design, the mask was simply a master copy of each IC layer that was used to transfer the designer's drawn shapes onto a silicon wafer. The engineer's patterns were duplicated through a photolithographic process of exposing the wafer with light passed through the mask. The mask was initially patterned through a combination of manual cutting of Rubylith and then demagnification to build 1X masks.

As the industry progressed to smaller geometries, it became difficult to pattern

the mask with sufficient fidelity. The industry compensated by writing masks at larger dimensions, then relying on sophisticated reduction lens systems to reduce the mask pattern during transfer to the wafer. By the 1990s, the sub-wavelength era drove the industry to develop OPC (optical proximity correction) techniques to pre-compensate the mask data for improved wafer image fidelity. Unfortunately this meant an explosion in data size, as the OPC more than quadrupled the number of shapes to be written on the mask. Additionally, the OPC figures were too small to write with the laser machines, and the industry was forced to switch back to eBeam machines which were much more expensive and had slower write times. At the same time, mask inspection equipment became more complex and sophisticated due to the smaller geometries needed for OPC and less tolerance in the manufacturing process for defects.

What used to be a simple inexpensive 1X master of the drawn layout has today become a very expensive active element of one of the most complex lens systems available.

## Overengineering

Currently there is a substantial amount of patterning on each mask layer, sometimes as high as 30 to 40 percent, which has nothing to do with the electrical functionality of the circuit. Examples of these are logos, layout annotations and metal fill shapes (see Figure 2). These shapes are often OPC-corrected and treated with the same tolerances as the critical device patterns. In other cases, the patterns are electrically significant but have already been designed to be tolerant of changes in dimensions or shifts in placement. Unfortunately, these patterns are treated with the same care and fidelity as all the other patterns, resulting in a significant amount of overengineering and waste. It seems obvious that with collaboration between design and manufacturing, much of this overengineering could be reduced with no impact to electrical fidelity and with a significant positive impact to the cost of the masks.

## Creating a Village

These problems and ideas are not new or revolutionary. They have been discussed at great length in conferences dedicated to the subject. The real problem seems to be of economics and cooperation across traditional handoff boundaries. No one island can fix the problems on its own, and there is no clear economic model for who will benefit and be willing to pay for the development and maintenance of a better solution. If it was just about making cheaper masks, then the mask suppliers and their customers seem to be the likely candidates to bear the costs of a better solution. However, neither the mask maker nor the end user purchasing the masks controls information from the design space or the equipment space – both of which are needed to complete a solution.

From this dilemma springs the beginning of a very interesting "virtual village" that is working to leverage their respective domain knowledge to reduce costs. Pyxis delivers auto-routing software used to create an IC's metal interconnect layout patterns. Photronics is a photo-mask manufacturer, and KLA-Tencor makes mask inspection equipment. Together these companies are taking a leadership role in reengineering the design-through-mask-manufacturing ecosystem to enable a more efficient mask manufacturing process. The general idea is to relook at how an IC's metal-interconnect layers are made during the design stage to create

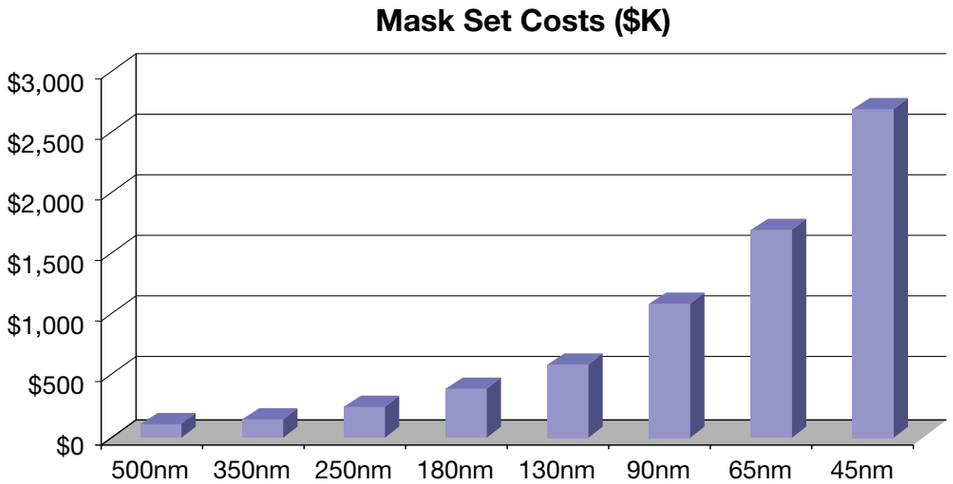


Figure 1. Average Cost of Photo-mask Set by Technology Node

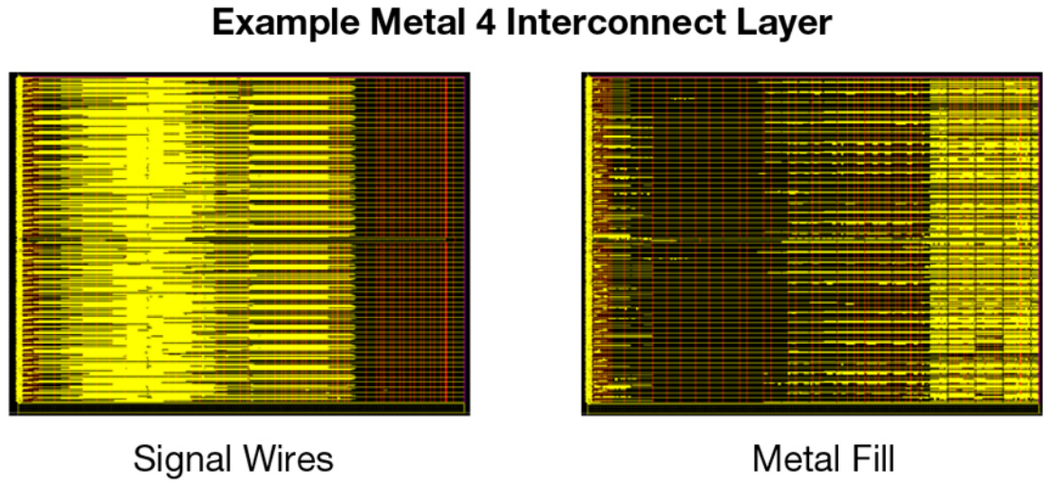


Figure 2. Comparison of Area Occupied on Metal-4 by Signal Wire vs. CMP Metal Fill at 65nm

patterns that are mask-manufacturing friendly. The effort then carries forward additional information about the design, captured as metadata, into the mask manufacturing process (see Figure 3). The metadata is used to identify layout areas where intelligent mask cost trade-offs can be made and verified that simplify the masks and reduce costs without compromising circuit fidelity or yield. This same metadata will also be used to augment mask inspection, defect dispositioning and mask repair in an effort to reduce costly scrap. Longer term, this same type of metadata could also be used to reach into the wafer manufacturing process as well.

## Conclusion

It is still early times for the collaboration, but initial investigations already point to what is believed to be a substantial savings to the bottom line for mask making. As data is gathered and successes mount, the village will grow to include other domains and partners like chip-finishing tool vendors, wafer-processing foundries and wafer-processing equipment manufacturers. In the end, the goal is to create a virtual village with a sustainable economic and technical ecosystem where all of the players get rewarded for their efforts. If successful, the collaboration could fuel a much needed move in industry toward virtual reintegration.

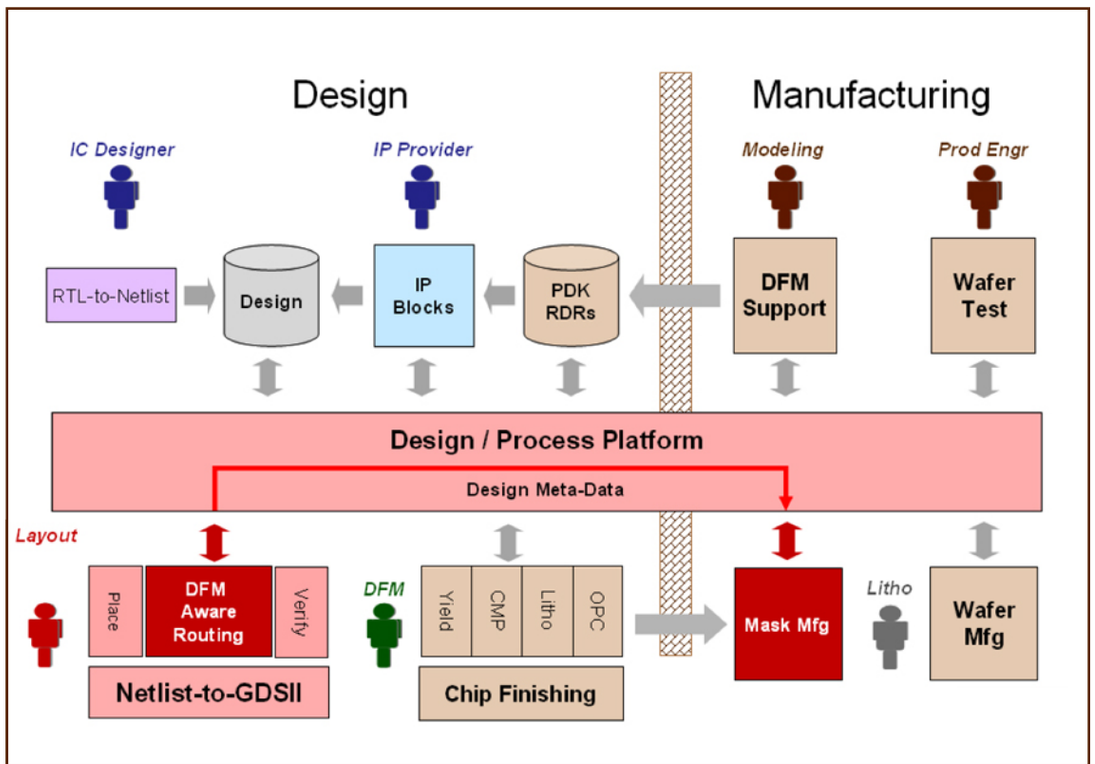


Figure 3. Forward Annotation of Design Metadata in the Design-Through-Manufacturing Ecosystem

### *References*

1. B. Eynon, B. Wu, et al., "Photomask Fabrication Technology," McGraw-Hill Electronic Engineering, 2005.
2. Y. Zhang, R. Gray, S. Chou, et al., "Mask Cost Analysis via Write Time Estimation," SPIE Microlithography Conference, March 2005.
3. Y. Zhang, R. Gray, O.S. Nakagawa, et al., "Interaction and Balance of Mask Write Time and Design RET Strategies," Photomask Japan, April 2005.
4. Y. Zhang, "Designing to Win in Sub-90nm Mask Production," 25th Annual BACUS Symposium on Photomask Technology, October 2005.

## *About the Authors*

### *Mitchell Heins*

Mitchell Heins is vice president of marketing at Pyxis Technology. He has 25 years' experience in the semiconductor and design automation industries, and has held management positions in several high tech companies, including HPL Technologies, Cadence Design Systems and Texas Instruments.

### *Dr. Christopher Progler*

Dr. Christopher Progler is executive vice president and chief technology officer at Photronics, responsible for global R&D, technology joint ventures and emerging technology opportunities.

### *Venu Vellanki*

Venu Vellanki is a senior product marketing manager at KLA-Tencor's Reticle and Photomask Inspection division. He has over 12 years of experience in the semiconductor industry, with a focus in photolithography and reticles. ■

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DESIGN IMPLEMENTATION & PROCESS INTEGRATION

# eDFM – Not "If" It Will Print, But "How"?

**Randy Smith**
Randysan Consulting

## Abstract

Electrical Design for Manufacturing (eDFM) is an emerging field of technology that asserts to predict how a circuit will behave as modified by distortions in the manufacturing process. While the original work in DFM was centered on lithography, eDFM goes further to predict and optimize the effects on power and performance of chip designs. This article provides an introduction to eDFM and an abbreviated canvas of the available tools in the market.

The term, DFM, or Design for Manufacturing, has been thrown around a lot the past eight years or so. Frankly, much of what was originally touted as DFM technology was more like MDP – or mask data prep technology – OPC, RET and the like. It was not built for the direct use of the designer. Most of the DFM discussions started to get heated around the 130nm node and got more intense the larger the gap between the lithography source and the feature size being exposed. Then we were concerned about overall yield, so finding catastrophic failures and solving them was the goal. So is the lithography problem mostly solved now? The designers have a few tools to assist them in avoiding lithography problems, so DFM is a done deal now, right? Well, sort of. Let's just say we have a better handle on it now. Unfortunately that is not the end of the story. Now that we can stop being as concerned about if something will print, we now need to be more concerned by exactly how certain things will print, especially transistors. Welcome to the world of electrical DFM (eDFM).

Transistor performance depends heavily on the way that the polysilicon gate and diffusion objects print. Small variations can significantly change the channel length, creating dramatic changes in current flow. Even small shape variations of diffusion and poly layers can translate into large nonlinear performance variation of the design. Lithography-induced variations therefore have a direct impact on timing, power and noise. Today's timing analysis techniques do not adequately model for these types of problems since the timing models used by these tools are built on idealized structures and do not account for the wide variety of structures used in actual designs.

As if the transistor shape was not cause enough for concern, the use of guard bands to model interconnect performance also seems to be breaking down. Today's guard bands in interconnect extraction are typically -20 percent to +30 percent. At 65nm, the layout parasitic extraction approach used in existing extraction methodologies is inadequate to predict the systematic variations in device and interconnect delays dominated by shape variations. You still need to be concerned about noise failure, and accurate device behavior prediction is essential for capturing all possible noise failures.

So, what can be done to address eDFM then? There have been several attempts at the major EDA companies to solve these problems, and their technology portfolios have been increased by a string of acquisitions in the past few years as well. A quick Internet search will reveal DFM solutions from Blaze DFM, Cadence, Magma, Mentor Graphics, Synopsys and a few others. These solutions are not exclusive either. Some tools focus on different aspects of the problem than others, so it is best if you are considering these tools to really focus on what each tool does. With that in mind, here is a brief overview of some of what is available commercially. This may not be complete, but it is a good starting point of solutions to consider (listed in alphabetical order).

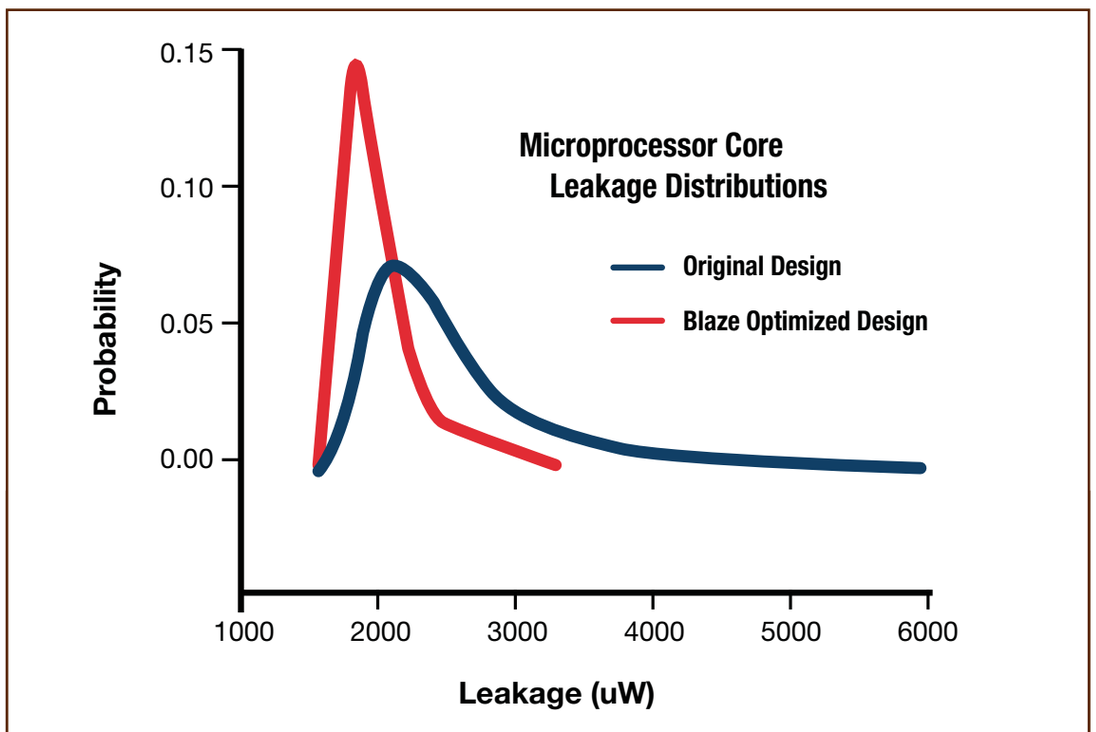


Figure 1. Leakage Reduction Using Blaze MO *(courtesy of Blaze DFM)*

## Blaze DFM

A bit more than a year ago, start-up Blaze DFM merged with start-up Aprio Technologies. The combination of Blaze DFM, which touted itself as "the electrical DFM company," and Aprio, a technology leader in the lithography side of DFM, was meant to enable Blaze to offer "the industry's only comprehensive electrical DFM solution." A year later, Blaze is making progress. The combined company closed $10 million in additional equity financing last year. The two products available on the website, Blaze MO and Blaze IF, were both announced prior to their merger; however, the company has announced that the latest release of Blaze MO will add lithography-aware capabilities from the HALO Lithography Engine originally developed at Aprio. A demo of this technology is available at http://www.demosondemand.com/dod/proddemos/vendors/pd_blaze.aspx.

Blaze's focus is on parametric yield and the optimization of designs to minimize leakage power. Blaze's MO tool is timing-driven, only biasing transistors on paths that have available timing slack. It is integrated with standard static timing analysis sign-off tools so that you do not need to support an additional timing tool to integrate Blaze MO into your design flow.

## Cadence

Cadence had initially sought to bolster its DFM offering by partnering with the ASML MaskTools division. That strategy had produced only minimal results when ASML then acquired Brion Technologies, making the ASML/Cadence partnership appear impotent. Now, after a string of acquisitions by Cadence – including Invarium and Clear Shape – an announced collaboration with STARC (an important Japanese consortium) and the release of its newest generation of WYDIWYG ("What you design is what you get") tools, Cadence has closed the gap considerably and can now be considered a serious provider of eDFM technology.

Cadence's approach implies that as designers move to 45nm and beyond, they will find that using model-based simulation followed by electrical evaluation of the resulting shapes leads to a more realistic and accurate design analysis and also avoids the costs associated with foundries' recommended design rules. Cadence is moving toward a methodology that achieves a more aggressive layout through limited usage of litho-related recommended design rules; the identification and fixing of hot spots; and improving tuning accuracy.

## Magma

Magma offers a variety of tools for addressing DFM and eDFM issues, including Talus DFM (implementation), Quartz DFM (analysis), and SiliconSmart DFM (characterization). While some of the tools appear to be simply lithography-specific, SiliconSmart DFM attempts to extend Magma's Talus implementation platform to provide designers with the ability to control and measure both systematic and random process variations. Magma's tools allow measurement for inter-cell and intra-cell characterization, silicon shape characterization and statistical leakage. Magma's systematic approach is quite interesting, and perhaps easier to use, if slightly incomplete at this time.

## Mentor Graphics

Bucking the trend, Mentor's DFM technology is home grown. Mentor's emphasis has been on capturing variability at the SPICE level first. This is because Mentor sees eDFM as an evolution from basic, as-drawn physical parameter inputs to a combination of physically modeled, as-manufactured parameters that are design-specific and context-specific. These parameters are then applied to next-generation device and interconnect models. With increased knowledge of how process variation impacts circuit performance, Mentor believes designers can optimally center a design on the risk-reward spectrum, between an aggressive design for better competitive performance and a conservative design that ensures high parametric yield, but leaves potential functionality and performance on the table.

Mentor's current eDFM offering includes the Calibre LFD tool, which is fully integrated with Calibre LVS Advanced Device Parameter (ADP) facility, allowing critical device dimensions to be extracted from the LFD-modeled contour geometries to determine a set of equivalent effective dimensions for the devices. The resulting device parameters, which reflect actual as-built device shapes, can then be plugged into a SPICE model to produce an accurate timing simulation of how the real device will work. The combination of Calibre LFD and LVS is a complete and integrated solution that augments current SPICE simulations by providing more accurate results that better reflect actual silicon performance.

## Synopsys

While long vying with Mentor for the leadership position in the lithographic DFM area, which is now also under assault from ASML/Brion, Synopsys has been somewhat slow to address the area of eDFM. Ultimately it is possible, given Synopsys' extensive TCAD offering, that they may come up with some strong and compelling technology in this area, but for now we must wait.

## Summation

The tool providers are working ever closer with the process developers to make the newest processes available for successful production use. No one company seems to have a complete solution yet, but the offerings are improving relatively quickly. If you are designing at or below the 65nm level, you need to address DFM, and you need to consider eDFM. At 45nm and below, eDFM is now part of your life. With so many competing solutions available, it is probably best to focus on the aspect of the problem that is most important to you – speed, yield or leakage – and start with the tools that best address that concern and integrate with your physical implementation tools. While challenging, it is your best path to functional silicon.

## *About the Author*

***Randy Smith***

Randy Smith, the principal/owner of Randysan Marketing (www.randysan.com), has been active in EDA and semiconductor IP since 1979, with 10 years of engineering background, and the balance in marketing, sales, and business development. ■

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**Alan Weber**
President, Alan Weber & Associates

Students of history know that it tends to repeat itself ...

So as the industry debate over a potential transition to 450 mm wafers intensifies, it is especially fitting that both papers in this section look at ways of improving factory performance at our current technology nodes. As we saw in the mid-90s, some of the operational improvements that were achieved in anticipation of the automation requirements for 300 mm actually reduced the urgency of the transition itself (not to mention a couple of years of industry down cycle). Sound familiar?

The first paper, from Zarifoglu et al. of ISMI, takes a quantitative look at the potential cycle-time benefits of three specific operational factors, namely improving equipment availability, setup time and first wafer delay; moving to single-wafer processing; and optimizing cascade parameters. The authors don't say *how* these improvements would be achieved, but the analysis does enable one to estimate the financial impact and weigh this against the investment required. Without getting into the details, it is clear that industrywide application of some of the ISMI next-generation factory automation principles that echo these factors would pay back handsomely, regardless of wafer size.

The second paper, by James Ignizio, offers an interesting retrospective on one of the earliest applications of effective manufacturing technology – the automobile industry. My initial reaction will likely be felt by most senior semiconductor manufacturing practitioners: "Well, our industry is different, and doesn't fit the basic model for which the ideal factory's 12 goals were established." But on a second and admittedly more open-minded reading, I found a few nuggets that could well apply. And since the first 450 mm facilities are still far into the future, there is much time available for evaluation and adoption of new ideas at 300 mm. Likewise with the single chip processing notion – a shift from the current multi-die round wafer substrate paradigm is highly unlikely, but if you suspend this assumption and consider the continuous flow of single substrates, some useful concepts for equipment, material handling and factory design will emerge.

But don't take my word for it – both articles are very approachable and well worth the time it takes to read and reflect.

MANUFACTURING, SYSTEMS & SOFTWARE

# Modeling Semiconductor Factories for Equipment and Cycle Time Reduction Opportunities, Part II

**Emrah Zarifoglu,[1] Robert L. Wright,[2] Chad Bubela,[3] Joey Preece[3]**
[1]The University of Texas at Austin, [2]ISMI, [3]Texas State University

## Quantifying Cycle Time Improvements in 25- and 12-Wafer Carrier Capacity Models

### Introduction and Background

International SEMATECH Manufacturing Initiative's (ISMI's) Small Carrier Capacity Task Force began with the purpose of investigating potential cycle time reductions when smaller carriers with a 12-wafer capacity are used. Other purposes included finding cycle time benefits while employing current 25-wafer carriers. This analysis quantifies the potential cycle time benefits to be achieved by implementing equipment improvements, replacing batch equipment with single-wafer processing tools, and adjusting lot cascade lengths. While previous models simulated a factory with assumed equipment improvements such as reducing the amount of time used for setups and first-wafer delays (FWDs) and increasing equipment availability, these models utilized a constant minimum cascade policy of two lots for all tool groups in ISMI's high-mix model.

ISMI's high-mix model contains five high-performance logic process flows of 100 products with varied product volume. The number of products varies among the five process flows. Monthly wafer starts total 34,500 wafers including 30,000 product wafers and 4,500 nonproduct wafers. In addition to the equipment improvements listed above, it was contemplated that each of the five process flows would require specific cascading scenarios to enhance cycle time reductions. Cascade sizes are predefined by specifying the minimum number of lots required in queue at the process equipment before performing a setup. Cascade assumptions can be specifically set for tool families, technology nodes and process steps. Decreasing the cascade size to one allows equipment to run one-of-a-kind lots if only one lot of any product is in a tool family queue. However, for some tool groups, employing a cascade size of one can create excessive lot congestion. When tool families have a higher-than-average lot count in queue, the processing equipment needs to be able to process multiple lots of the same product type in series to reduce queues more quickly.

Following numerous simulations testing cascade sensitivity, minimum cascade sizes were set to one in all serial processing tool families, except for lithography and implant equipment, to establish the 25-wafer baseline model. Sensitivity scenarios with a cascade length of both two and four lots for lithography and implant were simulated in separate models. The simulations with a cascade size of two for both lithography and implant equipment yielded the lowest cycle time. Wet processing and diffusion furnaces were modeled as batch process equipment in the baseline model. The final tool count, including metrology tools, was 712 tools for the 25-wafer baseline model.

| 25-Wafer ASSUMPTIONS 12-Wafer | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Tool Count: 712 | | | | | | | | |
| Batch Equipment | | Min | Max | Batch Size | | Min | Max | |
| Wet Tools | | 2 | 2 | | | 4 | 4 | |
| Furnace | | 6 | 6 | | | 12 | 12 | |
| 45 Layer | | 2 | 4 | | | 4 | 8 | |
| Wait No Longer Than __ before processing begins | | 30 minutes | | | | 30 minutes | | |
| Assumptions for Lot Cascading | | | | | | | | |
| Implant | | 2 | | | | Implant | | 4 |
| Lithography | | | | | | Lithography | | |
| Mask Layers | 33 | 2 | | | | Mask Layers | 33 | 4 |
| | 35 | 4 | | | | | 35 | 8 |
| | 37 | 1 | | | | | 37 | 2 |
| | 40 | 2 | | | | | 40 | 4 |
| | 45 | 1 | | | | | 45 | 1 |
| 25 WAFER RESULTS | | | Model Assumptions | | | 12 WAFER RESULTS | | |
| Cycle Time (Days) | Cycle Time/layer (Days) | X Factor | Mask Layers | # of Products | Wafer Starts per Month | Cycle Time (Days) | Cycle Time/layer (Days) | X Factor |
| 35.76 | 1.08 | 3.22 | 33 | 30 | 11,250 | 37.91 | 1.15 | 5.01 |
| 43.29 | 1.24 | 3.62 | 35 | 5 | 10,000 | 40.81 | 1.17 | 5.01 |
| 38.07 | 1.03 | 2.97 | 37 | 30 | 3,000 | 61.23 | 1.65 | 7.03 |
| 81.04 | 2.03 | 5.86 | 40 | 25 | 4,750 | 72.35 | 1.81 | 7.70 |
| 53.83 | 1.20 | 3.48 | 45 | 10 | 1,000 | 52.47 | 1.17 | 4.99 |
| 50.40 | 1.31 | 3.83 | Average | | | 52.95 | 1.39 | 5.95 |
| 46.25 | 1.28 | 3.75 | Weighted Average | | | 47.12 | 1.31 | 5.64 |

Table 1. Baseline Assumptions and Initial Comparison of 25-Wafer and 12-Wafer Carrier Results

| 25-Wafer ASSUMPTIONS 12-Wafer | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Equipment Availability Increased by 5% | | | | | | | | |
| Setup and First-Wafer Delay Decreased by 25% | | | | | | | | |
| Tool Count: 712 | | | | | | | | |
| 25 WAFER RESULTS | | | Model Assumptions | | | 12 WAFER RESULTS | | |
| Cycle Time (Days) | Cycle Time/layer (Days) | X Factor | Mask Layers | # of Products | Wafer Starts per Month | Cycle Time (Days) | Cycle Time/layer (Days) | X Factor |
| 31.43 | 0.95 | 2.83 | 33 | 30 | 11,250 | 31.67 | 0.96 | 4.18 |
| 38.53 | 1.10 | 3.22 | 35 | 5 | 10,000 | 35.54 | 1.02 | 4.37 |
| 34.43 | 0.93 | 2.69 | 37 | 30 | 3,000 | 55.44 | 1.50 | 6.36 |
| 74.60 | 1.87 | 5.39 | 40 | 25 | 4,750 | 65.24 | 1.63 | 6.95 |
| 45.99 | 1.02 | 2.97 | 45 | 10 | 1,000 | 45.51 | 1.01 | 4.32 |
| 45.00 | 1.17 | 3.42 | Average = | | | 46.68 | 1.22 | 5.24 |
| 41.39 | 1.15 | 3.36 | Weighted Average = | | | 41.09 | 1.14 | 4.90 |

Table 2. Cycle Time Results With Equipment Improvements

## Transition to 12-Wafer Carriers

The balanced 25-wafer baseline model with 712 tools was used as the reference point for simulating 12-wafer carriers. The objective of all simulations was to capture requirements to achieve the most cycle time reduction with equivalent equipment. Additionally, the 25-wafer and 12-wafer baseline models were simulated with relatively equal wafer batch sizes for all batch processing. Theoretically, transitioning from a 25-wafer to a 12-wafer carrier in an identical factory potentially causes twice the number of setups, resulting in higher equipment utilization. Table 1 compares the 25-wafer baseline model and the 12-wafer baseline model, both with 712 processing tools including metrology.

Next-generation factories are assumed to have advancements in processing equipment performance. Equipment improvements for a 5 percent increase in equipment availability and a 25 percent reduction in setup and FWD were simulated. These modeled improvements aided both 25-wafer and 12-wafer carrier capacity models to improve cycle time, as can be observed in Table 2. The 25-wafer model improved cycle time by 11 percent, and the 12-wafer model improved cycle time by 13 percent with the stated equipment improvements.

Although existing single-wafer processing (SWP) technology falls short of the complete replacement of all batch processing equipment, this analysis assumes full conversion of all batch tools to single-wafer processing. Assuming wafer throughput for SWP equipment is the same as batch equipment, the tool count was held constant at 712. Table 3 compares the 25-wafer and 12-wafer models with SWP combined with the improvements shown previously in Table 2.

The complexity of the high-mix model required adjusting cascading rules based on individual process flows. Early results (see Table 1) showed that the cycle times of individual process flows were highly variable. A single high-mix model contains 100 products spread among five process flows ranging from 33 to 45 mask layers. More than 70 percent of the volume resides in the shortest process flows. Conversely, this model represents a factory with the most complex (45 masks) and lengthiest process flow comprising the least volume (3.3 percent). The difficulty arises in the 37- and 45-mask layer flows. With the given number of wafer starts per month spread over the specified products, 100 wafers for each product are started only once per month. This creates a situation where like-lots are few when cascading rules can require multiple lots of the same product to batch or cascade. Therefore, cycle time of specific products can be lengthy because of stranded or isolated lots. Table 4 lists the cumulative factory improvements, including a sensitivity of cascading rules and the results.

## Observations

The efforts of the Small Carrier Capacity Task Force developed stable models for two different carrier capacity models with equivalent tool counts. In review of Table 4, relatively equal cycle time improvements were observed when assuming a 5 percent increase in availability for all equipment groups and 25 percent reduced setup time and FWD. However, the cycle time reductions generated by single-wafer processing greatly favored 12-wafer carrier models. Additionally, the effective application of lot cascading provided the most beneficial reductions in cycle time with a single-factor individual contribution of 31 percent in both 12-wafer and 25-wafer carrier models. It is important to note that the latter factor used intellectual investment as opposed to

| 25-Wafer ASSUMPTIONS 12-Wafer | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Single-Wafer Processing | | | | | | | | |
| Equipment Availability Increased by 5% | | | | | | | | |
| Setup and First-Wafer Delay Decreased by 25% | | | | | | | | |
| Tool Count: 712 | | | | | | | | |
| 25 WAFER RESULTS | | | Model Assumptions | | | 12 WAFER RESULTS | | |
| Cycle Time (Days) | Cycle Time/layer (Days) | X Factor | Mask Layers | # of Products | Wafer Starts per Month | Cycle Time (Days) | Cycle Time/layer (Days) | X Factor |
| 25.28 | 0.77 | 2.28 | 33 | 30 | 11,250 | 25.31 | 0.77 | 3.34 |
| 31.06 | 0.89 | 2.60 | 35 | 5 | 10,000 | 27.03 | 0.77 | 3.32 |
| 79.26 | 2.14 | 6.19 | 37 | 30 | 3,000 | 28.33 | 0.77 | 3.25 |
| 59.83 | 1.50 | 4.32 | 40 | 25 | 4,750 | 43.05 | 1.08 | 4.58 |
| 28.78 | 0.64 | 1.86 | 45 | 10 | 1,000 | 27.02 | 0.60 | 2.57 |
| 44.84 | 1.19 | 3.45 | Average | | | 30.15 | 0.80 | 3.41 |
| 38.17 | 1.06 | 3.08 | Weighted Average | | | 29.04 | 0.81 | 3.50 |

Table 3. Cycle Time Comparison With Single-Wafer Equipment

| 25-Wafer | ASSUMPTIONS | 12-Wafer |
|---|---|---|
| Single-Wafer Processing | | |
| Equipment Availability Increased by 5% | | |
| Setup and First-Wafer Delay Decreased by 25% | | |
| Tool Count: 712 | | |

**Cascading Assumptions**

| Implant | | MinQueue |
|---|---|---|
| | | 2 |
| | 45-Layer | 1 |
| Lithography | | |
| Mask Layers | 33 | 2 |
| | 35 | 2 |
| | 37 | 1 |
| | 40 | 1 |
| | 45 | 1 |

| Implant | | MinQueue |
|---|---|---|
| | | 4 |
| | 45-Layer | 2 |
| Lithography | | |
| Mask Layers | 33 | 3 |
| | 35 | 4 |
| | 37 | 1 |
| | 40 | 1 |
| | 45 | 1 |

| 25 WAFER RESULTS | | | Model Assumptions | | | 12 WAFER RESULTS | | |
|---|---|---|---|---|---|---|---|---|
| Cycle Time (Days) | Cycle Time/layer (Days) | X Factor | Mask Layers | # of Products | Wafer Starts per Month | Cycle Time (Days) | Cycle Time/layer (Days) | X Factor |
| 25.73 | 0.78 | 2.32 | 33 | 30 | 11,250 | 19.16 | 0.58 | 2.53 |
| 26.57 | 0.76 | 2.22 | 35 | 5 | 10,000 | 20.29 | 0.58 | 2.49 |
| 25.47 | 0.69 | 1.99 | 37 | 30 | 3,000 | 18.21 | 0.49 | 2.09 |
| 27.50 | 0.69 | 1.99 | 40 | 25 | 4,750 | 21.56 | 0.54 | 2.30 |
| 28.46 | 0.63 | 1.84 | 45 | 10 | 1,000 | 28.48 | 0.63 | 2.71 |
| 26.75 | 0.71 | 2.07 | Average | | | 21.54 | 0.56 | 2.42 |
| 26.35 | 0.74 | 2.18 | Weighted Average | | | 20.13 | 0.57 | 2.44 |

| 25 WAFER SUMMARY | | | | | 12 WAFER SUMMARY | | | |
|---|---|---|---|---|---|---|---|---|
| Cycle Time (Days) | Cycle Time/layer (Days) | Single-Factor % Change | Cumulative % Change | Simulation Scenario | Cycle Time (Days) | Cycle Time/layer (Days) | Single-Factor % Change | Cumulative % Change |
| 46.25 | 1.28 | | | Baseline | 47.12 | 1.31 | | |
| 41.39 | 1.15 | 11% | 11% | FWD/Setup Equipment Availability | 41.09 | 1.14 | 13% | 13% |
| 38.17 | 1.06 | 8% | 17% | Single Wafer Processing | 29.04 | 0.81 | 29% | 38% |
| 26.35 | 0.74 | 31% | 43% | Cascading Optimization | 20.13 | 0.57 | 31% | 57% |

Table 4. Results of 25-Wafer and 12-Wafer With Equipment Improvements, Single-Wafer Processing, and Effective Cascading and Summary of Results

requiring capital investment. Pertaining to our theory that setups would increase in a factory employing 12-wafer carriers, the simulation results showed that the number of setups actually decreased.

Significant decreases in cycle time were obtained in both 25-wafer and 12-wafer models by simulating the full combination of factors. This resulted in a 57 percent reduction in cycle time for the 12-wafer carrier model. Twenty-five wafer carrier models demonstrated a 43 percent reduction in cycle time when combining all factors. For this analysis, the 12-wafer carrier model demonstrated a greater overall potential for cycle time improvement.

These analyses assumed a material handling system simulated with stochastic delivery times but infinite capacity. Hence, as carrier capacity decreases, the material handling system needs to be studied and analyzed in future studies. Other future studies should be considered for near-term single-wafer processing capability. For additional background information, please refer to Part 1 of this article in issue 24 of Future Fab International.

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## About the Authors

***Emrah Zarifoglu***
Emrah Zarifoglu is a Ph.D. candidate in the Operations Research and Industrial Engineering program at The University of Texas at Austin. He received his M.S. in industrial engineering at Bilkent University in Ankara, Turkey. Mr. Zarifoglu currently develops and analyzes semiconductor simulation models at ISMI.

***Robert L. Wright***
Robert L. Wright manages factory simulation and cost modeling projects for International SEMATECH Manufacturing Initiative (ISMI). He has 12 years of cost modeling and simulation experience and is a member of the technical staff. Mr. Wright received his BBA in management and his M.S. in industrial technology from Texas State University.

***Chad Bubela***
Chad Bubela is a student at Texas State University majoring in industrial engineering. He works at ISMI as an intern under the NanoScholar program performing simulation analysis.

***Joey Preece***
Joey Preece is a student at Texas State University majoring in industrial engineering. He works at ISMI as an intern under the NanoScholar program performing simulation analysis. ■

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MANUFACTURING, SYSTEMS & SOFTWARE

# What Are the Alternatives to 450 mm Wafers?

**James Ignizio**
Manufacturing Science Consultant

## Abstract

Questions have been raised with regard to larger wafer diameters. In this paper, obstacles faced by 450 mm wafers are summarized. Two alternatives to larger wafers are proposed. The first is to employ methods available through lean manufacturing and manufacturing science to improve factory performance in 300 mm or 200 mm fabs. The second proposal is the consideration of efforts toward achievement of the "ideal factory" via single chip processing, or SCP.

## Wafers: Is Bigger Really Better?

Over a period of several decades the size of wafers employed in semiconductor fabs has evolved from 25mm (1 inch) to 300 mm (12 inches). The next increase in wafer size is planned to be a diameter of 450 mm (18 inches). Conventional wisdom within some portion of the semiconductor manufacturing community is that, the larger the wafer size, the more chips per wafer (and a lessening of the "edge effect," wherein chips deposited "too near" the edge of the wafer must be scrapped); thus the lower the cost per chip.

There are, however, two alternatives to larger wafer sizes that should receive consideration. These are:

- improve the efficiency of the production of existing wafer fabrication facilities
- seek the ideal factory state, a state that may be possible via investigation of the concept of single chip processing, or SCP

We first describe attributes of the "ideal," or utopian, factory state and then determine how those attributes compare to (i) a move to larger wafer sizes, (ii) improvement in the efficiency of existing fabs, or (iii) pursuit of the ideal state via SCP.

### *The Ideal Factory*

The scientific management pioneers and "wise men" of the Ford Company of the early 20th century cited certain goals they believed the ideal factory should strive to achieve. These goals were adopted and refined by the Toyota Company. Today most of these exist under the label of "lean manufacturing" and/or "manufacturing science." Specifically, it is believed the ideal factory should address the following 12 goals.

1. The primary focus of efforts dedicated to enhanced factory performance is – or should be – the elimination or mitigation of the three primary impediments to optimal production line performance. These three obstacles are complexity, variability and unhealthy business processes.
2. Product cycle time must be minimized while effective capacity is maximized.
3. Customer lead time, and uncertainty about lead time, must be minimized.
4. All improvements to cycle time, effective capacity, and customer lead time should be sustainable.
5. The factory's process machines should be no larger than four times the size of the product produced – unless otherwise dictated by the laws of physics.
6. There should be no reentrant operations (i.e., every workstation should support one and only one process step).
7. There should be no batching or cascading operations.
8. The factory must, as closely as possible, approximate a single-unit continuous flow system.
9. Production flow should emphasize and support flexibility and versatility.
10. The need for inspections should be minimized (i.e., machines and processes should be designed to support high-precision manufacturing).
11. Machines must be located according to the sequence of the process steps employed in manufacture of the product (i.e., a serial, non-reentrant layout as employed in automobile assembly should be used).

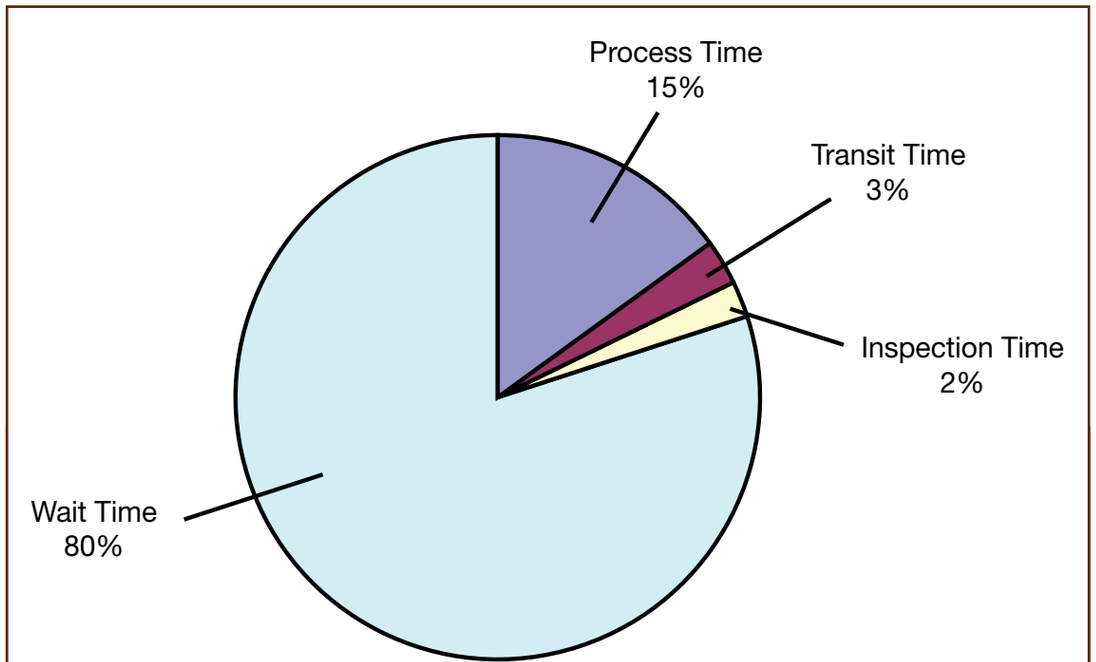


Figure 1. Cycle Time Components

12. Given the achievement of the ideal factory state defined by the previous goals, complex and problematic job-to-machine dispatch and dedication rules (e.g., "WIP management") may be discarded in favor of simple FIFO (first in, first out) job sequencing.

The most prominent of the relatively few manufacturing facilities that have been actually able to accomplish, or come close to achieving these goals are (i) the Arsenal of Venice, in fabrication of warships and merchant ships in the 16th century, (ii) the Ford Motor Company, in production of the Model T automobile, and (iii) the Toyota Company in implementation of the Toyota Production System. If, however, we compare the attributes of modern-day semiconductor wafer fabrication to each of the previously cited goals, it is clear that not a single one of these has been accomplished. Worse yet, few if any of these goals are even being addressed, nor – alas – is their importance fully comprehended.

A consequence of the failure to appreciate the importance of the goals of the ideal factory state is the fact that the productivity of today's fabs is far below their actual potential. Figure 1 depicts the components of the cycle time of a typical, traditional (i.e., nonsemiconductor) factory. As may be noted, the bulk of factory cycle time (i.e., 80 percent) is consumed by wait time; i.e., waiting for batches or cascades to form, or waiting for processing within a queue. The situation is even worse for the typical semiconductor fab, wherein wait time may consume up to 90 percent of the average wafer's cycle time.

### *The 450 mm Wafer*

A move to larger wafers, i.e., the 450 mm wafer, will – by itself – do nothing to improve the cycle time efficiency (CTE) of the typical semiconductor fab. In fact, if the consequences of the move from 200 mm to 300 mm are repeated, fab CTE will actually decline. This is not, however, the only drawback of the 450 mm wafer. Just a few of these problems are listed below:

- The resources required to make a 450 mm fab feasible diverts the time and funds that might be better allocated to improving the performance of 200 mm or 300 mm fabs.
- A move to a 450 mm wafer means that there will be 2.25 times more area per wafer over that of a 300 mm wafer (and 5.06 times more area than a 200 mm wafer). Given a trend toward more products in smaller quantities, the very size of the wafer may be a disadvantage.
- The scrapping of just one 450 mm wafer could have a significant impact on fabs running many products at low volume.
- A 450 mm wafer increases the problems associated with the need for wafer uniformity tolerances – and amplifies the impact of wafer bending and deformation.
- The larger the wafer, the more time required in heating and cooling process steps.
- Given the higher capacity, in terms of chips per wafer, a 450 mm fab will have more tool sets consisting of just one, two or three tools per tool set. Unfortunately, as the number of tools in a tool set decreases, the variability imposed on the factory increases (with a resultant increase in cycle time and decrease in effective capacity).
- A move to 450 mm wafers may reduce the cost per centimeter of silicon – but ignores costs associated with increased cycle times and decreased customer satisfaction.

### *Alternative 1: More-Efficient Factory Protocols*

The advantage of 200 mm and 300 mm fabs would likely outweigh those predicted for 450 mm fabs if these existing fabs would address the 12 goals of the ideal factory. More specifically, rather than focusing vast amounts of time and resources to changes in the physical attributes of a wafer or factory, concentrate instead on improving the protocols employed in running the fab. That is, address means to defeat the three enemies of factory performance: complexity, variability, and poor business processes.

This may be accomplished by means of the implementation of the methods inherent in lean manufacturing (e.g., scientific management, classical industrial engineering) and manufacturing science (e.g., operations research, factory physics). Factories that have adopted these approaches have shown substantial and sustained improvements in cycle time efficiency, effective capacity and customer satisfaction. Simulations have validated that the implementation of lean manufacturing (when specifically adapted to the unique nature of semiconductor fabs) and manufacturing science enable a 200 mm fab to surpass the performance of the typical 300 mm fab.

***The second alternative to larger wafer sizes* might be accomplished by means of single chip processing, or SCP.**

### *Alternative 2: The Utopian Fab?*

The second alternative to larger wafer sizes *might* be accomplished by means of single chip processing, or SCP. If we really want to achieve a near-continuous flow factory (the primary goal, by the way, of lean manufacturing) that addresses all 12 goals of the ideal factory, we might wish to consider an approach opposite to larger wafers.

That is, rather than moving to a fab with larger wafer sizes, why not explore the notion of SCP? While such a concept may seem improbable, recognize that those were precisely the same thoughts that crossed the minds of semiconductor manufacturing pioneers when the proposals for modern-day semiconductor fabs were first described. And the same reactions were expressed in the past to such "impossible" concepts as landing men on the moon, hitting a missile with a missile, cell phones or nanotechnology.

Consider, however, how an SCP fab might be designed. First, as evident by the name, each job in an SCP fab would consist of but a single, rectangular chip. Machines would be placed (as they are in the production of automobiles) according to the sequence of process steps. There would be one machine per process step and the resulting configuration would form a non-reentrant, serial, single-unit process flow. This change alone eliminates reentrancy, and all the problems associated with that phenomenon.

Rather than one (or a few) production lines, the small sizes of the SCP machines and material handling systems and their subsequent rapid process times might enable the employment of a multiple

"pipeline" fab design. A multiple pipeline fab would consist of hundreds of individual production lines (i.e., pipelines) and each individual production line would employ SCP. Each of these environmentally sealed pipelines would, as mentioned, consist of "tool sets" that employ but a single machine, and each machine would support but a single process step.

If the goal of having machines no more than four times the size of the individual product (i.e., four times the size of a single chip) is realized (wherever possible), then the hundreds of the pipelines might be enclosed in a space no larger than a typical 300 mm fab. Consequently, the SCP multiple pipeline fab might be capable of producing an output (i.e., in terms of the number of chips produced) comparable or greater than that of a conventional fab – and accomplish this in a fraction of the cycle times now necessary.

Just a few of the other potential advantages of the multiple pipeline SCP fab would include:

- a dramatic reduction in production line variability and complexity,
- an elimination or at least a reduction in the need to change reticles and implant sources,
- the reduction of the impact of blockages (and WIP bubbles) resulting from machine downtime (i.e., if a single or even several SCP pipelines went down, this would only amount to a small fraction of the total SCP fab output),
- since each job consists of just one chip, such problems as "edge effects" and bending/distortion may be eliminated, and finally
- there is no need to slice and dice a wafer so as to get the product you actually wanted in the first place: individual chips.

So, instead of spending vast amounts of time, energy and resources on larger wafer diameters – and correspondingly larger, more-complex and more-expensive processing machines and automated material handling systems, perhaps we should at least consider SCP. There are definitely obstacles to the development of SCP; but are they really any less than those faced and conquered in the realms of space travel, weapons systems, nanotechnology or a host of other seemingly impossible innovations?

## About the Author

***Dr. James Ignizio***

Dr. James Ignizio is a consultant in manufacturing science. He is a Fellow of IIE, ORS and WAPS; Professor Emeritus of the University of Virginia; and author of eight books and more than 300 technical publications. He can be reached at JamesIgnizio@aol.com. ■

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# FRONT END OF LINE

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**Janice Golda**
Director, Lithography Capital Equipment Development; Intel

The continued march to shrink feature sizes to double density every two years has enabled the industry to realize Moore's law. As feature dimensions continue to scale, a number of previously insignificant factors are becoming increasingly important to control in order to deliver high product performance at high yields. Keeping reticles defect free over their life cycle has always been essential to delivering high yields, as a single printable reticle defect can affect every die on every wafer if not caught. In this issue of Future Fab International, you will find a thought-provoking paper on a new consideration for managing reticles over the reticle life cycle.

Let's start with a historical perspective on reticle protection. Over the past 40 years, the handling of reticles has evolved from placing a 1x mask in direct contact with a resist-coated wafer to projection printing with a pellicle-protected 4x reticle. In the 1970s, changing from contact to projection printing eliminated a major mask defect source. In the 1980s, the introduction of pellicles fundamentally changed the game, physically protecting the reticle from defects using a protective film on a frame while also defocusing particles which landed on the pellicle, mitigating their impact. This eliminated a yield killer at the time. In the 1990s and early 2000s, mask handling has evolved from manual handling of a simple box to automated handling of sealed reticle SMIF pods (RSPs).

In recent years, new threats to mask cleanliness have emerged. The introduction of high-power lasers has enabled continuous improvement of lithography scanner productivity but has had the side effect of adding photo-induced reticle haze to the growing list of factors that must be controlled to keep reticles defect free. The introduction of EUV into manufacturing in the future will demand additional protective measures, as the concept of EUV pellicles is in its infancy.

Now, back to the present. In the current issue, Gavin Rider, a researcher from Microtome, exposes the prospect of electric field induced migration (EFM) of chrome, which can occur at electrical stresses 100x lower than those which cause "traditional" electrostatic discharge (ESD) problems and can cause critical dimension (CD) variation. Experimental data reported in this paper demonstrates the existence and impact of chrome migration.

# EFM: A Pernicious Threat to Reticles – Exposed

**Gavin Rider** – Microtome

## Abstract

In Issue 22, a brief overview was given of the changing nature of reticle electrostatic damage, and the consequences for semiconductor fabs were discussed.[1] The conclusions in that review were based on the interpretation of many pieces of evidence taken from different sources, but the risk assessment was empirical, so has not yet been widely accepted. This article presents new data from an experiment that was designed to quantify the damage effects under closely controlled conditions. It is now possible to say with certainty that reticles can be damaged by field-induced migration of chrome (EFM) at a level of electrical stress 100 times lower than that which causes ESD. Advanced reticles with feature spacings below 1 micron are found to be susceptible to field-induced damage when the potential differences induced in the reticle are below 1V.

## Recreating Field-Induced Reticle Damage in the Laboratory

EFM type 1 was first identified as a distortion of the edge of the chrome line in reticles that had been exposed to an electric field.[2] The rate of line spreading was seen to be almost independent of local field strength, suggesting that it was determined by parameters that were constant during the experiment, such as the temperature. Hence, EFM type 1 was thought to involve the thermal diffusion of neutral chrome atoms. EFM type 2 results in the formation of conductive tracks on the quartz and protrusions which develop on the positively biased chrome line, eventually leading to bridging between reticle lines. Since this mechanism is sensitive to both the strength and orientation of the electric field, it was attributed to the migration of chrome ions.

These interpretations have now been checked by conducting further experiments on a specially designed test reticle [3] containing structures as shown in Figure 1. Instead of stressing the reticle by applying an external electric field, which does not allow the local field strength

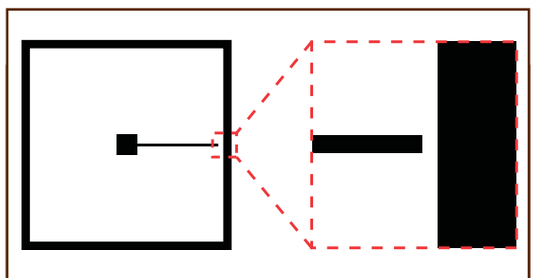

Figure 1. The Design of the Test Cells in the Special Test Reticle

around reticle features to be known, voltage was applied directly between adjacent chrome features. In this way the voltage and the electric field configuration would be known precisely. The experiment covered a range of discrete conditions so the behavior of the damage mechanisms could be studied in a systematic way. The current flowing during the experiment was recorded and no ESD events were observed, confirming that the damage produced was not related to ESD.

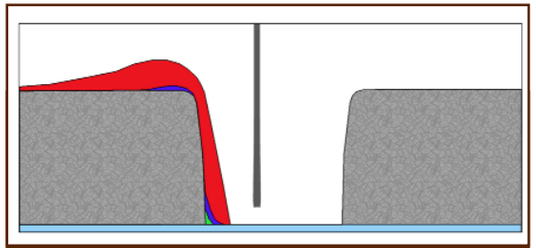

Figure 2. AFM line scans of reticle features stressed at different voltage and duration; Green: 50V for 15s, Blue: 100V for 15s, Red: 100V for 250s, Gray: original line profile. The AFM tip profile is also shown on the same scale (vertical scale magnified x10).

The stressed reticle features were subsequently examined by atomic force microscopy. Figure 2 shows surface profiles from test cells that had been exposed to different amounts of electrical stress, as measured with a Veeco X3D CD-AFM. The onset of EFM type 1, indicated by the formation of a meniscus at the boundary between the chrome and the quartz, is seen clearly.

The rate of development of the meniscus was >3nm per second at 50V, increasing to >6nm per second at 100V, at which voltage some modification of the upper surface of the chrome line was also evident. Extended stressing at 100V resulted in significant line distortion, as shown by the red profile.

While the surface profile data generated by CD-AFM measurements are highly precise and quantitative, they convey a limited amount of information about the processes that cause the line edge modification. Photo-realistic representation of the surface using "illuminated mode" presentation of the AFM data gives a clearer indication of the physical processes involved, as illustrated here.

Figure 3 shows AFM images of two identical 1 µm test cell structures that were stressed at the same voltage for similar durations, but with the polarity reversed. In both cases the positively biased chrome line has been distorted, matching the characteristics of field-induced damage in earlier studies. Figure 3b corresponds to the red profile in Figure 2.

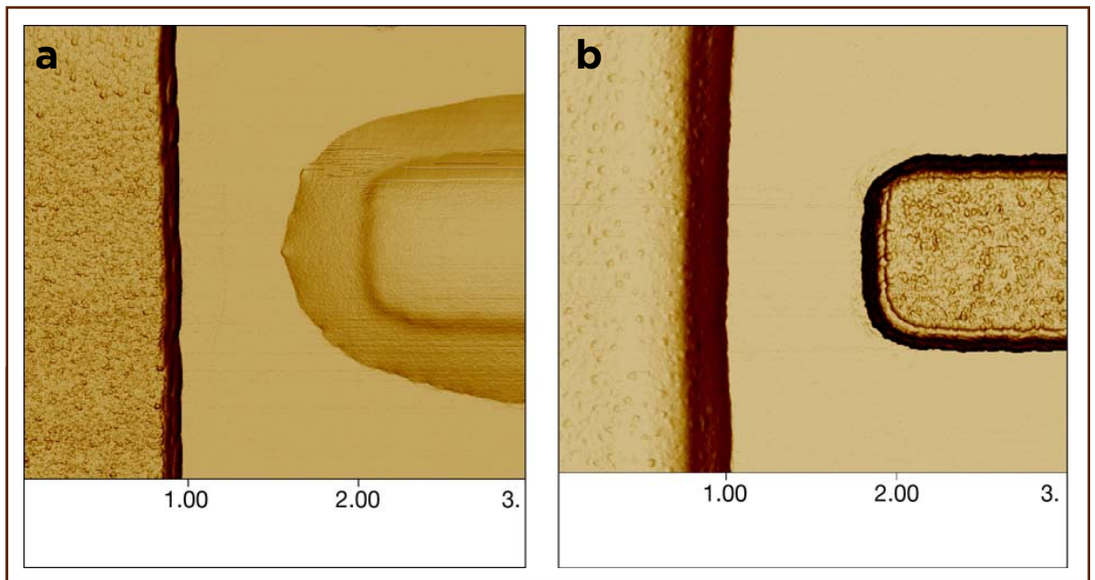


Figure 3. Atomic force microscope images of reticle features after stressing at 100V; a) with positive polarity applied to the spur line, and b) with negative polarity applied to the spur line.

Figure 4 shows the extent of the distortion after stressing a 1 µm line at +100V for 250 seconds. Note particularly the row of tiny beads on the quartz surface alongside the line and the swelling at the tip of the line. Figure 5a is a high-resolution image from the gap region of the same test cell, scanned with higher vertical and lateral resolution. This image reveals the presence of a thin film on the quartz adjacent to the chrome border. Even higher-resolution scans allowed extremely fine details of the surface deposits on the quartz to be seen, as shown in Figures 5b and 5c. The region adjacent to the spreading meniscus on the upper edge of the spur line was also imaged, and the quartz surface was found to be smooth and featureless (hence is not shown).

Similar characteristics were also seen on a 2 µm-wide line (Figure 6) which has been

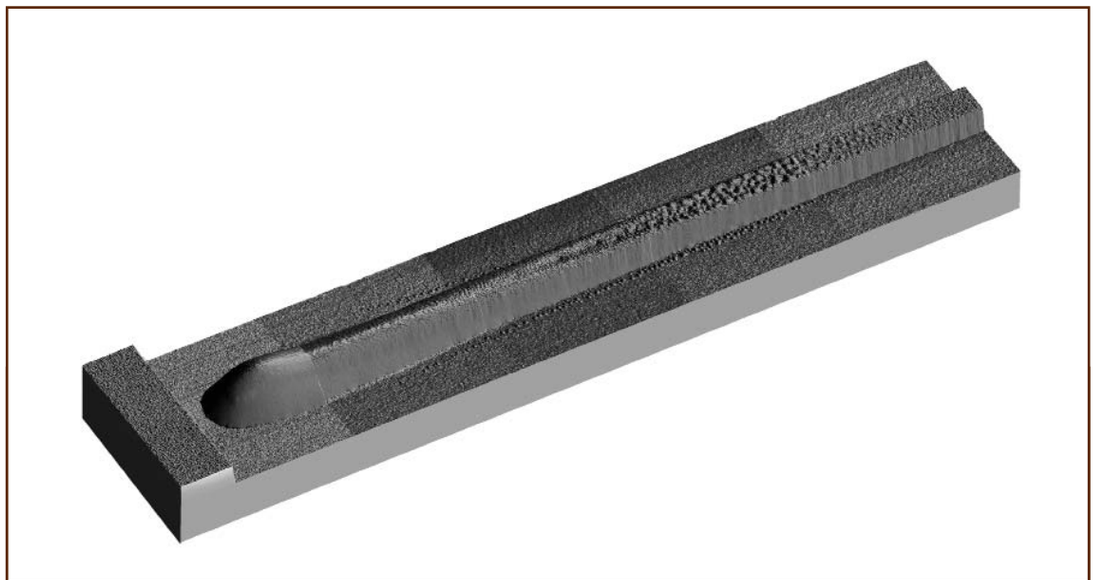

Figure 4. Perspective AFM view of a 1 µm-wide chrome line stressed at +100V for 250s (vertical scale x10 for clarity).

overlaid with a field strength vector matrix and colored field strength contours calculated by two-dimensional finite element analysis. These AFM images reveal a great amount of surface detail, and in conjunction with electric field simulation, this allows a fully quantitative determination of the changes that take place in a reticle as a function of electrical stress.

## Interpretation of the Damage Characteristics

### *The EFM Type 1 Meniscus*

The first sign of field-induced change on the edge of the chrome line is where the field strength rises to 2e6V/m, at which point the base of the line starts forming a meniscus and spreading out onto the quartz, as seen in Figure 2. For the 1 µm line-and-gap configuration used in this experiment, this field strength would be produced at the tip of the line by a potential difference of just 1V (whereas the voltage needed to cause an ESD event across the same gap would be 150V).[4]

The contact angle of the meniscus with the quartz is acute – about 10° – which indicates that the surface energy of the chrome film is low and that it is energetically favorable for chrome atoms to be on the quartz surface. The meniscus formation is interpreted as surface chrome atoms becoming mobile and diffusing thermally, following the reduction of their binding energy by the applied electric field. (Such

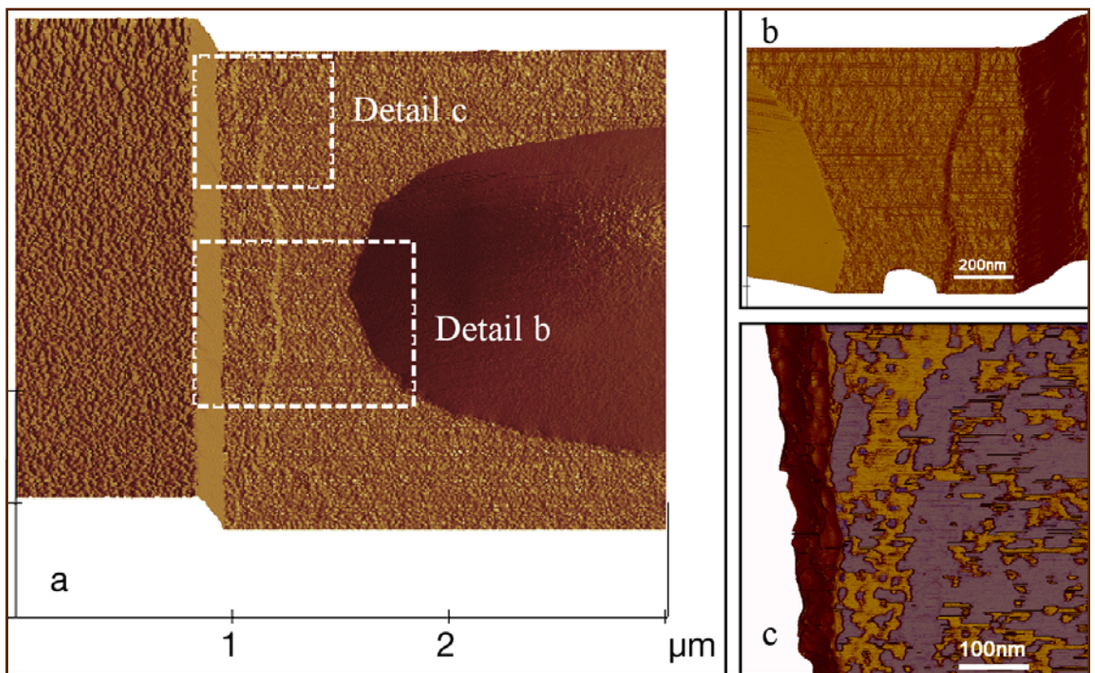


Figure 5. The gap region of a 1 µm cell stressed at +100V for 250s. Insets b and c show details of the outlined regions on the main image. The discontinuous part of the film in region c has been emphasized by tinting the areas between the image contrast contours using Photoshop.

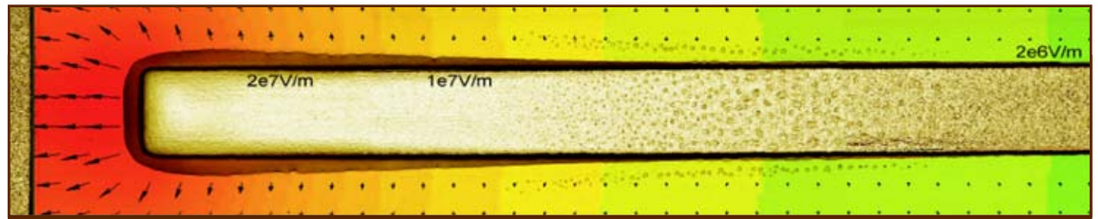


Figure 6. Plan view AFM image of a 2 µm-wide chrome line stressed at +100V for 250s. The electric field configuration calculated by finite element analysis has been overlaid on the image as a vector matrix and as colored field strength contours. Key values of the field strength have been marked with figures.

reduction of the binding energy of surface atoms by an electric field is well known – it is used during molecular beam epitaxy to produce better quality films.)[5,6]

It may seem implausible that an atom in a solid metal surface could be rendered mobile at room temperature simply by applying an electric field, but recent advancements in scanning probe microscopy lend support to this interpretation. It has been reported that the atoms in a copper surface are in constant motion at room temperature, exchanging places in the surface matrix at a frequency of about $10^8$Hz by moving through surface vacancies with an activation energy of only 0.29eV.[7] A "surface vacancy" is simply a position in a regular arrangement of surface atoms that is unoccupied, and it is relatively easy for an atom in a neighboring position in the matrix to "hop" into such an unoccupied site, as the low activation energy shows.

To an atom at the edge of the chrome line in a reticle, the quartz surface appears to be just like a surface vacancy, so it is easy for the atom to move onto the quartz once its binding energy is reduced by an electric field. As atoms at the chrome edge move outward onto the quartz, this causes the formation of the chrome meniscus. This proposed mechanism even explains the meniscus' shape, as described previously.[2]

### *Chrome Migration Across the Quartz – EFM Type 2*

As the field strength gradually increases along the line edge, small beads are seen forming on the surface of the quartz at a distance of 250-300nm from the chrome line. The line of beads extends further from the chrome edge as the field strength increases until it reaches about 1 µm, where the surface beads become progressively smaller and more dispersed until above about 1e7V/m, at which point surface beads are no longer seen.

This indicates the onset of field ionization at the leading edge of the chrome meniscus. As the meniscus forms on the quartz surface, it accentuates the field strength which soon becomes high enough to strip an electron from a surface atom. Once an atom is ionized, it would experience a strong force repelling it from the chrome line. A stream of chrome ions would spread across the surface of the quartz and remain separated by the mutual repulsion of their positive charge until neutralized by a free electron from the quartz or the air.

Once an ion is neutralized, it would become stationary and able to merge with passing ions. Polarization of the stationary chrome atoms would make them attractive to migrating ions, resulting in formation of the beads in the AFM images. Hence, the

distance between the chrome line and the surface beads indicates the diffusion range of ions on the quartz surface before neutralization. Above a certain field strength, the migrating ions no longer coalesce. In this region there is chrome dispersed on the quartz but it has no topography, so is invisible to the AFM.

Ions that traverse the gap become neutralized on contacting the opposite chrome line, so they build up on the quartz surface like a beach in front of a cliff (Figure 5b). Opposite the spur line where the field strength is strongest, the film against the chrome border is continuous. Close inspection of the AFM data shows that this film is less than 1nm thick and in some areas it may be no more than a monolayer. Outside the gap where the field strength is weaker, the film becomes patchy as ions are neutralized and nucleate just before they reach the opposite chrome line, as shown in Figure 5c.

### *Chrome Migration on Chrome*

The upper surface of the chrome line is also modified by the electric field, with the surface becoming progressively smoother and swelling in the region with the highest field strength. Atoms clearly migrate on the chrome surface as well as on the quartz.

At about 2e7V/m, the outward extent of the meniscus reaches a maximum and at higher values of field, the meniscus is slightly narrower. This indicates the point at which the rate of ion emission from the edge of the meniscus exceeds the rate at which the ions are replaced by atoms migrating across the surface of the chrome. Hence, above this field strength the growth of the meniscus stabilizes and further changes to the line shape are mainly due to migration of chrome on chrome, which causes the line to swell.

The final shape of the surface under such high levels of electrostatic stress represents the lowest-energy surface profile. This is similar to the equilibrium of forces that leads to the formation of a Taylor cone in liquid metal field ion sources. For those who are interested in the mathematics, an analysis of surface shape modification by electrostatic stress has been performed by Bilbro.[8] While his paper does not relate directly to the geometry used here, the principles of surface shape modification by an electrostatic stress are universal and will apply to all electrode configurations and all materials.

## Conclusions

The experimental data have shown conclusively that chrome migrates on the surface of a reticle when it is exposed to an electric field. Sufficient field strength can be produced between submicron reticle structures with an induced potential difference below 1V. It has been shown previously that as reticle feature spacings are reduced it becomes easier for an external electric field to induce EFM and more difficult to induce ESD.[3] So, EFM is seen to be the primary electrostatic risk to today's reticles. Since EFM's onset threshold is more than two orders of magnitude lower than ESD, conventional ESD precautions are inadequate against EFM, and handling activities that did not previously expose reticles to ESD risk could be hazardous with regard to EFM risk.

Comparison of the rate of CD degradation by EFM with the CD budget of future technology nodes shows that EFM can exceed the entire lithography CD budget within just two seconds. EFM would be particularly damaging to subresolution scattering bars, which could become printable. Furthermore, EFM can continuously damage a reticle's CD during its operational life, so the damage will depend on a reticle's total electric field exposure history rather than the strength of the stress from an individual source as with ESD. This, and the fact that the fields that can cause EFM are much weaker than those that cause ESD, will make it more difficult to trace and eradicate the sources of any field problem. To make matters worse, the chrome film that migrates onto the quartz will attenuate and change the phase of the light passing through the reticle, so even in its earliest stages before line bridging, EFM has the potential to seriously disturb today's critical lithography processes.

When considering the need for reticle electrostatic protection, the rules have definitely changed.

## References


1. G. Rider, "Zero yield – the price of field-induced reticle damage"; Future Fab 22, pp. 62-64, January 2007; http://www.future-fab.com/content/PDF/FF22_wp_Rider_wp.pdf
2. G. Rider, "EFM: A Pernicious New Electric Field Induced Damage Mechanism in Reticles"; SEMATECH ESD Symposium December 2003; http://www.sematech.org/meetings/archives/other/20031212/index.htm
3. G. Rider, "Experimental quantification of reticle electrostatic damage below the threshold for ESD," SPIE Advanced Lithography, February 2008.
4. A. Wallash, L. Levit, "Electrical breakdown and ESD phenomena for devices with nanometer-to-micron gaps," Proceedings of SPIE Vol. 4980, pp. 87-96 (2003).
5. I. Derenyi, C. Lee, A-L. Barabási, "Ratchet Effect in Surface Electromigration: Smoothing Surfaces by an AC Field." Phys Rev Letts, Vol 80 No 7, p. 1473, February 1998.
6. D. Sengupta, D. Pavlidis, "Control of Semiconductor Epitaxy by Application of an External Field," DTIC, June 2003.
7. R. van Gastel et al, "Nothing moves a surface: vacancy mediated surface diffusion," Phys Rev Letts, Vol 86-8, pp. 1562 -1565, February 2001.
8. G. L. Bilbro, "Theory of Nanotip Formation," J Vac. Sci. Technol. B 20(3) (2002).


## *About the Author*


***Gavin Rider***

Gavin Rider is VP of technology and development with Microtome of Colorado Springs (www.microtome.com). He was previously product manager for material handling with ASML. Before that, Dr. Rider spent 15 years working in the surface analysis and plasma processing equipment industries, after graduating with a Ph.D. in surface physics from Southampton University, England, in 1981. ■


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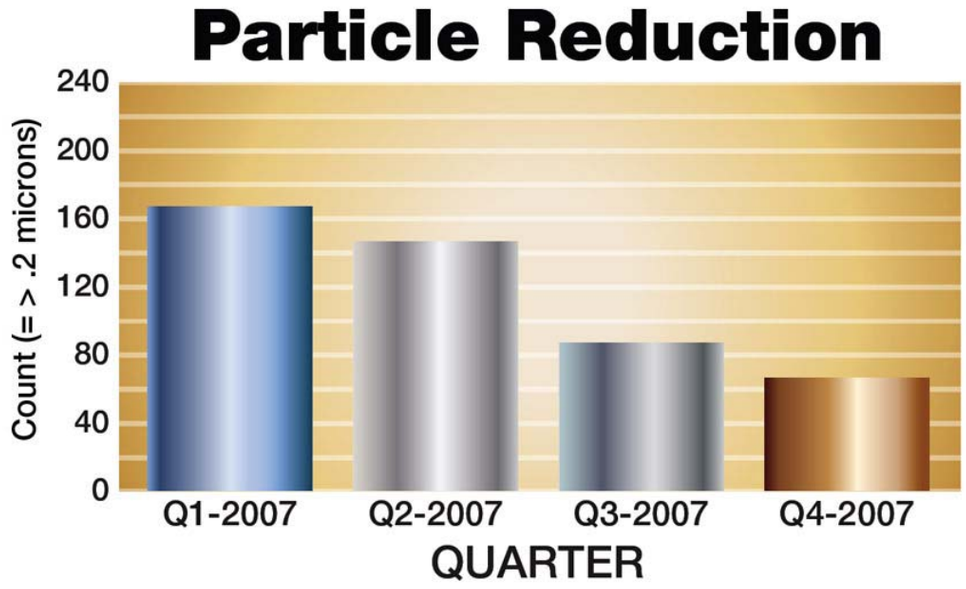
# When Other Graphite Materials Hit the Wall, Poco Graphite Breaks Through

Ten years ago, many people believed that graphite materials and their usefulness in semiconductor applications would soon hit the wall. Today graphite materials continue to be used as preferred component materials in many types of semiconductor manufacturing equipment.

In order to provide next-generation equipment that offers a technology advantage for its customers at an economic price, equipment manufacturers continually seek the best component materials and eliminate troublesome materials that reduce the uptime of equipment. Graphite, along with metals, was one of several component materials that industry experts predicted would not be able to meet the challenge of the new processes. Were their predictions wrong? Well, yes and no.




Advanced technology nodes and new materials have combined to increase the sources of defects that can negatively impact device yields.

## No, They Were Not Wrong

Some graphite grades have been eliminated as viable component materials due to unacceptable particle performance. In order to keep particles at an acceptable level, the preventative maintenance (PM) cycles had to be reduced. Poor performance of these graphite grades changed the economics of the equipment and processes.

## Yes, They Were Wrong

The continued development of super graphite grades, such as POCO ZEE®, extended the viability of graphite as the component material of choice. ZEE has allowed the PM cycle to be extended while maintaining acceptable particle levels. ZEE components allow the equipment manufacturers to satisfy the increasing demands for better particle performance from their end users.

ZEE was developed to solve production problems in implant systems caused by high part erosion and unstable beams which, in turn, lowered frequency of PM cycles. ZEE's exceptional performance is a direct result of its uniform microstructure and balanced physical properties. ZEE is a 1 micron grain size graphite with elevated hardness, greater strength values and good

You can clearly see how ZEE's ability to resist wear leads to less spalling or shedding of components and deposits in the chamber (left) when compared with a chamber using another material (right).

electrical properties. ZEE's ability to resist wear leads to fewer particles, even in the highest-energy environments. ZEE components enhance beam stability for extended machine up time and higher yields.

The development of POCO's unique ZEE grade produced a graphite that consistently exceeds the performance expectations for graphite components. This leaves some experts wondering if additional high-performance, semiconductor-grade graphites can be produced to meet new technology challenges. Graphite may eventually hit the wall unless there are continued material advances and development of new graphite grades. Most industry experts agree that new component materials will be required for 45nm production. Graphite may push through that wall or, perhaps, become part of another material system.

## New Material System

Silicon carbide, with its high thermal stability, process compatibility and wear resistance is one of the leading component materials that is being evaluated for next-generation equipment. Al-though there are several manufacturing methods for producing semiconductor-grade silicon carbides, the conversion process is proving to be unequalled in the production of complex, structural components. The silicon carbide material that offers the best balance of performance and cost will likely become the preferred material for next-generation components.

POCO draws on 40 years of research and development experience in graphite technology to design the best family of precursor materials for its unique conversion process that produces the high-purity SUPERSiC®, silicon carbide, Material System. SUPERSiC components outperform existing materials in overall throughput by increasing yields, reducing particles, improving plasma stability and exhibiting long part life for reduced cost of ownership.

This nontraditional conversion process allows complex machining to be done in the graphite state with minimal machining after the conversion to silicon carbide. Complex designs with thin walls and tight tolerances are as easy to produce as simple thin parts such as dummy wafers. These fully converted parts can then be subjected to a number of cleans, infiltrations and coatings in order to produce optimized silicon carbide components for specific applications.

The evolution of the design-to-manufacturing flow has necessitated a shift away from point tools to fully integrated solutions that can take into account a host of yield-limiting defect types and sources.

Unique to this conversion process is the ability to press fit multiple pieces into an assembly that can then be converted into a monolithic SiC component that can have internal pockets and channels. This ability creates maximum design flexibility.

This adhesiveless bonding process cannot be accomplished by any other silicon carbide manufacturing method. There are also several mechanical attachment methods for mounting finished silicon carbide components to other material structures.

## Moving Technology Forward

The possibilities are limitless due to the unique nature of POCO's chemical vapor conversion process and the favorable economics associated with customization of the final product.

Historically, POCO has been a market leader in specialty materials and materials research. This investment in leading-edge technology benefits its customers, whether they be OEMs or end users of POCO's products.

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*General Sales Manager*

**Phil Evans**
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**Poco Graphite, Inc.**
300 Old Greenwood Road
Decatur, TX 76234
Phone 940.627.2121
Toll-Free 800.433.5547
Fax 940.393.8366
info@poco.com
www.poco.com

**Poco Graphite, SARL**
1 rue des Vergers
69760 Limonest
France
Phone 33(0)472.520040
Fax 33(0)472.520049
Sales@poco-graphite.fr

**Poco Graphite, Inc.**
Shanghai Rep Office
Suite 1906
333 North Chengdu Road
Shanghai 200041
China
Phone 86.21.52980362
Fax 86.21.52980364
edm@poco.com.cn

**Jeff Wetzel**
Senior Member of the Technical Staff; SVTC, LLC

## The Interconnect Roadmap: Struggling to Make Progress?

The Interconnect low dielectric constant predictions incorporated in the ITRS road-map are a good example of overestimation of the pace of technology change in our industry. The predictions of the pace of change of low dielectric constant (low-k) materials were overly optimistic and were revised many times as different process technologies were evaluated for high-volume production. The development resources to implement low-k materials were spread over many consortia, universities, suppliers and IDMs. In phase with the development of low-k materials process technology, progress was made across a broad segment of material and equipment industry process technology products so that a stable dielectric constant through integration was achieved. Perhaps counting revisions is not the correct metric to measure progress when the scope and complexity of the change are unknown and communication between the resource holders is constrained?

The Interconnect Roadmap shows again that our industry faces a difficult challenge integrating Cu interconnect with smaller feature sizes. The issue is the effective interconnect metal resistivity increases as features are scaled to smaller dimensions. The effective resistivity is influenced by the resistivity, microstructure and feature size of the metals used to form the interconnect lines. Development resources to solve this problem are spread again over many, but fewer R&D partnerships. How will progress be made rapidly when communication is constrained and many pieces of information are needed to provide a solution?

The section's article focuses on one aspect of improving interconnect resistivity through the use of ALD/CVD methods to make thinner, conformal barrier layers for Cu damascene processing. It reports some promising new precursors for barrier and seed layer formation through ALD and MOCVD methods. Their efforts represent how progress to maintain the scaling demands of the ITRS Roadmap is borne by the material supplier segment of our industry. In their case, too, the challenge is more difficult since their process technology has not been widely adopted in production. As we consider the cost component of this development trend, it is also worthwhile to realize that equipment manufacturers are investing research dollars to extend PVD; e.g., sputter redistribution to improve barrier/seed conformality, reduce thickness and so improve resistance.

# Ultrathin Barrier/Seed Layers: Challenges of Scaling for Future Copper Interconnect

**Jeff Catlin, Jeff Roeder, Bryan C. Hendrix**
ATMI, Inc.

## Introduction

With the release of 45nm devices, there has been much attention focused around the challenges of scaling MPU devices and the use of high-k materials for gate dielectrics, marking one of the most significant FEOL changes in semiconductor process technology. In the BEOL, the very same challenges have been pushing the development and implementation of advanced interconnect. Starting with the introduction of Cu interconnect in the late '90s, the industry has focused immense effort on improving Cu interconnect process technology to keep pace with the ever-increasing demands of each tech node. The requirement for lower power consumption and high processing capacity has driven BEOL development. Introduction of ULK and even air gap ILD materials, combined with increased trench and via aspect ratios (A/R) are placing strain on traditional methods of producing the barrier/seed layers associated with Cu damascene integration. OEMs and device manufacturers are driven to examine alternative deposition technologies to address the extendibility of the incumbent PVD-based barrier/seed processes.

In this article, we will explore the scaling trends and subsequent process technology advances in ultrathin barrier/seed layers for Cu interconnect.

## Scaling Trends

Since the inception of Cu damascene, trench and via dimensions have aggressively scaled to keep pace with Moore's law and M1 $^{1}/_{2}$ pitches of 60nm or less are on the horizon as soon as 22nm.[1] To compound the difficulties of dimensional scaling, each node brings more and more Cu layers. The addition of more layers puts CoO stress on each process step in the Cu BEOL, so proposed technological solutions to new problems must be developed with ever-increasing economic pressure. The trend toward higher speed and lower power consumption has made a substantial jump in the last two-three years with the coming of age of high-k gate stacks. The jump in transistor per-

formance puts even more stress on the interconnect segment to manage RC delay for the future's ultrafast chips. The industry wants more layers, with better performance, for less money.

In managing RC delay, the industry has two paths to address. First is the C portion, which is related to the capacitance of the ILD and cap layers. Capacitance is defined as

$$C = k\frac{A}{d}$$

Where,
- k = dielectric constant of the ILD
- A = cross-sectional area of the dielectric
- d = the thickness of the dielectric film

Since A and d are driven smaller and smaller by the dimensional requirements of the device, it holds that k must be driven down. The ITRS roadmap indicates a reduction in $k_{eff}$ values by 0.2 to 0.3 per node. Advances in ILD films, such as porous low-k, require adjustments to the barrier/seed processes to maintain good adhesion, continuous films and provide an adequate barrier to Cu diffusion.

The other component of RC delay is the R, which is related to the resistivity of the conductor and barrier layers. Similar to capacitance, the resistivity is impacted by the shrinking dimensions of modern devices, defined by:

$$\rho = R\frac{A}{L}$$

Where,
- ρ = resistivity of the conductor materials
- R = V/I as defined in Ohms law
- A = cross-sectional area of the conductor films
- L = length of the line

As the bulk dimensions shrink, the interfaces of the barrier, seed and bulk conductors play a vital role in the management of R in the RC delay equation. ITRS has indicated that a resistivity target of 2.2μohms-cm must be met for Cu interconnect. This will require that barriers and seed layers become as thin as 4nm by the 22nm node.[1]

The factors stated above for RC delay management have remained fairly constant since 180nm. Incumbent processes of PVD barrier/seed and ECD Cu have provided the necessary process improvements to keep pace with the aggressive scaling trends. As we see the ramp of 45nm and the development of 32nm progress in the coming years, it is apparent that there are technological hurdles surfacing that warrant the evaluation of alternative processes for these critical interconnect steps. Current PVD processes for barrier/seed may well be approaching physical limitations.

## Current Technology

The mainstay of Cu damascene barrier/seed processes has been TaN/Ta. While TiN/Ti had been the contact barrier of choice for tungsten (W) contact, it was apparent early on that Ti-based barriers showed limitations due to the CMP requirements in the damascene barrier applications. The stacking of TaN/Ta was required to manage the adhesion requirements of the barrier to both dielectric materials and conductors. Additionally, since Cu does not direct plate to Ta metal due to oxidation, a seed layer of PVD Cu has been the process of record for damascene processes.

## Case for Change

PVD-applied TaN, Ta and Cu have been capable of meeting the scaling requirements for the last 12+ years of Cu interconnect. With each generation, we lurch closer to the physical limitations of PVD as a deposition technique for these materials. Much effort has been put into PVD technology advancements, such as iPVD and long-throw PVD to address the inherent necking issues with sputter deposition (see Figure 1). Cu interconnect requires uniform continuous diffusion barriers and seed layers, with adequate opening in the via and trench layers to facilitate ECD. While PVD equipment historically provides superior CoO to CVD or ALD (atomic layer deposition) processes, the development put into compensating for the "line of sight" behavior of PVD will quickly make PVD systems as complex and costly as CVD equipment. Additionally, as the metal $^1/_2$ pitch dips below 60nm, the lack of conformality of the PVD processes will impact the continuity of the barrier/seed layers as well as strain the filling capability of ECD (see Figure 2). Both of these issues are direct reliability concerns for device manufacturers.

Just as SiO2 gates were able to be extended much farther than most forecasts expected, it eventually became necessary to change from simple SiO2 to SiON to strained Si and eventually high-k. It is anticipated that the changes from PVD to ALD and CVD in the barrier/seed layers will undergo a similarly lengthy path.

The industry shift to a CVD-based barrier/seed will continue to be slow and the associated CoO impacts will warrant change only when the technical challenges are not able to be surpassed with the current process technology and materials. CoO for ALD processes can be as much as 3x the cost of a PVD process for the same film type, and depends heavily upon precursor sophistication and related cost.

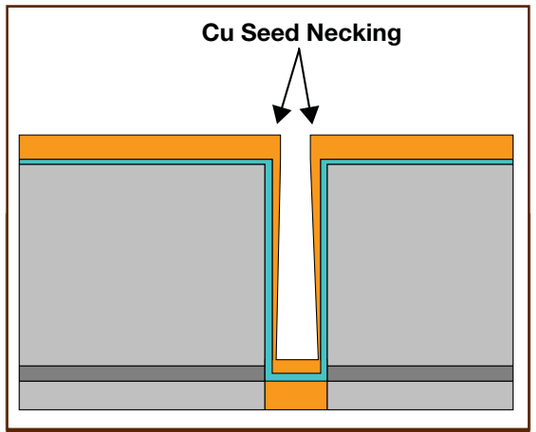


Figure 1. Cu Seed Layer Necking on Trench Pattern

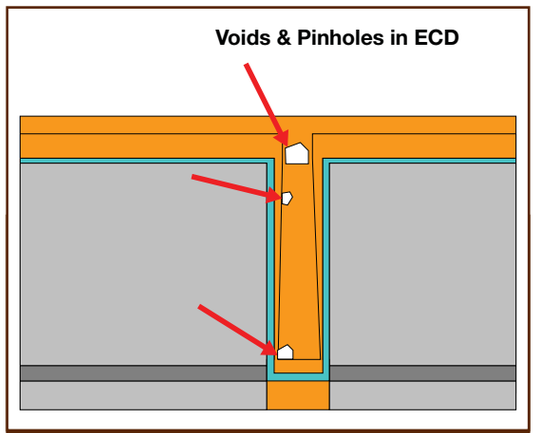


Figure 2. ECD Voids and Pinholes Resulting From Restricted Trench Openings

It is anticipated that the change path for barrier/seed will follow this type of cycle:

- Modification of current processes to maintain continuity of materials;
- Introduction of new process technology, again with continuity of materials; and
- Finally, a move toward new materials to address scaling issues.

We have seen the initial stages of this already in:

- PVD hardware improvements (i.e., iPVD, long throw) to address conformality and necking while maintaining the traditional TaN/Ta/Cu stack;
- ALD TaN has made advancements in recent tech nodes and is expected to be widely integrated at 32nm for at least M1. This change maintains the TaN/Ta/Cu stack, but introduces ALD to address conformality challenges in the barrier layer(s) related to shrinking dimensions and decreased barrier dimensions; and
- Interest in Ta & Ru (ruthenium) metal ALD as well as Cu ALD/CVD is aimed at allowing the interconnect dimensions to scale at the same pace while ensuring uniform coverage. CoO concerns are addressed through reduction of layer count (i.e., approaches such as direct plate TaN/Ru, eliminating Cu PVD).

## Advances in ALD/CVD of Barriers

As device dimensions shrink, processes with the ability to produce highly conformal films become a requirement. Chemical vapor deposition, an obvious choice as a conformal process, has limitations – among them, the ability to produce films of high enough purity for these applications. Pulsed CVD processes can allow the use of co-reactant schemes that produce purer films. ALD, a special class of a pulsed process where each process cycle produces a self-limiting ultrathin layer, offers the potential of extremely high conformality together with the environment for high-purity films.

As stated earlier, significant progress has been made in ALD of TaN films.[2,3] On the other hand, while sputtering of high-quality Ta is possible under good vacuum conditions, Ta metal is particularly challenging to produce by chemical vapor deposition methods due to its affinity for both oxygen and carbon. Tungsten has been proposed as an alternative, but has not seen widespread adoption as a Cu barrier. At the same time, and despite years of work, no published reports of a production-worthy Cu ALD process exists. This leaves a significant gap in replicating the well-known sputtered TaN/Ta/Cu stack with a highly scalable ALD process.

Alternative metal stacks have been proposed that include other noble metals, particularly Ru as a potential solution.[4] At first glance, Ru possesses highly attractive properties as a barrier/seed layer: It forms an oxide that is conductive, so adhesion will be good to dielectrics without forming an undesired insulating layer; it has lower resistivity as a bulk metal (~8 μΩ cm) than Ta (~12 μΩ cm); and it has little solid state miscibility with Cu (see Figure 3) The lower resistivity and good interfacial properties give Ru a significant advantage over Ta as features size stresses the total resistivity of the conductor stack. Although the Ru barrier is promising from a theoretical viewpoint, films composed of Ru/TaN bilayers have been reported to have improved barrier properties over Ru alone. [5] Other novel methods have been proposed to solve the barrier problem, including the use of Cu-Mn alloys for the interconnect that reportedly improve electromigration resistance and also strongly segregate to the outer surface of the interconnect, forming a barrier layer.[6] The problem of producing easily electroplatable layer remains, however. Direct plating on Ru appears viable,[7] as does the ability to produce good-quality metal films.[8] Although efforts continue on Cu ALD, one possible combination is a TaN/Ru stack to replace TaN/Ta/Cu.[5] ALD Ru on ALD WNC has also been investigated.[9]

## ALD/CVD Challenges

Development and implementation of materials for ALD/CVD has several challenges not present in PVD applications. In addition to material selection (i.e., Ta, TaN, Ru, etc.), when performing ALD/CVD, one must develop precursors and suitable delivery methods for these precursors. While ALD processes give the user enhanced flexibility over PVD processes, it is often difficult to obtain the same crystallinity from ALD that PVD can provide.[10] Complexity of process, equipment and materials adds significantly to any CoO baseline from PVD. Thus the technical hurdles must justify the expenditure.

In developing a suitable precursor for CVD of barrier materials, the following factors must be balanced in order to achieve high-quality films:

- The volatility and thermal stability of the molecule must be optimized to provide suitable vapor pressures for delivery

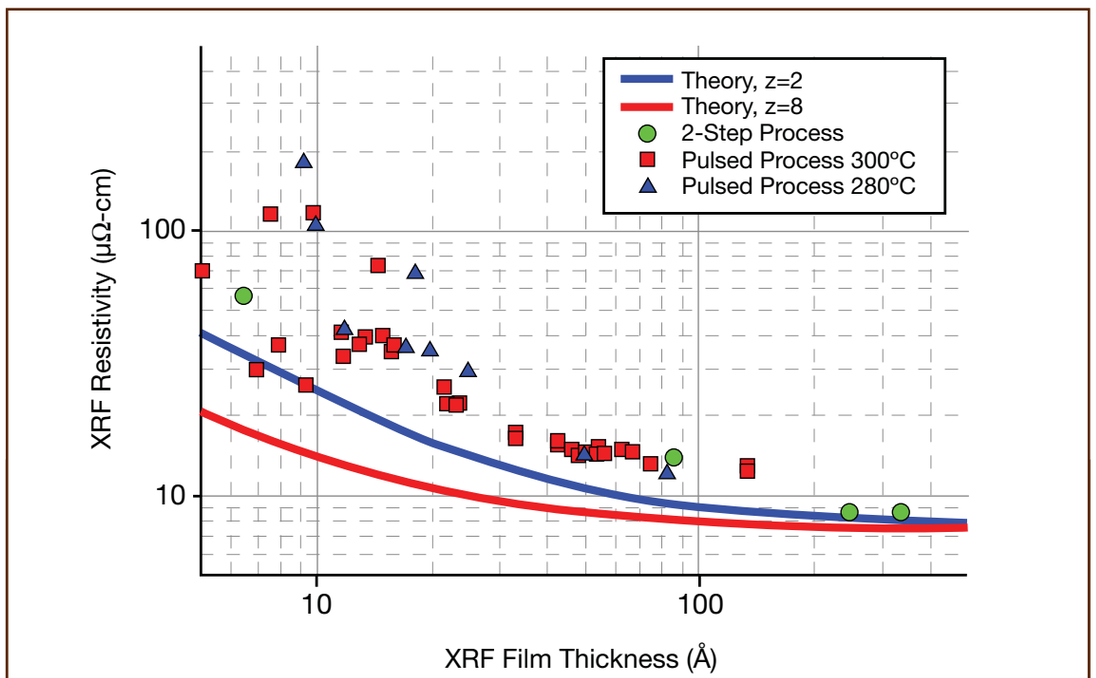


Figure 3. ALD Ru Resistivity (Ru(THD)3 Process)

while resisting thermal decomposition.
- The reactivity of the precursor must be suitable for the integration-based temperature restrictions of the process.
- For ALD, precursor screening must include surface adsorption optimization to avoid gas phase interactions prior to surface reaction.
- Ultimately, the combination of all these factors must result in wafer film properties that meet the parametric requirements for resistivity, uniformity, conformality and adhesion.

Two classes of precursor sources for ALD have been explored – volatile inorganics, e.g., $TaCl_5$, $TaF_5$, $Ta(NO)_5$; and metalorganic sources. The halide sources have low volatility, which makes obtaining appropriate flux for ALD challenging, but potentially represent a route to nitride without the potential for carbon incorporation. Metal-organic sources have much higher volatility, but the balance of thermal stability versus reactivity is tricky. In addition, highly reactive processes must be used to reduce carbon. ALD enables this approach. Choices for TaN precursors include pentakisdimethyl amido Ta (PDMAT), trisdimethylamidoamylimido Ta (TAIMATA), and others.[2,11] Novel delivery systems can help overcome the challenges of metalorganic thermal stability. Their utility has been proven to improve flux of low-volatility materials (e.g., $HfCl_4$) [12], and the lower temperatures afforded by these systems should mitigate any potential decomposition of metalorganic sources in delivery to the tool.

Chemical approaches can also be taken to improve stability. One remarkable example is an alternative TaN source, $\eta^2$-N,N′-dimethylethylenediamino-tris-dimethylaminotantalum (DEMAT). This molecule has virtually identical volatility compared to PDMAT, while showing higher thermal stability (see Figure 4). As such, it may offer the potential for higher-temperature ALD processes with improved film performance (conformality and purity).

Progress toward high-purity Ru films has been made using a variety of metalorganic precursors. Nucleation of the first layers of Ru can be quite challenging. One process that employs an oxidizing nucleation pulse has shown the ability to produce smooth, highly conductive Ru [13] (Figures 3 and 5). Although incompatible with a TaN barrier, the approach could be combined with other barrier approaches to create a viable stack.

## Conclusions

To keep pace with scaling requirements in Cu damascene, the semiconductor industry is exploring alternative solutions to PVD processes as well as novel materials in the barrier/seed applications. The transition from PVD- to CVD-based barrier/seed processes, most notably ALD have been explored, and manufacturable techniques are in existence today. The CoO demands placed on BEOL integration will continue to push existing technology to improve and resist migration away from proven technologies. During the next several years, advanced materials strategies will emerge that minimize the CoO impact and provide the necessary performance gains to warrant a migration to CVD-based processes.

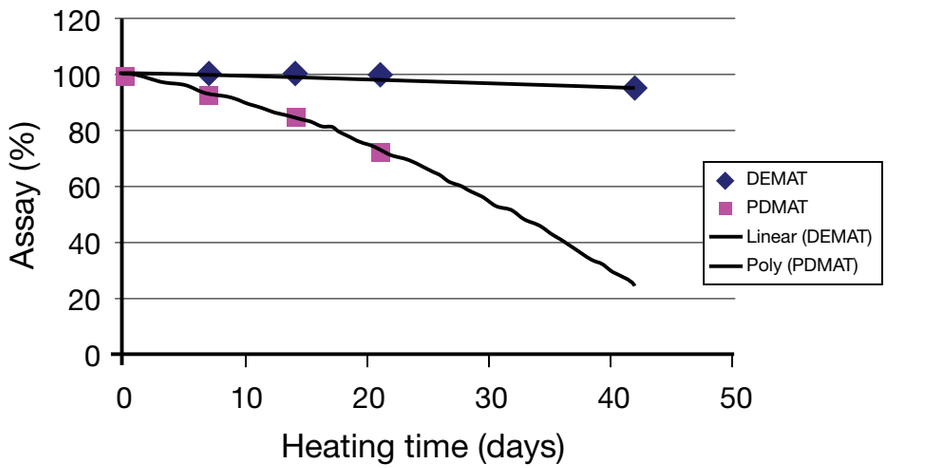


Figure 4. Thermal Stability of PDMAT vs. DEMAT

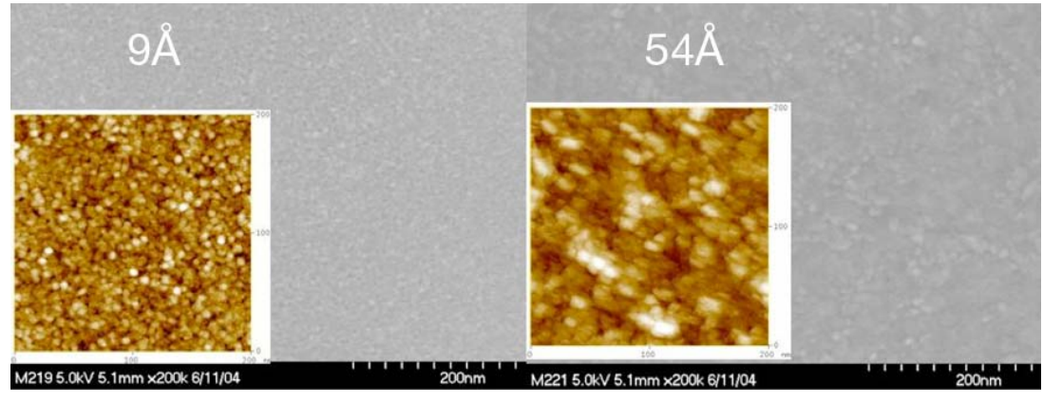


Figure 5. SEM and AFM of ALD Ru Showing Roughness Difference Between Thin & Thick Films

## References


1. ITRS 2007
2. H. Wojcik et al. "A Comparative Study of Thermal and Plasma Enhanced ALD Ta-N-C Films on SiO2, SiCOH- substrates, (2007) IITC, pp 19-21.
3. A. Furuya et al. "Low-resistivity atomic-layer deposited-TaN with ALD-TaN/PVD Ta Multilayer Structure for Multilevel Cu Damascene Interconnect, JVST A, vol. 24, pp 103-105.
4. S. Johnston, "Direct Plating of Cu on PVD Ru for Replacement of Ta(N) Diffusion Barriers, Proc. AMC, 2004, pp 335-340.
5. C.-C. Yang et al. "Physical, Electrical, and Reliability Characterization of Ru for Cu Interconnects," IITC (2006), pp 187-189.
6. J. Koicke et al. "Cu Alloy Metallization for Self-Forming Barrier Process, IITC (2006), pp 161-163.
7. T.P. Moffat et al. "Electrodeposition of Cu on Ru Barrier Layers for Damascene Processing, J. Electrochem. Soc, vol. 153, (2006), pp C37-C50.
8. J. Choi et al. Jap. J. Appl. Phys., vol. 41 (2002), 6852.
9. S.-M. Choi et al. Process Integration of CVD Cu Seed using ALD Ru Glue Layer for sub-65nm Cu Interconnect, VLSI Tech. Dig., (2004), pp 64-65.
10. Edelstein et al. IEDM (1997) p. 773; IITC (2001) p. 9; AMC (2001) p. 541.
11. Choi et al. "Characteristics of ALD-TaN Thin Films Using Novel Precursors for Copper Metallization, IITC (2003), pp 129-131.
12. M. Verghese et al. "Solid Source Design Impact on ALD," ECS (2005).
13. Hendrix et al. ECS Trans. vol. 11, (2007), pp 569-574.


## About the Authors


***Jeff Catlin***

Jeff Catlin is a technical marketing manager for ATMI. He received his B.S. in chemical engineering from Arizona State Univer-sity. In addition to product development, Jeff has 12 years of process integration experience at Intel and Tokyo Electron.

***Jeff Roeder***

Jeff Roeder is the director of Advanced Technology Development for deposition at ATMI. He has a Ph.D. in materials science and engineering from Lehigh University (Bethlehem, Pa.), and has focused on microelectronic materials for more than 20 years.

***Bryan C. Hendrix***

Bryan C. Hendrix is an advisory scientist at ATMI, where he has spent over 10 years developing ALD and CVD processes to deposit thin film materials for microelectronic applications. He received his Eng.Sc.D., M.S. and B.S. degees in metallurgy from Columbia University. Dr. Hendrix holds over 20 U.S. patents and has published over 60 papers. ■


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**Davide A. Lodi**
Wet Processes & Metrology Engineering Manager, Numonyx


"The need for speed" is not just my nephew's favorite Playstation game; nor is it a clause taken directly from the introduction of one of the papers. The "need for speed" is the imperative of our world, from its beginning. This imperative is inflected in different ways: from the technogeek who always wants quicker and more powerful PCs, to the big companies that flood the market with the latest-generation equipment immediately after I bought (darn!) the just-released, state-of-the-art mobile phone I was looking for, to the manufacturers that need to feed the supply chain, down to their facilities and design centers, in which "need for speed" translates into a large number of different concepts. One of them is cycle time: the quicker, the better, under all points of view (even financially, of course). Another one is taken at the bare subatomic level: To sustain all this "speed-chain," the properties of matter need to be modified to improve electrons' ability to move in a given direction... Yes, "need for speed" is our life, indeed!

This is what the following papers bring to our attention: Naot and Mohondro show us the benefits of adopting integrated metrology in our fabs. Of course, the main benefits are related to yield increase and process control improvement, but costs and cycle time are also in the number, and this goes back to our imperative once again.

Then, Chism and Vartanian introduce a new technique to measure silicon strain and other silicon properties, meeting precision and throughput (again...) requirements from ITRS roadmaps.

Enjoy reading (and, for a while, slow down and take it easy!)

METROLOGY, INSPECTION & FAILURE ANALYSIS

# Integrated Metrology Role in Improving Fab Productivity and CoO

**Ira Naot, Robert Mohondro**
Tevet Process Control Technologies

## Abstract

Using integrated metrology (IM) in semiconductor wafer processing can benefit wafer fabs in many ways. This article outlines the IM concept, discusses the requirements for a successful integrated metrology tool and outlines the benefits of using IM in terms of improved fab yield, improved process control, automated material handling system (AHMS) and metrology cost reduction, and fab cycle-time improvement.

## Integrated Metrology Concept

Integrated metrology means a metrology tool measuring some property of the product wafer is integrated into the process tool. A well-known example was a thickness measurement integrated into CMP tools in 0.25µm and 0.18µm node processes. At the time, CMP processes were an enabling technology, but were viewed as having poor process stability. Integrating a measurement module in the CMP tool, measuring thickness on every wafer immediately after the polishing step enabled wafer-to-wafer closed-loop control, and contributed to CMP process stability.

Present-day integrated metrology modules include layer thickness measurement for CMP, CVD and other dielectric deposition systems, optical-CD measurement in lithography or etch tools, and inspection tools for immersion-lithography top-coat tracks.

A typical setting of an integrated thickness measurement module on a multi-chamber CVD tool is shown in Figure 1.

In this setting, each wafer is taken from the FOUP (front-opening unified pod) to one of the vacuum load-locks and then to one of the process chambers. After the process, the wafer is taken to the load-lock. From the load-lock, the atmospheric robot takes the wafer to the metrology module, and from it, back to the FOUP.

In general, the requirements from a successful integrated-metrology module are:

- High throughput, to allow high sampling rate (preferably every wafer) without slowing down the process tool and hurting its productivity;
- High MTBF (mean time between failures) and low maintenance, avoiding any reduction in process tool availability;
- Low cost;
- Easy setup and calibration, good tool-to-tool matching. This is crucial for maintaining a large set of metrology tools, each monitoring one process tool; and
- Measurement sensitivity and repeatability suitable for process control of the processes of interest.

Tevet's Trajectory IT$^3$ is an integrated thickness-monitoring tool for integration with CVD, spin-on, etch or CMP process tools. Its unique design and algorithm allow monitoring of layer thicknesses on product wafers, with throughput of over 200 wafers/hour, scheduled maintenance of four hours per year and MTBF in excess of 10,000 hours. The Trajectory IT$^3$ costs about 10 percent of a typical stand-alone metrology system.

## IM Role in Fab-Yield and Process-Control Improvement

IM has two key advantages that enable gains in fab yield and process control. These are small measurement delay and high sampling rate. In process monitoring using a stand-alone metrology tool, most fabs measure two–three wafers out of each product lot. In contrast, an IM tool will usually measure every product wafer processed in the process tool it is mounted on. In terms of delay, the transport and queue time for a stand-alone measurement tool are usually 30 minutes or more. With high-throughput process tools processing up to 250 wafers/hour, this means a delay of 100 wafers. The IM, on the other hand, measures wafers immediately after process, so the delay, in terms of wafers, is reduced to the

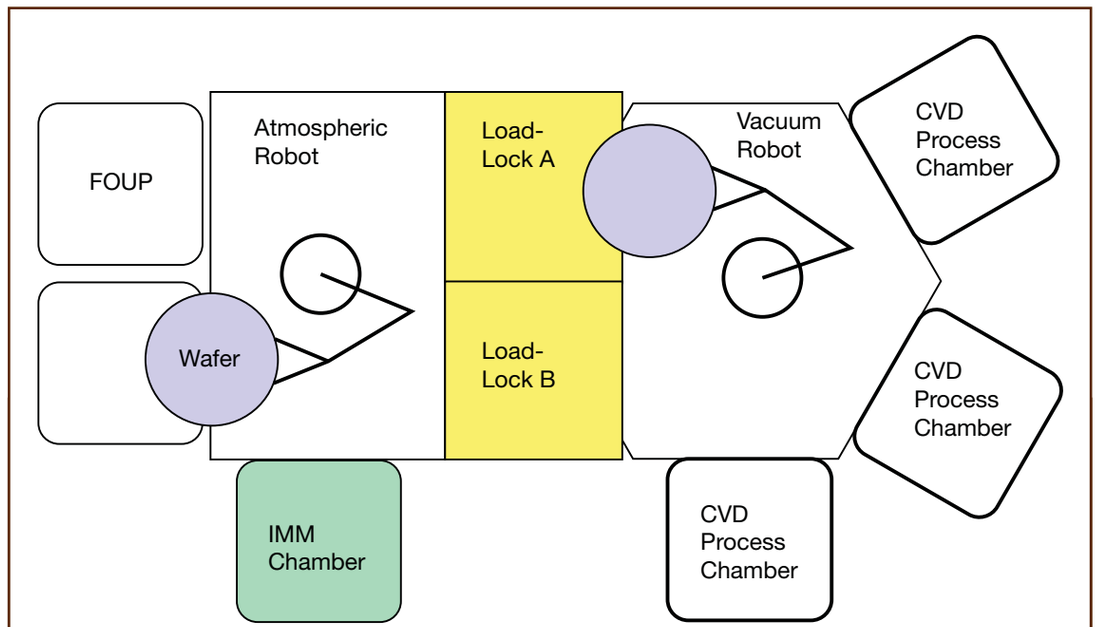


Figure 1. Integrated Metrology Module on a Multichamber CVD Tool

wafers already inside process chambers. In most tools, the delay will be one–two wafers, and in multichamber tools, up to six wafers.

One example of the advantage in using IM is in a spin-on dielectric process. The spin-on process suffers occasional bad-dispense events. These were mostly single-wafer events that resulted in out-of-spec thickness at the wafer center. Using Tevet's IM as process monitor enabled catching the out-of-spec wafers immediately after the spin-on process, as shown in Figure 2. This allowed a simple rework and saved wafer-scraps down the line. Using low-rate sampling in a stand-alone measurement would have meant missing many of these out-of-spec wafers. If the stand-alone measurement was not done immediately after the spin-on process, subsequent processing would have prevented rework, forcing the fab to scrap the affected wafers.

A second example is in a multichamber CVD tool, as shown in Figure 1. The use of every-wafer monitoring, combined with the IM sensitivity, allows a quick identification of chamber-to-chamber mismatch, as shown in Figure 3.

## IM Impact on Fab AHMS Cost and Cycle Time

In modern 300 mm fabs, all material handling is to be done by an automated material handling system (AHMS). The handling system moves all product wafers, in FOUPs to and from the process tools. In such fabs, the cost of the AHMS is very significant; some industry sources [1] estimate it at 4–5 percent of total fab construction cost. If the expected life span of the fab, at full capacity, is five years, then the AHMS cost per wafer move (taking construction cost alone) is over 8 cents.

In many production flows, the processing step is followed by sending the wafers to an inspection or a metrology step. After processing, each lot is transported to the metrology tool where a sample of the wafers (usually two or three) are measured or inspected. Each measurement requires an AHMS move for transporting the wafer to and from the measurement tool, as shown in Figure 4a. If an integrated metrology module (IMM) is used instead of the stand-alone tool, the AHMS move to the measurement station is saved, as shown in Figure 4b.

If an IMM is installed on a process tool processing 50 wafers per hour, the saving in reduced AHMS moves is over $30K per year. New process tools have ever-higher throughput, so a single tool requires more AHMS moves. If an IM is installed on a high-throughput tool, processing 150 wafers per hour, the savings in reduced AHMS moves is more than $90K per year for one tool equipped with IMM. This brings ROI for the IM to under two years.

Another aspect of the interaction of AHMS with metrology tools has to do with the traffic to and from the stand-alone measurement tool. Modern measurement tools may process over 50 wafers per hour in "production-monitoring" mode. Due to their high throughput, stand-alone metrology tools are usually designated for monitoring multiple

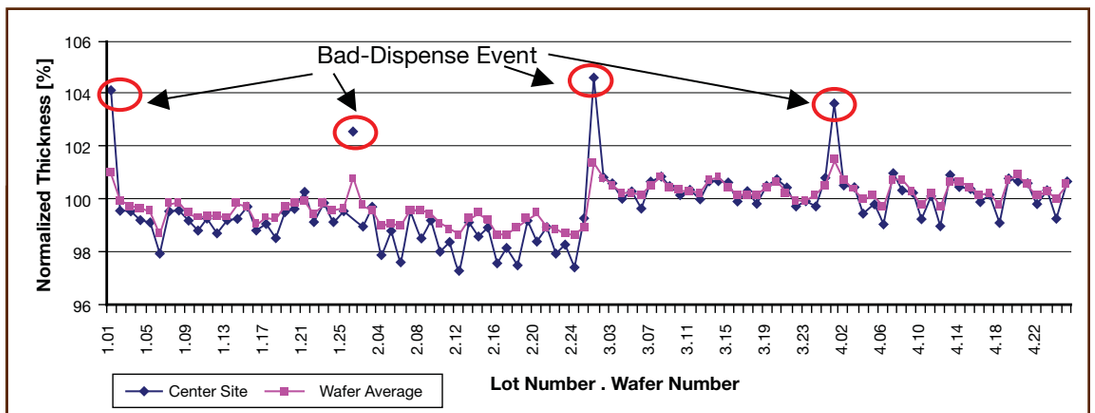


Figure 2. SOD Process-Monitoring Results

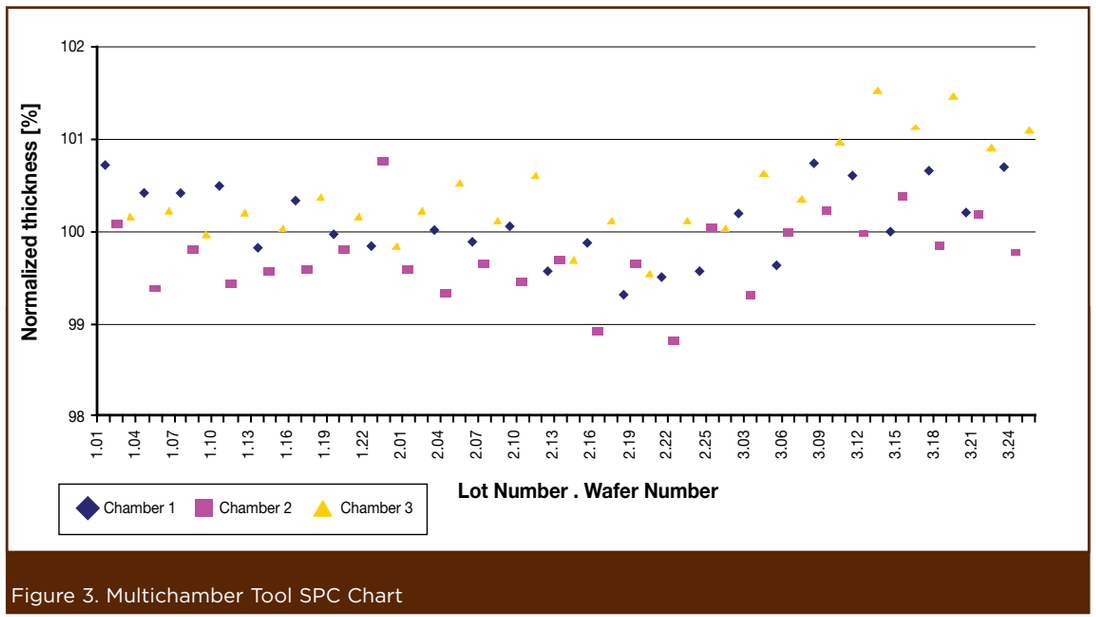


Figure 3. Multichamber Tool SPC Chart

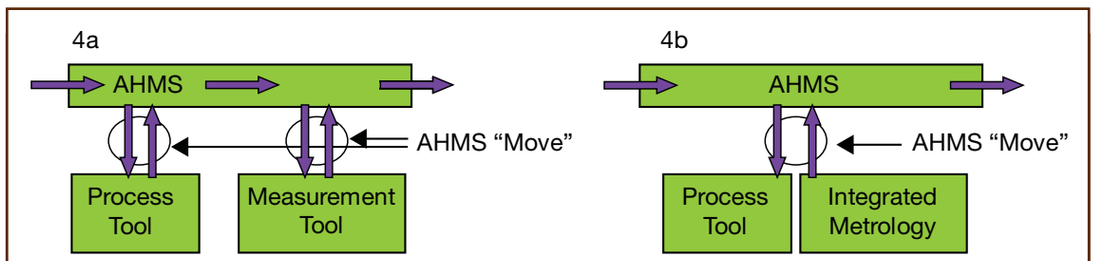


Figure 4. a) Process Tool With Stand-alone Monitoring, and b) Process Tool With Integrated Monitoring

process tools in sampling mode. To realize the metrology tool full potential in a monitoring scheme, where the sampling is two–three wafers per lot, the AHMS has to transport to and from the measurement tool 20 FOUPs or more each hour. Such heavy traffic is a challenge to any AHMS. To overcome this localized "traffic jam," the AHMS requires costly additions at the stand-alone metrology tool. In addition, this traffic jam causes cycle-time increases at the metrology step.

## IM Impact on Metrology Tool-set Cost

Using integrated metrology tools instead of a stand-alone tool requires installing an IMM on every process tool. In contrast, one stand-alone tool may monitor several process tools. Leading-edge stand-alone optical thickness measurement tools cost over $1.8M. Such measurement tools are the tools of choice for engineering analysis or process development work. In contrast, the Tevet Trajectory T$^3$ IMM costs about 8 percent of a stand-alone tool, and is suitable for monitoring most dielectric layers used in wafer processing.

Table 1 compares the cost of equipping a group of process tools with stand-alone measurement tools versus equipping them with integrated metrology.

If we assume each product lot has to be sampled by the measurement tool, IMM-based monitoring is the lower-cost option. In a high-throughput tool set, this tendency is even more pronounced. The proper strategy is obviously using IMM for process monitoring wherever possible, and limiting the use of stand-alone metrology tools to the in-depth process analysis in which they excel.

| Example | A | B | C |
|---|---|---|---|
| Process tool throughput [Wfr/Hour] | 50 | 100 | 150 |
| Measurement tool throughput [Wafers/Hour] | 50 | 50 | 50 |
| Single IMM cost (normalized to stand-alone measurement tool cost) | 8% | 8% | 8% |
| Stand-alone tool sampling | Every lot, 3 wafers/lot | Every lot, 3 wafers/lot | Every lot, 3 wafers/lot |
| Process tools monitored by one stand-alone measurement tool | 8-9 | 4-5 | 3 |
| Cost of equipping every process tool with IMM (normalized to stand-alone tool cost) | 64-72% | 32-40% | 24% |

Table 1. Monitoring-Tool Costs Comparison

## Conclusion

Many aspects of fab operation can benefit from using IM: Process yield and process control can benefit from the high sampling rate and quick feedback; AHMS costs are cut by reducing the number of wafer moves needed; and cycle time is reduced. In addition, using Tevet's Trajectory IT3 offers a low-cost alternative to process monitoring based on stand-alone tools.

## Reference

1. SEMI International Semiconductor Strategy Symposium 2008 Proceedings

## *About the Authors*

***Ira Naot***

Ira Naot has B.Sc and M.Sc degrees in chemical engineering from the Technion-IIT. His Work experience includes over 12 years in various positions in the semiconductor industry, including process engineering, equipment engineering and maintenance, and process integration. Ira is presently an application engineering manager in Tevet Process Control Technologies.

***Robert Mohondro***

Robert Mohondro has over 30 years of management, process engineering equipment and marketing experience in the semiconductor industry. He is presently a senior application engineer in Tevet Process Control Technologies. ■

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# Industry Sub-Cycles Spark Diversity

## IC Industry Cycles

Through 2004, IC industry cycles could be labeled as generally either "up" or "down." Since then, device manufacturers have been concentrating more on the products they know best, and this one big cycle is fracturing into individual product sub-cycles.

As product technologies, DRAM/Flash, MPU, Foundry/Logic and Analog can be in different cycles of the pie chart below, and can show relative strength or weaknesses, depending on the market (pie chart on opposite page).

For a capital equipment company tied into one technology niche, a shift downward in a sub-cycle can have a significant impact on their business model.

## Diversity Is Key

So diversity is key. One equipment technology must be able to work for many different product applications.

Jordan Valley's novel, noncontacting, nondestructive X-ray technologies enable the power and flexibility to develop current- and next-generation materials and processes across a wide variety of applications.

## Technology Drivers

Technology drivers that are propelling Jordan Valley into diversified market segments include:

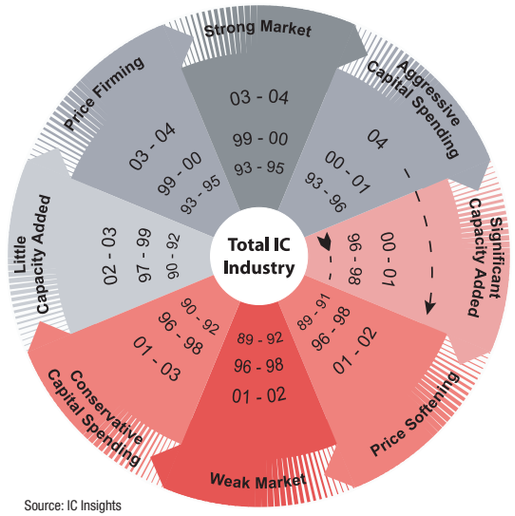
- Copper in flash
- High k gate stacks in DRAM (and the pending adoption of copper)
- Metal gates, high k and Cu in logic
- WLP and UBM (under bump metallization) technologies

## X-Ray Metrology for Thin Film Measurement

Jordan Valley provides X-ray metrology for thin film measurement applications in:

- Copper seed barrier
- Copper CMP
- Silicides
- Other FEOL processes (advanced gate stacks, high k, ONO, HAH or ZAZ, SiGe, metal gates, organic ARCs, advanced resists, SOI
- Other BEOL processes (low k dielectrics, Cu ECD, top barriers, aluminum processes, UBM, Flip Chip/WLP)

The IC Industry Cycle (Up Through 2004)




Source: IC Insights

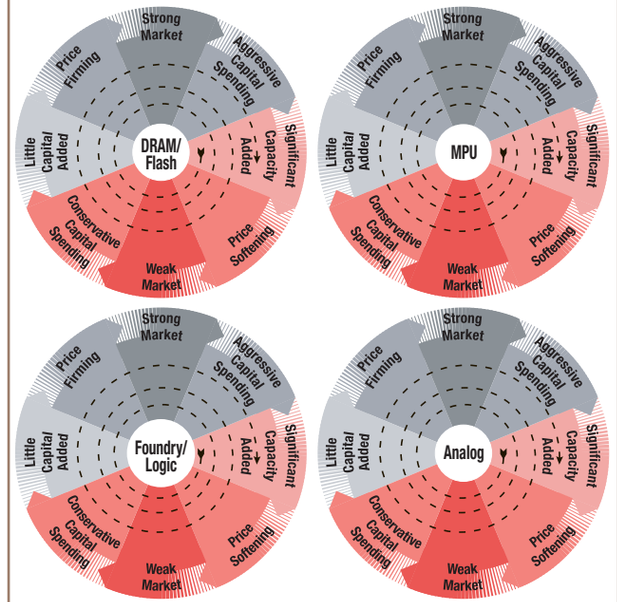
Jordan Valley sets the standard for extendibility, versatility and cost of ownership. With the improved CoO of the model JVX6200i, Jordan Valley can now deliver a viable tool for the Foundry segment. And with the explosive growth in high-density, high-pin-count devices that necessitate the more sophisticated types of WLP, Jordan Valley now offers advanced metrology for packaging.

Delivering unmatched speed, resolution and precision for all film types. Delivering tools to all product market segments – DRAM/Flash, MPU, Foundry/Logic, Analog and WLP.

That's why we have been recognized as:

- Deloitte Technology's Fast 50 – 2006 & 2007
- Semiconductor International's Best Product Award – 2005

The IC Industry Sub-Cycles (Post 2004)

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METROLOGY, INSPECTION & FAILURE ANALYSIS

# A New Photo-Reflectance Approach to USJ and Strain Metrology

**Will Chism[1] and Victor Vartanian[2]**
[1]Xitronix Corporation, [2]International SEMATECH Manufacturing Initiative

## Abstract

This paper is the first of a two-part series which describes the use of a new photo-reflectance technique for the in-line characterization of strain and USJ dopant activation in advanced FEOL processing.

## Introduction

The introduction of strain in the transistor channel and new USJ annealing techniques has created a very high-priority need for new high-speed precision metrology capabilities. The 2007 ITRS establishes a new line item for in-line stress metrology with a measurement resolution of 50MPa and a throughput of two wafers per hour at 25 sites per wafer. Industry consensus is that XRD and Raman spectroscopy can meet the resolution requirement but are deficient in throughput. Additionally, the 2007 ITRS sets forth a near-term USJ dopant concentration precision target of ~2-4 percent across the concentration range. This requires significant improvement over existing methods.

Xitronix Corp. has pioneered a new nondestructive photo-reflectance approach which meets or exceeds the strain resolution and dopant concentration precision requirements set forth in the 2007 ITRS, and which provides throughput of approximately an order of magnitude greater than Roadmap requirements. In this first part, the principles of the Xitronix approach are described along with results of proof-of-principle measurements, followed with initial estimations of strain and active dopant measurement resolution.

## Principles of Photo-Reflectance Measurement

Due to their extreme sensitivity, modern photo-reflectance techniques are ideal for applications requiring measurement of electronic performance of semiconductor nanostructures. In the typical photo-reflectance (PR) setup, a pump laser beam is used to periodically modulate the carrier density in a semiconductor sample, which in turn induces a periodic variation in the reflectivity of the sample. The variation in reflectivity is due to the modulation of one or more physical quantities such as internal electric fields, interband transition energies, and/or temperature. This reflectivity modulation is then recorded by phase-locked detection of a coincident probe light beam.

The PR metrology technique pioneered by Xitronix attains sensitivity to the active electronic properties of Si nanostructures by using a probe wavelength near the "$E_1$" interband transition in Si. In the vicinity of such a transition, the induced change in reflectivity is proportional to the third derivative of the semiconductor dielectric function. This derivative is large only nearby strong optical absorptions in the semiconductor band structure, and therefore may isolate these features with great precision. This is what allows the PR technique to precisely measure strain in nanoscale strained silicon layers, for example, since the Si $E_1$ transition energy undergoes a known shift under strain. A simple way of estimating the sensitivity of PR to strain in Si is to compare the known shift of the Si $E_1$ interband transition, under target strain values, with the known capability of PR to resolve said transitions. These values are ~100meV and ~4meV, respectively, which would imply a strain resolution of ~0.04 percent, or ~40MPa. Nearby to these strong optical absorptions, the amplitude of the PR response also has excellent sensitivity to electric fields in activated silicon transistor channel regions. In fact, the amplitude of the PR signal is typically two orders of magnitude larger than the thermally modulated optical reflectance signals achieved in conventional implant monitoring systems. Moreover, by reason of the fact that the PR signal is highly sensitive to the near surface crystallinity, it may be

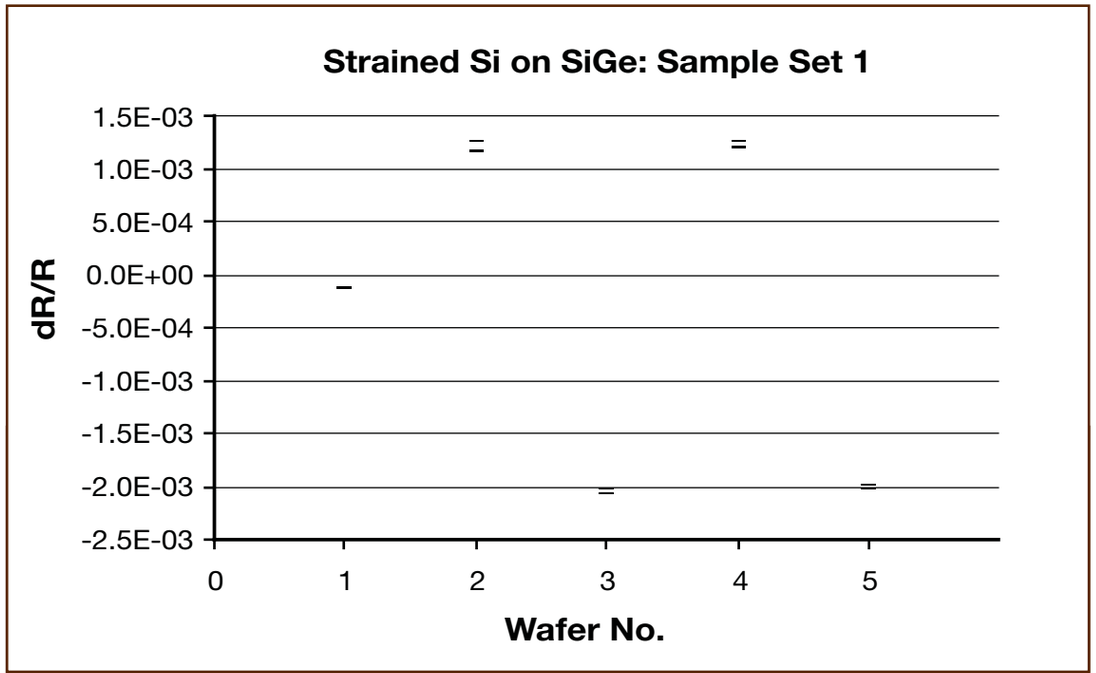


Figure 1. PR Signal Obtained From Ultra-thin Strained Si Layers on SiGe, Plotted for Each Wafer in S-Si Sample Set 1

used to precisely measure activated dopant in Si transistor channels.

## Characterization of Strain in Nanometer Scale Si Layers

As mentioned, the principle underlying PR measurement of strain is the characterization of certain interband transition energies in the semiconductor band structure. Now, for a given interband transition, a probe beam wavelength situated on either side of the transition will exhibit a different sign of the PR response, i.e., the sign of the change of reflectivity will change with respect to the pump phase. Thus, by selecting a monochromatic laser probe beam with wavelength near the Si $E_1$ transition, the phase of the PR response will be very sensitive to strain. Accordingly, the Xitronix 200 mm automated platform was configured with a probe wavelength of 375nm. Other details may be found elsewhere; however, it is worth noting the measurement times are typically 1 second or less, leading to throughputs easily above 20 wafers per hour at 25 measurements per wafer.

In order to perform proof-of-principle experiments and initial capability assessment for strain, ISMI generated two sample sets containing blanket strained-silicon layers on silicon-germanium substrates. S-Si sample set 1 contained five wafers: an unstrained silicon substrate; two unstrained silicon-germanium substrates (18.5 percent Ge); and two wafers with nanometer scale strained silicon films of approximately 6nm thickness on top of unstrained silicon-germanium substrates (18.5 percent Ge). S-Si sample set 2 contained eight wafers, each comprising nanometer scale silicon films on SiGe substrates, with variations in top silicon thickness and Ge concentration.

Figure 1 shows the XP450 data taken on S-Si sample set 1. Each pair of bars represents the ±1 standard deviation of 100 measurements taken along a 200 micron line. Wafer No. 1, the unstrained silicon substrate, shows a negative PR signal of roughly $-1x10^{-4}$. Wafers Nos. 3 and 5, the unstrained SiGe substrates, also show negative PR signals of around $-2x10^{-3}$. However, wafer Nos. 2 and 4, the wafers with top silicon of approximately 6nm, show PR signals of opposite sign. Since the PR spectra is a linear superposition of the response from the top silicon film and the relaxed SiGe layers, we may conclude that if wafer Nos. 2 and 4 contained unstrained top silicon, the PR response of these wafers must be negative as well. Therefore, the positive PR signals seen for wafer Nos. 2 and 4 correlate to the presence of strain in the top silicon.

Figure 2 shows the XP450 data taken on S-Si sample set 2. Wafer Nos. 1, and 5-8 each show negative PR signals of magnitude ~$1-3x10^{-4}$. However, wafer Nos. 2, 3 and 4 show PR signals of opposite sign, with magnitude ~$5-9x10^{-4}$. The positive PR signals correspond to wafers with top silicon film thicknesses of approximately 10nm or less, while the negative signals correspond to films of thickness approximately 20nm. This implies that for S-Si sample set 2, the strain becomes relaxed when the top silicon thickness exceeds its critical value between 10nm and 20nm. The estimated strain measurement resolution is 20MPa or better. These proof-of-principle results suggest the PR approach pioneered by Xitronix is effective for process control of strain in nanometer scale silicon films.

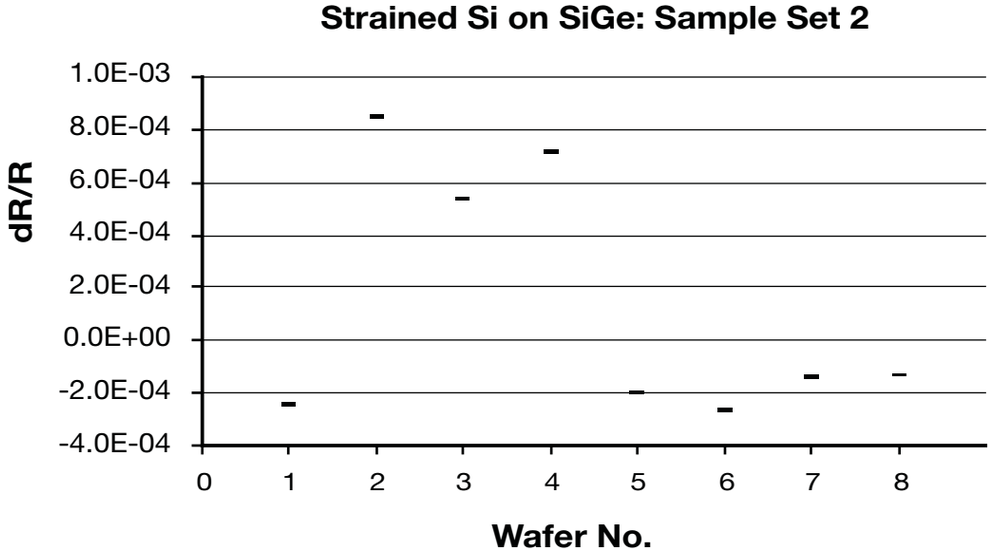


Figure 2. PR Signal Obtained From Ultra-thin Strained Si Layers on SiGe, Plotted for Each Wafer in S-Si Sample Set 2

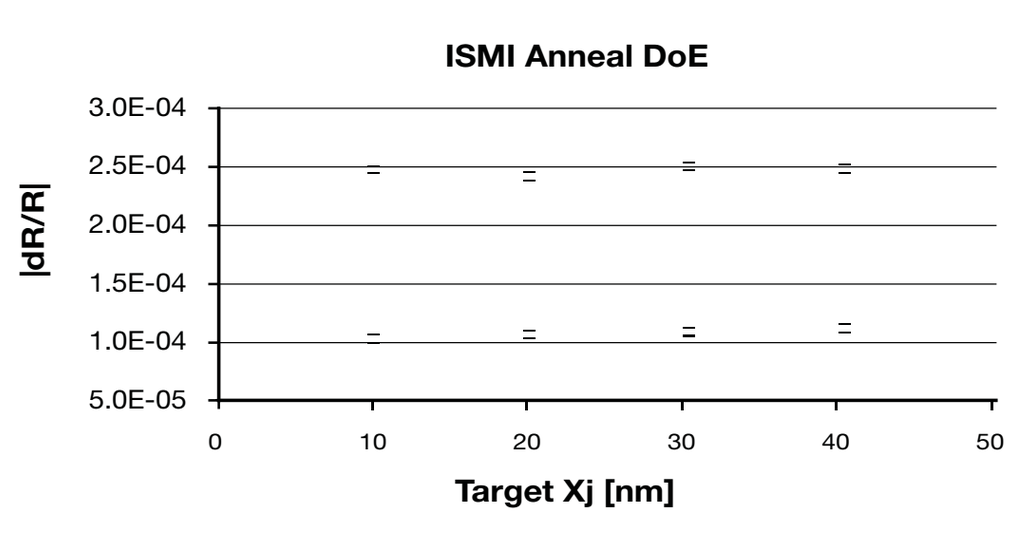


Figure 3. Modulus of the PR Signal Obtained From Nanometer Scale Active Layers in Si, as a Function of Ultra-shallow Junction Depth

## Characterization of Active Dopant in Ultra-Shallow Junctions

In order to perform proof-of-principle experiments and initial capability assessment for active doping levels in USJs, ISMI generated a set of arsenic-implanted silicon wafers with varying implant dose and implant energies. The implant ion energies were varied to provide four implant depths of approximately 10, 20, 30 and 40nm. Each target depth comprised dose splits of approximately constant doping concentrations of $10^{18}$ and $10^{20}$ atoms/cm$^3$. Finally, an anneal resulting in maximal activation was performed. Figure 3 shows the modulus of the PR signal for the annealed samples, as a function of junction depth. For each junction depth, the modulus of the PR signal demonstrates excellent sensitivity to active dopant concentrations under investigation. It may also be seen that the data is again highly reproducible – each pair of bars represents ±1 standard deviation of 100 measurements taken along a 200 micron scan.

Figure 4 shows the results of short-term precision testing of the Xitronix 200 mm automated platform on the ISMI samples. The annealed sample with the ~20nm junction depth and the 2x$10^{14}$/cm$^2$ dose was loaded into the tool, a 100-site measurement performed, and then unloaded. This cycle was repeated a total of five times. The repeated measurement scans provide the measurement repeatability, while the load/unload cycles provide an approximation of the reproducibility. The overall PR measurement precision may then be estimated, yielding a relative precision of ~2 percent. This provides an estimation of the smallest detectable change in dose at the target value, and which precision satisfies the requirements for dose control stated in the 2007 ITRS.

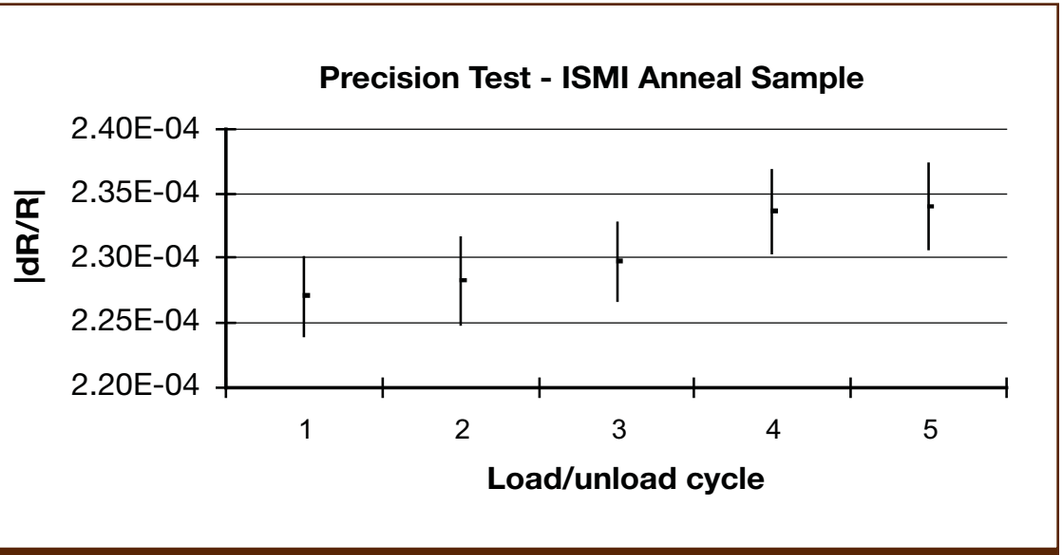


Figure 4. Precision data from the Xitronix 200 mm automated tool obtained on 20nm active layers in Si doped at 2x$10^{14}$/cm$^2$. Estimated relative precision is ~1.93 percent.

## Conclusion

The Xitronix PR approach has demonstrated sensitivity and precision suitable for process control of strain in ultra-thin strained Si layers and activated dopant in ultra-shallow junctions, and hence holds great promise as an enabling technology in FEOL manufacturing. Further work is under way with ISMI to establish correlations with analytic measurement techniques and transistor performance.

## About the Authors

***Will Chism***

Dr. Will Chism is CTO of Xitronix and the inventor of Xitronix's photo-reflectance technology. He has a Ph.D. in physics from the University of Texas at Austin and is the author of approximately 25 scientific publications and patents.

***Victor Vartanian***

Dr. Victor Vartanian is currently the films metrology program manager at ISMI. He was at Motorola/Freescale from 1997 to 2007. Victor holds B.Sc. and Ph.D. degrees in chemistry from the University of Texas at Austin. ■

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**Peter Ramm**
Head of Dept., Si Technology, Fraunhofer IZM, Munich

## Chip design and material already "perfect" for 3D IC production?

3D system integration is a promising and more and more accepted approach for fabrication of high-performance applications as advanced processors, memory stacks and image sensors, as well as so-called "More than Moore" applications, focusing on smart system integration rather than transistor density (e.g., wireless sensor systems, "e-CUBES"). In the near future, wafer-level-based die stacking technologies using thinned chips and through silicon vias will be introduced into production. But there are still enormous challenges for the fabrication of 3D ICs: On one hand, such technological issues as reliable and cost-effective fabrication of thin dies (thinning, dicing, handling etc); on the other hand, such 3D design tasks as modeling and simulation – the design process of high-performance 3D ICs must take into account the influence of the corresponding manufacturing technologies on the system behavior. The articles included in this section are dealing with these production challenges.

Peter Schneider is head of department for Heterogeneous Systems at Fraunhofer IIC in Dresden. His co-authors Sven Reitz, Roland Martin and Jörn Stolle are serving the Design Automation division with modeling and simulation research. Their article is targeting design support and major output design guidelines for 3D integrated systems, introducing a modular modeling approach that covers detailed simulations of thermal and electromagnetic effects.

The "Perfect Chips" article by Peter Heinze, Martin Amberger and Therese Chabert is underlining the importance of stress relief after dicing for fabrication of advanced 3D packages and is referencing the corresponding early R&D work of Infineon and Fraunhofer IZM Munich. Their company, PVA TePla, introduced a stress relief step after dicing of thinned chips in addition to the conventional relief after wafer back-side grinding with the advantage of healing the crucial chip-sides too (so-called five-side restoration).





# Modeling and Simulation for 3D Design Support

**Peter Schneider, Sven Reitz, Roland Martin, Jörn Stolle**
Fraunhofer Institute for Integrated Circuits, Design Automation Division

## Abstract

Due to high-integration density, the influence of manufacturing technologies on the system behavior must be considered in the design process of 3D systems. Therefore, information from different physical domains must be provided to designers. The variety of structures and physical effects requires efficient modeling approaches and simulation algorithms. The following describes a modular approach which covers detailed analysis with PDE solvers and more abstract behavioral modeling.

## Introduction

New technologies for three-dimensional integration of ASICs or microcontrollers, sensors, power supplies and energy harvesters, as well as wireless communication devices, enable a wide range of new system concepts and form factors, e.g., for sensor networks or ambient intelligence applications.[1] Due to the dense integration of different functional blocks, a variety of physical interactions within the 3D system must be considered, preferably early in the design process. Basically, parasitics of semiconductor devices, the electrical behavior of interconnects, thermal management within the stacked structure, as well as thermomechanical effects, must be investigated to meet requirements concerning high system performance and reliability.[2,3]

Within the design process of integrated circuits, mostly on-chip interconnects are considered today. Using field solvers which are integrated in commercial design environments, an extraction of parasitic RLC values is performed. For digital circuits, these values are provided using dedicated data formats like SPEF or DSPF and used for timing and crosstalk investigations. Thermal effects as well as EMC are usually considered after IC-design.

## Modular Modeling Approach

The variety of structures and effects of different physical domains require efficient modeling approaches and simulation algorithms as key methods to solve several problems in this field. Therefore, an appropriate methodology is required for multi-level and multiphysics analysis of interconnect structures. The main idea is to carry out analysis on one level of abstraction and use the output for optimizing on the same level and as an input for modeling on the next level. For instance, performing electrostatic and electromagnetic calculations of single vias and local interconnect structures in the RF domain using PDE solvers, parasitic circuit elements like resistors, capacitors, and inductors can be

extracted and later used to derive behavioral models for system-level simulation. PDE solvers are also applied to investigate the thermal behavior of local interconnect structures and the stack assembly and to derive behavioral models. Electromagnetic and thermal behavioral models can be combined with the electrical model of the entire system to enable the complete system simulation considering the effects mentioned above.

Our methodology is based on a modular modeling approach which will be illustrated by thermal investigations of a stacked pressure sensor microsystem as an example (Figure 1).

We are aiming at a tool-independent structural representation using XML and a semi-automatic generation of models for PDE solvers. The basic idea is to generate parametric models of basic structures, which can be modified concerning geometrical and material properties as well as the element type of the PDE simulator, which represents different physical effects (in this case thermal ones). Complementary, network and behavioral models (SPICE, VHDL-AMS, Verilog-AMS) for electrical and thermoelectrical simulations are also provided for these basic structures.

These parametric models, so-called basic modules, are stored in a library and can be used to build up a model of the complex stacked system. In this case, we have developed basic modules for the three chip layers, interchip via in chip 3, hollow tubes, tracks, pads, and different interconnect technologies between chip 2 and 3. These structures are realized using SLID (solid liquid interdiffusion), Au-Stud Bumping or Micro-Flip-Chip. Exemplarily, some of these basic modules are shown in Figure 2.

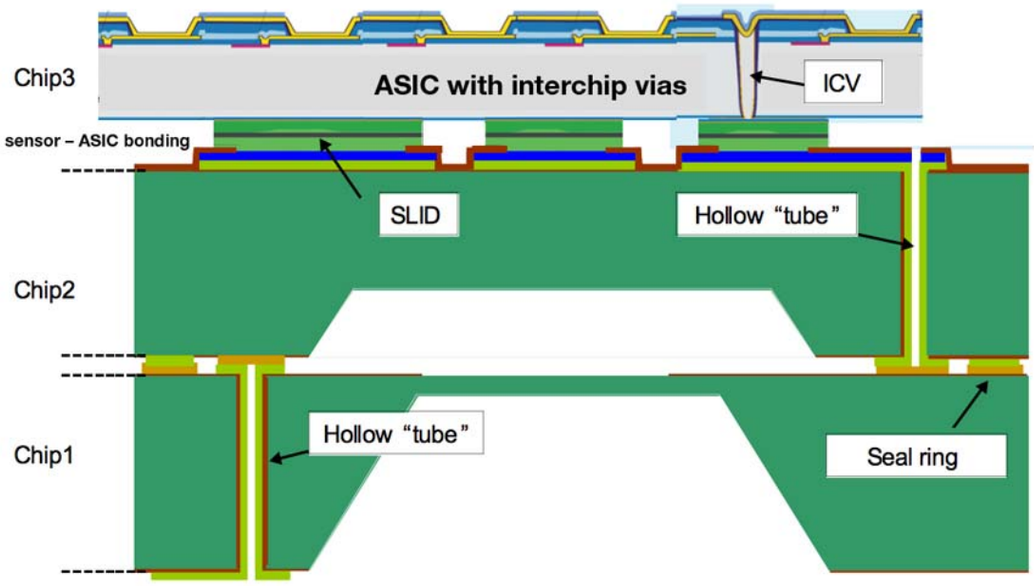


Figure 1. Stacked microsystem of pressure sensor *(Source: SINTEF, Oslo, Norway)*

The basic modules have unified "interfaces" at geometrical boundaries to enable a combination inside the PDE solver or the system-level simulator. Therefore, used material data, numbered items like element types and material numbers, layer thicknesses, meshing, interface nodes, etc., must be identical or at least adaptable.

The modular approach previously described allows on one hand performance of detailed analysis of the thermal behavior of single basic modules, e.g., computing thermal conductivities and capacities as function of geometry or technology parameters; and on the other hand, investigation of the thermal management of the built-up complex 3D structures. Figure 3 illustrates one result of the entire system simulation – the temperature distribution at the upper side of the pressure sensor membrane for a power loss in the ASIC chip with a value of $P_V$=10mW and an environmental temperature of T=300K. The membrane temperature is important because of its influence on mechanical stresses in the membrane, which are the measuring quantities for the acting pressure.

The model previously described can also be used to derive a thermal model of the stack for thermoelectrical simulations on system level. It can be derived either from the finite element model by order reduction methods, or using parameter optimization or approximation algorithms based on the thermal simulation results of ANSYS.[4] Combined with the electrical (circuit) model and thermoelectrical device models, thermal interactions in 3D systems can be analyzed efficiently.

## Electrical Behavior at High Frequencies

Especially at high frequencies, selected wires and chip interconnects within a complex stacked system strongly influence the overall system performance, e.g., cause capacitive and inductive coupling between

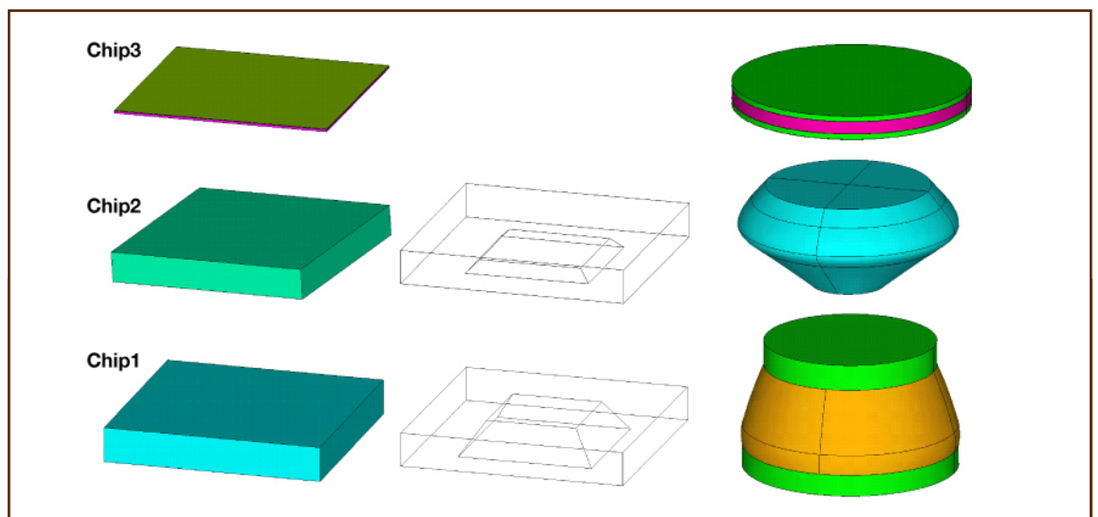


Figure 2. Selected basis modules according to 3D system in Figure 1; left: 3 different chip layers; right: possible interconnect structures – SLID, Au-Stud Bumping, Micro-Flip-Chip (not to scale).

conductors or skin effect. Mainly, signal integrity, timing issues and interconnect delays of distributed blocks related to the 3D interconnect structures must be investigated.[5,6]

To consider electromagnetic coupling in system design, the previously mentioned hierarchical and modular modeling approach is also suitable. First, detailed analyses of structures and physical effects (e.g., skin effect and proximity effect) must be carried out using PDE solvers. Next, S-parameters, SPICE models, or behavioral models (characterizing the behavior of single and adjacent interconnects) can be derived. Finally, these models are included into the electrical network of the entire system to take the electrical behavior at high frequencies into account. Figure 4 illustrates the current density distribution of an interconnect structure at a frequency of 5GHz.

## Conclusions

The goal of all investigations previously described is design support and derivation of design guidelines for 3D systems. Therefore, the adaptation of design flows and the integration of simulation results within these design flows are important tasks. For that reason, simulation results are provided using data formats and languages of the dedicated design tools. Depending on the design task, models on different levels of abstraction are supported. Therefore, our modular modeling approach covers detailed simulations of thermal and electromagnetic effects using PDE solvers, the generation of system-level models in languages like SPICE, VHDL-AMS or Verilog-AMS for analog and mixed-signal systems or special formats like SPEF for digital systems.

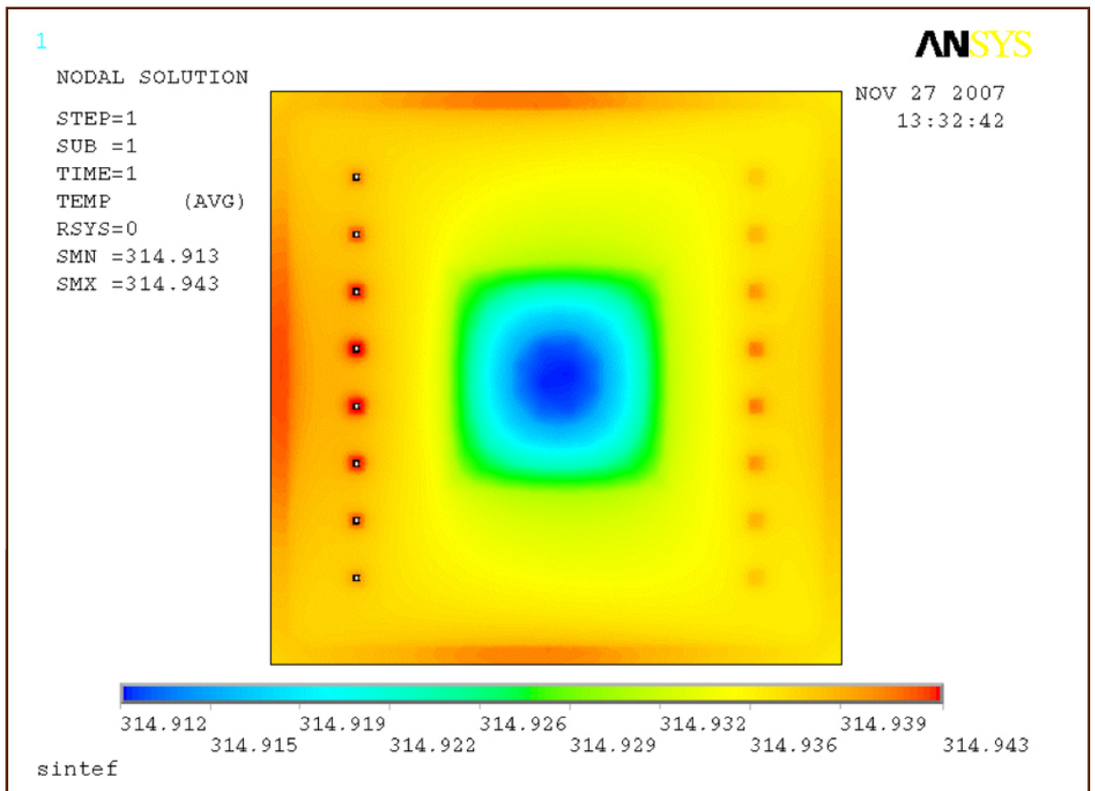


Figure 3. Simulation Result – Temperature Distribution at Top of Chip 1 (Membrane of Pressure Sensor)

***Acknowledgments***

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## *About the Authors*

***Peter Schneider***

Peter Schneider studied electrical engineering at the Dresden University of Technology. In 1993 he joined the Fraunhofer Institute for Integrated

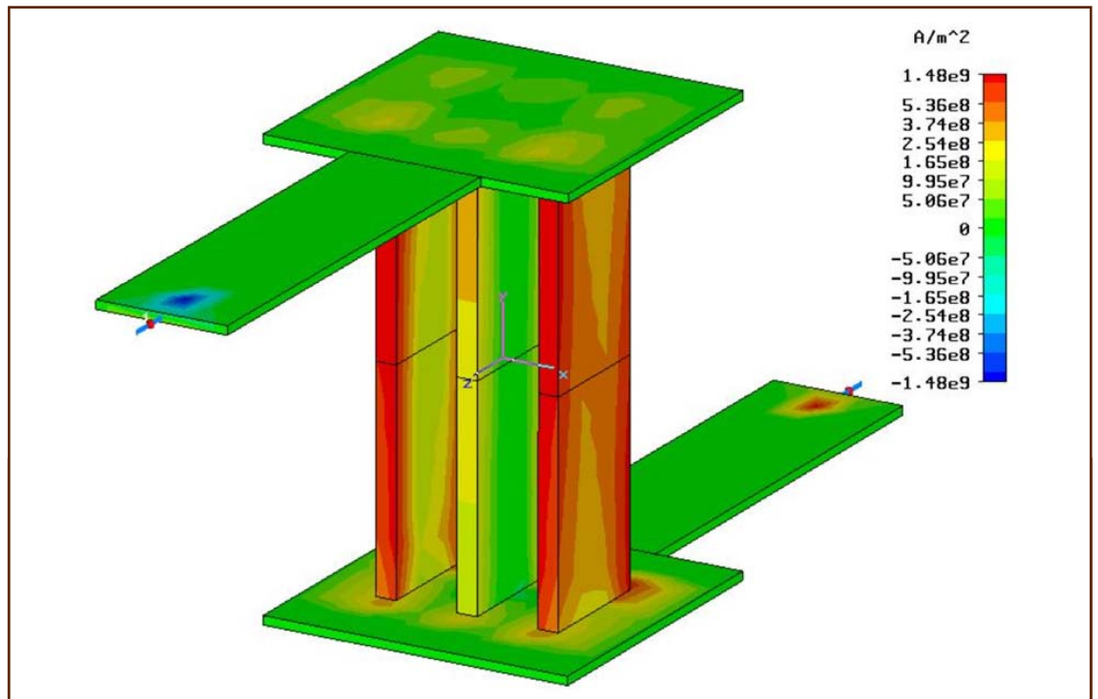


Figure 4. Current Density Distribution in an Interconnect Structure (Frequency of f=5GHz)

Circuits, Design Automation Division, Dresden. Since 2006, he has been head of the department for Heterogeneous Systems. His scientific interests are modeling methodology, simulation of electromagnetic systems, 3D system integration, and development of adaptive control algorithms.

***Sven Reitz***

Sven Reitz received the diploma in electrical engineering from the University of Technology Chemnitz, Germany. Since 1997, he has been with the Fraunhofer Institute for Integrated Circuits, Design Automation Division, Dresden. His main research interests include FE modeling, order reduction, behavioral modeling, and optimization.

***Roland Martin***

Roland Martin studied physics at the Technical University Dresden, Germany in 1972. He worked in different fields of investigation, e.g., microelectronics and building climatology. Since 1999, he has been with the Fraunhofer Institute for Integrated Circuits, Design Automation Division, Dresden. His main research interests include FE modeling and behavioral simulation.

***Jörn Stolle***

Jörn Stolle studied electrical engineering at Dresden University of Technology from 2000–2007. Since 2007 he has been with the Fraunhofer Institute for Integrated Circuits, Design Automation Division, Dresden. His main research interests include RF simulation, physical modeling and optimization.

## Endnotes


1. De Man, H., "Ambient Intelligence: Broad Dreams and Nanoscale Realities," IEEE International Solid-State Circuit Conference ISSCC 2005, San Francisco, February 6–10.
2. Wunderle, B., Kaulfersch, E., Ramm, P., Michel, B., Reichl, H., "Thermo-Mechanical Reliability of 3D-integrated Microstructures in Stacked Silicon," Proc. 2006 MRS Fall Meeting, November 27 – December 1, 2006, Boston.
3. Shakouri, A., Kang, S.-M., Bar-Cohen, A., Courtois, B. (Editors), Proc. of IEEE, Special Issue, "On-Chip Thermal Engineering," August 2006, Vol. 94, No. 8.
4. Schwarz, P., Schneider, P., Model library and tool support for MEMS simulation. Conf. "Microelectronic and MEMS Technology," Edinburgh, Scotland, 2001, SPIE Proc. Series Vol. 4407.
5. Reitz, S., Bastian, J., Haase, J., Schneider, P., Schwarz, P., "System level modeling of microsystems using order reduction methods," Proc. DTIP 2002, Cannes, France, pp 365-373.
6. Schneider, P., Reitz, S., Wilde, A., Elst, G., Schwarz, P., "Towards a Methodology for Analysis of Interconnect Structures for 3D-Integration of Micro Systems," Proc. DTIP2007, 25–27, April 2007, Stresa, pp 162–168. ■


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# Perfect Chips: Chip-Side-Wall Stress Relief Boosts Stability

**Peter Heinze, Martin Amberger, Therese Chabert**
PVA TePla AG


## Abstract

An increase of up to 500 percent die strength is achieved applying the new chip-side-healing technology introduced by PVA TePla as a stress relief step after blade or laser dicing, in addition to the conventional wafer-level back-side stress relief after grinding. Hence, after the chip-side healing, the complete five-side restoration of silicon lattice integrity for each single chip can be achieved – a must for any ultrathin die assembled in advanced 3D packages. The methods and results are presented herein.


## Introduction

Silicon as the base material and semiconductor support for thin chips requires the highest standards in surface integrity and uniformity of crystal Si-planes. This is necessary to counteract its brittle nature; otherwise, the die strength upon mechanical load or thermal stress will become very low and cause low yield in production or early failures in application. Without exception, each physical-mechanical treatment of silicon, e.g., wafer grinding or any kind of singulation technique, whether done by dicing blade (half or full cut), laser (full cut or stress-induced weak zone) or scribe and break disturbs more or less the crystal line integrity of the monocrystalline silicon material – and therefore diminishes its strength according to the weakest link in the chain model upon mechanical-loaded stress.

Some of the first publications addressing the positive impact on die strength by dry etching on laboratory level were published in 2001 by Kröninger et al. [1] and Landesberger et al.[2] A summary of die strength improvement on precut wafers singulated by grinding was published by Takyu et al.[5] Here the authors focus strictly on normal bending studies and have not considered potential reverse bending issues. However, reverse bending is important for any characterization of stress relief technologies applied to chip sides and edges. The specific stress relief shortcomings of this process have been addressed by Heinze et al.[3,4]

Due to the high negative impact of the thin chip sides on die strength, we focus our machine and process development on

this subject, since so far no reasonable technology is available for sufficient stress relief at this location with restricted access. In order to relieve the whole mechanical stress and restore the die flexibility or bending capability, the 100 percent of silicon surface must be healed: at the back side of the chip where the stress relief on wafer level is a standard process in pre-assembly today, but in particular, additionally after singulation at the front-side and back-side chipping areas, as well as along the chip side wall.

Our chip-side-healing (CSH) process describes the isotropic etch of the chip sides after blade or laser dicing. In a first step, the ground wafers are remote cold plasma (dry) etched stress-relieved on wafer level, then singulated by laser or blade, followed by the second stress relief step: the chip side healing, applied on dicing tape frame etching the sides of the chips.

## Material and Methods

In this study, the isotropic remote cold plasma dry etching was applied. Here, F-radicals in an Ar-downstream remotely generated by a plasma source are etching the silicon surface. The etching processes were run on the PS 4008 ASYNTIS system with integrated high-uniformity kit and optimized chamber geometry. This kind of precisely controllable remote cold plasma technology setup prevents any negative surface charge impact by ions and electrons as well as any microwave and additional heat impact to the taped substrates during the etching process. The remote cold plasma dry etching technology does allow the etching access to 100 percent of the offered silicon surface, all the deep grinding scratches on the wafer backside, the wafer edge, as well as access to the depth inside the dicing kerf down to the bottom of the die. For the methodological comparison of wafer-level stress relief, we applied ball-ring test for 50 chips (75 µm, 10x10 mm) each, broken in normal direction. The ball-ring method avoids the impact of the die edges. To elucidate the CSH effect, we selected the 4-point breaking method. We have measured the die strength of 35 chips at normal, and 10 chips at reverse bending for each data set.

Normal bending means tensile stress is applied at the ground surface; reverse bending means tensile stress is applied to the active chip side. The chips have been picked from expanded dicing UV-tapes in order to avoid negative picking effects on the die strength. The CSH-chips (14x5 mm) are 100 µm thick. The material was bare silicon (100), prime wafer quality. The die breaking tool (Zwick & Roell) down speed was set to 1 mm/min. The force data (N) have been converted into flexural stress data (MPa) and plotted in Weibull diagrams.

The Weibull regression line was calculated according to the maximum likelihood method; the confidence level is set to 90 percent. The slope of the regression line (the steeper the better distribution), the characteristic die strength values (CDS: die strength at 63.2 percent probability of breakage), and in particular the minimum die strength (MDS) finally determine the line yield.

The minimum die strength (MDS) we set as the crossing point of the 1 percent probability of breakage line with the regression line. Thus, the CDS and MDS depend directly on the slope of the regression line (Weibull Modulus) and reflect on the bulk data quality. Not any accidentally measured minimum value, but only the proposed 1 percent definition for the MDS statistically takes also potential low flyers into account at every reasonable number of chips broken, and therefore allows the direct comparison of different data sets or manufacturing methods.

## Results

### *Wafer-Level Stress Relief – The Backside of the Die*

The dry polish as anomalous brittle grinding gives MDS no higher than ground-only chips (Figure 1).

The CMP technology achieves reasonable CDS values, but the MDS is still low due to missing access of a polishing pad down to the bottom of the randomly distributed deep grinding scratches.

For all previously mentioned parameters, the two pure chemical-based methods – the wet etching and the remote cold dry etching – do show by far the best values summarized in Figure 2; about 85 percent better MDS values compared with the DPE (direct plasma etch). Here the plasma is burning 3–5 cm directly above the wafer and the impact of local charging and ion impacts are inevitable.

Along with the best die strength values, the remote cold dry etching also allows the silicon removal in a wide range between, e.g., 0.1–20 µm, as well as the easy integration into cluster lines with wafer grinder and mounter. However, the main reason to use the remote cold dry

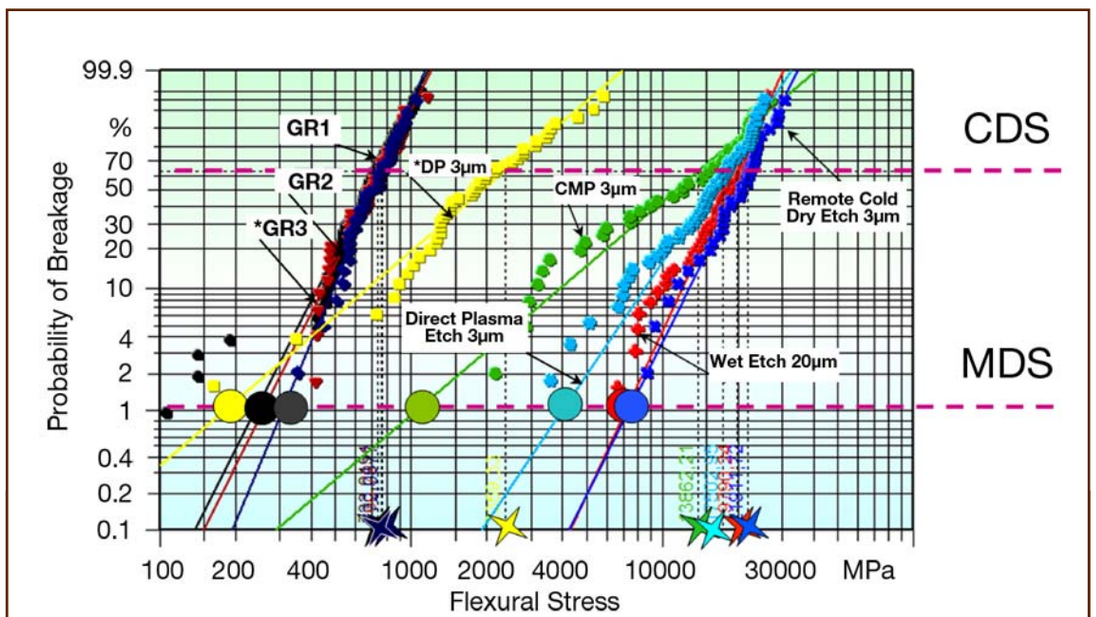


Figure 1. Die strength after current stress relief methods. The ball-ring method minimizes the impact of singulation on the results. The minimum silicon removal amount for stress relief after Z2 mesh #2000 is given in µm for each method. GR1=ground wafer ref. for CMP, remote cold dry etch, wet etch. GR2=ground wafer ref. for DP (dry polish). GR3=ground wafer ref. for DPE. GR2 and DP data source DISCO Corp, GR3 and DPE data source Hanke & Malachowski, Microproduktion 4/2007, adapted to fit the graph.

etching technology in this study is its unique capability to etch between the singulated dies in the depth of the dicing kerfs, along with the compatibility to a wide range of usual back-grinding and dicing tapes. Therefore, in the CSH process, the singulated chips have been etched in the second stress relief step on dicing tape in order to heal the chip sides (CSH). The usual back-side chipping after blade dicing is in the range of 15–25 µm; the front-side chipping in the range of 5–10 µm; the damage along the chip side about 3 µm. Hence, we have etched this amount in order to eliminate all silicon damages. Before singulation, the active side has been coated with an appropriate etch-resistant protecting layer which has been removed after the chip side healing.

## Data

### *CSH*

At normal bending and compared to ground-only-diced-only chips, the chips with conventional backside stress but without the chip side healing improve their CDS from 578 MPa to 623 MPa (7.8 percent), the MDS from 195 MPa to 265 MPa (35 percent) (Figure 3). The dies with both backside-stress relief and CSH show a CDS improvement from 578 MPa to 1683 MPa (191 percent) and the MDS increased from 195 MPa to 1,150 MPa (490 percent). The slope of the regression line is consequently steeper, reflecting the improved distribution due to the strong positive impact on minimum die strength.

At CSH reverse bending, the results of the 10 dies measured are not Weibull analyzed but plotted in the box plot. Here, the same high level of die strength is achieved

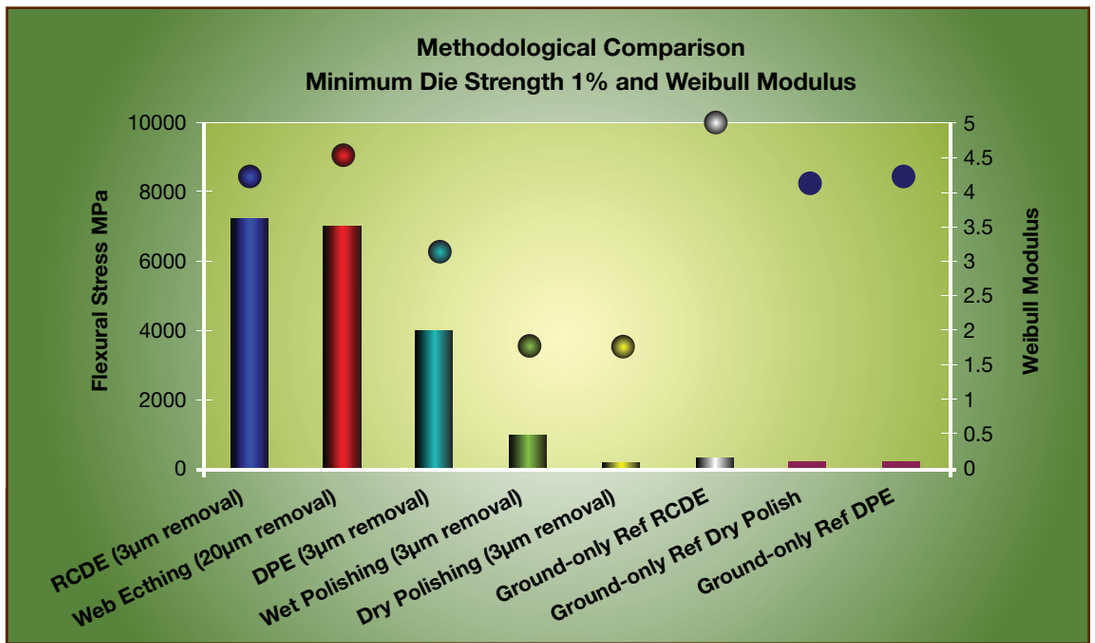


Figure 2. Summary of the methodological comparison of current stress relief methods. The minimum die strength and the Weibull-Modulus are the characteristic parameter to define the quality of stress relief for production line yield. The pure chemical-based methods remote cold dry etch (RCDE) and wet etch give the best results. Any kind of additional mechanical-physical impact on the brittle monocrystalline silicon surface diminishes the die strength.

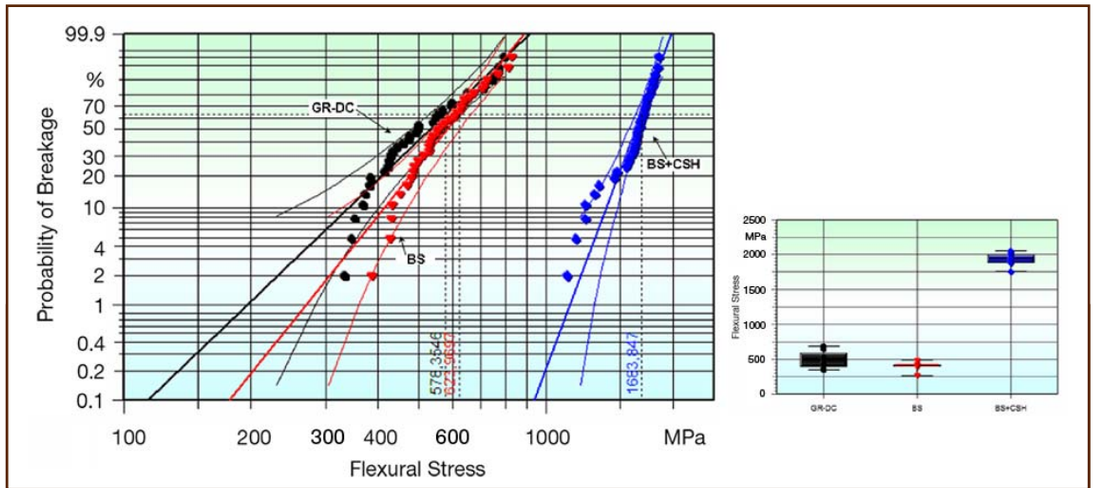


Figure 3. Weibull Diagram CSH die strength. Left side: normal bending; right side: reverse bending: GR-DC=ground-only-diced-only, BS=Back-side stress relief, CSH=chip side healing. Note: The GR-DC-data and BS-data are comparable to the GR-data and RCDE data in Figure 1; the minimized gap between the two data sets here demonstrates the edge-impact enabled by the 4-point measurement method.

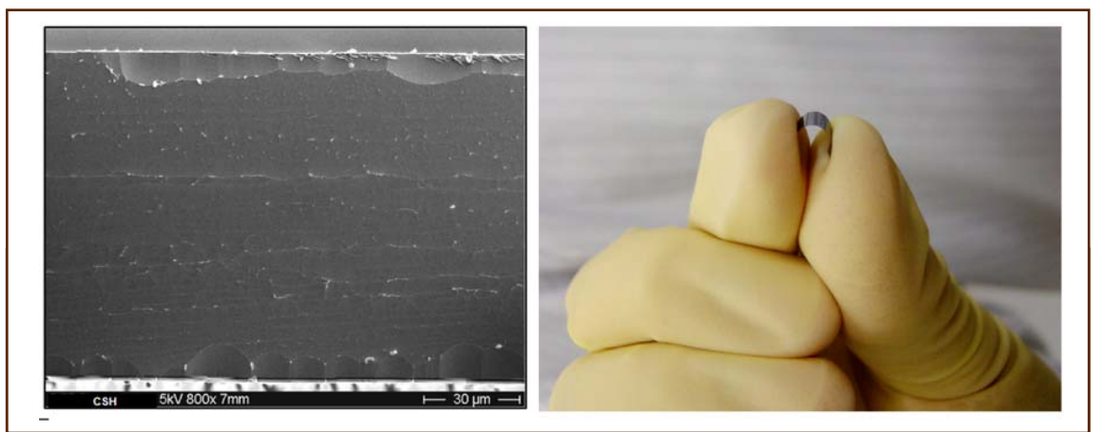


Figure 4. Typical surface of a chip side after the CSH by RCDE (left). Front- and back-side chippings are eliminated and stress relief is completely done on the silicon surface along the chip side wall. Ultrathin chip (60 µm) bending after the complete removal of any predetermined breaking points like grinding marks on the backside and dicing injuries in the chip side walls by RCDE (right).

as normal bending, in case of back-side plus side-wall-etched chips. The median value increased from 525 MPa to 1,900 MPa (262 percent).

For CSH, the conventionally singulated dies show basically the same extreme high level of die strength improvement bended in both directions, normal and reverse after the two-step process of remote cold remote plasma (dry) etching. The damage zones, front-side chipping, back-side chipping, side wall damage) caused by the dicing wheel singulation is completely eliminated. Using the tensile-stressed wafer maker surface here as reference, we can say that the RCDE back-side treatment restores the silicon quality in regard to mechanical stress on the chip backside completely.

A completely etched and successfully stress-relieved chip side is shown in Figure 4. The rounded structures of the front-side and back-side chipping area indicate the successful removal of damaged silicon material on the chip sides.

For CSH, the overall mechanical yield improvement as the common average of both normal bending plus reverse bending values is 220 percent CDS (characteristic die strength) and 580 percent MDS (minimum die strength). Taking an average chip surface ratio of 98 percent for the back side and 2 percent for the remaining surface of the four chip side walls, the positive impact of the additional healing of the 2 percent side-wall surface by CSH is summarized in Figure 5.

The retrofit of the CSH process in any of the existing thin wafer/chip production lines can be done very easily and will have two positive effects:

### *Package Design*

The die strength improvement goes along with an increase of die flexibility where the allowed die bending radius is minimized and the die flexibility is maximized in both bending directions (Figure 4). The new quality of die shapes may result in new combination of chips in terms of single chips as well as multiple chip packages.

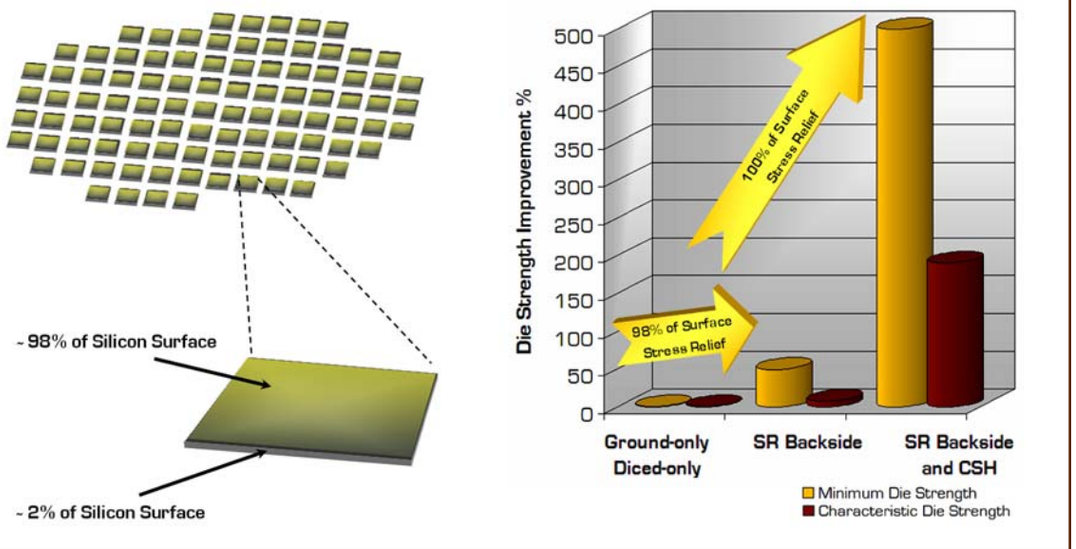


Figure 5. Die Strength Improvement Effect of the CSH Process

### *Assembly Line*

The back-end assembly production will appreciate the opportunity of higher throughput and line yield at lower die breakage due to the increased mechanical tolerance of CSH-treated silicon chips. The implementation of the CSH process and the ASYNTIS 4008 system will positively affect the CoO of the existing back-end fabs.

## References

1. Kröninger, W. et al. (2001), "The Stability of Silicon Chips," Proceedings of Fraunhofer Gesellschaft FhG workshop, Thin Semiconductor Devices-Manufacturing and Applications 2001, Munich.
2. Landesberger, C. et al. (2001), "Structural investigations and mechanical behaviour of thin silicon substrates," Proceedings of Fraunhofer Gesellschaft FhG workshop, Thin Semiconductor Devices-Manufacturing and Applications 2001, Munich.
3. Heinze, Amberger, Chabert (2007), "Five-Side Stress Relief - The method to get the 'Perfect Die,'" Advanced Packaging Conference, October 10–11, 2007, SEMICON Europa 2007, Stuttgart, Germany.
4. Heinze, Amberger, Chabert (2008), "So macht man den Perfekten Chip," Mikroproduction January 2008, pp 45-50.
5. Takyu et al. (2005), "Chip Thinning Technologies Realizing High Chip Strength," IEICE Transactions on Electronics (Japanese Edition) Vol. J88-C, No. 11, pp 882-888.

## About the Authors

### *Peter Heinze*

Peter Heinze is director preassembly, PVA TePla AG, and has worked for 18 years in the semiconductor arena. After receiving his Ph.D. in natural sciences, he has been employed at several equipment companies in the front and back end. He has been focusing on the preassembly production (from thick wafers to thin chips) for nine years.

### *Martin Amberger*

Martin Amberger is manager of technology and application. He was with Applied Materials for nine years as a process engineer for PECVD and has also developed innovative MOCVD - FRAM processes. Since being involved in preassembly, Martin has developed several production-proven stress relief and passivation processes.

### *Therese Chabert*

Therese Chabert is a senior application engineer. She obtained her master's degree in physics, focusing on "Fabrication and Utilisation of Advanced Materials" (University Limoges). She gained 13 years experience in the semiconductor front-end industry at Applied Materials supporting worldwide customers in plasma dry etching. ■

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**Steve Greathouse**
Global Microelectronics Technology Manager
Plexus Corporation - Nampa, Idaho

New technologies are the lifeblood of the electronics industry. Engineers with their "out of the box" thinking are working on leading-edge pathfinding projects that create significant changes in the way the industry does things. Revolutionary advances change the direction of a technology, while evolutionary advances refine the current state of the art to a better level.

Pathfinding can be defined as investigating ideas, technologies or processes that sound good and make sense on paper, but where there is little data or a realistic method of testing the viability of it without actually building it and testing the results. Modeling can help, but many times, the nature of what you are investigating requires so many assumptions to be able to properly construct the model that it is little more than an educated guess.

The 14th-century English logician William of Occam expressed his thoughts as a "law of succinctness." Generally it is paraphrased as, "All things being equal, the simplest solution is usually the best."

In the ensuing article, Joe Fjelstad presents his paper titled, "The Occam Process: Solderless Assembly and Interconnection of Electronic Packages." This is a debated and much-discussed technology that uses a plated copper process to interconnect the contacts on the electronic components. He shows several drawings and an example of how this process can be utilized to produce simple boards. The scale-up to production will require some significant changes to a production area, but he points out that the costs and reliabilty of the final product could be worth the investment. His main point is that this process completely avoids the ROHS requirements for tin/lead replacements as this process uses no solder at all.

We will have to see if this process is the revolutionary change in board construction that we've been looking for.





# The Occam Process: Solderless Assembly and Interconnection of Electronic Packages

**Joseph Fjelstad**
Verdant Electronics

## Abstract

Since the earliest days of the electronics industry, assembly of printed circuits has been both defined and limited by the use of electronic solder technology for component attachment. In July 2006, the European Union's parliament banned the use of lead in electronic solders used for assembly with only a few exceptions, thus lead-free solders have been legislatively elevated to the default choice. The result has been a significant disruption to the entire electronics manufacturing infrastructure, necessitating sweeping changes, not only in terms of the materials, processing and finishes used for PCBs and their assembly, but also for the equipment used. The impact has been stunning in its reach, including even the introduction of a new term to its lexicon, $T_d$ (temperature of decomposition of PCB laminate resin) to account for phenomenon not seen before the new higher temperatures now required for assembly with lead-free solders. In this new era of lead-free soldering, electronic solder has morphed from faithful electronic assembly partner to technological nemesis, causing the electronics assembly industry to conform to its more demanding needs.

This increasingly hostile environment for electronics assembly has sparked innovations within the industry, including proposed methods for electronic assembly that are completely solderless. The new methods are essentially the reverse of traditional methods, in that circuits and interconnections are produced directly on monolithic assemblies that are comprised of molded or embedded components. The method has been capturing the attention of the rapidly growing number of forward-looking companies from around the globe since its introduction in August of 2007. This article will describe details of the process and some of its variations, which have come to be collectively known as the Occam Process, so named to honor the 14th-century English philosopher and logician, William of Occam, whose rigorous thinking and arguments favored and encouraged the finding of the simplest possible solution to every problem.

## Introduction

Long-standing and well-understood approaches to electronics manufacture and assembly based on tin-lead soldering were dealt a crushing blow by the European Union's parliament when they made the ecologically unsubstantiated and unilateral decision to prohibit the use of metallic lead in electronic solders as of July 2006. In the wake of that decision, a host of new problems have arisen some that were unknown when tin-lead was the de facto solder of choice. Many of them are the result of the higher temperatures required for lead-free which can damage components and PCBs and reduce reliability. More frustrating is that other problems, such as tin whiskers, for example, that had once been put to rest, have reappeared. It would be of substantial benefit to the electronics industry if the EU parliament were to reverse itself relative to its ban on lead in electronic solders; however, it is generally agreed that such a reversal is highly unlikely at best. Given this sobering reality and the increasing challenges surfacing as the industry tries to comply, a new method for electronic assembly, which obviates completely the need for solder of any sort, has been devised and promises to provide a useful pathway which skirts the problems and concerns of solder completely. The new technology solutions build on earlier efforts by researchers developing embedded function and multichip module technologies that date back to the 1970s when the first embedded resistance and capacitance solutions were proposed, and on to the 1980s with the first smart cards, and more recently to the late 1980s and 1990s where bare IC chips were being embedded to create multichip modules, and takes the technology to a new level of organization that will make the assembly of electronics much simpler.

To understand the benefits of what is now being called the Occam process, it is necessary to understand standard practices of today for the manufacture of a conventional electronic assembly. Following is a description of the most salient steps. The process begins with a schematic of the electronic circuit from which a printed circuit board (PCB) is designed. The printed circuit design is then sent to a PCB manufacturer, where it is fabricated and tested for electrical functionality. The printed circuit boards are then shipped to a contract assembler. The assembler generates a bill of materials (BOM) and procures the components. Surface mount (SM) components are most common today, and thus the surface mount process is the process of choice today.

The SM process is comprised of the following commonly used steps. First, a solder paste is stenciled on to component lands. The components are then accurately placed on the board using pick-and-place equipment. The components are temporarily held in place by the tacky solder paste until the solder is reflowed to provide the permanent interconnection between component leads and the PCB terminations. The assembly is then thoroughly cleaned and tested to make certain that no shorts were created or opens remain due to non-wetting or insufficient solder paste and, as well, to assure that no components were damaged by the high temperatures of the lead-free soldering process.

In contrast to traditional surface mount technology (SMT), the Occam process is fundamentally a reverse-order interconnection process, in that the components (i.e., tested and burned in IC packages and other devices including discrete and integrated passives, inductors, antennas, connectors and the like) are first attached to a carrier (either permanent or temporary) where they are encapsulated in place and then interconnected using processes and technologies that are mature, low-risk and industry-familiar. The encapsulated components and other circuit and interconnection elements are interconnected to one another by copper plating circuits to the component lands after they are assembled into their

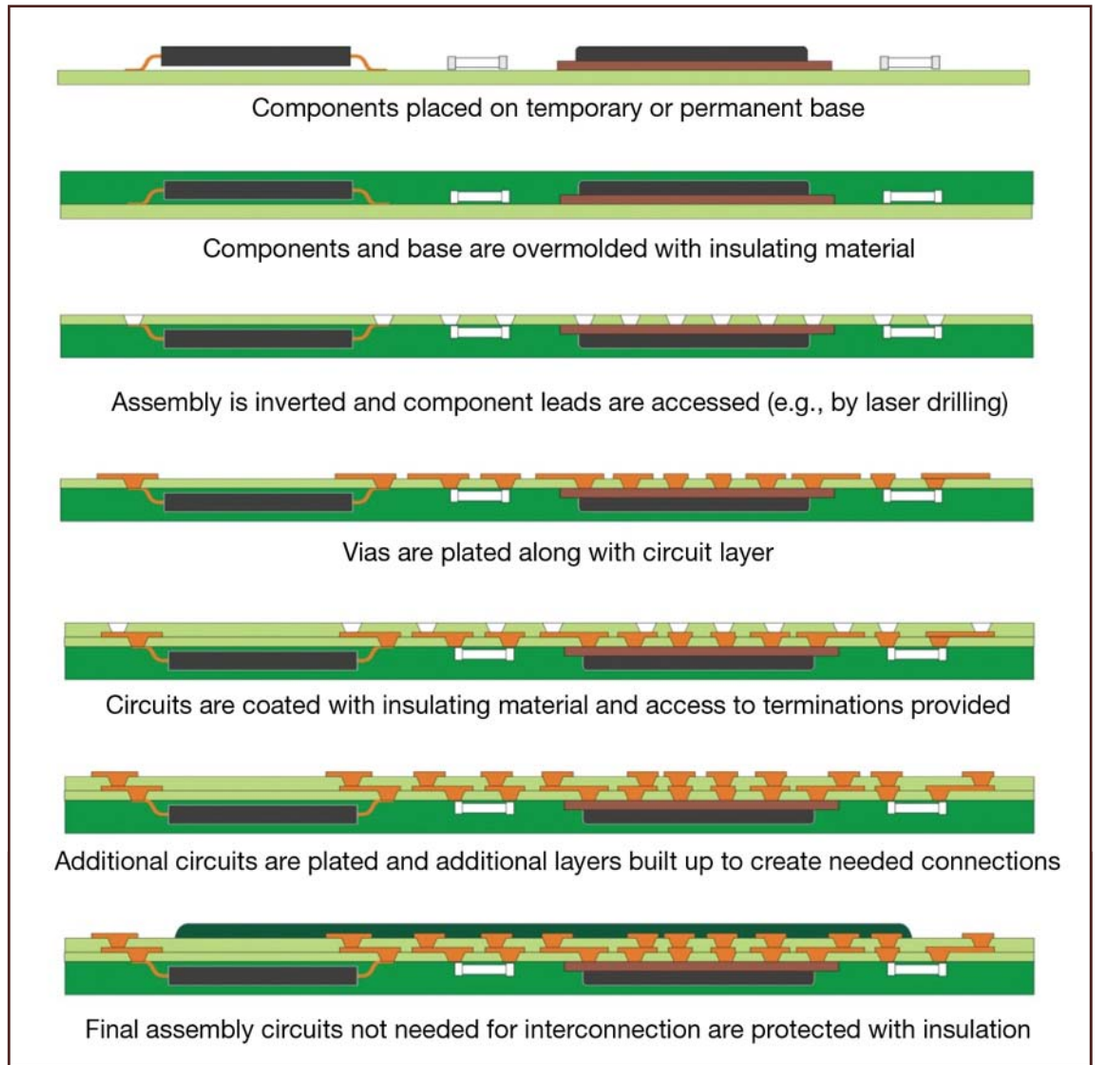


Figure 1. The basic Occam process manufacturing steps are illustrated. The process greatly shortens the supply chain and can speed time to market while reducing cost.

final positions. The basic process steps of the Occam process embodiment are illustrated in Figure 1, where it can be seen that the conventional sequence of creating an electronic assembly is fundamentally reversed, creating an assembly sequence where, in the most basic terms, components are placed and then electroplated with circuits to create electrical interconnections.

Thus in the fabrication of an Occam type of assembly as illustrated, the components are first placed on temporary or permanent carrier. In the former case, this could be a removable tacky film and in the latter case, a permanent base to which the components are bonded using a permanent adhesive. The film and base temporarily immobilizes the components, holding them accurately in place until the structure is encapsulated, locking the components permanently into place. The result is that the entire array of tested and burned-in components becomes a monolithic assembly, with each component now solidly and accurately locked in position and place. The bottom surfaces of these interconnection terminations can then be exposed by removing the temporary base and film or by making holes in a permanent base by such means as mechanical abrasion or laser ablation.

Using any suitable metallization technology that has been developed over many years, such as sputtering or electroless plating, the connections to the component terminations are then created by copper plating to the exposed surfaces of the terminations distributed across the encapsulated assembly of electronic components' surface. This can be accomplished using either built-up circuit layers as just described, or alternatively by the use of some of the evolving direct-write techniques, or by proven direct-wire interconnection techniques or even by co-lamination processes developed in the 1990s for PCB manufacture. Figure 2 offers visual examples of the latter two concepts.

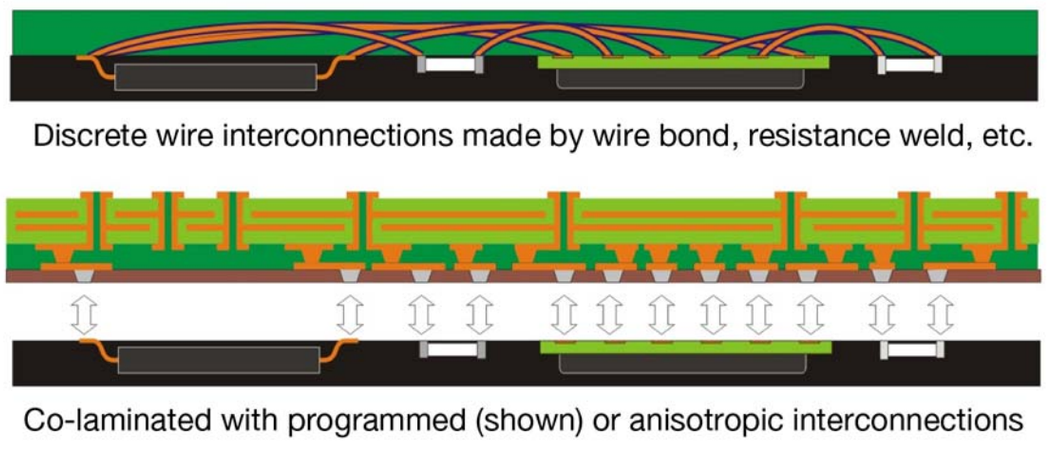


Figure 2. Once the components are secured in place, interconnection can be made in a number of different ways, such as discrete wiring and lamination with programmed or anisotropic bond layers. Direct writing techniques (not shown) are also possible.

There is a great deal of potential flexibility in the alternative Occam techniques just described. For example, with direct-write solutions, it is anticipated that it will be possible to redesign interconnections right up to the moment the process begins. This capability should open wide the doors for prototyping in real time. The Occam process is expected to allow production of electronic assemblies that will not only be low cost and highly reliable, but also provide many important design needs. For example, thermal enhancement can be easily built in; with a metallic coating, hermeticity is possible, as is integral EMI shielding. There is also the potential for the embedment of various electromechanical and optical components.

## Advantages of Low-Temperature Assembly

There are numerous advantages to this evolving approach to assembly, one of which is that it does not involve exposing the components and PCB to the extreme temperatures required for lead-free soldering. As a result, concerns over component moisture sensitivity level (MSL) are eliminated. For the reader's reference, MSL is a measure of the risk of component damage due to explosive outgassing of absorbed moisture in the package during soldering devised by the Joint Electron Device Engineering Council (JEDEC). While traditional lead-free solder processing is limited to a maximum temperature of 220°C, SAC alloys approach 260°C and the vapor pressure of water

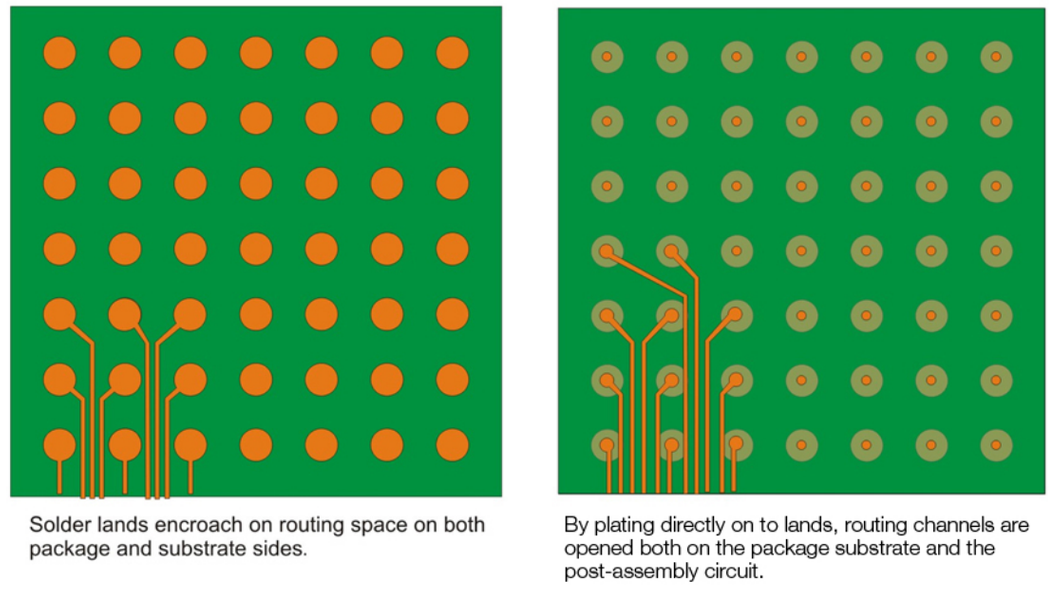


Figure 3. Routing advantages are possible for both peripheral and area array packages. Moreover, because there is no need for reflow and cleaning, the Occam process allows for edge-to-edge tiling of BGAs to create shorter path interconnections with reduced energy use and higher performance.

more than doubles over this amount of temperature increase.[1]

Because of this important low-temperature assembly advantage, with assemblies created using Occam-type processing, all components can be treated as if they were MSL-1. This means that IC packages do not require dry storage, special handling, pre-baking or accurate hold time recordkeeping in normal environments. Moreover, the process also allows the use of components that are not capable of withstanding lead-free soldering temperatures (aluminum electrolytic capacitors, certain optoelectronic devices, connectors, etc.). Another important prospective advantage of solderless assembly is that heat spreaders, heat sinks or even heat pipes can be embedded directly into or made an integral part of the assembly because no high-temperature solder is required.

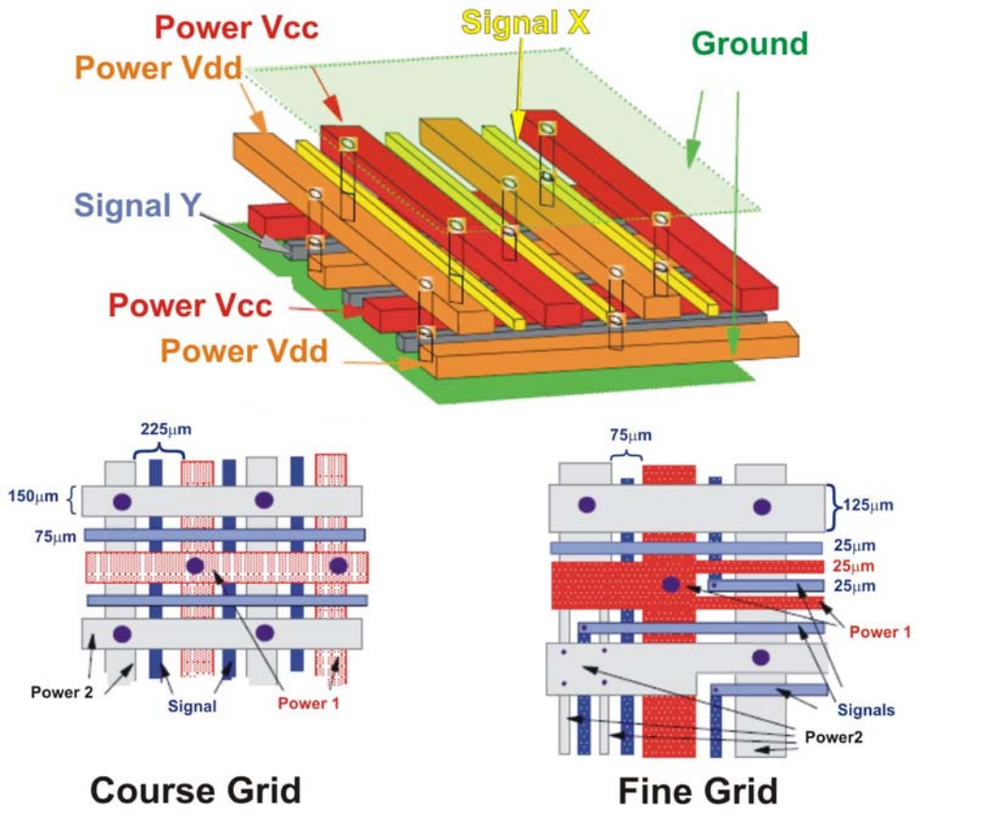


Figure 4. The Occam process is well-suited to designing with the IMPS approach developed at the University of Arkansas or the similar Power Grid concept developed at HP which employs full metal grounds. Significant layer reductions can be achieved. With Power Mesh multilayer routing, efficiency for each layer approaches 95%. *(Image courtesy of Happy Holden)*

## Circuit Design Advantages

As it is with standard printed wiring board, the interconnect structures circuit patterns must still be generated for Occam-type assemblies; however, with the new approach, a number of design constraints can be relaxed. For example, need for large component pads or lands that are required for soldering the components to the PCB is obviated. With space-wasting and performance-sapping terminations eliminated, it is possible to simplify the circuit routing for area array packages. This is illustrated in Figure 3. This layout easing feature not only allows for higher circuit density but it also offers potential reduction in the number of layers required for the design. Yet another advantage is that there is no need for drilling high-aspect-ratio vias all the way through the assembly, as special structures have been anticipated to address the need when it is encountered.

Occam-type processes are also amenable to implementation using the interconnected mesh power system (IMPS) design approach developed at the University of Arkansas by Professor Len Schaper and his colleagues. IMPS designs start with a grid of power and ground conductors that are three times the width of a selected minimum width signal conductor and separated by the minimum space.

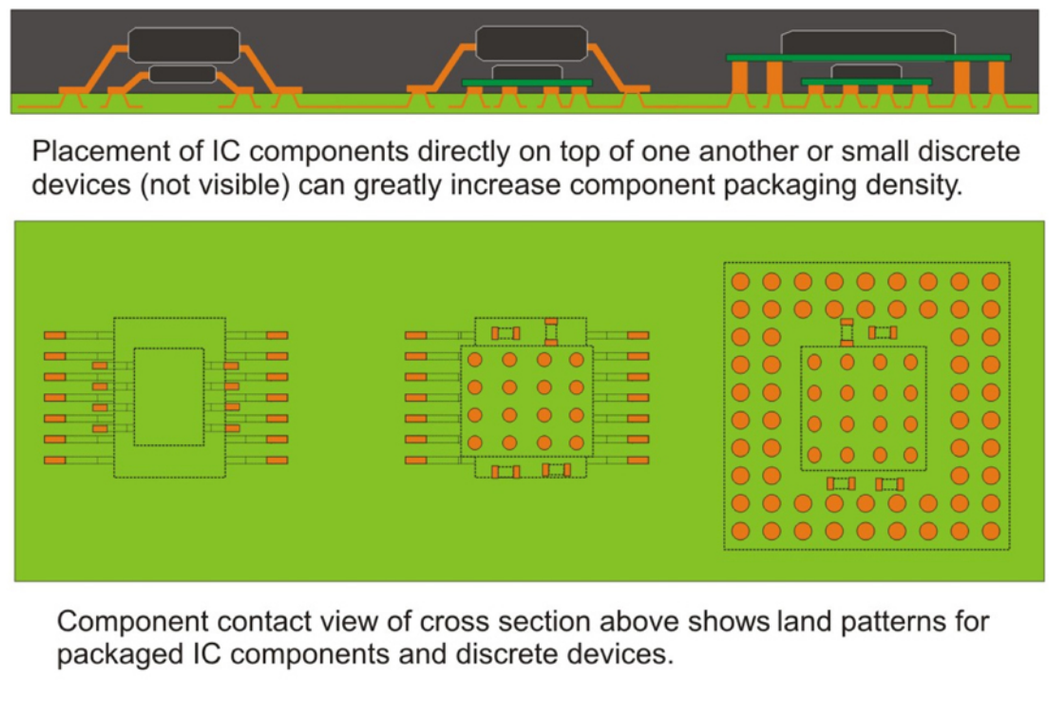


Figure 5. The Occam process allows for components to be stacked one over another without requiring through package connection if desired and package choices permit, allowing for even higher-density designs.

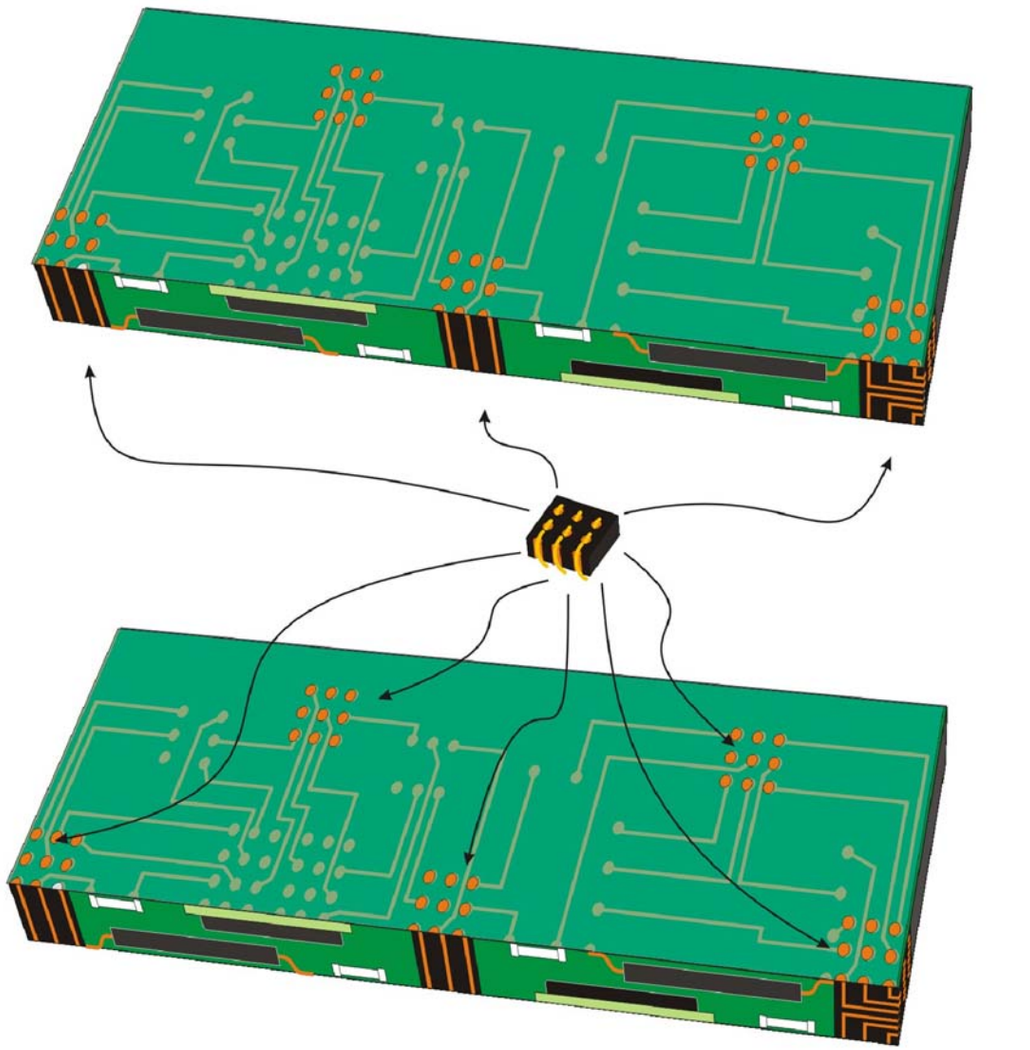


Figure 6. Low-profile connectors as shown above can be used to make connections between assemblies creating a three-dimensional interconnection assembly.

Signal conductors are then routed to the spaces of the mesh, with the power and ground narrowed to accommodate them when and where required. The implications in terms of cost reduction and performance increase are impressive.

While IMPS structures were originally developed and designed with surface-mountable IC modules as a target product, the concepts are applicable to next-level interconnections as well. For example, a similar power mesh concept was developed at HP for courser features commonly found on standard PCBs and using full metal ground planes (see Figure 4).[2] The mesh is never broken or disconnected. All of the signal conductors are coplanar transmission lines referenced to both power and ground, and the reference is preserved when the signal goes from X to Y. Crosstalk is very low, because there is always an AC ground conductor between every pair of signal conductors. The initial mesh establishes the allowed signal tracks. The concept is ideal for components laid out using a common grid pitch, and under such circumstances any EDA router can be used to lay out the signal wiring in the channels. A design rule check is still used to impose minimum clearance on the power and ground to narrow traces as required.

The general design method has been shown capable of significant layer reductions compared with traditional design approaches while offering lower noise and lower crosstalk, based on measurements.[3] These innovative wiring architectures can replace as many as 14-18 layers of conventional through-hole wiring. For example, a 14-layer board of standard design could potentially be reduced to as few as 4 layers and an 8-layer board down to 2 layers. When coupled to Occam-type processing to create a direct HDI interconnection to component terminations without the need for soldering, the combination could well support requirements for I/O connections up into the 400 I/O $cm^2$ (2500 I/O per $in^2$).[4] Finally, highly dense structures are possible with the Occam process because components can be densely tiled with component edges abutted, due to the fact that cleaning flux from under the components after assembly is not needed.

## Stacking Assemblies for Better Performance

Another advantage of the new approach to solderless assembly is that the assemblies can be stacked and interconnected both on the edges and in mezzanine fashion simultaneously as illustrated in Figure 5. The result of such structures is a highly dense IC package assembly. It is perhaps not beyond the realm of reason that it could be possible

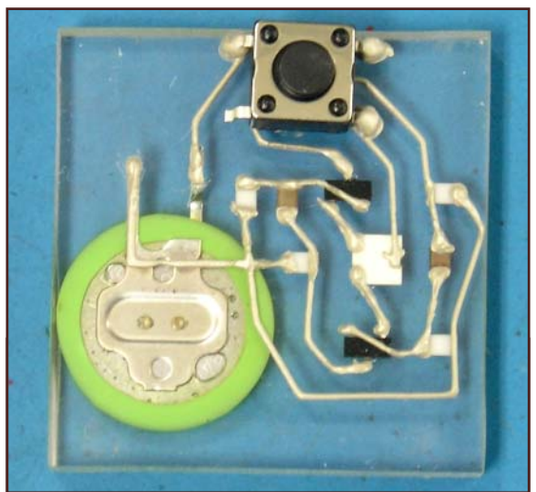

Figure 7. Example of a simple prototype Occam assembly. Circuits were drawn using a programmable dispensing tool. A dome switch would normally be employed to reduce assembly height. *(Assembly by Promex Industries)*

to create an interconnection structure that could approach supercomputer performance within a 1 meter cube. This is made possible by the significantly reduced signal pathway lengths, with improved signal integrity and the provision of clean power. There is also the prospect for including ESD management solutions within the assembly rather than on the IC itself to further improve performance. Such approaches would further reduce power demand, as both the I/O and the core power requirements for the integrated circuit are minimized, especially when clean channels are provided by interconnections within the overall system. Even so, energy densities will not be zero, and thus the advantages of having an integral heat spreader or even a heat pipe built within the assembly and directly connected to the IC packages, or in the case of flip-chip packages, directly to the chosen integral heat spreader technology. A prospective embodiment of such and assembly is provided in Figure 6.

## Rapid Prototyping

While the focus thus far in this discussion has been on the potential for volume production, the potential of the technology for rapid prototyping should be of high interest to those seeking to move products rapidly to market. There is presently interest and activity to build a machine that will take care of all aspects of an Occam assembly in a relatively small area by adapting various technologies both current and evolving that can be brought together to create assemblies in a matter of hours rather than the typical cycle of weeks or months. For example, there are numerous types of machines that are capable of creating 3D structures by layering polymers and/or metals. These same concepts can be employed for Occam-type structures. In such cases, a component set could be placed on surface and scanned with a laser to create a database for the 3D carrier constructed using the 3D layering tool into which the devices are later placed. The components are bonded in place in the carrier depending on the process; the circuits could be then built/written directly onto the component terminations using any of a number of different prospective methods, such as a programmable dispenser or ink jet printer loaded with conductive ink. The assembly can then be coated for protection. Multiple layers can be "written" in this fashion provided openings are provided for contacts. An example of a simple assembly created in this fashion is shown in Figure 7.

## Conclusion

In conclusion, the improved approach to assembly offered by the Occam process gives the OEM a new choice for producing products in the face of growing concerns over the efficacy of high-temperature lead-free soldering. The new approach should prove a highly reliable and cost-effective approach to electronic assembly, and offer the printed circuit manufacturer the possibility to reinvent and redefine their circuit manufacturing processes in a way that adds significant value while reducing overall costs, and increasing reliability while easily clearing the hurdles put in place by the EU's RoHS legislation. A test vehicle is being defined and designed at the time of writing, and full qualification of the process will begin soon with the efforts of progressive companies in the electronics interconnection community around the globe. Given the promise of lower cost, better reliability, reduced supply chain, faster time to market, less waste, virtually automatic RoHS compliance with even greater environmental friendliness, the Occam process is being given serious consideration by major OEMs; what remains to be seen is how quickly it can deliver those promises.

## References


1. W. Englemaier, Posting on IPC Technet 24, August 26, 2007.
2. H. Holden, "A Design Technology Innovation-The Power Mesh Architecture for PCBs," The Board Authority - *Circuitree*, Vol. 2, No. 4, December 2000, p. 42.
3. L. Schaper, M. D. Glover, and M. Kabumoto, "Comparison of the Interconnected Mesh Power System (IMPS) and Buried Stripline Interconnect Topologies," proc. 2001 Int'l. Conference on High Density Interconnect and System Packaging, 2001, pp 58-63.
4. Personal communication with Happy Holden (see also Mr. Holden's "Happy Thoughts" column in the November 2007 issue of *Circuitree* Magazine).


## *About the Author*


***Joseph Fjelstad***

Joseph Fjelstad, founder of Verdant Electronics, is a 36-year veteran of the electronics industry. He has authored or co-authored numerous articles, columns, papers and books on electronic interconnection technologies and holds 125 U.S. patents, with many others still pending. ■


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