Future Fab

INTERNATIONAL

Special Focus:

International Technology Roadmap for Semiconductors

In Association with:

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WELCOME to the 28th edition of Future Fab.

As we enter into this New Year, it's customary to look at what the year held and what the New Year will bring to us. What a volatile and unprecedented year this has been. We all know what has been happening in the global economy, and I suspect that everyone has felt its effects in some way, shape or form. But, here at Mazik Media, we have been trying not to focus so much on the negative impact this economy has been having on us all, but rather, we have chosen to look forward and focus on all of the positive things that we have been doing (yes, we did say positive).

To begin – welcome to this very special issue of Future Fab. We are pleased to be able to bring you our first annual ITRS Focus issue. For the first time in our history, we are dedicating an entire issue of Future Fab to our newest collaborator: the International Technology Roadmap for Semiconductors (ITRS). We have a special introduction from the Chair of the ITRS, one of our longest-standing Editorial Board members, Dr. Paolo Gargini, who formally introduces the ITRS content.

As for what else we have been up to in the halls of Mazik Media, our transfer away from paper to the digital realm has proven to be one of the wisest and most timely decisions that has been made in the 13 years that Future Fab Int'l has been in existence. It's no secret that in an age of free and real-time information, publishing in general – and B2B publishing specifically – is an endangered species. As the world evolves, we MUST evolve with it, and so after taking our first steps into the all-digital world (over a year ago), we're now embarking on rolling out a series of new products & services that are going to aid our digital expansion and give our readers a whole new way to connect & collaborate (that's a hint, by the way) in this rapidly evolving and unpredictable market. The first of these services will be Future Fab Connect – which you may already know about, but if you don't, fear not; word will reach you soon.

For now – read on, and from all of us here, we thank you for your continued support and wish you all a Happy New Year.

Nikki Wood Matt Grimshaw

converse@mazikmedia.com

Paolo A. Gargini
Chairman of the International Technology Roadmap for Semiconductors (ITRS)

For more than four decades, the semiconductor industry has been guided by Moore's Law. First introduced in 1965 by Dr. Gordon Moore – one of the founders of Fairchild Semiconductor in 1957 – it projected a doubling of the number of transistors every year for the subsequent decade; this Law was further revised in 1975, as Dr. Moore had then become one of the founders of Intel Corporation in 1968. The new prediction stated that the number of components per chip will double roughly every 24 months for the foreseeable future. The most significant result of this law occurs in the continuously decreasing of cost-per-function by 50 percent every two years. This unbelievable cost reduction benefit, unprecedented in any other industry, has led to significant improvements in economic productivity and overall quality of life through proliferation of computers, communication and other industrial and consumer electronics. Think of what life would be like without cell phones, portable computers, the Internet, car navigation, DVD players and all the other devices that have become "indispensable" elements of our lives.

In 1972, Robert Dennard published a set of equations and derived several guidelines that provided simple rules on how to scale down all the vertical and horizontal physical dimensions of a transistor in conjunction with many other physical parameters. These equations accurately predicted how the electrical performance of the scaled-down transistor would behave. This methodology was referred to, for simplicity, as "transistor scaling."

In the last three decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia and other cooperative ventures. To help guide these R&D programs, the Semiconductor Industry Association (SIA) initiated The National Technology Roadmap for Semiconductors (NTRS), which had 1992, 1994 and 1997 editions. In 1998, the SIA was joined by corresponding industry associations in Europe, Japan, Korea and Taiwan to participate in a 1998 update of the Roadmap, and to begin work toward the first International Technology Roadmap for Semiconductors (ITRS), published in 1999. Since then, the ITRS has been updated in even-numbered years and fully revised in odd-numbered years. The overall objective of the ITRS is to present industrywide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, universities, governments and other research providers. The ITRS has improved the quality of R&D investment decisions made at all levels, and has helped channel research efforts to areas that most need research breakthroughs.

The ITRS is a dynamic process, evident by the evolution of the ITRS documents. Since 2001, the ITRS has responded by introducing new chapters on System Drivers (2001); Emerging Research Devices, and Radio Frequency and Analog/Mixed-Signal Technologies for Wireless Communications (2005); and, in 2007, Emerging Research Materials, to better reflect this evolution of the semiconductor industry. The 2008 edition also began to address the subject of Energy.

In order to properly represent the continuously evolving facets of the semiconductor industry as it morphs into new and more-functional devices in response to the broadening requirements of new customers, the 2008 ITRS has addressed the concept of Functional Diversification ("More than Moore"). This new definition (MtM) addresses an emerging category of devices that incorporate functionalities that do not necessarily scale according to "Moore's Law," but provide additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the nondigital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board level into a particular package-level System in Package (SiP) or chip-level System on Chip (SoC) potential solution, and ultimately into Stacked Chip SOC (SCS).

It is forecasted that by the end of the next decade, it will be necessary to augment the capabilities of the CMOS process by introducing multiple new devices that will hopefully realize some properties beyond those of CMOS devices. However, it is believed that most likely these new devices will not have all the properties of CMOS devices, and therefore it is anticipated that heterogeneous integration either at the chip level or at the package level will integrate these new capabilities around a CMOS core.

The participation and continued consensus of semiconductor experts from Europe, Japan, Korea, Taiwan and the U.S. will ensure that the 2008 ITRS remains the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology and the integrated circuit market. The complete 2008 ITRS and past editions of the ITRS are available for viewing and printing as electronic documents at the website http://www.itrs.net.

Beginning with this inaugural ITRS Special Focus Issue, Future Fab International will be bringing to readers a series of very comprehensive articles reporting on the ITRS highlights, written by each of the Technology Working Groups themselves, providing coverage of the latest 2008 update, chapter by chapter, and links back to the ITRS chapters on itrs.net. This is planned to be an annual collaborative event that will see the 2009 ITRS featured in the January 2010 issue, bringing the critical roadmap information to Future Fab's broad audience.

FRONT END OF LINE

BACK END OF LINE

METROLOGY, INSPECTION & FAILURE ANALYSIS

ASSEMBLY, TEST & PACKAGING TECHNOLOGIES

Biographies of Future Fab's Panel Members
For the full version of the following biographies, please click here.

Thomas Sonderman

Vice President, Manufacturing Systems Technology; AMD

Thomas Sonderman is the VP of Manufacturing Systems Technology for AMD. He obtained a B.S. in chemical engineering from the Missouri University of Science and Technology in 1986 and an M.S. in electrical engineering from National Technological University in 1991. He is the author of 43 patents and has published numerous articles in the area of automated control and manufacturing technology.

Luigi Colombo

TI Fellow

Dr. Luigi Colombo is a TI Fellow working on the Nanoelectronic Research Initiative (NRI). He has led the development of high-k dielectrics for CMOS devices, and HgCdTe for infrared detectors. He is author and co-author of over 130 publications, three book chapters, and holds over 60 U.S. patents. Dr. Colombo received his Ph.D. in materials science from the University of Rochester.

Paolo A. Gargini

Director of Technology Strategy for Intel Corporation

Dr. Paolo Gargini is the director of Technology Strategy for Intel Corporation in Santa Clara, Calif. He is also responsible for worldwide research activities conducted outside Intel for the Technology and Manufacturing Group by consortia, institutes and universities. Dr. Gargini received doctorates in electrical engineering and physics from the Universita di Bologna, Italy.

Alain Charles Diebold

Empire Innovation Professor of Nanoscale Science, College of Nanoscale Science and Engineering, University at Albany; AVS Fellow; Senior Member of IEEE

Alain's research focuses on the impact of nanoscale dimensions on the physical properties of materials. He also works in the area of nanoelectronics metrology. Alain is a member of the International Metrology Technical Working Group, founder and co-chair of the U.S. Metrology Technical Working Group for the 2007 International Technology Roadmap for Semiconductors, and chair of the Manufacturing Science and Technology Group of the American Vacuum Society.

Daniel J. C. Herr

Director of Nanomanufacturing Science Research, Semiconductor Research Corporation; SPIE Fellow

Dr. Herr leads a team that provides vision, guidance and leveraged support for collaborative university research in emerging nanoelectronics-related materials and assembly methods, environmentally benign high-performance manufacturing and future factory technologies. He is an adjunct associate professor in materials science and engineering at North Carolina State University, where he also serves as a graduate thesis advisor.

Janice M. Golda

Director, Lithography Capital Equipment Development; Intel

Janice Golda manages an organization responsible for creating strategies and working with Intel's lithography, mask and metrology suppliers and subsuppliers to deliver equipment meeting Intel's roadmap technology, capacity and cost requirements. She is a member of the Berkeley CXRO Advisory committee, is Chairman of the Board for the EUV LLC and holds one U.S. patent. She earned her B.S. in electrical engineering from Cornell University.

Steve Greathouse

Global Microelectronics Process Owner; Plexus Corporation, Nampa, Idaho

Steve Greathouse is the Global Microelectronics Process Technology manager at Plexus Corporation, in Nampa, Idaho, responsible for the development and deployment of microelectronic devices worldwide for Plexus. He has published many articles on technical topics related to semiconductor packaging, failure analysis and lead-free packaging. Steve has a B.S. in electronic physics from Weber State University with advanced studies in material science and computer science.

Daniel C. Edelstein

IBM Fellow; Manager, BEOL Technology Strategy, IBM's T.J. Watson Research Center

Dr. Edelstein is an IBM Fellow, and Manager of BEOL Technology Strategy at IBM's T. J. Watson Research Center. He played a leadership role in IBM's industry-first "Cu Chip" technology in 1997, in the introduction to manufacturing of Cu/Low-k insulation in 2004, and most recently in the airgap wiring announcement. Dr. Edelstein received his B.S., M.S., and Ph.D. degrees in Applied Physics from Cornell University.

William T. Chen

Senior Technical Advisor, ASE (U.S.) Inc.

William (Bill) Chen is senior technical advisor at ASE (U.S.) Inc. He is the co-chair of the ITRS Assembly and Packaging International Technical Working Group. Bill has published extensively in the fields of microelectronics packaging and mechanics of materials. He has been elected a Fellow of IEEE and a Fellow of ASME. Bill received his B.Sc. at University of London, M Sc at Brown University and Ph.D. at Cornell University.

Pushkar Apte

Vice President of Technology Programs, Semiconductor Industry Association

Dr. Pushkar Apte is currently the vice president of Technology Programs at the Semiconductor Industry Association. He received his master's and Ph.D. degrees from Stanford University in materials science and electrical engineering, and his bachelor's degree in ceramic engineering from the Institute of Technology, Varanasi, India. Dr. Apte has worked with Texas Instruments Incorporated on cutting-edge research and technology development, and with McKinsey & Company as their global semiconductor business expert.

Christian Boit

Head of Semiconductor Devices at Berlin University of Technology, Germany

The Berlin University of Technology is an institution for research and development in the areas of device simulation, technology, characterization and reliability. Christian Boit received a diploma in physics and a Ph.D. in electrical engineering on power devices, then joined Siemens AG's Research Laboratories for Semiconductor Electronics in Munich and has been a pioneer on photoemission.

Alan Weber

President, Alan Weber & Associates

Alan's consulting company specializes in semiconductor advanced process control, e-diagnostics and other related manufacturing systems technologies. He was previously the VP/GM of the KLA-Tencor Control Solutions division, acquired from ObjectSpace in March 2000. Prior to that, he spent eight years at SEMATECH and 16 years at TI. He has a bachelor's and a master's degree in electrical engineering from Rice University.

Peter Rabkin

Director of Device and Process Technology, Sandisk Corp.

Dr. Peter Rabkin is director of Device and Process Technology at Sandisk Corp., focusing on development of novel 3D memory technologies and products. Previously, he served as program director for Advanced Technology Development at Xilinx, Inc., responsible for process-to-design integration and DFM. Dr. Rabkin holds a master's degree in physics from Tartu University and a Ph.D. in physics of semiconductors from the St. Petersburg Institute of Physics and Technology.

Kazuyoshi "Kazu" Yamada

VP & General Manager, Custom SoC Solutions Group, NEC Electronics America, Inc.

Kazu Yamada oversees the company's custom ASIC-related business as well as engineering and system memory and power management business. In his 25-plus years with NEC companies, he has held several key positions in marketing and engineering. Mr. Yamada holds bachelor's and master's degrees in electrical engineering from the Musashi Institute of Technology in Tokyo and holds 20 patents in Japan for bipolar-related designs.

Giuseppe Fazio

Advanced Process and Equipment Control Sr. Engineer; Numonyx, Inc.

With a laurea degree in applied physics from Milan University, Giuseppe has working experience in several sectors, from research to industry, and vast experience in industrial and scientific instrumentation, as well as in the sector of components for industrial automation. After many years with ST Microelectronics, he is now in the R&D division of Numonyx. Giuseppe has authored and co-authored numerous articles, is an avid contributor at conferences and holds several patents in the semiconductor field.

Klaus-Dieter Rinnen

Director/Chief Analyst, Dataquest

Klaus-Dieter Rinnen is director for Dataquest's semiconductor and electronics manufacturing group, which covers trends and competitive positioning in semiconductor capital equipment, materials, contract manufacturing (foundry and SATS), and electronics manufacturing services. He received a diploma degree in physics with minors in physical chemistry and mechanical engineering in Germany, and a Ph.D. in applied physics from Stanford University.

Gilbert J. Declerck

President and CEO, IMEC

Gilbert Declerck is president and CEO of IMEC, Europe's largest independent research center in the field of microelectronics, nanotechnology, enabling design methods and technologies for ICT systems. He has authored and co-authored over 200 papers and conference contributions. Declerck received his Ph.D. in electrical engineering at the University of Leuven in 1972 and became a professor there in 1983.

John Schmitz

Vice President, NXP Semiconductors Research

Prior to working with NXP, John Schmitz served as VP and COO for manufacturing technology of SEMATECH from April 2002 to December 2005. There he launched the Advanced Technology Development Facility (ADTF) for-profit subsidiary as well as the International SEMATECH Manufacturing Initiative (ISMI) subsidiary. Schmitz holds a master's degree in chemistry, and a doctorate in physical chemistry, both from Radboud University of Nijmegen, Netherlands.

Lode Lauwers

Director Strategic Program Partnerships for Silicon Process and Device Technology at IMEC

Lode Lauwers has an M.S. in Electronics Engineering and a Ph.D. in Applied Sciences. He joined IMEC in 1985 as a researcher. In 1992, he became scientific advisor at IWT, and in 2000 general manager at Easics NV. He is currently Director Strategic Program Partnerships for Silicon Process and Device Technology at IMEC, managing IMEC's core partner research program on sub-32nm CMOS technologies.

Ernst Richter

Technology Transfer Manager, Inotera/Qimonda

Ernst Richter joined Inotera in Taiwan at its start-up in 2003, as Qimonda (previously Infineon) assignee for DRAM technology transfers. His professional employment in semiconductors started in 1998 at Siemens Corporate Research. He holds a Ph.D. and an M.Sc. in chemistry from the University of Regensburg and an M.Sc. in materials science from the University of Kent.

Ehrenfried Zschech

Sr. Manager, Center for Complex Analysis; AMD Fab36 LLC & Co KG

Ehrenfried Zschech has held this position in Dresden since joining in 1997, responsible for the analytical support for process control and technology development, as well as physical failure analysis. He received his diploma degree in solid-state physics and his Dr. rer. Nat. degree from Dresden University of Technology. He has published three books and more than 100 papers in scientific journals in the areas of solid-state physics and materials science. He is an honorary professor for nanomaterials at the Brandenburg University of Technology in Cottbus, Germany.

Steven E. Schulz

President and CEO, Silicon Integration Initiative, Inc.

Since 2002, Steve Schulz has served as president and CEO of Si2, the leading worldwide consortium of semiconductor and software companies chartered to develop EDA standards. Steve was previously employed by Texas Instruments for 19 years. He has a B.S. in electrical engineering from the University of Maryland at College Park, and an M.B.A. from the University of Texas at Dallas.

Raj N. Master

Senior AMD Fellow, Chief Technologist; Advanced Micro Devices

Raj Master manages the advanced packaging group involved in developing strategic enabling technologies and is also manager of the lead-free program of AMD. He joined AMD after spending 21 years at IBM, where he was a senior technical staff member. Master has 36 U.S. patents issued to him and has published more than 70 technical papers.

Stephen J. Buffat

Staff Research Scientist, Lockheed Martin

Stephen Buffat is a staff research scientist and operations manager of the Jordan Valley Innovation Center for Lockheed Martin in Springfield, Mo. He is an adjunct faculty member at the Center of Applied Science and Engineering/JVIC Center at Missouri State University. Stephen is responsible for the startup and operation of Lockheed Martin's nanotechnology facility and operation in Springfield, Mo. He has authored or co-authored numerous articles on photolithography, etch and 300 mm surface preparation process technologies.

Davide A. Lodi

Wet Processes & Metrology Engineering Manager, Numonyx, Inc.

Davide Lodi graduated from Milan University in 1997, having studied solid state physics, with a thesis on shape memory alloys. Soon after, he joined STMicroelectronics, where he started as a process engineer; after becoming the manager of Wet Processes and Metrology Engineering at the NVM R&D site in Agrate, Italy, he moved to Numonyx, where he holds the same position. He has authored and co-authored several papers in both fields.

John Caffall

Director of Operations, Submicron Development Center (SDC); Spansion Inc.

John Caffall is director of operations for the Submicron Development Center (SDC) at Spansion, the world's largest pure-play provider of Flash memory solutions. He is responsible for overseeing engineering, manufacturing and maintenance activities for the company's R&D center for advanced technologies for Flash memory. He holds an M.B.A. from San Jose State University and a B.S. in electronics engineering technology from the University of Houston.

Jeff Wetzel

Emerging Technology Manager, SVTC Technologies, LLC

Dr. Jeffrey (Jeff) T. Wetzel was recently appointed to the role of senior member of the Technical Staff of SVTC Technologies, LLC in Austin, Texas. His previous experience includes material characterization, tool, process and device integration at IBM, Motorola, SEMATECH and Tokyo Electron in engineering and management roles in silicon microelectronics R&D since 1983.

Peter Ramm

Head of Dept. Si Technology and VSI, Fraunhofer IZM, Munich

Peter Ramm received the physics and Dr. rer. nat. degrees from the University of Regensburg. He worked for Siemens in the DRAM facility and joined Fraunhofer in 1988 focusing on 3D integration technologies. Dr. Ramm is head of the Silicon Technology and VSI department at Fraunhofer IZM, Munich. He has authored over 50 papers and 20 patents, and is editor of the *Handbook of 3D Integration* (Wiley-VCH).

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FUTURE VISIONS AND CURRENT CONCERNS

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Pushkar Apte

Vice President of Technology Programs, Semiconductor Industry Association

Since 1965, "Moore's Law" has been the benchmark of the semiconductor industry's technological progress – primarily signifying progress in digital technology. While "Moore's Law" and digital scaling remain integral to industry progress, the ITRS also recognizes that there are additional ways of enhancing performance and capability. The industry is pursuing multiple paths for adding value for customers; for example, the "More than Moore" path, which involves incorporation of nondigital functionalities such as RF communication, power control, passive components, sensors and actuators to be incorporated into chip-level solutions. These nondigital functionalities do not necessarily scale according to Moore's Law, but provide added value to customers in different ways; for example, sensors to monitor tire pressure and traction for driving safety, or advanced wireless transceivers for clearer and more-reliable phone calls. The A/MS chapter covers in detail many of the technologies that enable these nondigital functionalities, and offers insight into potential new applications.

While we remain confident that we can continue to progress in accord with Moore's Law for another 10 to 15 years, we are approaching some limits to geometrical scaling. New materials already are being researched and introduced into production at a never-before pace, and we will soon go deeper into the nanotechnology era with new nanomaterials and nanomanufacturing techniques. These innovations bring up major ESH challenges, which the ESH chapter of ITRS explores in detail. It is clear that proactive ESH research will be necessary to ensure that these new nano-technologies can be introduced in an effective and safe way. In addition, the "environmental" part of ESH now addresses an element of global concern – energy. The ESH chapter and other roadmap chapters are exploring how we can set goals and quantify the energy savings that can be effected in fabs making chips, in chips themselves and in systems that use chips.

Future Fab Special ITRS Focus

ITRS CHAPTER: Environment, Safety & Health

Michael Mocella
DuPont Electronic Technologies

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The importance of ESH issues in the semiconductor industry is clearly stated in the ESH chapter's opening sentence of the 2007 ITRS: "The semiconductor industry views responsible action in environment, safety, and health (ESH) as critical to success. Continued ESH improvement is a major consideration for semiconductor manufacturers, whose business approach to ESH employs strategies that are integrated with manufacturing technologies, products, and services." With the recognized breadth of that integration, the ESH chapter influences, and is influenced by, a number of the ITRS' technical thrusts, most notably Interconnect, Front End Processing, Lithography, Assembly and Packaging, Emerging Research Materials, Yield Enhancement and Factory Integration.

The 2007 ITRS continued the historic focus on fundamental ESH concerns: the protection of employees, the public and the environment.

The 2007 ITRS continued the historic focus on fundamental ESH concerns: the protection of employees, the public and the environment. In addition, there was a recognition of the growing concerns both regarding climate change (energy usage and greenhouse gas emissions), as well as chemicals issues – beginning with waste disposal, but also including product content, and now more directly engaging the topic of precautionary limitations (or bans) on chemical use.

The overall issues are summarized in the ITRS-prescribed format of Difficult Challenges. For the 2007 ITRS, these were: Chemicals and Materials Management (chemical and materials selection), Process and Equipment Management (tool and process design), Facilities Technology Requirements (fab support systems), and Sustainability and Product Stewardship (design and decision making for product ecology and technology end of life). These Difficult Challenges serve three important ITRS functions:

1. They capture the inherent ESH considerations for evolving semiconductor technology (e.g., the need for nanomaterials assessment methodologies).
2. They highlight the need for incorporation of anticipated regulatory and legislative limitations into future technology planning.
3. They form a framework for evaluating each technical thrust: Such "cross-thrust filtering" provides the information needed for incorporation into the ITRS-prescribed ESH Technology Requirement tables.

For 2007, these five tables reflected the four ESH Difficult Challenges, as well as ESH Intrinsic Requirements. That last area is included so the scientists and engineers responsible for new technology development have an explicit target set for making ESH-related technology decisions. Finally, for 2007, there were four basic strategies embodied in the ESH tables that led to significant technology requirement revisions:

1. Understand (characterize) processes and materials to create a development baseline.
2. Use materials that are less hazardous or whose by-products are less hazardous.
3. Design products and systems (equipment and facilities) that consume fewer raw materials and resources.
4. Make the factory safe for employees.

For the 2008 Roadmap update, the primary ESH focus has been on updating the energy and water resource conservation requirements. Using a revised data and analysis model, it was evident that the 2007 ITRS requirements here were potentially in conflict (i.e., meeting one goal could drive up another). It was also clear from the analysis that water and energy use are mutually dependent, and therefore must have numerical values that reflect such dependence.

Looking forward to the 2009 Roadmap revision and beyond, a growing ESH challenge will be to focus on new technology development needs, while effectively anticipating ESH requirements expressed in public policy and regulatory agendas (see Figure 1). For most of the industry's history, a major role for ESH has been to respond to technology developments. However, policy decisions (at many levels, and both internal and external to the industry) will increasingly begin to impact the technologies which

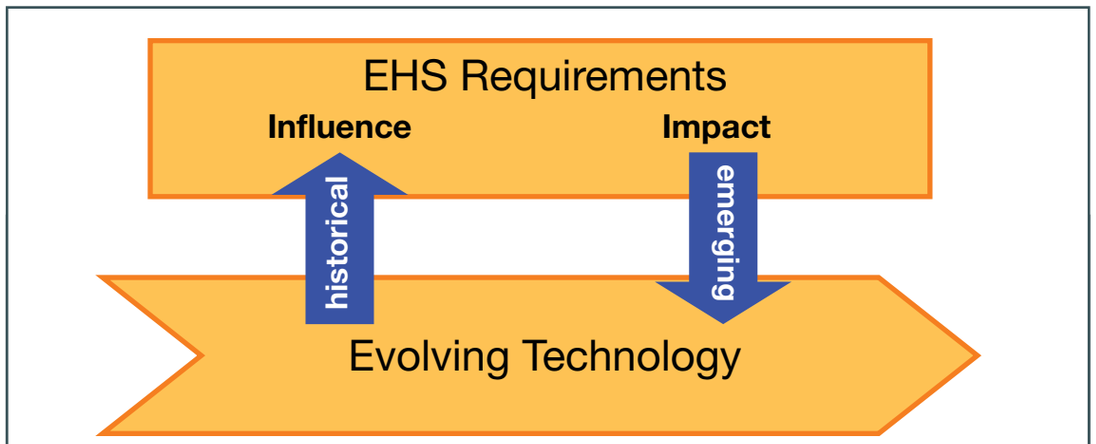

Figure 1. The Relationships Between Technology Evolution and ESH Requirements

can be brought into manufacturing. For example, there are emerging needs for new and exotic materials that have little ESH characterization (both in the precursors used, and the processes practiced with them), but are necessary to achieve device performance in areas such as improved energy efficiency. In addition, energy-intensive processes such as EUV lithography (a leading patterning candidate for sub-32nm processing) are in potential conflict with improved energy conservation goals. As a final example, trends toward different chemical restrictions among the many political geographies in which the semiconductor industry operates make it difficult to develop global technology for a global industry.

Summation

In summary, the ESH Roadmap provides a framework both for engineers and research scientists to design and create new wafer processing and assembly technologies in which ESH is an integral part. The results must meet local, national and international needs, with positive impact on cost, technical performance and product timing. They must also minimize risk, public and employee health effects and environmental impact. Solutions must be timely, yet far reaching, to assure long-term success. To this end, the 2009 ESH Roadmap will finalize the development of an ESH Risk Prioritization scheme. This effort will characterize ESH Technical Requirements that are critical to manufacturing technology implementation, versus those that are enabling (mitigating limits on the technology) or improving (compared with the ESH technology in prior generations).

Acknowledgments

The work of the regional ESH DTWGs, and of our technical thrust partners (especially Andreas Neuber of Applied Materials), are essential to the development of the ESH Roadmap. Coordination of this overall effort is by the ESH ITWG, co-chaired by Jim Jewett (Intel) and Tetsu Tomine (Seiko Epson); other members include myself, Hans-Peter Bipp (Infineon), Joey Lu (TSIA), Joseph Mou (TSIA), Takayuki Ohgoshi (NEC Electronics) and Harry Thewissen (NXP).

For most of the industry's history, a major role for ESH has been to respond to technology developments.

About the Author

Michael Mocella

Michael Mocella is the Technology Planning Manager for DuPont Electronic Technologies' Semiconductor Fabrication Materials business, where he focuses on new materials and processes for the IC industry. He has been a member of the ITRS' US ESH DTWG since its inception in 1996, and is currently co-chair of that group. ■

- Link to 2007 ITRS ESH Chapter
- Link to 2008 ITRS Update Table (download CROSSCUT.xls)

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ITRS CHAPTER: RF and A/MS Technologies for Wireless Communications*+

Herbert S. Bennett,[1] Margaret Huang,[2] John J. Pekarik[3]
[1]National Institute of Standards and Technology, [2]Freescale Semiconductors, Inc.
[3]International Business Machines Corporation

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Scope

The demands to bring new and advanced features in various wireless and mobile communication products continue to drive the revenue growth of semiconductor ICs used for wireless and mobile communications.[1-4] (A list of acronyms is at the end of this article.) The RF and AMS devices in these products depend on many materials systems, some of which are compatible with CMOS processing, such as SiGe, and others of which are not compatible with CMOS processing, such as those compound semiconductors composed of elements from group III and V in the periodic table. As shown in Figure 1, wireless and mobile communications cover a very wide spectrum of applications, including radio and TV broadcasting, cellular phones (GSM, GPRS, EDGE, CDMA, 3GPP), wireless cables and wireless local area networks (Bluetooth, Wi-Fi, ZigBee), broadband wireless access (UWB, WiMAX), global position system, phased array RF systems, RFID and smart handheld devices. The impact of wireless and mobile communications on our daily lives has been significant, as they empower us to communicate voice, data, image and video to anywhere at anytime. In future years, it is expected that the frequency axis in Figure 2 will lose its significance in defining the boundaries among technologies for some of the applications listed therein.

The impact of wireless and mobile communications on our daily lives has been significant, as they empower us to communicate voice, data, image and video to anywhere at anytime.

RF and AMS ICs are the critical and enabling elements in these wireless and mobile communication applications. The drivers for wireless communications systems are cost, power consumption, functionality, size of mobile units, production volume, and standards and protocols. Also, RF technologies often require additional headroom with respect to performance because several conflicting or competing requirements must be met simultaneously. These include power-added efficiency, high output power, low current and low voltage. Increased RF performance for silicon is usually achieved by geometrical scaling. Increased RF performance for III-V compound semiconductors is achieved by optimizing carrier transport properties through materials and band gap engineering. During the last two decades, technologies based on III-V compounds have established new business opportunities for wireless communications systems. When high volumes of product are expected, silicon, and more recently silicon-germanium, replace the III-Vs in those markets for which these group IVs can deliver appropriate performance at low cost. The wireless communication circuits considered as application drivers for this roadmap may be classified into AMS circuits (including analog-to-digital and digital-to-analog converters), RF transceiver circuits (including LNAs, frequency synthesizers, VCOs, driver amplifiers and filters) and PAs.

Figure 2 shows the circuit functions of a typical mobile communication system with operating or carrier frequencies of the wireless systems between 0.8 GHz and 10 GHz. The four basic circuit functions shown therein are power management, PA, RF transceiver and, AMS, which interfaces with the digital signal processor. The RF and AMS 2008 ITRS Update considers the latter three circuit functions that drive RF and analog technology needs. The roadmap is subdivided into technologies for applications below 10GHz (CMOS, bipolar, passives and power amplifier) and those above (mm-wave roadmap).

In 2007, the wireless roadmap was expanded to include a new section on "More than Moore" that includes discussions on solutions to realize multiband, multimode portable applications. RFMEMS and embedded passives requirements are added, which are considered essential technologies to realize the switching filtering network and added handheld user interface.

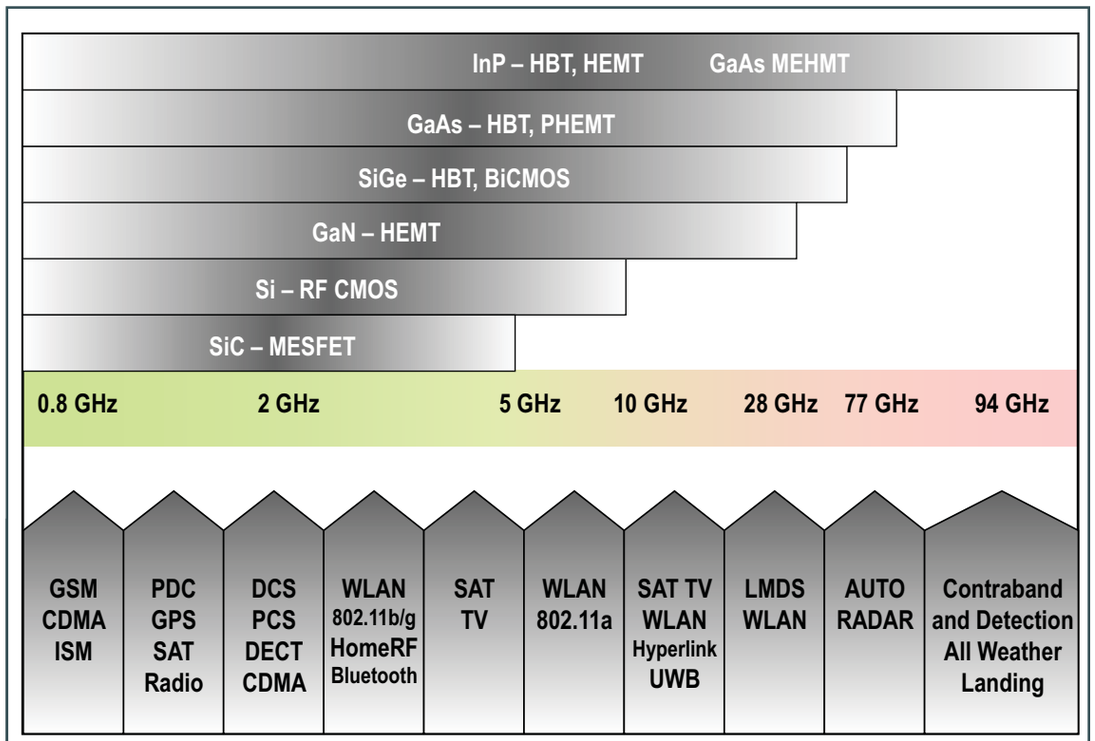

Figure 1. Applications Spectrum

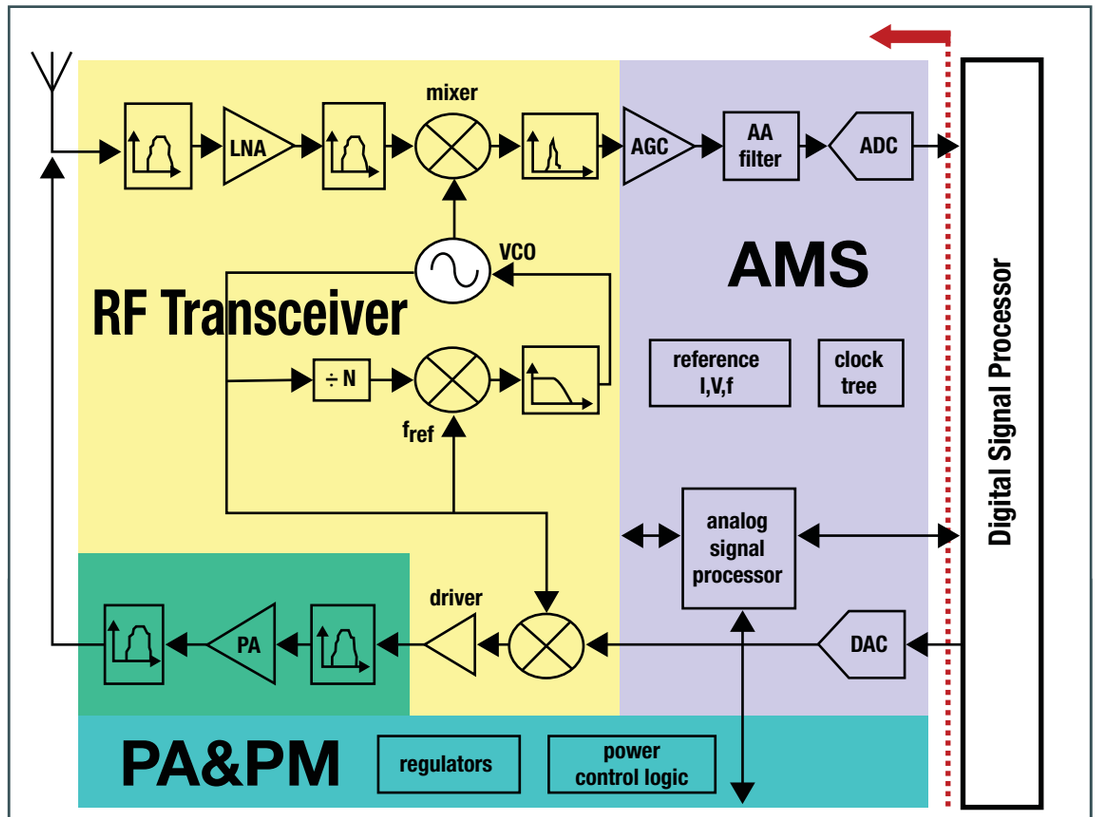

Figure 2. Circuit Functions

What Is New in the 2008 ITRS Update of Technical Requirements Tables for Radio Frequency and Analog/Mixed-Signal Technologies for Wireless Communications?

RF and AMS CMOS – The technology requirements tables are linked with PIDS. The Performance RF/Analog table is linked to low stand-by power CMOS with a one-year lag and the mm-wave CMOS is linked to high-performance CMOS with a two-year lag. The RF analog parameters now reflect the ORTC update of gate length scaling with year. The mm-wave noise figure scaling now matches published data and requirements for 94 GHz are added.

RF and AMS Bipolar Devices – Minor adjustments made in the tables to align PA bipolar requirements with recently published data.

On Chip and Embedded Passives for RF and Analog – MIM and MOM capacity density, varactor Q and inductor Q have all been updated to be consistent with new published data. The capacitor density was lowered to reflect new forecasts on the actual requirements for this application.

Power Amplifiers (0.8 GHz–10 GHz) – Due to the technical challenges associated with battery advances, the end-of-life battery voltage remains at 2.4 V to 2020 instead of at 1.6 V as stated in the 2007 Chapter.

MEMS – The table maintains the four device choices of bulk acoustic wave (BAW), resonator, switch with capacitive contacts, and switch with metal contact. Each of these devices will be treated with more details in the 2009 RF and AM Chapter. Specific performance and cost-driver applications will be added and design tool requirements will be clarified.

Millimeter Wave (10 GHz–100 GHz) – The geometry scaling for most III-V technologies is delayed by one to two years to be consistent with trends in industry. In general, the mm-wave tables reflect the migration from GaAs PHEMT to alternate III-V technologies.

2009 RF and AMS Challenges

Some portions of the RF and AMS technology roadmap reflect prototype capabilities rather than volume production as in most of the other ITRS Chapters. Production requires markets. But in certain emerging applications, such as mm-wave connectivity and imaging applications, markets currently lag technology capabilities as predicted by the roadmap.

In 2009, we plan to add discussions on whether the entries in the technical requirements tables correspond to technologies that are prototype-capable versus in-production.

In 2009, we plan to add discussions on whether the entries in the technical requirements tables correspond to technologies that are prototype-capable versus in-production. We also hope to create a matrix of applications and corresponding technologies. Other specific technology challenges include: the need of alternate high gain and high voltage CMOS device, especially since digital CMOS scaling greatly degrades gain and voltage handling performance; impact of fully depleted/double gate devices and other emerging research devices on RF and AMS performance; and expanding MEMS device list to cover microphones, accelerometers and gyroscopes, which have increasing influence in mobile device user interface. Integrated MEMS devices will add challenges in the area of design tools and packaging. In addition to handling EM and thermal simulation, added mechanical simulation needs to be considered. Unique reliable packaging requirements needed for MEMS need to be addressed while maintaining overall low-cost product.

Integrated MEMS devices will add challenges in the area of design tools and packaging.

* *All views expressed in this paper are those of the authors and of others to whom attributions are given and are not necessarily those of the ITRS nor of the authors' host institutions (NIST, Free-scale and IBM) nor of any of the institutions cited therein. Certain commercial equipment, instruments or materials are identified in this article to specify experimental or theoretical procedures. Such identification does not imply recommendation by any of the host institutions of the authors, nor does it imply that the equipment or materials are necessarily the best available for the intended purpose.*

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References

1. Worldwide WiMAX Semiconductor 2006–2010 Forecast and Analysis, IDC, February 2006.
2. WiMAX: Wireless Super-Chips, In-Stat, November 2005.
3. Worldwide WLAN Semiconductor 2005–2009 Forecast, IDC, April 2005.
4. Forecast: Mobile Phone Production and Semiconductor Market, Worldwide, 2003–2010, 1Q06 Update, Gartner, March 2006.

Acronyms

AMS	Analog/mixed-signal
CDMA	Code division multiple access
CMOS	Complementary metal oxide semiconductor
EDGE	Enhanced data rates for GSM evolution
GPRS	General packet radio service
GSM	Global system for mobile
IC	Integrated circuit
LNA	Low noise amplifier
MEMS	Microelectromechanical system
MIM	Metal insulator metal
MOM	Metal oxide metal
ORTC	Overall roadmap technology characteristics
PA	Power amplifier
PHEMT	Pseudomorphic high electron mobility transistor
PIDS	Process integration, devices and structures
RF	Radio frequency
RFID	Radio frequency identification
RFMEMS	Radio frequency microelectromechanical system
UWB	Ultra-wideband
VCO	Voltage controlled oscillators
Wi-Fi	Trade name for IEEE 802.11 wireless technologies
WiMAX	Worldwide interoperability for microwave access

WPAN	Wireless personal area networks
ZigBee	Protocols based on the IEEE 802.15.4-2006 standard
3GPP	3rd-generation partnership project

Acknowledgments

We thank the members of the ITRS RF and AMS Working Group (*listed below*) for their numerous contributions to the ITRS 2008 Update and for their continued efforts in developing a global consensus on technical requirements and challenges for RF and AMS technologies. We thank members of other ITRS Working Groups for their helpful comments and discussions, and acknowledge the guidance of the ITRS International Roadmap Committee under the leadership of Paolo Gargini. All of us thank our respective companies, universities and government agencies for their continued financial support of our activities in technology road-mapping.

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- Link to 2007 ITRS RF & A/MS for Wireless Chapter
- Link to 2008 ITRS Update Table (download FOCUS_A.xls)

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NEW TECHNOLOGIES & DEVICE STRUCTURES

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John Schmitz
VP Process Technology Research, NXP Semiconductors

The Electronic Landscape in the Next Decade

In addition to the current economic turmoil and the downward revenues trend in existence for several years now, our industry also faces tough technology barriers to overcome. The million-dollar question is, indeed, how to maintain the CMOS scaling rat race. To overcome the immense scaling problems, we must now resort to nearly the entire periodic system (copper, low-I, high-κ, CESL, Si-Ge, etc.) as well as new devices (nanotubes, finFETs, spintronics, etc).

The real problem of this combination of new materials and new devices is that we run quickly into dealing with a multidimensional space. Of course, that in itself is an interesting situation for an R&D community, but it may be a formidable problem to come up with a sensible solution in an acceptable time period. It is therefore that within the ITRS community two working groups have been established: the Emerging Research Devices and the Emerging Research Materials Working Groups. They have been charged with the question of what in that multidimensional space of materials and devices are the most likely combinations that could serve as the successors of the current devices in sub-16nm technology nodes.

In this section, we have two papers that provide the first approach and answers to these questions: "Emerging Research Devices" by James A. Hutchby and Michael Garner, and "Emerging Research Materials" by Michael Garner, Daniel Herr and Yuji Awano.

At the same time, we see everywhere more and more emphasis on a parallel R&D process in the electronic landscape, namely that of "More than Moore." In fact, here we are also dealing with new devices as well as new materials in order to let mixed-signal electronic circuits interact with the analog world. Here also we have the challenge of finding our way in a multidimensional space. The big difference with the CMOS scaling, however, is that of dimensions. In many applications, no sub-90nm dimensions are required, but such issues as 3D integration, materials and costs are of key importance.

I expect that both the scaling activities as well as the More than Moore research will produce exciting results in the decade to come.

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ITRS CHAPTER: Emerging Research Devices

James A. Hutchby,[1] Michael Garner[2]
[1]Semiconductor Research Corporation, [2]Intel Corporation

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Introduction

Over the past 40 years, geometrical and performance scaling of silicon CMOS integrated circuit technology has enabled many affordable new products for business and consumer applications. Recognizing that scaling of CMOS is becoming increasingly difficult, the global electronics research community has begun an intense search for a new device paradigm for extending information processing technology for decades into the future. Research approaches include new charge-based devices such as single electron transistors (SETs), nanowire crossbar approaches (e.g., CMOL), spin-based approaches including magnetic or collective spin (e.g., ferromagnetic) and single particle spin-based devices (e.g., spin transfer torque devices). Other approaches include nano-electromechanical devices, atomic or electrochemical metallization switches and carbon-based nanoelectronics. Some of these technologies have the potential to extend

Device Technology Entry	Augment/Extend CMOS	Beyond CMOS
Nanoelectromechanical Switch	X	
Spin Transfer Torque		X
Collective Strongly Correlated Many-electron Spin Devices		X
Carbon-based Nanoelectronics	X	X
Atomic/Electrochemical Metallization Switches		X
Single Electron Transistors	X	
CMOL/FPNI	X	

Table 1. Domain of Impact for Seven Device Technologies Chosen for This Study

CMOS somewhat beyond its currently projected limit, while others may provide a new, highly scalable paradigm for "Beyond CMOS" information processing.

The ITRS' International Roadmap Committee (IRC) recognized that it is timely to accelerate development of one or two of the most promising proposals for well-defined new information processing devices. As a result, they requested the Emerging Research Devices (ERD) and Emerging Research Materials (ERM) Working Groups to recommend one or two of the most promising device technologies for detailed roadmapping and accelerated development.

The ERD/ERM Working Groups responded by conducting a workshop titled "Maturity Evaluation for Selected Beyond CMOS Emerging Technologies" followed immediately by an ERD/ERM Working Group meeting to develop our recommendation to the ITRS IRC.[1] This is the report of the ERD/ERM Working Group evaluation and recommendation.

The domain of impact for each of seven technologies evaluated in this study is shown in Table 1. Note that Carbon-based Nanoelectronics is the only entry that may extend CMOS and provide a new "Beyond CMOS" paradigm.

Objective and Scope

Objective

The objective of this study was evaluation of several "Beyond CMOS" candidate information processing technologies, followed by selection and detailed technology roadmapping of one or two promising specific candidates for paradigm shifting information processing. These candidates were recommended to the semiconductor industry via the ITRS' IRC for *its* decision regarding intensified research and development. In addition, the ERD/ERM Working Groups will provide more detailed roadmapping in their 2009 ITRS chapters.

Scope

As a minimum, evaluation of each candidate device technology addressed the following:

- A brief description of the device technology proposed, including its physics of operation in processing information and the means for interconnecting its primitive unit cells and providing input/output functions.
- The potential for extending the candidate technology for multiple generations in terms of device and/or functional density beyond density projected for ultimately scaled CMOS.
- A plausible means of fabricating a unit cell and a simple higher-level functional circuit.
- Other potential performance benefits offered by the proposed technology (e.g., speed, power dissipation, gain, bit throughput, etc.)
- Current state-of-the art for the proposed technology using ultimately scaled CMOS as a benchmark.
- Key scientific and technological issues that must be addressed to realize the technology's full potential.

Process and Methodology

The process used was the following:

For each of the seven selected technologies, the workshop participants:

- Received expert inputs on the potential and readiness of each candidate technology for extending information processing beyond the 2022 time horizon of CMOS. The expert inputs included two presentations, one from a "proponent" and another from a "friendly critic." Each proponent also submitted a white paper as input to the workshop. A third participant summarized the inputs received from the experts and those from the workshop and meeting participants. This discussion served to clarify the current status, potential and remaining challenges for each technology to provide a new paradigm in information processing.
- The workshop formulated the critical path discussion/decision points to be considered by the Working Group meeting the day after the workshop.
- The ERD/ERM Working Groups considered if one or more of the seven candidate technologies are ready for accelerated research and development and detailed roadmapping.

Metrics

The metrics used in preparation of the Proponent white papers and presentations are based on the performance projected for ultimately scaled CMOS in 2022. These metrics are centered on those to be addressed by emerging information processing device technology, where information processing encompasses processing and manipulation of information, and may include a memory function.

These metrics use the silicon MOSFET as a model device to illustrate a response to the categories for this structure. However, the ultimately scaled MOSFET was not a candidate device considered in this exercise. The proponents typically addressed as many of the categories as they could using either quantitative or qualitative information. We also invited the proponents to add their own category(ies), particularly to the last two sections, titled "Potential" and "Limitations," if necessary, to most effectively advocate their approach.

Methodology

Candidate Technology Selection: The seven candidate technologies were selected by an email process of interaction with the ERD Working Group. A preliminary set of candidates were first proposed. This list was then edited through a substantial amount of group interaction, and the final list of seven candidate technologies was approved by the ERD Working Group.

Candidate Technology Evaluation: Two face-to-face meetings on contiguous days were used to complete this process. The all-day workshop was used to receive the Proponent and Friendly Critic presentations and to develop consensus summaries of pros and cons for each candidate technology. On the second day, the ERD/ERM Working Groups met to discuss and vote on the candidate options. The summary pros and cons for each candidate technology were further refined on this second day.

Results

Many technologies, each of varying maturity, were considered for their potential to scale information processing for decades beyond that accessible by ultimately scaled CMOS. The ERD/ERM Working Group chose seven candidate technologies for in-depth review to determine which are sufficiently appealing and/or mature to warrant accelerated development and more detailed roadmapping. These candidate technologies are outlined in Table 2. Each of the seven technologies selected for review has potential, and, in some cases, reasonable prospects for providing a new paradigm for information processing scalable beyond that offered by ultimately scaled CMOS in 2022. These devices are discussed and evaluated below.

The result of this workshop and the following ERD/ERM Working Group meeting was the ERD/ERM Working Group recommended to the IRC "Carbon-based Nanoelectronics" for accelerated research and development and detailed roadmapping targeting practical demonstration within five–10 years. Important factors in this recommendation were that Carbon-based Nanoelectronics may be used to extend CMOS to its ultimate performance and then be extended for "Beyond CMOS" technology.

Overview of Evaluated Technologies

The *nanoelectromechanical switch (NEMS)* and the *nanoelectromechanical FET (NEM-FET)* each offer a subthreshold slope S << 60mV/dec. This would allow the drain voltage, V_{dd}, to be substantially lower than that of a MOSFET, which would lower power dissipation by the square of the change in V_{dd} allowed by the reduction in the subthreshold slope. The NEMS switches and FETs, however, are slow (>1nsec) and still charge-based devices, subject to the same scaling limits as the MOSFET, and therefore have only limited scaling potential.

Spin Transfer Torque (STT) technology is emerging as a very promising approach to nonvolatile memory applications, by potentially increasing the bit density and lowering the power dissipation beyond that attainable by the magnetostatic RAM or MRAM. However, the STT RAM switching speed may be rather slow, and its meaningful application to logic that is highly scalable beyond CMOS is seen as very difficult.

Collective Strongly Correlated Many-electron Spin Device technology is emerging as a potentially fruitful domain of materials science and technology. In some cases, ferroelectric and ferromagnetic order parameters are coupled in multiferroic materials. An important advance in applying this phenomenon to information processing is demonstration of using spin transport via a "spin wave" as an information carrier or token without requiring concomitant charge transport. This requires sustaining the coherence of spin states enabling a spin wave, but avoids all limitations associated with the spatial movement of charge. Although this advance is quite important, there is no clear advantage of increasing functional density using spin waves due to their requirement for sizable waveguides. Also, the spin wave is quite slow, ~10^3 slower than a photonic wave.

Carbon-based Nanoelectronics has a major advantage in that the science and technologies resulting from accelerated development of carbon nanotubes (CNTs) and graphene nanoribbons (GNRs) for MOSFET applications can provide a substantial basis for exploring and developing new physical phenomena in these materials for "Beyond CMOS" information pro-

Device Structure	Device Parameters						
	State Variable	Control Variable	Density	Switching Speed	Switching Energy	Static Energy	Gain
MOSFET	Charge or Voltage	Electrostatic Potential	$1/F^2$	0.1ps	$4x10^{-18}$J	$V_{dd}*I_{off}$	g_m/g_d
NEMS Relay	Charge or Voltage	Atoms	$1/(F^2R)$	ns range	aJ range	~ 0J	
NEMFET	Charge or Voltage	Atoms	$1/(F^2R)$	ns range	aJ range	$V_{dd}*I_{off}$	g_m/g_d
Spin Transfer Torque	Charge or Voltage	Spin	$1/(4F^2)$	0.1 ns		0?	
Carbon-based Nanoelectronics	Charge or Voltage	Charge or Voltage	$1/F^2$	1fs	$0.5C_{load}*V_{dd}^2$	$V_{dd}*I_{off}$	g_m/g_d
Carbon-based "Quantum Interference"	Charge or Voltage	Quantum Interference?			V_{dd}^2/R_{load}	Depends on Device Architect	I_d*g_m
Atomic Switch or Electrochemical Metallization	Charge or Voltage	Atoms		ns range	$0.5C_{load}*V_{dd}^2$	$V_{dd}*I_{off}$	
Collective Spin Device	Spin	Spin Waves			1kT – 100kT		
SED/SET	Charge or Voltage	Electrostatic Potential	$1/F^2$	0.1ps	$0.5C_{load}*V_{dd}^2$	$V_{dd}*I_{off}$	
CMOL/FPNI	Charge or Voltage	Electrostatic Potential	$1/F_{nano}^2$	<100ns	$0.5C_{load}*V_{dd}^2$	$V_{dd}*I_{off}$	

Table 2. Candidate information processing technologies chosen by the ERD/ERM Working Group compared to a silicon MOSFET. (NEMS Relay and NEMFET are counted as one technology, as are the two Carbon-based Nanoelectronics entries. CMOL/FPNI is device architecture rather than a single device.). The MOSFET is shown for comparison and is not a candidate entry.

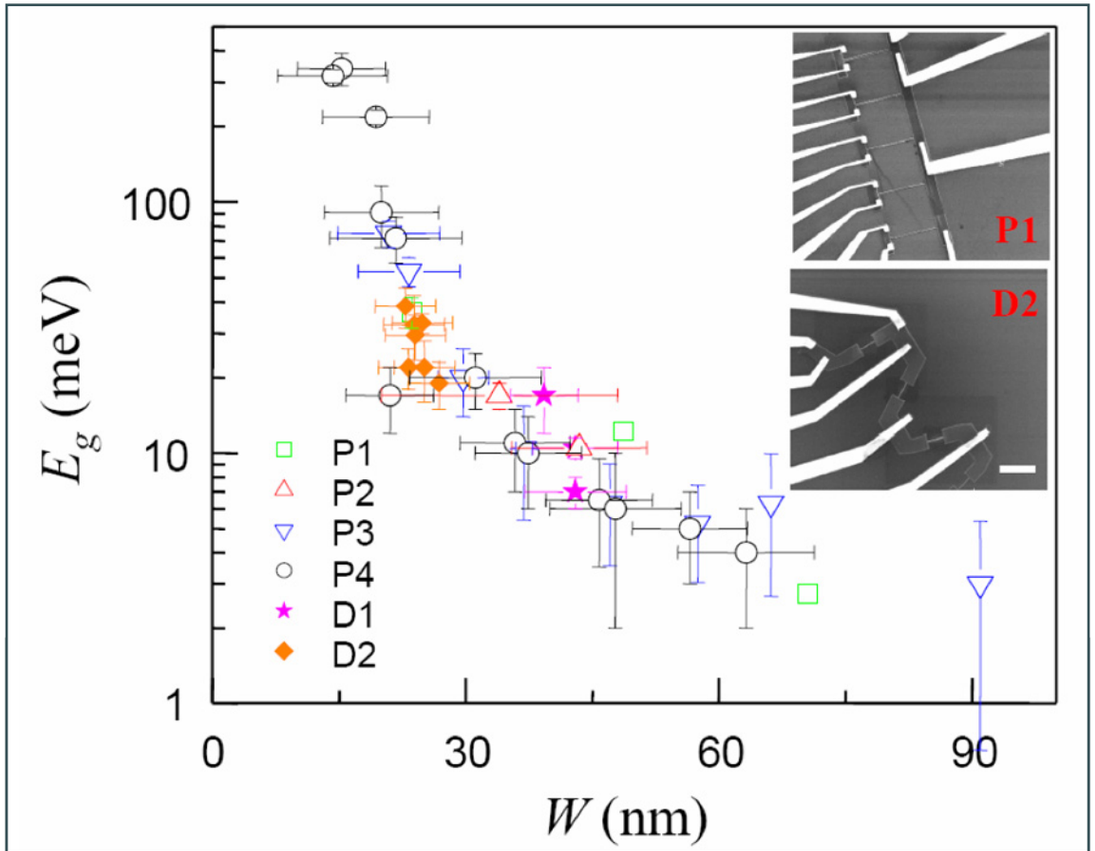

Figure 1. Energy gap versus width of the nanoribbons for six different device sets: four (P1-P4) of the parallel type, and two (D1, D2) with varying orientation. The inset shows SEM images of two representative device sets.

cessing paradigms. The field of Carbon-based Nanoelectronics has bifurcated into two related topics: carbon nanotubes and graphene. Carbon nanotubes, based on one or more layers of sp^2 bonded carbon atoms to form either single-wall or multi-wall cylinders of varying chirality, can be metallic or semiconducting. Exploration of CNTs for MOSFET applications has shown CNTs to have excellent electron transport properties, exhibiting ballistic transport over substantial distances. Using the cylindrical shape of CNTs in a vertical MOSFET format enables the ideal MOSFET structure, a "gate all around" transistor, which provides near-ideal gate control of the channel electrostatics. This would minimize short channel effects, e.g., drain-induced barrier lowering (DIBL). CNTs are also amenable to band-to-band-tunneling MOSFETs which could provide subthreshold slopes, S << 60mV/dec, leading to lower dissipated power. The major issue that has challenged CNT MOSFETs for some time is lack of a growth process to control placement, alignment, chirality, conductivity, diameter, single or multiple wall, energy band gap, etc. The second field in Carbon-based Nanoelectronics is founded on graphene, typically a single planar layer of sp^2 bonded carbon atoms. A graphene ribbon can be imagined as a CNT cut lengthwise and opened to form a mono-atomic ribbon or sheet of sp^2 bonded carbon atoms. Similar to CNT MOSFETs, a GNR MOSFET exhibits ballistic electron transport and excellent MOSFET properties.

However, while the CNT technology requires multiple CNT MOSFETs connected in parallel to achieve a desired I_{on}, the GNR MOSFET can achieve the required I_{on} by increasing the width of the transistor, although this will reduce the band gap energy of the channel (see Figure 1). Graphene also exhibits some new physical phenomena, e.g., "pseudospin," zero effective mass charge carriers, band gap energy as a function of ribbon width (Figure 1), etc. These properties may be exploited to realize a new charge-transport independent paradigm for information processing. Examples of possible new applications of graphene are illustrated in Figure 2. A major issue challenging development of graphene is lack of a reasonable process for growing graphene epitaxially on a suitable substrate. Also, new paradigms to exploit graphene for Beyond CMOS information processing applications await discovery.

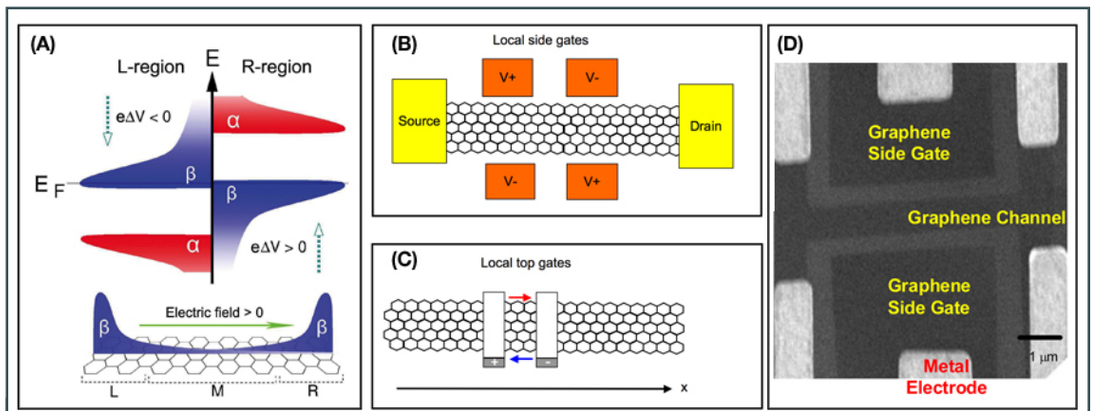

Figure 2. (A) Top: with a transverse electric field, the electrostatic potential on the left edge is lowered (eΔV< 0), whereas the one on the right edge is raised (eΔV> 0). Correspondingly, the energies of the localized states at the left edge are decreased and those of the localized states at the right edge are increased. Bottom: the resulting states at EF are only, β-spin and spin polarized current is allowed. (B) Schematic diagram for spin filter switch based on local side gate control of spin polarized edge currents. (C) Schematic diagram for valley filter switch based on local top gate control of valley polarized edge currents. (D) SEM picture of a patterned graphene bar with side electrodes for local gating local gate. Scale bar represents 1μm. *2(A): From "Half-metallic graphene nanoribbons," Young-Woo Son, Marvin L. Cohen and Steven G. Louie, Nature 444, pp 347-349 (Nov. 16, 2006) i:10.1038/nature05180; 2(D): From private communication with Philip Kim of Columbia University*

Atomic/Electrochemical Metallization Switches and their derivatives, operating via creation and annihilation of conducting filaments, are scalable and very attractive for dense nonvolatile memory applications. They are compatible with CMOS/ CMOL architecture and require a relatively simple fabrication process. Major issues challenging their application to logic are lack of a gain mechanism, a relatively slow switching time (1-10ns) and low power operation.

Single Electron Transistors (SETs) operate by transferring electrons one at a time from a source to a quantum dot and subsequently from the dot to a drain. Both transfers are accomplished via a tunneling process moderated by a gate potential controlling a Coulomb blockade mechanism. While using the mechanism for electron tunneling to and from a quantum dot to operate, the SET behaves much like a MOSFET to enable voltage-state logic. The same Coulomb blocking mechanism can be used to enable charge-state logic using a mechanism for transferring charge between quantum dots. One challenge facing voltage-state logic (in which SETs are integrated with MOSFETs) is V_{th} fluctuation caused by random fluctuations related to background charges. Another is lack of a fabrication process with acceptable controllability and scalability. Two important issues related to charge-state logic are: 1) a significant error rate requiring new error correction technology, and 2) the need for a clock to maintain unidirectional flow of data.

CMOL, and its relative, *FPNI (Field Programmable Nanowire Interconnect)*, are technologies proposed to reliably integrate nano-scaled variable resistive devices embedded in a crossbar structure of nanowires with substantially larger CMOS gates, accomplished without requiring nano-scale alignment accuracy. CMOL is proposed to provide memory and logic functions, whereas FPNI is intended to provide switches for programming an underlying CMOS chip. A study of the CMOL approach was conducted by the Friendly Critic in preparation for this workshop. The study concluded that CMOL offers a density advantage of 100-400x for a speed reduction of 1/10th compared to CMOS FPGA, but CMOL does not offer an advantage in gate density or performance compared to CMOS ASICs. Consequently, CMOL and FPNI may offer an advantage in scaling of density, but they are not a solution for power and speed. In addition, fabrication of CMOL is very difficult, if not prohibitive. Conversely, fabrication of FPNI appears to be attainable, but FPNI offers limited functionality. In summary, CMOL/ FPNI offers a possibly attractive incremental extension of CMOS beyond the 2022 time horizon, but they do not appear to offer an information processing technology addressing the "Beyond CMOS" domain.

Topic	Proponent	Friendly Critic	Summarizer
NEMS	Kerem Akarvardar Adrian Ionescu	David Elata	Paul Franzon
Spin Transfer Torque	Jim Allen	Supryo Bandyopadhyay	George Bourianoff
Collective Strongly Correlated Many-electron Spin Devices	Kang Wang	Eli Yablonovitch	Sadasivan Shankar
Carbon-based Nanoelectronics	Philip Kim	Ali Javey	Michel Brillouet
Atomic/Electrochemical Switches	Philip Kuekes	An Chen	Wilfried Haensch
Single Electron Transistors	Akira Fujiwara	Konstantin Likharev	Toshiro Hiramoto
CMOL/FPNI	Konstantin Likharev	Andre DeHon	Erik DeBenedictis

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Endnote

1. In no sense does this mean that research addressing emerging research device technologies not selected for accelerated development should be abandoned. Conversely, the ERD Working Group believes that several promising candidate technologies considered in this exercise, but not recommended for accelerated development at this time, should remain the subject of fundamental research to clarify their potential.

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• Link to 2007 ITRS Emerging Research Devices Chapter
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ITRS CHAPTER: Emerging Research Materials

C. Michael Garner,[1] Daniel Herr,[2] Yuji Awano[3]
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For more than three decades, between the mid-1960s through the mid-1990s, only a few new materials were added into an integrated circuit technology and modifications to interconnect metallurgies. During that period, the few new materials integrated into the process flow typically offered evolutionary enhancements; however, since the mid-1990s, each new technology generation incorporated several new materials technologies. By 2003, with the emergence of high dielectric constant (κ) materials in transistors, the International Roadmap Committee (IRC) identified the need to add emerging research materials to the Emerging Research Devices (ERD) Inter-national Technology Working Group (ITWG). In 2005, the International Technology Roadmap for Semiconductors (ITRS) ERD chapter added a section on device-related research materials, which included low-dimensional materials (nanotubes & nanowires), materials for molecular devices, materials for spin-based devices and strongly correlated electron state materials. In 2006, the IRC chartered an Emerging Research Materials (ERM) ITWG to identify and track research materials that had the potential to provide solutions to strategic ITRS difficult challenges across the technology-related ITWGs. The first ITRS ERM chapter, launched in 2007, will be updated and revised in 2009.

2007 Emerging Research Materials Chapter

The 2007 ERM chapter assessed the potential of low-dimensional materials, such as nanotubes, graphene and nanowires; macromolecules; self-assembled materials; spin materials; and complex metal oxides to enable solutions for future Emerging Research Devices, Lithography, Front End Processes, Interconnect, and Assembly & Packaging, as highlighted in Table 1. Highlighted table elements reflect ITWG-identified application opportunities for specific families of materials that exhibit the potential to enable performance improvement over conventional approaches, but significant obstacles must be overcome before they could be adopted. To validate improvements in performance, enhanced metrology and modeling capabilities are required to characterize structure, performance and property control at the nanometer scale. Also, research is needed to characterize and manage potential environmental safety and health issues of some of these new materials for application in nanometer scale structures. The following text provides a brief survey of ERM's current set of material families that exhibit application potential.

Low-Dimensional Materials

Low-dimensional materials include carbon nanotubes, graphene, semiconducting and metallic nanowires, and oxide nanoparticles. Because of their nanostructure, size, shape and surface area, these materials have properties that could enable new devices, lower-resistivity electrical interconnects, improved packages and high refractive index immersion lithography fluids.

Carbon nanotubes have very high electrical carrier mobility, thermal conductivity and mechanical strength, which could enable solutions to difficult challenges for future devices, interconnects and packages; however, significant challenges must be overcome to realize each potential application opportunity. The high electrical mobility (conductivity) of carbon nanotubes makes them attractive as potential device channel materials for extreme CMOS applications, but significant progress is needed to be able to deposit carbon nanotubes with the required band gap control in desired locations and directions, and to integrate them in device structures. Similarly, their electrical conductivity would make them attractive for on-chip electrical interconnects and vias, but the ability to deposit them with high

Materials	ERD Memory	ERD Logic	Lithography	PIDS	Front End Processes	Interconnect	Assembly & Package
Low-Dimensional Materials	2009: Critical Assessment	2009: Critical Assessment	2009: Critical Assessment			2009: Critical Assessment	2009: Critical Assessment
Macromolecules	2009: Critical Assessment	2009: Critical Assessment	2009: Update		2009: Update	2009: Update	2009: Update
Self-Assembled Materials			2009: Critical Assessment		2009: Update	2009: Update	2009: Update
Spin Materials	2009: Update	2009: Update					
Complex Metal Oxides	2009: Update	2009: Update					2009: Update
Alternate Channel Materials (III-V, Ge)		2009: Add		2009: Add			
Heterostructures and Interfaces		Update		2009: Add			

Application in 2007 ITRS ERM

Application to be added in 2009 ITRS ERM

Table 1. Potential Applications of Emerging Research Materials

density in required locations and directions, with low resistance, is a serious challenge. In packaging, there is interest in potentially using carbon nanotubes for thermal heat spreading materials, and electrically connecting chips to packages, but techniques must be developed to reduce electrical and thermal contact resistances and to assemble the nanotubes in dense aligned arrays.

Similarly, single-crystal semiconductor (e.g., Si, Ge, III-V) nanowires offer opportunities for high-performance devices. While techniques are emerging to grow nanowires in controlled locations and directions, significant challenges remain in the areas of controlled doping and device fabrication complexity.

Macromolecules

The key challenge for molecular devices is to identify molecules and contact formation processes that enable reproducible switching, due to interactions with molecular electronic states. In many cases, electronic switching results from the physical migration of contact materials within the molecular film. Consequently, reliable top contact formation is critical.

For lithography to continue progressing to smaller dimensions, resists are needed that can print smaller features with reduced variation in shape and dimension. In addition to evolutionary approaches, new concepts in molecular structure are being investigated, including molecular glasses and pixilated resists, which correspond to fully functionalized, single-resist molecules. Molecular innovation, material design and a foundational understanding of structure-property correlations are required to extend lithography into the deep nanometer domain.

Self-Assembled Materials

The controlled assembly (i.e., directed self-assembly) of block co-polymers (two or three dissimilar polymer chains that are chemically attached) into patterns through phase segregation, similar to the process by which oil and water separate, is progressing; however, difficult challenges must be overcome for this technology to become a viable potential solution. The ERM ITWG identified a number of critical capabilities and projected research requirements that must be achieved for the ITRS Lithography ITWG to consider directed self-assembling materials technology as an extensible lithographic option. These challenges include the ability to: 1) generate features at 2X higher density than can be achieved by conventional lithography, 2) assemble lines or openings in predefined array locations, and 3) demonstrate a sufficiently low-defect density.

Spin Materials

For spin devices, new materials are needed to enable spin state switching, low loss spin transport, specific electron spin orientation selectivity and the "reading" of spin state. While ferromagnetism has been demonstrated in semiconductor materials at temperatures up to 195K, room temperature operation is needed to satisfy projected ITRS research requirements. Selective injection of spin-aligned electrons from a ferromagnetic metal (such as iron), though an insulating material (such as crystalline magnesium oxide), has been demonstrated. This suggests that spin alignment and filtering operations are being enabled. Metrology is needed to characterize the concentration of spin-aligned electrons in nanometer scale structures. Also, models are needed to identify material improvements that could enable the improvement of desired functions.

Complex Metal Oxides

Complex transition metal oxides are being investigated for a wide range of novel memory devices. Material property degradation, caused by high-electric-field-induced generation and migration of defects over time, remains a key challenge. Research is needed to understand and control the defect formation and migration mechanisms in these materials and their interfaces. Strongly correlated electron state (SCES) materials, a special class of these oxides, exhibit electrical polarization and complex magnetic states that could enable new devices. Recent research on interfaces formed between different compositions of these SCES materials has identified an unexpected coupling of electrical and magnetic properties, which could enable new device functions, but this area needs further study.

The key challenge for molecular devices is to identify molecules and contact formation processes that enable reproducible switching, due to interactions with molecular electronic states.

Complex transition metal oxides are being investigated for a wide range of novel memory devices.

2008: Preparing for the 2009 ITRS ERM Chapter

In 2008, the ERM ITWG has chosen not to change the 2007 ERM chapter. Instead, the ERM ITWG has focused on developing a critical assessment process and on reviewing the progress of identified emerging research materials. The assessment process and progress reviews will help drive the 2009 revision of the ITRS Emerging Research Materials chapter and clarify the set of materials that warrant consideration as potential solutions for specific ITWG-identified applications. Based on the joint ERD/ERM workshop on promising device technologies, the 2009 ERM chapter will provide an increased focus on the assessments of graphene and carbon nanotubes for extreme CMOS and beyond CMOS device applications. The 2009 revision of the ERM chapter also will add III-V materials as alternate channel materials and review progress in the integration of high-κ dielectrics and contact materials.

During 2008 through early 2009, several face-to-face workshops, e-Workshops and teleconferences with Web-shared presentations were held to provide the basis for the ERM ITWG's 2009 critical assessments and to identify new material additions and transitions in the 2009 ERM chapter. In September 2008, a joint ERD-ERM face-to-face workshop was held in Tsukuba, Japan, on graphene for MOS applications and spin torque transfer devices and materials. In November, a workshop was held in Austin, Texas, to review materials for spin devices. During

2008, e-Workshops were held on the following topics:

- Challenges for III-V Integration for CMOS Extension
- Graphene Deposition Technologies
- Technologies for Deterministic Dopant Processing
- Materials Challenges for Low-Temperature Package Assembly
- Analysis of Nanotubes for Package-to-Chip Electrical Interconnects
- Nanotube Composites for Thermal Heat Spreading
- Nanoparticles for Control of Polymer Properties
- Macromolecules for Control of Package Polymer Properties
- Nanowires for Package Applications

Additional workshops are scheduled, in 2009, on complex metal oxides and novel macromolecules for resist and lithography applications.

The proposed ITRS ERM scope updates and changes are identified in Table 1. Please note that the proposed plans and changes for the 2009 revision of the ERM chapter are subject to change.

Acknowledgments

First, we would like to acknowledge the members of the Emerging Research Materials (ERM) Working Group and Emerging Research Devices Working Group for their contributions to the development of the 2007 ERM Chapter. Second, we would like to acknowledge the members of the ITRS Lithography; Front End Processes; Interconnect; Process Integration, Devices & Structures; and the Assembly & Packaging Technology Working Groups for identifying needs for new materials. We would also like to thank the Environment, Safety & Health; Modeling & Simulation; and Metrology Technology Working Groups for supporting the identification of new capabilities required by the ERM. Finally, we would acknowledge the support of Linda Wilson and the ITRS Editorial team for their support in the development and improvement of the 2007 Emerging Research Materials Chapter.

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See bio on page 10.

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Steven E. Schulz
President and CEO, Silicon Integration Initiative, Inc.

During the mid-to-late '90s, I had the good fortune to be part of the ITRS team(s) authoring the Design, System, and Test chapters. These teams were superb experts in their field, dedicating many hours in detailed face-to-face discussions and many more in background tasks. This tradition of excellence continues, as evidenced by the papers in this section.

Several common elements are evident. Both papers explain how the full ITRS chapters they represent have been structured, so the reader understands the critical interdependent relationships. They also summarize several key challenges, and hint at what is likely to come. While complementary both in terms of content and style, each paper covers distinctly different aspects of need.

The paper by Carballo and Kahng focuses on design and system drivers. For example, the authors reveal the need to double design productivity with each technology generation, demanding far greater IP reuse than is prevalent today. Power management is another example of a critical risk to industry. Yet challenges clearly extend into embedded software, multi-core architectures, system-in-package technology, 3D stacked die and "More Than Moore" design needs.

The paper by Lorenz addresses modeling and simulation, a "crosscut" technology shared across the ITRS. The author covers numerous challenges – such as devising models to predict thermal-mechanical-electrical interactions, or new simulation models for next-generation lithography. Yet delaying research into modeling nanowires, or dopant atom migration, could forestall the production potential of promising technologies.

A perpetual challenge in the field of Design is that, unlike many manufacturing areas, it is more difficult to associate any specific measurable need to any specific target year of introduction. This owes to the relative degrees of independence from one another and diversity of application priorities. That is not to say that design methodologies and parameters are not tightly coupled (device physics rules otherwise!), but rather that an improvement in one area (say, power estimation) is always useful even if another improvement (say, in multi-core architectures) is delayed. Defining a numerical metric for exploitation of multi-core architectures, for instance, could be futile!

Clearly, the ITRS cannot define all solutions required over the next 15 years, yet it remains the industry's best reference for technology challenges we can expect to face. Those making investment decisions should take the time to understand it, then integrate it into a strategic technology investment portfolio to help secure our industry's long-term success.

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Simulation to the Rescue of ITRS Roadmap Complexity

Today's MOSFETs look like distant cousins of the MOSFETs we studied at university a mere decade ago. Far from simple scaled versions of previous designs, they feature silicon germanium embedded in raised source and drain regions, high-k gate dielectrics and, in a curious revivalist twist, metal gates. And lurking in the background are the multi-gate FETs, emerging from research laboratories and poised to upend the stalwart planar MOSFET.

By now it is no secret that CMOS technology is increasingly reliant on new materials and structural innovations to achieve the International Technology Roadmap for Semiconductors (ITRS) performance targets. Yet, with the new materials and structures, the number of process and architectural choices increase, raising the complexity and cost of the technology development effort. For example, current lithographic technology is insufficient to print the small feature sizes of future nodes, leading to active research into alternatives such as dual patterning, extreme ultraviolet and direct write lithography.

It is because of this environment that simulation will be called upon more and more to support technology development; for example, by using computational manufacturing to assess the merits of competing techniques, enabling the early exploration of novel device structures, or guiding experimental design during process integration, to reduce the number of costly engineering wafers and development time.

And when the process is transferred to production, simulation will increasingly become the foundation for yield-enhancement and mask synthesis tools and methodologies. These are key driving forces within the Silicon Engineering Group at Synopsys.

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ITRS CHAPTER: Modeling & Simulation

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Fraunhofer IISB

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Technology Modeling and Simulation is the virtual counterpart of semiconductor device and chip fabrication and characterization: Computer programs are used to predict the geometries, strain and dopant concentrations of devices, their electrical performance and reliability, and finally, the behavior of circuits and systems. As an example, Figure 1 shows the electrostatic potential in a state-of-the-art FinFET transistor, simulated with commercial 3D process and device simulation software. The overall aim of Modeling and Simulation is to support the development of real-world technologies, devices, circuits and systems by providing information that is difficult, costly, less efficient or too time-consuming to obtain from experiments, and in this way to reduce development times and costs. To enable this, Modeling and Simulation tools must contain appropriate physical models including appropriate parameter settings, and meet various requirements in terms of generality of application, speed of simulation, complexity of the applications that can be addressed, and last but not least, user interfaces and interactions. In turn, dedicated research and development activities on Modeling and Simulation capabilities are needed.

Modeling and simulation capability is mainly developed at universities and research institutes funded by government and/or projects. TCAD vendors play an important role in the development of those capabilities, and are in most cases the interfaces between R&D and the end customer in industry, customizing the R&D results into commercially supported simulation tools. Simulation efforts in the semiconductor industry mainly focus around the adaptation and application of the simulation capabilities to the exploration, development and optimization of technologies, devices and ICs.

The development of new simulation capabilities generally requires long-term research, and increasingly interdisciplinary activities, which can best be carried out in an academic or a laboratory setting. For this reason, a vigorous research effort at universities and independent research institutes is a prerequisite for success in the modeling area, together with close cooperation with industry, along the simulation food chain mentioned above. Because the necessary basic work generally needs significant development time, it is vital that adequate research funds be made available in a timely manner in order to address the industry's future critical needs.

To best meet the needs of the various technologies addressed by the ITRS, the Modeling and Simulation group generally bases its work on discussions with the

other ITRS groups, such as "Lithography" or "Process Integration, Devices and Structures," in order to extract their requirements for simulation models and tools. These were summarized in so-called crosscut sections of the 2007 Modeling and Simulation chapter, and have been updated since then.

The main part of the overall Modeling and Simulation chapter then details the conclusions drawn from these crosscut requirements. In turn, it contains the following topical areas as subchapters, as shown in Fig. 2: 1) *Equipment/feature scale modeling*—hierarchy of models that allows the simulation of the local influence of the equipment (except lithography) on each point of the wafer, starting from the equipment geometry and settings; 2) *Lithography modeling*—modeling of the imaging of the mask by the lithography equipment, the photoresist characteristics and processing; 3) *Front end process modeling*—the simulation of the physical effects of manufacturing steps used to build transistors up to metallization, but excluding lithography; 4) *Device modeling*—hierarchy of physically based models for the operational description of active devices; 5) *Interconnect and integrated passives modeling*—the operational response (mechanical, electro-magnetic, and thermal properties) of back-end architectures; 6) *Circuit element modeling*—compact models for active, passive, and parasitic circuit components, and new circuit elements based on new device structures; 7) *Package simulation*—electrical, mechanical, and thermal modeling of chip packages; 8) *Materials modeling*—simulation tools that predict the physical properties of materials and, in some cases, the subsequent electrical properties; 9) *TCAD for design, manufacturing and yield*—the development of additional models and software to enable the use of TCAD to study the impact of inevitable process variations and dopant fluctuations on IC performance and in turn design parameters, manufacturability and the percentage of ICs that are within specifications; 10) *Numerical methods*—all algorithms needed to implement the models developed in any of the other sections, including grid generators, surface-advancement techniques, (parallel) solvers for systems of (partial) differential equations, and optimization routines. As shown in Figure 2, these areas can be grouped

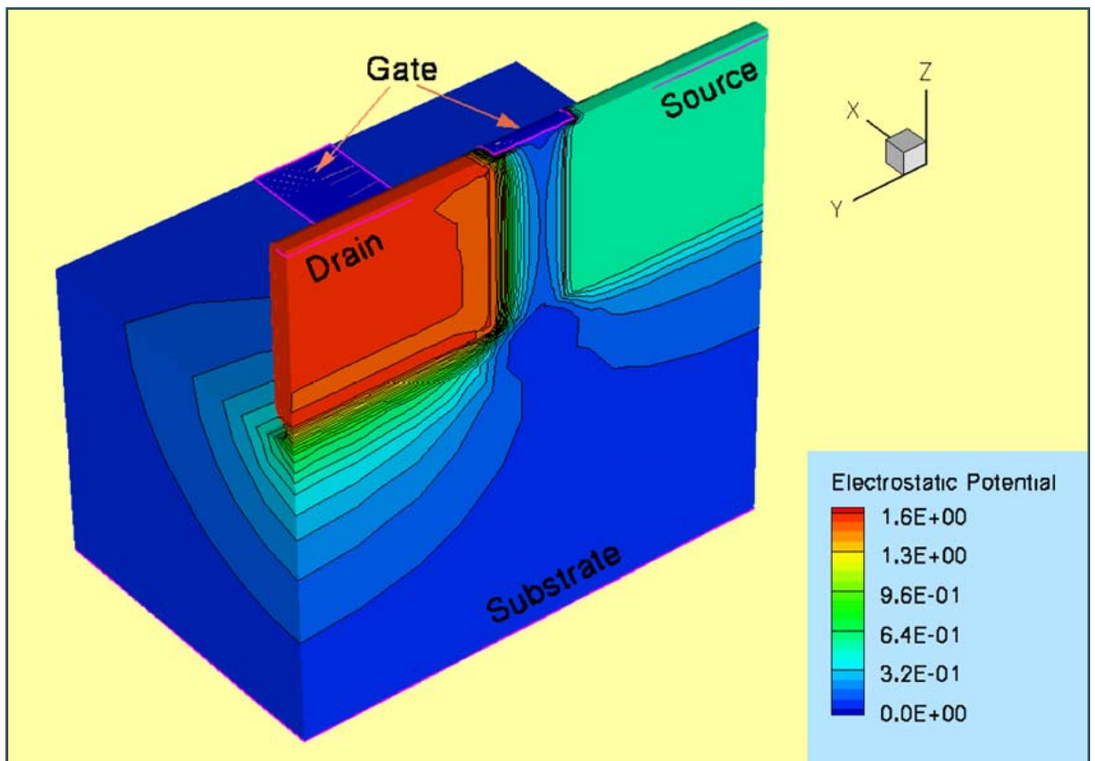

Figure 1. Electrostatic Potential in a State-of-the-Art FinFET Transistor, Simulated With Commercial 3D Process and Device Simulation Software

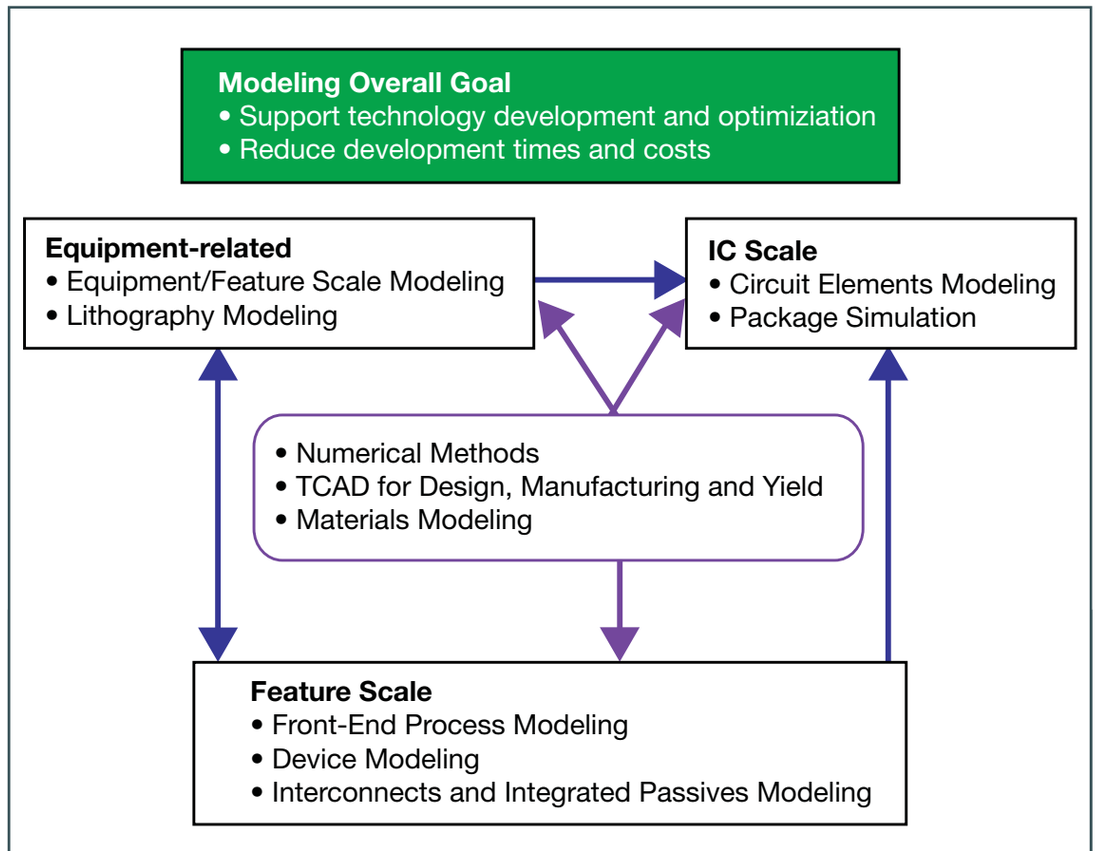

Figure 2. Modeling and Simulation Scopes and Scales

into equipment-, feature and IC-scale. Items 8 to 10 are unique because they in fact cross-cut almost all other topics in Modeling and Simulation. Material and equipment issues are becoming more and more important in all processes as well as for active devices and interconnects. Numerical algorithms are shared by most of the areas in simulation. For all these 10 topical areas, the ITRS contains a detailed description about the research and development work needed.

Similar to other areas of the ITRS, also in Modeling and Simulation, several difficult challenges have been identified. On a short-term time scale (until 2015), these are in 2008:

- Lithography simulation including EUV (Extreme Ultraviolet Lithography)
- Front-end process modeling for nanometer structures
- Integrated modeling of equipment, materials, feature scale processes and influences on devices, including variability
- Ultimate nanoscale device simulation capability
- Thermal-mechanical-electrical modeling for interconnects and packaging
- Circuit element and system modeling for high frequency (up to 160 GHz) applications

Additional difficult challenges on the long-term time scale (until 2022), are:

- Modeling of chemical, thermomechanical and electrical properties of new materials
- Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials
- Optoelectronics modeling
- NGL (next-generation lithography) simulation

All these difficult challenges contain several issues that are explained in detail in the Modeling and Simulation chapter of the ITRS.

Besides the texts and the challenges mentioned above, the Modeling and Simulation chapter contains tables on the short-term requirements for all kinds of semiconductor simulation tools, starting from Lithography Simulation and extending to Package Modeling. Also, specifications on the required accuracies are given.

Throughout the Modeling and Simulation chapter, the main trends for changes in 2007 and 2008 have been:

- An increased need and emphasis on the modeling and simulation of material aspects;
- Extended requirements on the simultaneous simulation of electrical, mechanical and thermal effects;
- An increasing need to strengthen developments and applications of simulation also beyond the traditional areas of process, device and circuit simulation, e.g., for interconnects, packages and 3D integration;
- Extended needs and requirements for the simulation of nonclassical CMOS and Beyond CMOS devices (such as nanowires and nanotubes);
- Increased demand for ab-initio simulation;
- Increased demand for the simulation of the impact of individual dopant atoms, interfaces and process variations.

In previous releases of the Modeling and Simulation chapter, an assessment on the cost reduction, which can be achieved by the use of Modeling and Simulation during the development of new processes, devices and circuits, was given. This was based on a survey held some years ago in Japan, and resulted in an estimate of about 40 percent cost reduction for best practice cases. In 2008, this survey has been re-conducted and extended to all regions. TCAD users almost exclusively from the semiconductor industry were asked to respond to several questions on their use of TCAD tools, their positive and negative experiences made and their further suggestion and expectations. TCAD developers were excluded from the survey in order to assess the user's perspective only. In total, more than 130 filled-in questionnaires were received from all regions that participate in the ITRS. It is important to note that compared to the 2007 ITRS, the meaning of the cost reduction estimate extracted from this new survey has strongly changed: First, both the reduction of development time and costs were asked for and separately displayed in the 2008 ITRS. Secondly and most important, in the preceding years, the figure referred to the cost reduction *potential* if TCAD were appropriately used. In contrast to this, the new 2008 figures refer to the estimate for application cases that have already happened in the respective companies. In consequence, the numbers given in the 2008 Update are systematically lower than in 2007, because existing cases do not necessarily exploit the full potential for cost and time reduction, and also, in part, because people with quite little knowledge of the appropriate use of TCAD contributed to the survey. Nevertheless, the average current figures of about 30 percent reduction in development time and nearly 30 percent in development costs achieved by the appropriate use of TCAD demonstrate the high relevance and potential for the industrial use of TCAD. Further relevant information extracted from the questionnaires will be displayed in the 2009 ITRS.

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ITRS CHAPTERS: Design and System Drivers

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Introduction

The Design and System Drivers chapters of the ITRS delve into the design issues that are critical to the development of electronic products today. Every aspect of a semiconductor product that comes *before* manufacturing is within the scope of this portion of the ITRS roadmap, and forms a *Design Technology Roadmap*. Given the increasing difficulty and monstrous expense of scaling semiconductor products on the sole basis of manufacturing technology, the design technology roadmap has become a centerpiece in the roadmap of semiconductor-based product enablement, and is increasingly interconnected with the other "manufacturing" chapters of the ITRS.

The *Design* Chapter provides a roadmap of specific quantified – and dated – challenges and solutions pertaining to the design of chips, regardless of what type of application these chips are made for. As a result, this chapter attempts to determine a specific roadmap for *suppliers of design technology*, i.e., suppliers of design software tools and methodologies (e.g., a tool that synthesizes a chip's layout automatically), as well as structured design techniques (e.g., the number of different voltage supplies and how they are leveraged within a silicon die).

The *System Drivers* Chapter provides a roadmap of characteristics and challenges that are *application-dependent*. For each "type of chip" or "type of fabric inside the chip" denominated a *driver*, a clear roadmap of key design characteristics is provided. For example, the Portable Consumer Driver section describes characteristics of a chip for such an application, and the MPU Driver represents a key driver given by leading-edge microprocessor circuits. This roadmap also sheds light on how each *driver* achieves such a designation, and what exactly it drives within the industry. The portable consumer

The Design and System Drivers chapters of the ITRS delve into the design issues that are critical to the development of electronic products today

driver, for example, has recently become a driver for leakage (or "standby") power consumption, given its stringent requirements related to battery life in portable devices.

The Design Chapter: Main Design Challenges and Required Solutions

The Design chapter covers design challenges in a top-down fashion, from the highest/earliest levels of the design process, to the lowest/most-detailed/latest phases in the design of a product. As such, challenges and solutions are organized in "red brick" tables and "blue" tables respectively, in the following order:

1) **System-level design** – deals with the requirements of the chip itself, and subsequent initial high-level decisions involving such elements such as software, processors, memory blocks, etc.
2) **Logic/circuit/physical design** – the core of chip design for the last 20 years, it deals with two steps in sequence. First, the generation of combinations of logic function "gates" (e.g., NAND), storage devices (e.g., latches) and wires connecting these gates to each other, such that system-level requirements are met. Second, the generation of circuits and layouts that corresponds to these logic descriptions.
3) **Design verification** – deals with the verification of the system logic, circuits and even layouts listed above.
4) **Design for Test** – deals with the incorporation of features during design that will make testing the chip easier.
5) **Design for Manufacturability** – deals with the communication and coordination aspects of connecting all of the design process with the subsequent manufacturing phase.

Figure 1 depicts one sample requirement challenge for each of the five levels above, normalized to its 2007 value for consistency. Note that all of these requirements present an exponential growth profile, which underlines the challenge from the start.

However, there are "cross-cutting challenges" in the Design chapter, i.e., challenges that cut across these levels of abstraction since they can apply to an entire design, earlier or later. These are:

- **Design Productivity**. To avoid exponentially increasing design cost, overall productivity of designed functions on chip must double each technology generation. Reusing existing designs, verifications and tests is a huge boost to productivity and must also scale at > 2X per technology generation.
- **Power Management**. Because CMOS technology no longer scales linearly, and because of the limitations of interconnect materials and package technologies, a variety of challenges related to power management and current delivery have become critical to the roadmap.
- **Design for Manufacturing**. Challenges that are impossible to solve within a single technology area of the ITRS may be solvable (more cost-effectively) via appropriate synergies between Design Technology and all other manufacturing-related disciplines, leading to the rise of Design for Manufacturability (DFM), to which the Design chapter devotes an entire section. Indeed, the feasibility of future technology nodes will come to depend on this communication.

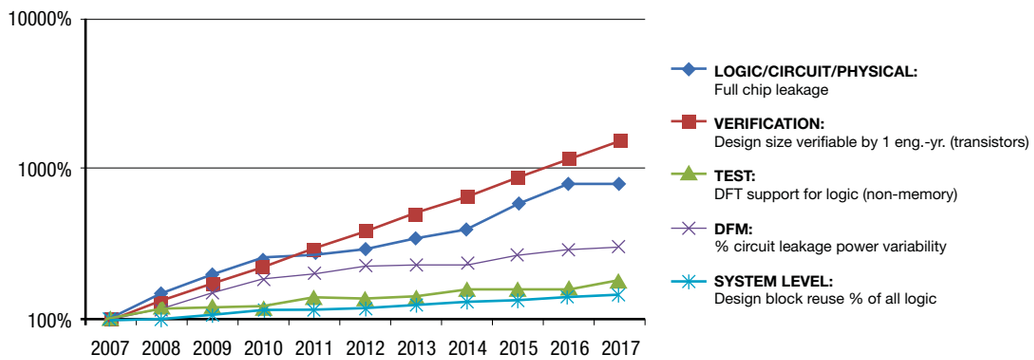

Figure 1. Graph Showing One Requirement Trend for Each of the Five Abstraction Levels in the Design Chapter

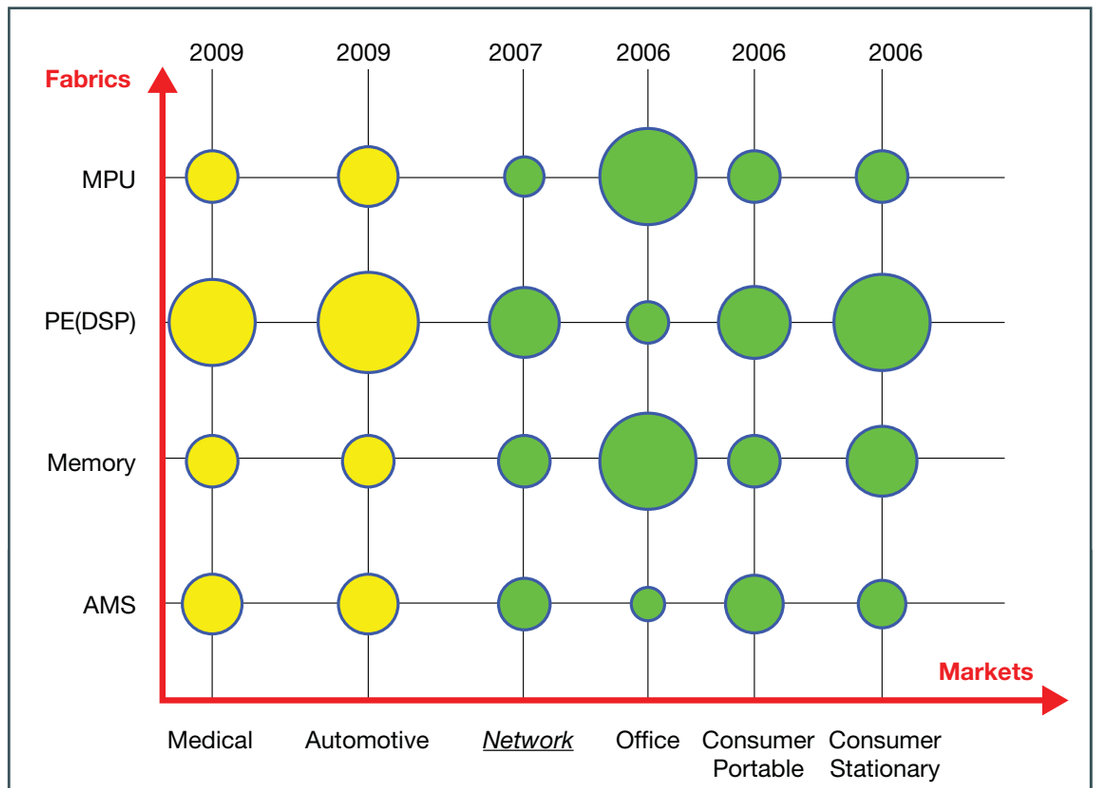

Figure 2. Matrix Depiction of (a) Fabric System Drivers versus (b) Product System Drivers

- **Interference and Reliability**. These have been identified as smaller-impact cross-cutting challenges. Interference has to do with resource-efficient communication and synchronization, already challenged by global interconnect scaling trends, and increasingly hampered by noise and interference. Reliability comes into play when relaxing the requirement of 100 percent correctness for devices and interconnects that may dramatically reduce costs of manufacturing, verification and test.

The System Drivers Chapter: Key Industry Drivers

Semiconductor technologies – both manufacturing and design – are developed in response to economic drivers given by types of products. The ITRS must comprehend how technology requirements arise for these product classes. Some technological advances are deployed in some semiconductor products and not others. Today, introduction of new technology solutions is increasingly application-driven, i.e., applications drive technology. Computer microprocessors have been joined as drivers by mixed-signal systems, battery-powered mobile devices, wall-plugged consumer devices and networking devices. In-house chip designs are replaced by system on chip (SoC) and system in package (SiP) designs incorporating building blocks from multiple sources. The System Drivers chapter of the ITRS covers these drivers.

There are two types of ITRS system drivers: "fabric" drivers and "product" drivers. This concept is illustrated in Figure 2.

a) *Product drivers*, such as networking, consumer portable, consumer stationary, or office, represent product classes directly, i.e., types of designed manufactured chips based on application. For example, the consumer portable product represents systems on chip typically used in cell phones, including a number of processors and memory fabrics inside the chip. An example instance of this driver is a cell phone application processor.
b) *Fabric drivers*, including MPU, PE/DSP (processing engine/digital signal processor), AMS (analog mixed signal) and embedded memory, represent silicon fabrics, or "cores," a combination of which can form a product class such as the above. For example, embedded SRAM and DRAM memory, plus a couple of MPU cores, plus AMS circuits (serial communication circuits, clocks, etc.) may form a certain type of networking product.

Semiconductor technologies – both manufacturing and design – are developed in response to economic drivers given by types of products.

An example of driver trends is shown in Figure 3. For the consumer portable driver, we can see that leakage power (i.e., the energy consumed by the device when it is not doing useful work), is a major challenge, and that its maximum allowable value consistent with battery life requirements will be exceeded in the next 10–15 years unless major innovations occur.

New in 2008, Plans for 2009, Conclusions

In the 2008 Update of the ITRS Design and System Drivers chapters, we focus on a few key messages and updates, some of which are described below.

First, we have confirmed software as an integral part of semiconductor products, and software design productivity as a key driver of overall design productivity. We include additional rows in the tables for system-level design, and we highlight how productivity growth can only be ensured with heavy use of special-purpose multi-core architectures.

The key system drivers (MPU, consumer portable, consumer stationary, etc.) have been updated for 2008 for accuracy and completeness, without major changes. In 2009 and beyond, we will continue to broaden the System Drivers to reflect key markets such as Medical and Automotive. We have also done a special preliminary impact analysis of the three-year shift in certain technology requirements, such as HP GL (high-performance transistor gate length), and are including the impact on our system drivers. The impact is estimated to be very small-to-nonexistent, depending on the driver.

For certain drivers (consumer), we have corrected the power modeling to reflect more realistic dynamic power roadmap. This results in memory dynamic power approximately 10X less than what was modeled previously. We have also started to identify new key driver requirements, including the coloring (e.g., red when there is excessive power beyond the 1 watt limit for portable devices). In future drivers, we

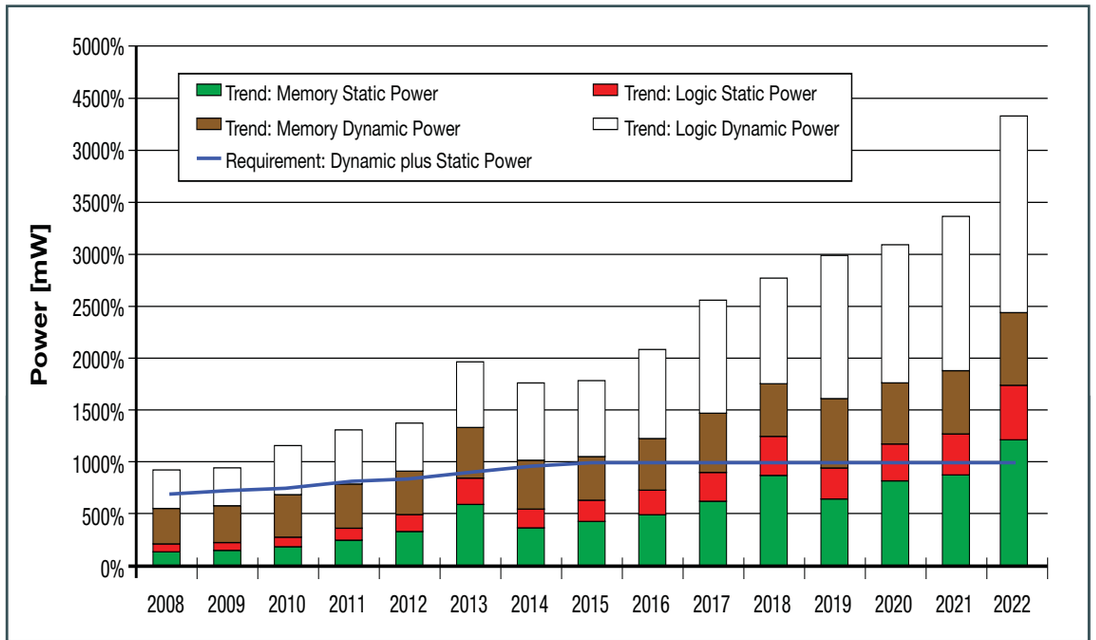

Figure 3. SoC Consumer Portable Driver Power Consumption Trends

will explore adding RF/analog/mixed signal components to the portable consumer driver, and potentially a new "wireless" (extension of an existing) driver to the overall roadmap.

On the "More than Moore" side, a new set of design requirements and solutions is being developed specifically coming from new functional diversification trends. Spe-cifically, a new set of system driver parameters is under development and will likely be deployed in 2009, related to system in package and "3D" (stacked-die) integration.

Finally, in both the ITRS Design and System Driver chapters, there is increasingly direct influence of energy factors on design technologies, continuing a trend that started a number of years ago. Power consumption has become a first-class constraint in chip design, and for nearly a decade, we have identified it as one of the top three overall design and semiconductor industry challenges. Leakage power consumption and leakage power variability have been identified as clear long-term threats to semiconductor product viability, and as a focus for design technology in the next 15 years. Their connection with the energy crisis worldwide is direct given the extremely rapidly increasing percentage of energy consumption by information technology devices that include semiconductor integration.

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Dr. Andrew B. Kahng is a professor of CSE and ECE at UC San Diego and Chair/co-Chair of the ITRS Design ITWG since 2000. His research focuses on physical design, performance analysis and design for manufacturability of integrated circuits. Dr. Kahng is the author of over 350 papers, two books and four issued U.S. patents. He received his Ph.D. in computer science from the University of California at San Diego in 1989. ■

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Alan Weber
President, Alan Weber & Associates

I still remember vividly the initial set of workshops that spawned the first National Technology Roadmap for Semiconductors (NTRS). It is gratifying to see how broadly this process has spread throughout the global industry community, and it is a genuine privilege to contribute to this special ITRS-focused issue of Future Fab International.

The paper authored by Shigeru Kobayshi of Renesas Technology explains the scope, objectives and current priorities in the Factory Integration chapter of the ITRS, and highlights some of the key concepts in this domain that can address the "difficult challenges" now facing the industry. One of these concepts is the idea that incremental improvements in manufacturing technology at the 300 mm wafer size can extend the historical productivity trends we've seen to date well into the future. The resultant "next-generation factory" (NGF) will certainly require significant changes across the food chain, from factory operations and supporting software to equipment to factory operations to infrastructure and standards technology. Another unifying concept is that of "waste reduction management," which offers a complementary and useful perspective on productivity improvement.

The paper from Kwok Ng of Semiconductor Research Corporation (SRC) focuses on the challenges relating to the future characteristics of the actual devices that must be manufactured. The key concept in this chapter is the speed metric, which combines gate capacitance, supply voltage and maximum on-current to provide a relatively application-independent target for the industry. From a solution standpoint, the roadmap deals with the fidelity of the horizontal (gate length) and vertical (dielectric thickness) scaling models for various device structures, and their relationship to the overall speed metric to forecast a realistic set of requirements for the coming years.

Both of the papers in this section provide excellent summaries of their respective sections of the ITRS, but I believe it is the authors' true hope that these will pique the readers' interest sufficiently to read and digest the actual ITRS document, and perhaps consider participating in the next update round in 2009.

Future Fab Special ITRS Focus

ITRS CHAPTER: Process Integration, Devices & Structures

Kwok Ng
Semiconductor Research Corporation

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Scope

Process Integration, Devices and Structures (PIDS) was one of the original chapters when ITRS was first formed. Its charter is to provide guidance on physical and electrical requirements and solutions for sustaining IC performance scaling. Here performance can mean speed, density, power, functionality, etc. The scope covers logic and memory devices, their structures, integration issues, as well as their reliability.

Under logic devices, they are further divided into three types: (1) High-performance (HP) logic is for the highest speed achievable, where power is not a main concern. (2) Low Operating Power (LOP) logic is a compromise between speed and power where speed is still an important requirement. An example is the notebook (laptop) computer. (3) Low Standby Power (LSTP) logic is for applications where power is the main consideration, such as for cellular phones. Under memory devices, they are divided into DRAM and non-volatile memory.

One of the main functions for PIDS is to provide technology target for the Roadmap. Given the scaling factor improvement per year on the device speed as required by the industry, PIDS needs to propose a set of solutions for the device structures and parameters that meet the performance requirements. It is always required to consider trade-offs of many parameters, such as gate dielectric thickness, gate length, channel doping, etc., because each can impact speed performance, but each has its own degree of difficulty.

The speed metric for the Roadmap has been *CV/I*, where *C* is the total gate capacitance including its parasitics, *V* is the supply voltage, and *I* is the maximum on-current. Although this metric does not give the true circuit speed in the absolute sense, it gives a relative performance figure of merit, which is the essence of scaling. Calculation of *CV/I* is performed by the analytical software MASTAR. It is provided and supported by the Europe PIDS team.

Traditionally, scaling is based on geometric miniaturization. Mainly in the horizontal dimension is the gate length, and in the vertical dimension, the gate dielectric. Such physical scaling has become significantly more difficult to continue with the same pace as in the past, and we fortunately have help from what has been called "equivalent scaling" of material properties and structural properties. These features include high-κ gate electric, metal gate, strain-enhanced mobility, ultra-thin-body (UTB) fully depleted (FD) SOI, and double-gate (DG) structures. These features, with their years of introduction, are shown in Figure 1. Their effects on *CV/I* scaling can be appreciated in Figure 2. It is seen that once the performance cannot keep up with the desired scaling target, introduction of new structures can help to get back to the required path.

Difficult Challenges

For HP logic devices, thin gate dielectric EOT and gate leakage requirements continue to push the demand on next-generation high-κ dielectrics. Metal gate materials also have to yield the right work functions for designing the threshold voltages, as well as the stability for high-temperature processing. Associated with these new dielectrics and gate metals are reliability issues resulting from new materials and interfaces. Voltage scaling has caused the channel off-current to increase and thus standby power to increase. This limitation is bound by the fundamental subthreshold slope of *kT/q*. The channel doping has to increase as channel length is scaled. This causes detrimental effects in mobility degradation, tunneling, avalanche, etc. The device structure is being moved to FD-SOI and FinFET type in which the body can be undoped. However, the thickness control of the thin body poses new challenges. The source/drain parasitic series resistance becomes increasingly important as the device carries higher and higher current density. Meanwhile it calls for higher doping levels and sharper profiles, and is becoming harder to optimize. General device reliability and variability issues are getting worse due to scaling and new materials.

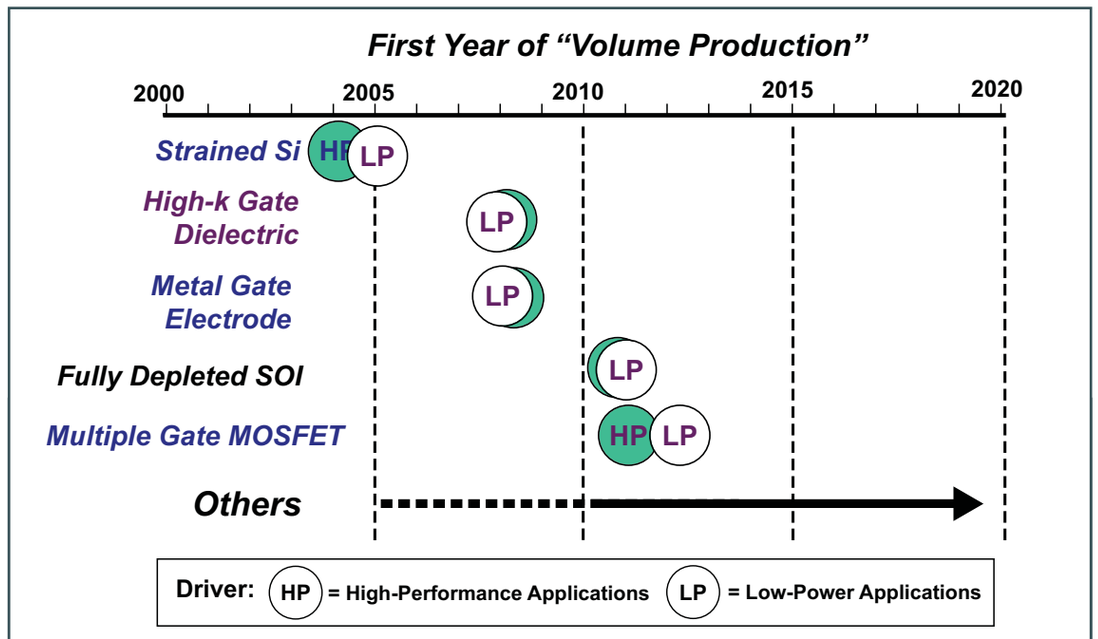

Figure 1. Multiple, Major Technology Innovations Required Over the Next Few Years to Meet Key MOSFET Targets

For nonvolatile memories, the floating-gate type of cells are losing coupling ratio as the device is scaled. The industry is moving to charge-trapping type of cells (SONOS), which have greater challenges in reliability issues. Both kinds of cells, categorized as charge-storage type, suffer from nonscalability of tunnel oxide due to charge retention problem. Prototypes of novel cells being studied are FeRAM, MRAM and PCM. Some of these have made commercialization, but large bit size has not been demonstrated yet.

For DRAM, high-capacity capacitor continues to push for higher-κ dielectrics. It is anticipated that κ >60 for beyond 50nm node is required. Low sheet resistance for bit lines and word lines is critical and challenging to meet.

2008 Update

The major changes in this update are to incorporate the new physical gate length (L_g) scaling models adopted by the ORTC, in response to our recent survey results and the reverse-engineering findings. These new scaling models slow down the L_g scaling compared with those in the 2007 ITRS. Because of this, the speed scaling of 17 percent per year in the HP Technology *CV/I* is relaxed. Accordingly, the introduction of UTB FD and DG structures are also assumed to be delayed. In this update, the UTB FD structures start in 2013, while the DG structures start in 2015, for all HP, LOP and LSTP technologies.

For HP logic, the physical gate length L_g scaling is slowed down by three to five years, with a change of slope. It is observed that with the new L_g scaling model, the *CV/I* speed metric has a slope of ~13 percent per year instead of 17 percent. This speed requirement will be a topic of discussion for the major year 2009 ITRS.

Similar changes were made to LOP Technology. Physical gate length suggested by the ORTC has a slowed-down scaling by one to three years, with a change of slope.

All other tables pertaining to LSTP Technology, nonvolatile memory, DRAM and Reliability remain unchanged as in 2007.

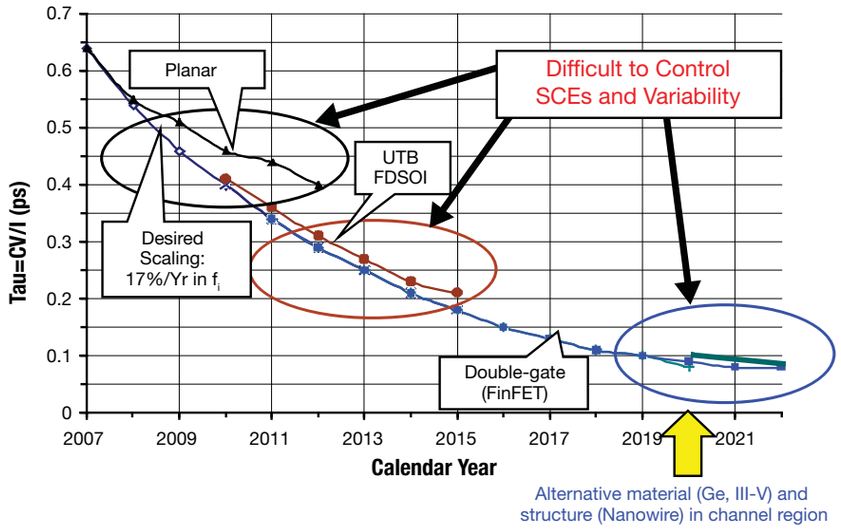

Figure 2. High-Performance Logic: Scaling of Transistor Speed Metric; $f_i = 1/[CV/I]$

Ongoing Activities for 2009

Most of the new data entries in the 2008 Update are from linear interpolation of data from the 2007 tables. We plan to recalculate these values based on MASTAR, which would be more accurate, although these values are believed to be within 10 percent of that obtained from MASTAR. Surveys on DRAM and nonvolatile memory products are being conducted by our Japan PIDS team. Adjustment of this technology pacing might be necessary, depending on the survey results.

The market recently indicates that the Roadmap assumption of speed scaling of 17 percent per year might have been slowed down. Discussion is ongoing between ORTC and different working groups to adopt a new speed scaling factor. For the major year 2009, we anticipate more changes compared with other major years. There are a few new proposals being discussed, that may or may not be adopted in 2009. These include a new speed metric using ring oscillator or inverter speed which are more indicative of real circuit speed. Also, to obtain the speed metric, whichever will be adopted, it has been proposed to present equations to derive it, in addition to MASTAR results which will be kept for comparison. Another proposal is to include variability as a factor in consideration of scaling limitation.

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Future Fab Special ITRS Focus

ITRS CHAPTER: Factory Integration

Shigeru Kobayashi
Renesas Technology

Scope of Factory Integration Chapter

The Factory Integration Technology Working Group (FITWG) is one of the key sections of the International Technology Roadmap for Semiconductors (ITRS) that strives to integrate all the factory components in order to efficiently produce the required products in the right volumes on schedule while meeting cost targets. The FITWG consists of semiconductor factory experts from around the world to evaluate the challenges and update the near-term and longer-term technology requirements and potential solutions in wafer manufacturing to meet these requirements.

The FITWG is divided into five thrust teams as shown in Figure 1. These teams clarify how difficult challenges translate into technology requirements and potential solutions. In addition to these five thrusts, the FITWG also addresses key focus areas that cut across all the five factory integration thrusts as well as the crosscut issues that impact technology areas other than wafer manufacturing.

It is paramount to sustain the decades-long trend of 30 percent per year reduction in cost per function that requires capturing all possible factory cost reduction opportunities. Factory Integration traditionally focuses on: 1) maintaining cost per unit area of silicon, 2) decreasing factory ramp time, and 3) increasing factory flexibility to changing technology and business needs.

The key challenges addressed by FITWG in 2008 activity are:

1) Integrating complex business models with complex factories including high mix;
2) Production equipment reliability, reduction of variability, utilization and extendability; and
3) Step-wise productivity improvement that should be well-coordinated in the industry in terms of improved 300 mm technology or by the transition to the next wafer size (450 mm).

The concept of acquiring step-wise productivity improvement using *300 mm wafer is called 300 mm NGF (Next-Generation Fab)* or *300 mm Prime*, and has been discussed as a candidate for significant cost reduction, as shown in Figure 2.

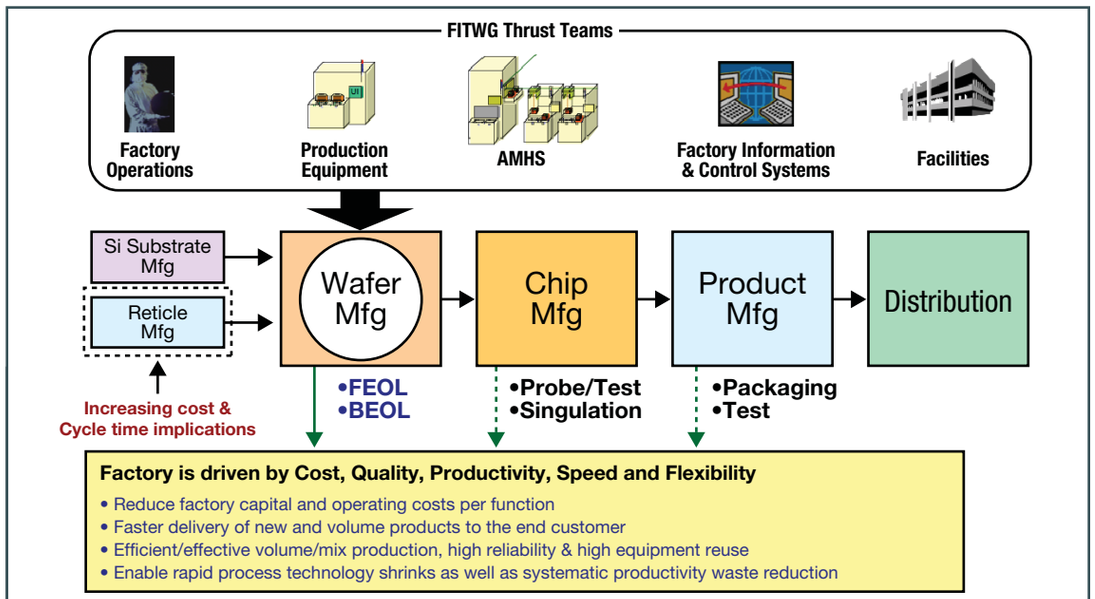
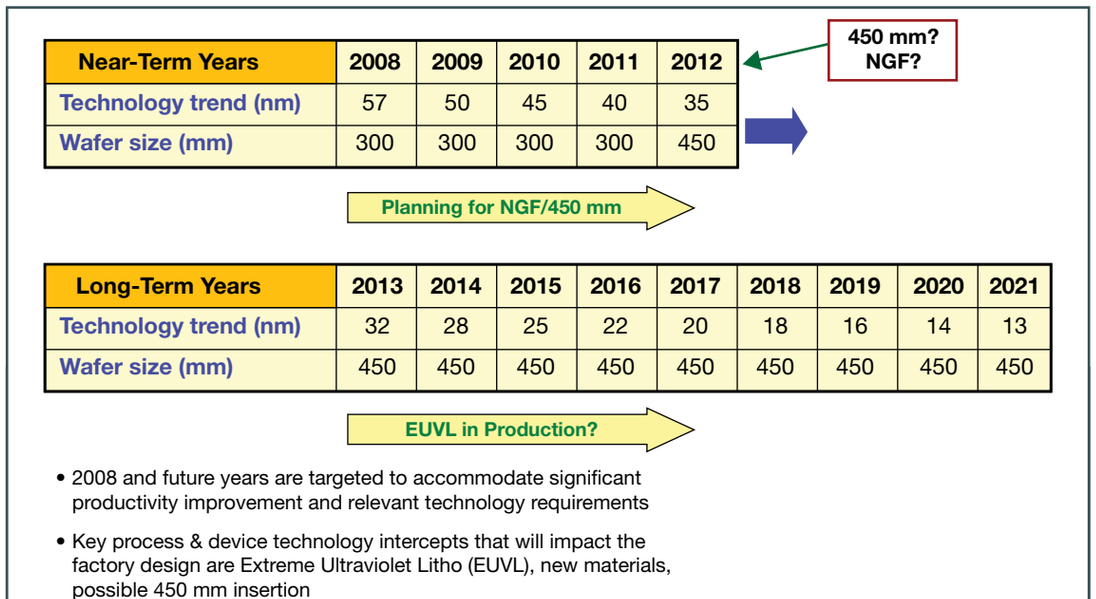


Figure 1. Factory Integration Technical Working Group Scope and Drivers



Near-Term Years	2008	2009	2010	2011	2012
Technology trend (nm)	57	50	45	40	35
Wafer size (mm)	300	300	300	300	450

Long-Term Years	2013	2014	2015	2016	2017	2018	2019	2020	2021
Technology trend (nm)	32	28	25	22	20	18	16	14	13
Wafer size (mm)	450	450	450	450	450	450	450	450	450

Figure 2. Planned Step-Wise Productivity Improvement

Highlights of 2008 Factory Integration Chapter

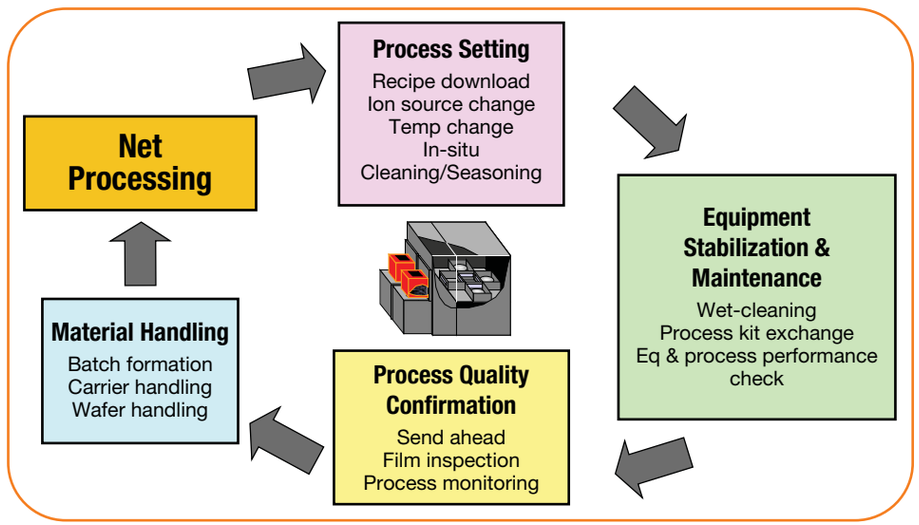
The thrust teams revised *Technology Requirement Tables* only for small editorial changes, and some carry forward the 2007 values to 2008.

The FITWG decided to concentrate our resources on the new item in *Focus Areas* where the FITWG examined the possible message for how we will keep up with Moore's Law that should trigger a step-wise productivity improvement, presumably starting between 2012 and 2015. FITWG concluded that along with the traditional device feature size shrinkage requirement trend, a waste reduction concept should be introduced into the ITRS showing annual waste reduction requirements in *Technology Requirement Tables*.

Introduction of Waste Reduction Management Concept

The 2008 edition FITWG chapter has an explanation of the Waste Reduction Management (WRM) concept showing the importance of the approach over the 2012–2015 time frame. WRM is an effort to enable waste to be exposed through the definition of standardized waste metrics, thereby enabling waste to become measurable so it can be reduced based on rigorous scientific measurement and analysis. FITWG members agreed that WRM is a fundamental lever for the step-wise improvement of productivity.

Figure 3 shows waste elements in terms of *Equipment Output Waste (EOW)* and *Wait Time Waste (WTW)*. The former is related to the factory resource and the latter relates to a wafer- or product-oriented view of cycle time.



	Equipment Output Waste	Wait Time Waste
Net Processing	NO Waste per definition	
Process Setting	X	X
Equipment Stabilization & Maintenance	X	X
Process Quality Confirmation	X	X
Material Handling	X (otherwise sufficient WIP is provided)	X

Figure 3. Waste Elements Around Process Execution

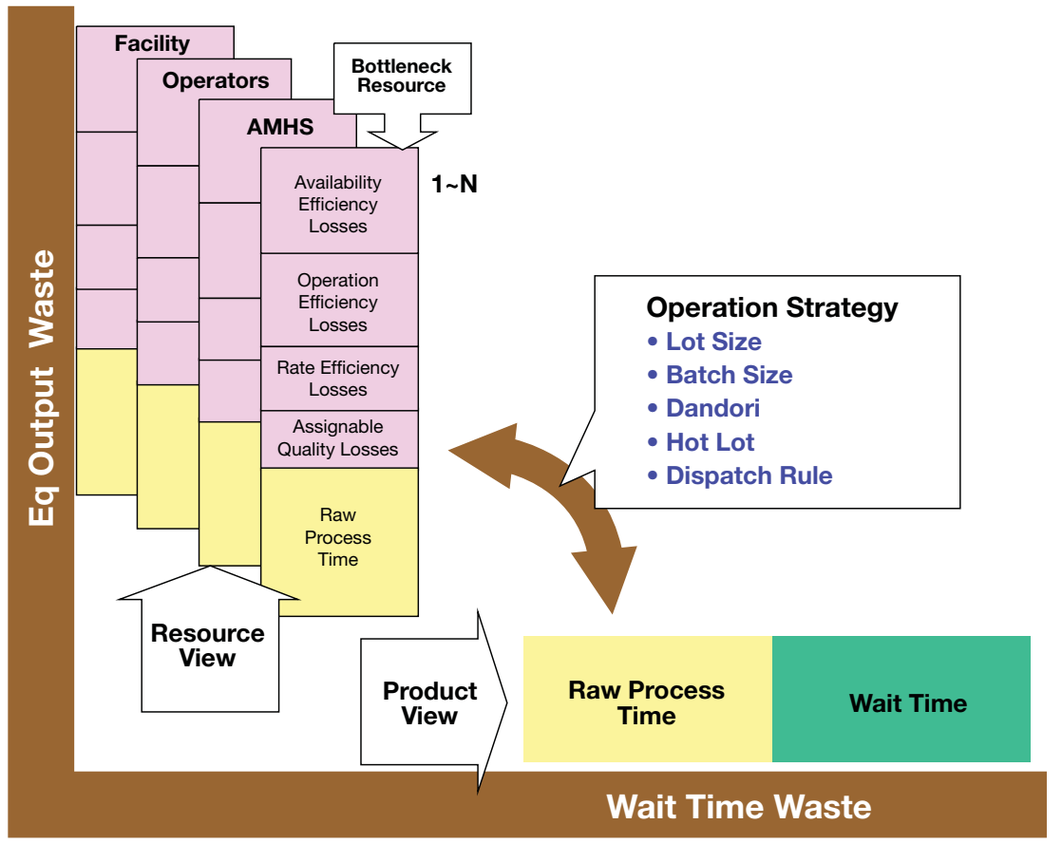


Figure 4. Proactive Visualization of Waste

Following the introduction of standardized waste reduction metrics, accompanied by measurable data definition, the FITWG is calling for the collection and visualization of waste data and a harmonized language for referring to EOW and WTW losses as shown in Figure 4, so that meaningful business discussions can be held between equipment suppliers and equipment users.

2008 Activity for 2009 Revision

In 2009, the FITWG will continue to work toward the goal of supporting cost per unit area requirements of silicon with a focus on productivity waste reduction. Currently the FITWG is further working on inclusion of a new Waste Reduction Management metric in the *Factory Operations Technology Requirements Table.* The FITWG will further discuss requirements for the systematic visualization of waste.

Acknowledgments

The author would like thank Tom Jefferson for his contributions to the ITRS FI as co-chair for 2007 and 2008, and STRJ members for their participation in sharing understanding of the industry's current challenges.

Reference

International Technology Roadmap for Semiconductors, 2007 Edition

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Shigeru Kobayashi joined Hitachi's Production Engineering Research Laboratory in 1978, involved in semiconductor processing equipment and process control development. From 1999 to 2002, he was responsible for 300 mm implementation technology development at Selete Semiconductor Leading Edge Techno-logies, Inc.). He currently serves as co-chair for the Japan Region Standard Committee of SEMI and for the Factory Integration International Technology Working Group of ITRS. ■

In 2009, the FITWG will continue to work toward the goal of supporting cost per unit area requirements of silicon with a focus on productivity waste reduction.

The FITWG will continue to work on other key focus areas and crosscut technology areas such as Airborne Molecular Contamination (AMC) control; Advanced Process Control to support stringent litho overlay tolerances and to control line width roughness/line edge roughness; and to seamlessly utilize circuit, mask and litho process information through Design For Manufacturing (DFM), energy conservation and 300 mm Prime/450 mm requirements.

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John Caffall

Director of Operations, Submicron Development Center (SDC); Spansion Inc.

The International Technology Roadmap for Semiconductors (ITRS) is a forecast of the advances in performance of semiconductor industry technologies as defined by industry experts. It is sponsored by semiconductor associations in the U.S., Europe, Japan, Korea and Taiwan. As stated in the ITRS website, the objective of the ITRS is "to ensure cost-effective advancements in the performance of the integrated circuit and the products that employ such devices, thereby continuing the health and success of this industry."

Looking back at how the ITRS began, we have to reference Gordon Moore's 1965 original publication in *Electronics* magazine. Moore examined the advancement in semiconductor transistor density and performance over time. At first he defined the transistor density as doubling yearly, and then later (1975) updated this to a doubling every two years. This began the history and foundation of semiconductor roadmaps that are still used widely today. The Semiconductor Industry Association (SIA) took the initial responsibility to maintain the roadmap for the industry, and then in 1998, collaborated with the other international associations to form the ITRS, which is the current industry standard.

The ITRS is used by most semiconductor manufacturing and equipment companies as a gauge to generate their own internal roadmaps. The ITRS has evolved over time and now comprises many sections including System Drivers; Design; Test; Process Integration, Devices & Structures; Assembly & Packaging; Yield Enhancement; and Modeling & Simulation, to mention only a few. To give an idea of the level of detail the document contains, the Executive Summary is over 100 pages long.

The following two articles are great examples of how the ITRS is used to influence the advances in process technology. Michael Lercel gives a detail of the challenges and options for photolithography processing, and Jeffery W. Butterbaugh, Larry Larson and Raj Jammy explore the roadmap details and future of the Front End Processes.

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ITRS CHAPTER: Lithography

Michael Lercel
IBM

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Introduction

The lithography roadmap continues to evolve as timing of the introduction of new technologies continues to change. Historically this has always been true because lithography is on the forefront of dimensional scaling for the semiconductor industry. So although new technologies are highly desired, they must be available on aggressive schedules to meet semiconductor process technology roadmaps – or methods to extend existing technology will be implemented. Today that is represented by an increasing interest in extending optical lithography with process techniques in the near term, and with continued hope for new technologies for continued roadmap scaling for the 22nm node and beyond.

Lithography Roadmap Evolution

With a continued need to introduce new semiconductor nodes on a rapid pace

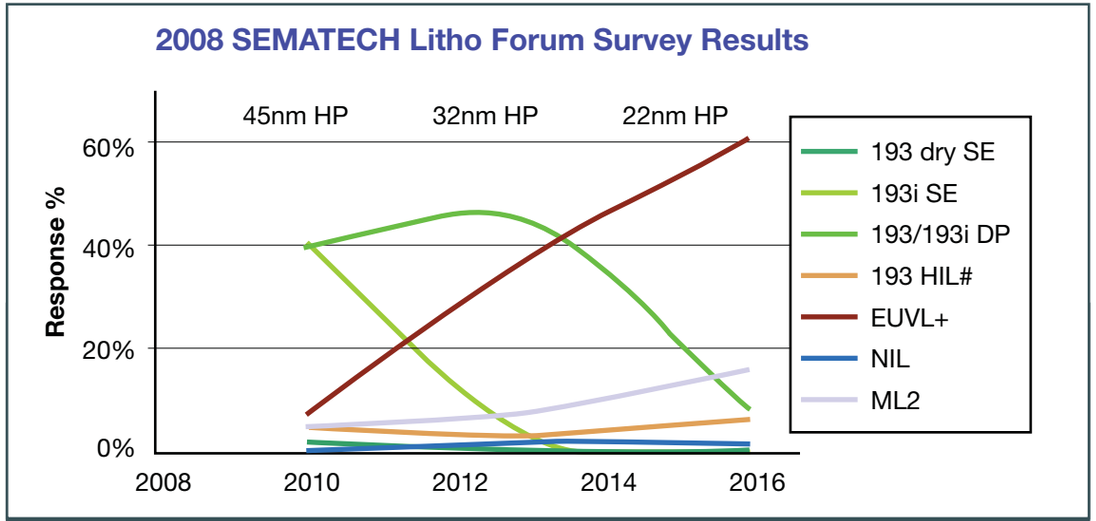

Figure 1. Participant survey results from the 2008 SEMATECH Litho Forum indicating which lithography technology is most likely to be used for leading-edge products in manufacturing (as indicated on the horizontal scale). SE=single exposure; DP=double patterning; HIL=high-index immersion; NIL=nanoimprint lithography; ML2=maskless litho

of every two years, the choice of lithography technology is dependent upon which ones are available. At the 2008 SEMATECH Litho Forum, the consensus of the group was measured through a survey including questions on when technologies would be utilized and the status of remaining technical hurdles. For the 32nm half-pitch generation, the use of double patterning is expected to be the dominant lithographic technique. This represents a substantial increase in interest in double patterning since the 2006 Litho Forum survey, and reflects a later anticipated introduction of EUVL at the 22nm half-pitch (see Figure 1).

The ITRS Lithography roadmap updates therefore include more definition of what will be required to implement double patterning. In 2007, the lithography chapter began to include requirements for the several forms of double patterning that are possible. In particular, spacer self-aligned processes require film deposition and etch steps that are distinct from those of litho/etch/litho/etch steps (see Figure 2). In addition, patterns can be defined independently by each exposure or by the superposition of two exposures. The latter, referred to as dependent double patterning in the ITRS, has a line-width control requirement that includes the overlay of the two exposures. This drives much tighter requirements on overlay and mask pattern placement (which is a component of the overlay budget). Therefore, to implement dependent patterning requires a larger acceleration of the mask technology roadmap as compared to independent double patterning (see Figure 3). Compared to single exposure, however, both require tighter mask specifications. Hence, implementing double patterning will require some acceleration of mask specifications and especially those associated with complex patterns.

For the other lithography technologies, such as Extreme Ultraviolet Lithography and Nanoimprint, the ITRS updates do not have significant changes. The target requirements for these technologies to become successful remain mostly the same. Most of the numerical values are calculated from the overall roadmap tables. So with some slight changes to these parameters (such as physical gate size), minor updates to the numerical targets for CD uniformity, overlay and defect sizes have been made. Fundamentally, the changes are minor and the delay in introducing new technologies is not caused by more-stringent requirements, but simply slow progress toward meeting those targets.

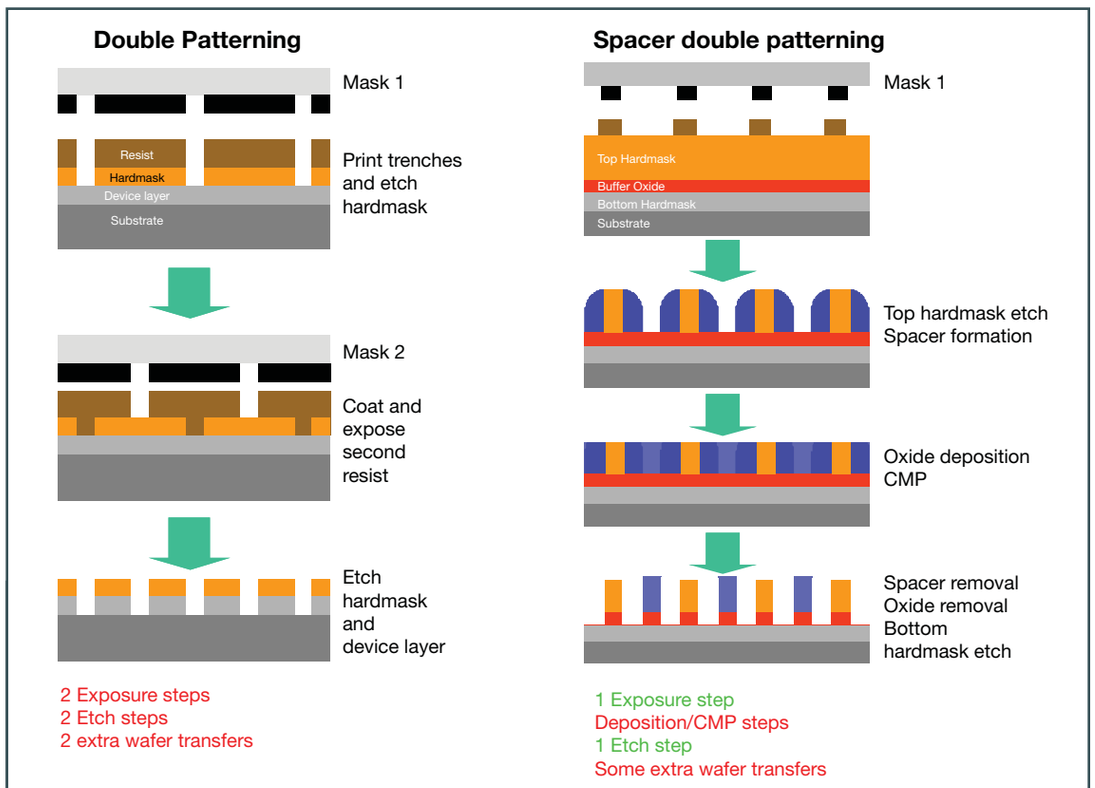

Figure 2. Double patterning options as defined by the ITRS lithography chapter. On the left is the litho/etch/litho/etch approach with two critical exposures. On the right is spacer double patterning where process steps convert each patterned critical feature into two features.

Gate Scaling and CD Uniformity

One of the traditional challenges in the ITRS Lithography roadmap has been the control of gate CD uniformity. In 2008, two significant changes occur in the ITRS tables. First, the MPU gate physical size requirements from the FEP chapter have been relaxed, reflecting the less-aggressive gate size scaling practiced in the industry. Therefore, the printed gate size has also been relaxed, and therefore also the printed CD uniformity which is calculated as 12 percent of the gate size. Second, many companies have been achieving the aggressive CDU by implementation of design restrictions. In prior

Optical Mask Requirements	2007 65	2010 45	2013 32	
Image Placement (Single Exposure)	8.2	5.4	3.8	1 node
Image Placement (Double Exposure) (Independent)	5.8	3.8	2.7	
Image Placement (DE) (Lines Dependent)	2.4	1.6	1.1	4 nodes
Mean to Target (MTT)	5.5	3.6	2.5	
Difference in CD MTT for DE	2.7	1.8	1.3	2 nodes
CD Uniformity (nm, 3 Sigma) Isolated Lines	3.3	1.8	1.4	
CD Uniformity (nm, 3 Sigma) Dense Lines	5.2	3.4	2.4	
DE - Dual Line Mask CD (nm, 3 Sigma)	2.4	1.6	1.1	2 nodes

Figure 3. Mask requirements for double patterning compared to those for single exposure. Double exposure with independent features requires a small acceleration of the mask roadmap, but achieving full specifications with dependent feature exposures requires a much larger acceleration.

roadmaps, this has been reflected by using the orange "work-arounds available" coloring in the roadmap. Now the definition for MPU gate CDU will change to reflect the use of restricted pitches and orientations in MPU designs. Both of these changes help to improve the ability to meet the gate CDU target.

However, one additional table change reflects a newly identified challenge for achieving CDU. At small gate widths, fluctuations in line width roughness can cause changes in the effective gate size. This effect is dependent upon the spatial frequency of the roughness as measured parallel to the edge of the line. So a certain error budget of the gate CD was assigned to this effect and a corresponding maximum correlation length of the roughness was calculated for each half-pitch. For the 32nm half-pitch, the maximum correlation length is about 20nm.

Year of Production	2010	2013	2016
DRAM 1/2 pitch (nm) (contacted)	45	32	22
DRAM			
DRAM 1/2 pitch (nm)	45	32	22
CD control (3 sigma) (nm)	4.7	3.3	2.3
Contact in resist (nm)	50	35	25
Contact after etch (nm)	45	32	23
Overlay (3 sigma) (nm)	9.0	6.4	4.5
Flash			
Flash 1/2 pitch (nm) (un-contacted)	36	25	18
CD control (3 sigma) (nm)	3.7	2.6	1.9
Contact in resist (nm)	39	28	20
Contact after etch (nm)	36	25	18
Overlay (3 sigma) (nm)	11.8	8.3	5.9
MPU			
MPU/ASIC Metal 1 (M1) 1/2 pitch (nm)	45	32	23
MPU gate in resist (nm)	35	25	18
MPU physical gate length (nm)	27	18	14
Gate CD control (3 sigma) (nm)	2.8	1.9	1.5
Contact in resist (nm)	56	39	28
Contact after etch (nm)	51	36	25
Overlay (3 sigma) (nm)	11	8.0	5.6

Figure 4. Format of ITRS 2008 Lithography Technology Requirements Table Showing the Comparison of Requirements for DRAM, Flash and MPU Products

Lithography Requirements: Memory and Logic

Because several of these changes now reflect differing requirements between MPU and memory technologies, the ITRS Litho tables are being reorganized. The overall lithography technology requirements table is separated into sections for Flash memory, DRAM and MPU. This change was implemented to clarify the timing for CD uniformity and overlay needs for each technology.

For example, at the 32nm DRAM half-pitch with 2013 manufacturing target, the Flash half-pitch is 25nm (two years acceleration), which results in Flash having a 2.6nm CD uniformity target. But MPU gate CD uniformity in the same year is 1.9nm (about a three-year acceleration) (see Figure 4). And the tight requirements for overlay for DRAM drive represent about a two-year acceleration for DRAM overlay compared to Flash and DRAM. It is not certain whether these different requirements will drive different lithography solutions, but the ITRS tables now provide a clear outlook for the industry development teams.

Summary and Outlook

The current ITRS Lithography updates reflect the need to implement double patterning in one or more forms to enable the lithography roadmap through the 32nm half-pitch. Double patterning requirements have been clarified from the earlier ITRS updates and reflect the complexity of different versions of double patterning. These requirements do drive acceleration of the mask roadmap, and implementing double patterning beyond 32nm half-pitch will be challenging. So if the new lithography technologies can be enabled by meeting the key roadmap targets, they are likely to displace double patterning. However, for the 32nm half-pitch, a narrowing of the accepted lithography options is highly likely in the next roadmap update. Lithogra-phy technology continues to enable dimensional scaling, but the roadmap continues to evolve. The ITRS lithography chapter is far from a perfect predictor of the future, but represents the best guess of the industry experts today.

Acknowledgments

The author would like to point out that the ITRS litho chapter represents the input of all of the litho working groups around the world (U.S., Japan, Europe, Taiwan and Korea) and owes many thanks to the dedication and contributions of these teams.

About the Author

Michael Lercel

Michael Lercel is the manager of IBM's Strategic Equipment council, which oversees the microelectronics equipment selection for all process sectors. Formerly, he was director of the Lithography division of SEMATECH as an assignee from IBM. He served as chairman of the ITRS Lithography Working Group from 2005 to 2008. ■

- Link to 2007 ITRS Lithography Chapter
- Link to 2008 ITRS Update Table (download FOCUS_B.xls)

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SAFC Hitech: Changing the Face of Materials Technology

Materials science is playing a pivotal role in the ongoing evolution of the semiconductor industry, as electronic devices offer enhanced functionality in smaller footprints. Greater complexity in device manufacturing means that "traditional" semiconductor materials are unable to continue to deliver the performance demanded, and there is a rapid expansion in the scope of materials being considered for use in future semiconductor iterations. The molecular chemistry required to manufacture advanced materials in the high purity and volume required are key factors in the continuation along the ITRS roadmap.

SAFC Hitech™ is at the forefront of the electronic materials revolution, providing unique chemistry services translating an in-depth understanding of silicon semiconductor performance requirements into the materials required to achieve them. Through collaborative partnerships and an integrated approach – from research and development, process development and scale-up to commercial manufacturing – SAFC Hitech continues to invest in innovation and manufacturing, enabling current and future technology needs.

With significant success both in materials development and delivery systems for high-k oxides such as Al_2O_3, we have developed high-volume manufacturing processes for high-purity materials for hafnium and zirconium oxides, including some previously unknown materials that offer improved process performance. As we continue to develop our advanced materials program by adhering to the ITRS roadmap, our customer-centric approach means that, through early-stage engagement with customers, we are able to address the issues facing them and, by designing molecules that deliver next-generation performance and/or resolve issues in fab processes, help them to stay ahead of the curve.

ITRS CHAPTER: Front End Processes

Jeffery W. Butterbaugh,[1] Larry Larson,[2,3] Raj Jammy[2]
[1]FSI International; Chaska, MN [2]SEMATECH Inc.; Austin, TX [3]Texas State University at San Marcos, TX

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Scope

The Front End Processes (FEP) chapter of the ITRS (International Technology Roadmap for Semiconductors) focuses on future process requirements and potential solutions for the continued scaling of devices based on field effect transistors (FET); including high-performance, low-operating power and low-standby power logic devices; dynamic random access memory (DRAM) devices; and nonvolatile memory devices. This chapter defines comprehensive future requirements and potential solutions for the key front end wafer fabrication process technologies and materials associated with these devices. It addresses equipment and materials, as well as unit and integrated processes beginning with the substrate and extending through contact silicidation and deposition of strain layers. This chapter also addresses fabrication of storage nodes for the various memory devices.

The FEP chapter is divided into several subsections: starting materials, surface preparation, thermal/thin films, doping, plasma etch, DRAM, flash memory, phase-change memory and ferroelectric memory (FeRAM). Each subsection provides a forecast of scaling-driven technology requirements and potential solutions. As much as possible, the requirements tables are model-based, with the models described in the table notes. The potential solutions figures serve to benchmark known examples of possible solutions, and are intended for researchers and interested parties. They are not to be considered the only approaches. Indeed, innovative, novel solutions are sought, and their need is identified by red-colored regions of the requirements tables.

Materials-Limit Device Scaling

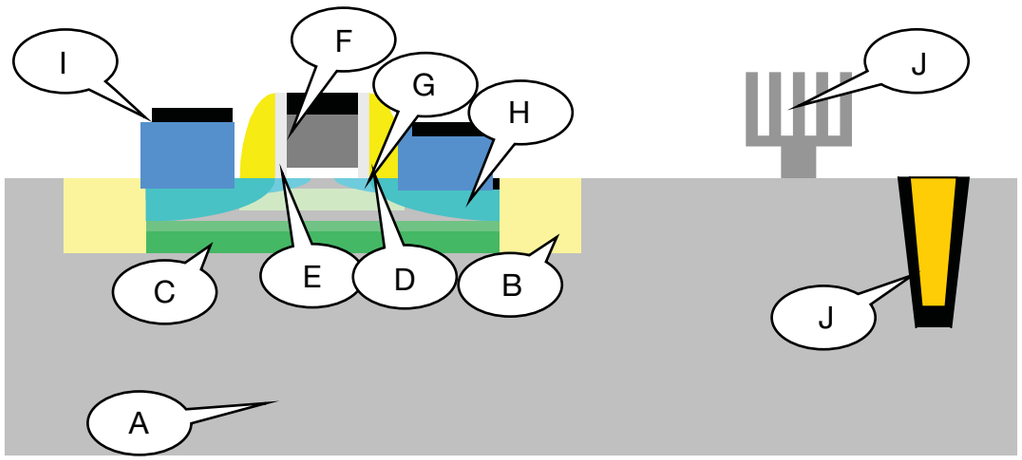
FET scaling has been the primary means by which the semiconductor industry has achieved the historically unprecedented gains in productivity and performance quantified by Moore's Law. These gains have traditionally been paced by the development of new lithography tools, masks, photoresist materials and critical dimension etch processes. In the past several years, it has become clear that despite advances in the ability to produce ever-smaller feature sizes, front end process technologies have not kept pace, and scaled device performance has been compromised. The traditional transistor and capacitor formation materials – silicon, silicon dioxide and polysilicon – have been pushed to fundamental material limits, and continued scaling has required the introduction of new materials. The current situation can be defined as "material-limited device scaling." In addition, new approach-

es to device structure, such as nonplanar multi-gate devices, will be needed for future performance scaling.

Material-limited device scaling has placed new demands on virtually every front end material and unit process, starting with the silicon wafer substrate and encompassing the fundamental planar CMOS building blocks and memory storage structures.

In no area is the issue of material-limited device scaling more clear or urgent than in the FET gate stack. Here, new gate dielectric materials having a higher dielectric constant than SiO_2 have been introduced to full production in 2008, along with metal in place of polysilicon for the gate electrode. Mobility enhancement and channel-length scaling, which requires accelerated scaling of junctions to control short channel effects, will continue to provide enhanced device performance.

In addition, the end of planar bulk CMOS is becoming visible within the next several years. As a consequence, we must be prepared for the emergence of CMOS technology that uses nonconventional FETs or alternatives such as planar fully depleted SOI (FDSOI) devices and dual- or multi-gate devices, either in a planar or vertical geometry. The introduction of these devices will require the replacement of bulk silicon substrates with ultrathin, silicon-on-insulator (SOI) substrates and double- or multi-gate devices. The transition from extended bulk CMOS to nonclassical device structures is not expected to take place at the same time for all applications and all chip manufacturers. Instead, a scenario is envisioned where a greater diversity of technologies are competitively used at the same point in time – some manufacturers choosing to make the transition to nonclassical devices earlier, while others emphasize extensions of bulk technology. This is reflected in the Thermal/Thin Films/Doping and Etching Technology Requirements Table FEP4 by the projection of requirements for multiple approaches in the transition years from 2010 through 2015.



A: Starting Material
B: Isolation
C: Well Doping
D: Channel Surface (Preparation)
E: Channel Doping and Channel Strain
F: Gate Stack (including Flash) and Spacer
G: Extension Junction and Halo
H: Contacting Source/Drain Junction
I: Elevated Junction and Contacts
J: DRAM Stack/Trench Cap. & FeRAM Storage

Figure 1. Front End Process Chapter Scope

In starting materials, the projection of a 450 mm silicon substrate in 2012 is identified as a difficult challenge.

In the memory area, high-κ materials are now in use for DRAM capacitors. DRAM stacked capacitors are also now using metal-insulator-metal (MIM) structures. It is expected that high-κ materials will be required for the floating gate Flash memory interpoly dielectric by 2010, and for tunnel dielectric by 2013. The introduction of these diverse materials into the manufacturing mainstream is viewed as important difficult challenges. In addition, phase-change memory (PCM) devices are expected to make a commercial appearance by 2010.

In starting materials, the projection of a 450 mm silicon substrate in 2012 is identified as a difficult challenge. Such a diameter move is indicated to maintain pace with historic productivity enhancements based on augmented transistor count performance enhancements. However, so-called "More than Moore" approaches, which leverage enhanced design and/or inclusion of non-CMOS content, continue to find more applications within the industry. Also, higher productivity 300 mm fab approaches are being pursued. These trends may delay the need for 450mm wafers. The ITRS is actively considering how such approaches will impact overall productivity requirements. Should it be necessary to adopt the next diameter silicon wafer, there are concerns whether the incumbent techniques for wafer preparation can be cost-effectively scaled to the next generation.

Front end cleaning processes will continue to be impacted by the introduction of new front end materials such as high-κ dielectrics, metal gate electrodes and mobility-enhanced channel materials. Scaled devices are expected to become increasingly shallow, requiring that cleaning processes become completely benign in terms of substrate material removal and surface roughening. Scaled and new device structures will also become increasingly fragile, limiting the physical aggressiveness of the cleaning processes that may be employed. In addition, these new device structures will require precise cleaning and characterization of vertical surfaces. DRAM stacked and trench storage capacitor structures will show increasing aspect ratios, making sidewall contamination removal increasingly difficult. Also, there is a challenge for particle scanning technology to reliably detect particles smaller than 28nm on a wafer surface for characterization of killer defect density and to enable yield learning.

2008 Update Highlights

Most of the FEP tables have required updates for 2008. The most significant updates occurred in Tables FEP4a and FEP4b – Thermal/Thin Films/Doping/Etch. The changes in FEP4 are driven by the new ORTC model of physical gate length scaling for high performance (HP), low operating power (LOP) and low standby power (LSTP) logic devices. Ideally, the FEP and PIDS teams would have liked to completely rework all of the device scaling models, adjusting CV/I scaling and taking into account the projected implementation of new CMOS structures, such as fully depleted SOI (FDSOI) and multi-gate/FinFET (MG). However, due to limited resources in this "update" year, the FEP and PIDS teams decided to use the calculated table metrics from the 2007 ITRS publication by shifting and interpolating columns, using the physical gate length as the interpolation scaling factor. For the years 2007 through 2009, table metrics from the 2005 ITRS publication are used. In some years (2007, 2012, 2013 and 2016 for HP) the new ORTC physical gate length matches that for an earlier year in the 2007 or 2005 publication (2005, 2009, 2010 and 2012, respectively, for HP). In those cases, the metrics in that column are simply shifted to the new year. In most other cases, the new physical gate length in a particular year falls between the values in the 2007 roadmap. In those cases, the metrics for the new column are calculated by interpolating the values in each row using the physical gate length as the interpolation factor. This method of shifting and interpolating is used for HP and LOP metrics, but not for LSTP metrics, since the change in LSTP physical gate length scaling is relatively minor. FEP and PIDS recognize that this is not a completely satisfactory approach to accommodating the new ORTC physical gate length roadmap. This approach produces some "artifacts" that are discussed below. Both FEP and PIDS are committed to a complete recalculation of table parameters in 2009.

One artifact of the 2008 update "shift/interpolate" approach is a push out of metrics for FDSOI and MG devices and an extension of metrics for bulk planar devices. For HP logic, bulk planar metrics, which previously ended in the year 2012, now end in the year 2016. Metrics for HP FDSOI, which previously ran from 2010 to 2015 now run from 2013 to 2019, and metrics for HP MG, which previously started in 2011, now start in 2015. Similarly, for LOP logic, bulk planar device metrics which previously ended in 2012 now end in 2013; LOP FDSOI metrics, which previously ran from 2011 to 2016, now run from 2013 to 2018; LOP MG metrics, which previously started in 2011, now start in 2015. LSTP metrics for FDSOI prior to 2013 and for MG prior to 2015 are deleted so that FDSOI and MG start in the same year for all devices. At this time, FEP and PIDS are not sure if these shifts accurately represent when bulk planar will no longer be used in leading-edge device manufacturing or when FDSOI or MG will first be implemented in full manufactur-

Difficult Challenges < 22nm	Summary of Issues
Starting Materials	FDSOI Si and buried oxide thickness control
	SOI defectivity
	Surface particles
Surface Preparation	Surface particles not measurable
	Ability to achieve clean surfaces while controlling material loss and surface damage
	Metrology of surfaces that may be horizontally or vertically oriented relative to the chip surface
	Achievement of statistically significant characterization of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface
	Achievement and maintenance of structural, chemical and contamination control of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface
Thermal/Thin Films/ Doping/Etch	Continued scaling of HP multi-gate device in all aspects: EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation
	Continued EOT scaling below 0.7nm with appropriate metal gates
	Gate CD Control
DRAM	Continued scaling of capacitor structures for both stacked and trench type as well as continued scaling of dielectric thickness
Non-volatile Memory	Floating gate Flash technology considered unscalable beyond 22nm – new Flash NVM technology will be required
	Continued scaling of phase change memory technology
	Continued scaling of FeRAM technology

Table 1. Front-End Processes Difficult Challenges <22nm – 2008 Update

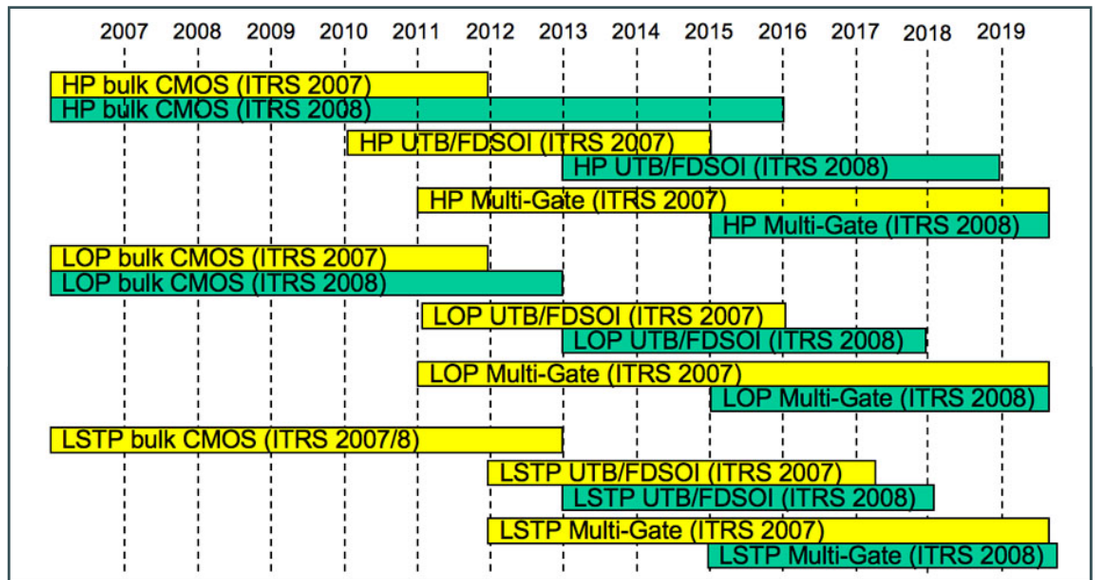


Figure 2. "Artificial" shift in expected introduction of FDSOI and MG structures due to "shift/interpolate" method used to accommodate the change in physical gate length scaling for the 2008 update. This will be fully reviewed and addressed in 2009.

ing. The timing of the implementation of these new device structures will be fully reviewed in the 2009 roadmap.

Another artifact is caused by using metrics from the 2005 publication. In 2005, some of the model assumptions were different, so some metrics from 2005 do not flow smoothly into the metrics published in 2007. In those cases, minor changes are made to smooth the transition. In addition, the six rows which are included in both the PIDS and FEP tables were compared and minor adjustments are made for complete consistency.

Updates are also made in the Starting Materials, Surface Preparation, Stacked DRAM, Trench DRAM tables. Most of these changes are related to a small change in the ORTC DRAM 1/2-pitch scaling for 2007–2009. For Trench DRAM, all table entries from 2009 through 2022 have been deleted, recognizing that the last developer of stand-alone trench DRAM devices announced the end of trench DRAM after the 58nm generation.

Summary

This article summarizes the 2008 Changes in the Front End Processes (FEP) chapter of the ITRS. This document focuses on future process requirements and potential solutions for the continued scaling of devices based on field effect transistors (FET), including high-performance, low-operating power and low-standby power logic devices, dynamic random access memory (DRAM) devices, and nonvolatile memory devices.

The current scaling situation is termed "material-limited device scaling." Material-limited device scaling has placed new demands on virtually every front end material and unit process, starting with the silicon wafer substrate and encompassing the fundamental planar CMOS building blocks and memory storage structures.

In no area is the issue of material-limited device scaling more clear or urgent than in the FET gate stack. Here, new gate dielectric materials having a higher dielectric constant than SiO_2 have been introduced to full production in 2008, along with metal in place of polysilicon for the gate electrode.

In no area is the issue of material-limited device scaling more clear or urgent than in the FET gate stack.

Updates were also made in the Flash and PCM Tables (FEP7 and FEP8). Information from Flash manufacturers show that the oxy-nitride-based technology can survive until 28nm for NAND and until 32–40nm for NOR with a transition period. Also, selective trench fill technology should overcome the intrinsic limitations of spin-on-dielectric. In FEP8, heater resistivity change is made less aggressive in consideration of the parallel increase of the reset current density.

In addition, new approaches to device structure, such as nonplanar multi-gate devices, will be needed for future performance scaling. The end of planar bulk CMOS is becoming visible within the next several years. As a consequence, we must be prepared for the emergence of CMOS technology that uses nonconventional FETs or alternatives such as planar fully depleted SOI (FDSOI) devices and dual- or multi-gate devices, either in a planar or vertical geometry.

Each Technical Working Group assembled a list of their most difficult challenges. This table is included in this document for your review. We would like to call attention to several of these, as they clearly are challenges that will shape the future of the industry in years to come.

The most significant updates occurred in Tables FEP4a and FEP4b - Thermal/Thin Films/Doping/Etch. The changes in FEP4 are driven by the new ORTC model of physical gate length scaling for high performance (HP), low operating power (LOP) and low standby power (LSTP) logic devices. These changes in device scaling timing resonate throughout the ITRS, and 2009 will have a focused effort to produce consistency in our tables.

In starting materials, the projection of a 450 mm silicon substrate in 2012 is identified as a difficult challenge. Front end cleaning processes will continue to be impacted by the introduction of new front-end materials such as high-κ dielectrics, metal gate electrodes and mobility-enhanced channel materials.

In the memory area, high-κ materials are now in use for DRAM capacitors. DRAM stacked capacitors are also now using metal-insulator-metal (MIM) structures. It is expected that high-κ materials will be required for the floating gate Flash memory interpoly dielectric by 2010, and for tunnel dielectric by 2013.

These are all truly critical issues facing the future development pathway of our industry. We have a clear vision of changes that need to be accommodated in the 2009 update of the roadmap, and we look forward to the challenge of facing these critical issues.

About the Authors

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Jeffery W. Butterbaugh is chief technologist for FSI International. He joined FSI in 1993. Prior to FSI, Dr. Butterbaugh worked for IBM and for Seagate Technology. He received his Ph.D. in chemical engineering from MIT and his B.S. from the University of Minnesota. He holds nine U.S. patents and is an author/co-author of more than 50 publications/presentations.

Larry Larson

Larry Larson joined SEMATECH in 1990, and currently coordinates the ITRS participation for the Front End Processes division in addition to coordinating academic efforts. He simultaneously has served as a professor in various roles at Texas State University at San Marcos since 2001. Dr. Larson received his Ph.D. in physics from Washington State University. He is an author/co-author of more than 120 publications/presentations.

Raj Jammy

Raj Jammy is vice president of Materials and Emerging Technologies at SEMATECH. Previously on assignment from IBM, he has joined the SEMATECH staff and will continue to direct SEMATECH's Front End Processes division as well as lead efforts to tap in to emerging technologies with disruptive scaling potential. Jammy holds a doctoral degree in electrical engineering from Northwestern University. He holds more than 50 patents and is an author/co-author of over 170 publications/presentations. ■

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Jeff Wetzel
Senior Member of the Technical Staff; SVTC Technologies, LLC

The Interconnect Technical Working Group (TWG) has briefly summarized the evolution of copper interconnect process technology over the past 10 years.

They point out that many challenges thought best solved by material and/or process innovation – such as lowering dielectric constant aggressively or refining metallization microstructure – were in fact bypassed by innovations in design or chip architecture.

The TWG has highlighted current development efforts to improve reliability of interconnects and how these will be correlated with a new metric, known as the Power Metric, which is related to dynamic power and its influence on the thermomechanical stability of the interconnect layers.

The TWG ends its roadmap update by reviewing development of new materials and process architectures that are candidate solutions for the future as interconnect features are scaled to smaller dimensions.

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replisaurus technologies

The Future of Copper Redefined

Replisaurus' advanced metallization technology targets micro and nanoscale metal structures used for applications within microelectronics, optoelectronics, sensors, flat panel displays and advanced circuit boards. Replisaurus' ECPR™ technology redefines the fundamentals of micro and nanoscale metallization and delivers a metallization process with superior performance/cost ratio.

The integrated "ElectroChemical Pattern Replication" (ECPR) process is an enabling technology targeted at key growth markets such as integrated passives, copper pillars and 3D integration (TSV). The company has demonstrated fine pitch/high-resolution capability (<280nm space) and significantly improved thickness uniformity. The Replisaurus process offers a simple and cost-effective integrated solution eliminating several traditional process steps, thereby reducing complexity. The number of process steps in a typical metallization flow are reduced from eight (8) to three (3), resulting in shorter cycles times and a simplified production flow.

ECPR™ is a fab-friendly, environmentally clean process that does not use any solvents, developers or strippers and has extremely fast plating rates. The ECPR™ technology is a "Design Enabling" technology for integrated passives enabling advanced designs, eliminating the need for prototyping and dummy plating patterns. The electrochemical replication principle of ECPR™ combines the precision and resolution of advanced lithography with the ease and efficiency of electrochemical deposition into one single integrated process solution.

Consequently, ECPR™ is a clean technology that significantly reduces costs for equipment, maintenance, personnel, clean room, and direct materials as well as provides high throughput capabilities due to its cycle-time efficiency. Replisaurus Technologies offers complete production solutions including IP-enabled equipment, replication templates (masters), chemicals and technology transfer.

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ITRS CHAPTER: Interconnect

Christopher Case
The Linde Group

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The Interconnect chapter of the ITRS concerns the wiring system that distributes clock and other signals to the various functional blocks of the integrated circuit, along with providing necessary power and ground connections. The scope covers the interlevel dielectrics (ILD) and conductors, beginning at the contact level with the pre-metal dielectric and continuing up through the device from metal 1 through global wiring. It includes associated planarization and any necessary etches, strips and cleans. The chapter also addresses reliability and system and performance issues. The "Grand Challenge" has traditionally been viewed as the delay associated with global wires, and delay generally remains a key challenge. Enabling high-bandwidth low-power signaling is the current approach of the 2008 Interconnect Technology Working Group (TWG) for addressing delay. Although the group continues to forecast the use of copper as the primary conductor in a dual-damascene architecture through the end of the 15-year forecast horizon, much of the current work focuses on new challenges and trends associated with 3D integration and emerging technology.

A brief review of the changing face of interconnect is valuable for understanding the latest focus. The original 1991 Micro Tech 2000 Workshop[1] report identified the importance of metallization as a technology driver for integrated circuits. It was not until the second edition of the SIA[2] National Technology Roadmap for Semiconductors in 1994 that the Interconnect group first discussed the need to make basic changes in the silicon dioxide/aluminium wiring technology and began addressing the challenges of low dielectric constant materials and a switch to copper wiring to address the global wiring delay. The switch to copper and low κ along with the introduction of a hierarchical wiring approach, allowing for wider wires with higher conductivity at the upper levels, have been the two most significant changes in integrated circuit wiring technology since the first CMOS devices. Local wiring has never been considered an RC delay challenge because of the short wiring lengths used to connect transistors within an execution unit.

The original 1991 Micro Tech 2000 Workshop report identified the importance of metallization as a technology driver for integrated circuits.

The intervening decade from 1994 saw the firm establishment of electrochemically deposited copper for logic devices but a failure of the industry to achieve roadmap goals associated with lowering the dielectric constant of the insulator. In spite of this, and accompanied by numerous revisions to the dielectric constant roadmap (Figure 1) frequently showing a push-out in implementation,[3] the IC industry has managed to maintain the productivity improvements attributed to Moore's Law suggesting that delay concerns are not a simple issue. Further, the impact of copper wiring resistance increases due to scattering at grain boundaries and surfaces has been established as real and matches modeled predictions well, but has not impeded the designers' ability to achieve necessary performance.

Dealing with delay has always been a crucial activity for high-performance chip designers. The scaled wires in the local and intermediate levels are less impacted by scattering and have smaller increases in RC

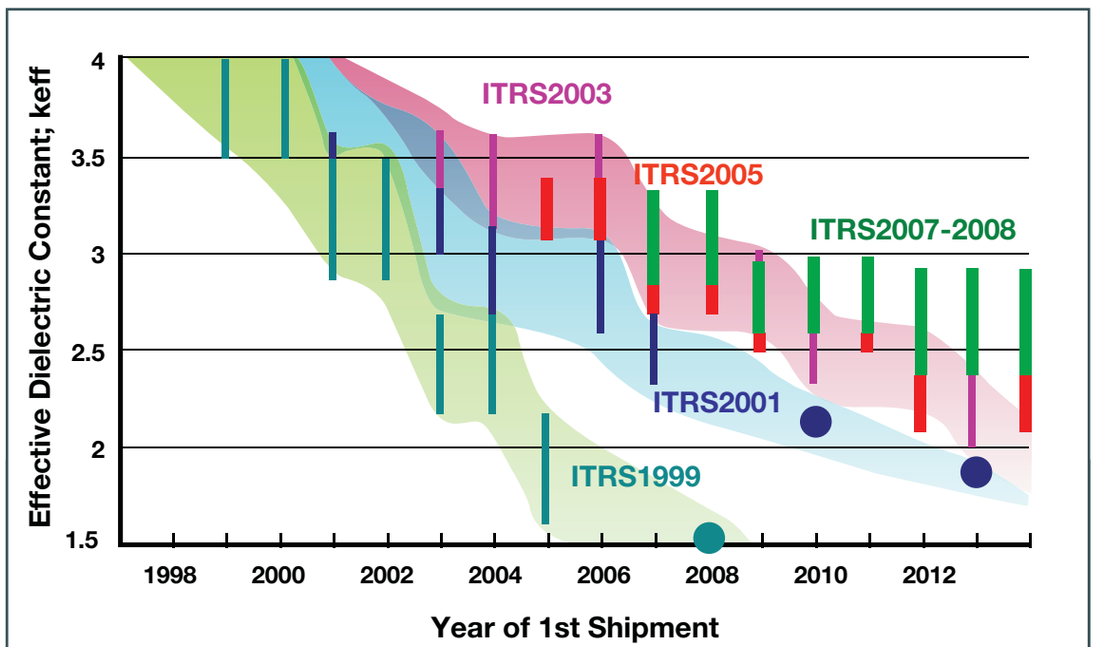

Figure 1. Historical Transition of the Low-κ Roadmap
Courtesy of H. Shibata (Toshiba) and the Japan Interconnect TWG

delay. Semi-global and global layers often need repeaters to manage delay, consuming chip real estate and power. The relatively recent introduction of multiple-core architectures helps by shortening wiring lengths. This allows operation at lower core frequencies and decreases power consumption. The reduced supply voltage for devices has exacerbated cross-talk issues. The MPU[4] Interconnect Technology Requirements Table contains a cross-talk metric that is calculated as the line length at which 25 percent of the switching voltage is induced on a minimum pitch wire. A related issue is power distribution at which the reduced V_{dd} and higher supply current causes larger voltage drops. As much as 50 percent of the power of a microprocessor is consumed by losses in the interconnect, and projections for the next few years are that this figure could rise to 80 percent.[5]

Copper wiring was adopted partly due to the expectation that it would have higher intrinsic reliability than aluminum. Unfortunately, the accelerated scaling of the MPU pitch has aggravated the electromigration of copper wiring as well. Metal reliability is strongly dependent on the properties of the wiring system (the surrounding dielectric, barrier, nucleation layer stack). Although not all device manufacturers require the highest reliability, those that do are exploring modifications of the copper surface to form CuSiN or are implementing selectively deposited caps such as CoWP.[6] This capping approach does enhance the electromigration resistance but at the expense of reduced yield from metal shorts.

Thermo-mechanical worries are not new to IC designers, with the high power dissipation of many MPUs. A principal benefit of the combination of high-κ materials for transistors and low-κ materials for the ILD has been to reduce power, mitigating to an extent failures from heat. An increase in the number of levels and the lowest-κ ILDs with limited mechanical strength has again made these concerns relevant, along with worries about noise. Although the capacitance per unit length is decreasing, the dynamic power is expected to increase again due to the greater number of metallization layers. The TWG has introduced a new metric, the Power index (W/GHz-cm^2),[7] to highlight these issues, and the latest changes can be found there, along with updates to the capacitance per unit length.

The 2008 difficult challenges of the traditional scaled metal/dielectric systems are concerned with new dielectrics, the filling of small features and reliability. It is not only new materials, but the complexity of managing many materials that is challenging. Increasing ILD porosity will increase the efforts required to manage line and via sidewall roughness. Copper sidewall and surface roughness will adversely affect electron scattering, which continue to cause significant increases in resistivity. The challenges of thin barrier and nucleation layers, expected to have been addressed by atomic layer deposition (ALD) approaches, has emerged as a top area of concern. Finer features, delays in commercializing ALD solutions and rougher interfaces with porous ILDs are all contributors. Consequently, the working group has classified meeting the barrier cladding thickness technology requirement as a red challenge (beginning in 2012). Continued concerns over sidewall damage of the porous low-κ films and the impact on the effective dielectric constant have pushed integration technologists to look at ways to minimize damage, repair damage or seal the pores. Solutions here, along with the reduction or elimination of intermediate etch stops, are key to a successful realization of the benefits from the use of lower-κ materials. For 2008, there are minor updates to the High Performance dielectric constant specifications, but there has been a major delay for DRAM. The use of materials that deliver an effective κ in the range of 3.1–3.4 has been pushed back by three years to 2011. In addition, the contact aspect ratio metric has been amended to match those published by the Front End Processes TWG. Although they are aggressive (>40 in 2015), they have been relaxed from 2007, and only apply to the stacked capacitor configuration; metrics for trench capacitor have been deleted from the table. New calculations of Jmax based upon the revised (reduced) roadmap suggest that the current specified limit of 10E6 A/cm^2 will not be exceeded during the current roadmap horizon.

The 2008 difficult challenges of the traditional scaled metal/dielectric systems are concerned with new dielectrics, the filling of small features and reliability.

The projection for interconnect evolution in the short term is to address interconnect delay problems in new ICs by circuit design, within the constraints of planar technology, with special attention to minimizing critical path lengths. This will be done in concert with a substantial push in Cu/low-κ technology, as well as more innovative packaging and board approaches, to minimize the changes needed in design architectures while still meeting the contin-

2a

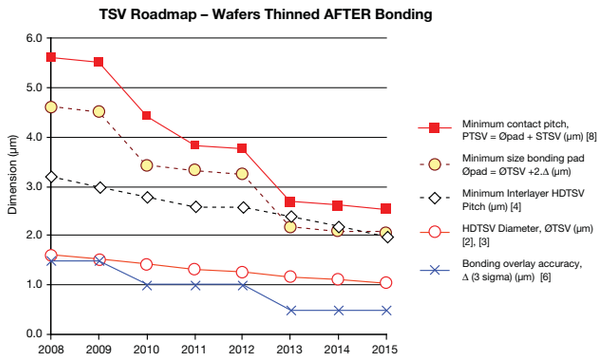

Figure 2a. TSV Roadmap Wafers Thinned After Bonding
Courtesy of L. Smith; SEMATECH

2b

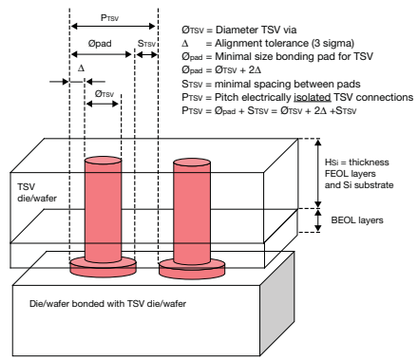

Figure 2b. TSV Model
Courtesy of Eric Beyne; IMEC, Belgium

ued advances in performance projected by the ITRS. In the intermediate term, Cu/low-κ will be pushed to the limits, and new design architectures, as well as chip-package co-design, will be achieved with new CAD tools to significantly facilitate needed performance advances. The Interconnect TWG has embraced the man-tra "More than Moore," and has identified challenges associated with meeting the requirements for equivalent scaling to highlight that traditional scaling is not the only approach for advancing IC technology. These are predominantly design and architecture changes that include 3D approaches with through silicon vias (TSV). The design and processing of 3D chip stacking through the use of high-density TSVs (HDTSV) is a key focus area to address delay and power concerns; developing manufacturable and cost-effective solutions is a new interconnect challenge.

The primary interest in 3D interconnects is to reduce line lengths by stacking active devices. Calculations show that up to a 50 percent reduction in total global wiring length can be achieved via 3D stacking, which would bring a fourfold increase in clock frequency, accompanied by a halving of power dissipation.[8] HDTSVs implemented for 3D stacking of chips will enable the highest bandwidth and lowest energy interfaces between memory and logic systems. This architecture could be used for heterogeneous integration with minimal parasitics. Analog and digital systems can be mixed, along with the stacking of devices fabricated on different substrate materials. To be most effective, the architecture of the chip will have to change, and macros or functional units might be better separated on different tiers (i.e., wafers). The 2008 roadmap forecasts the critical dimensions (based upon a model of a stacked-wafer arrangement in which the wafers have been thinned to 10 microns) (Figure 2a). The model (Figure 2b) assumes that the TSV diameter is limited by the wafer thickness and TSV aspect ratio. Further, the pitch is limited by TSV diameter, misalignment tolerance and minimum pad spacing. This face-to-face wafer bonding approach is not the only approach to 3D integration but would have very high bandwidth and low power dissipation.

The roadmap addresses traditional scaling, equivalent scaling and functional diversity with the use of both conventional materials along with approaches the TWG has identified as emerging. The possible use of new signaling technologies is not new to the working group, and progress has been made in several of the fields, including the use of carbon nanotubes for wires and vias. Options for progressing interconnect performance significantly beyond that which is enabled by 3D integration will require materials and structures that differ from the conventional metal/dielectric system and could use carriers other than charge for transfer. It is expected that any system that uses different physics for signal propagation must still be fabricated with CMOS-compatible tool sets. Optical interconnects will not replace the lower levels of copper and low κ because of pitch constraints, but would be used where appropriate to increase overall system performance. Optical signal transmission paths have an additional advantage: They suffer from virtually no cross talk between paths.

Optical signal transmission paths have an additional advantage: They suffer from virtually no cross talk between paths.

The high electrical and thermal conductivity have made carbon nanotubes a potentially disruptive but attractive materials change for use in chips. Five years have marked significant progress from the first demonstrations of metal-seeded via bundles. The one-dimensional nature of the phase-space for CNTs gives rise to mean free paths in the micron range versus tens of nanometers for copper. Densely packed CNT bundles can have conductivity that exceeds copper wires at long lengths, although it is limited by quantum resistance, which in turn depends upon the number of conduction channels. CNTs, which are of course just rolled graphene sheets with strong sp^2 bonds, have very high current densities, reportedly in excess of 10E9 A/cm^2.[9] Contrasted with practical limits around 1E6 A/cm^2 for copper, the potential for enhanced reliability is clear. The longitudinal thermal conductivity of an isolated CNT has been modeled and is expected to be very high, on the order of 6000 W/mK,[10]or 15 times that of copper.

Of course, CNT-bundles can only outperform copper if the bundle density is sufficiently high; many technical challenges remain. The nature of the catalyst is critical for determining the diameter and density of the nanotubes, and research efforts are focused in this area. One of the most exciting implementations is the use of graphene in ribbon that can be patterned by conventional lithography,[11] although performance degrades by electron scattering if the edges are imperfect.

There are more radical options beyond even carbon nanotubes, including molecular interconnects,[12] quantum waves[13] and spin coupling[14] that are in the infant stages of development, but in each case, the goal is propagating terabits/second at femtojoules/bit.

Acknowledgments

The ITRS Interconnect Chapter is prepared with the joint efforts of more than 50 technical experts from the five regional working committees: North America, Japan, Europe, Korea and Taiwan. Particular appreciation goes to the coordinating efforts of the other regional chairs: Hideki Shibata (Toshiba), Nobuo Aoi (Panasonic), CH Yu (TSMC), Hans Barth (Infineon), Alexis Farcy (ST Microelectronics), Hyundeok Lee (Samsung), Sibum Kim (Magnachip), and to Harold Hosack (SRC), Mauro Kobrinsky (Intel), Larry Smith (SEMATECH) and Robert Geffken from the U.S. Technical Working Group and Osamu Yamazaki (Sharp) from Japan.

Endnotes

1. National Advisory Committee on Semiconductors "Micro Tech 2000 Implementation Task Force Report," Feb. 28, 1992.
2. Semiconductor Industry Association
3. C. Case, "Low-κ Dielectrics: Was the Roadmap Wrong?" *Future Fab Intl.* Issue 17, 2004.
4. Microprocessor
5. N. Magen, A. Kolodny, U. Weiser, N. Shamir, "Interconnect-Power Dissipation in a Microprocessor," ACM System-Level Interconnect Prediction Workshop, February 2004.

6. C.K. Hu et al, "A Study of Electromigration Lifetime for Cu Interconnects Coated with CoWP, Ta/TaN, or SiCxNyHz," Proceedings of AMC, p. 253, 2003.
7. $P_{layer}\left[\frac{W}{GHz-cm^2}\right] = C \cdot V^2 \cdot a \cdot (1\,GHz) \cdot \left(e_w \cdot \frac{1\,cm^2}{\text{p}}\right) =$ Power per GHz per cm^2 of metal layer.

   C = capacitance per unit length.
   $V = V_{dd}$, p = pitch, e_w = wiring efficiency = 1/3,
   a = average activity factor of interconnects = 0.03
8. J. W. Joyner et al, "Impact of Three-Dimensional Architectures on Interconnects in Gigascale Integration," *IEEE Trans. On VLSI Systems*, vol. 9, No. 6, December 2001.
9. B. Q. Wei, R. Vajtai, P. M. Ajayan, "Reliability and current carrying capacity of carbon nanotubes," *Applied Physics Letters*, vol. 79, pp. 1172–1174, 2001.
10. S. Berber, Y.-K. Kwon, D. Tománek, "Unusually High Thermal Conductivity of Carbon Nanotubes," *Physical Review Letters*, vol. 84, p. 4613, 2000.
11. C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First, W. A. de Heer, "Electronic Confinement and Coherence in Patterned Epitaxial Graphene," *Science*, vol. 312, pp. 1191–1196, 2006.

    R. Van Noorden, "Moving towards a graphene world," *Nature*, vol. 442, pp. 228–229, 2006.

    D. A. Areshkin, D. Gunlycke, C. T. White, "Ballistic Transport in Graphene Nanostrips in the Presence of Disorder: Importance of Edge Effects," *Nano Lett.*, vol. 7, pp. 204–210, 2007.

    A. Naeemi, J. D. Meindl, "Conductance Modeling for Graphene Nanoribbon (GNR) Interconnects," *Electron Device Letters*, IEEE, vol. 28, pp. 428–431, 2007.
12. N. Rana et al. "Investigation of substrate selective covalent attachment for genetically engineered molecular interconnects," *Materials Research Soc. Research Soc. Symp. Proceedings*, vol. 728, 2002.
13. A. Raychowdhury, K. Roy, "Nanometer Scale Technologies: Device Considerations" in *Nano, Quantum And Molecular Computing: Implications To High Level Design And Validation*, Kluwer Academic Publishers, ISBN: 1402080670, June 2004.
14. *Transactions on Electron Devices*, Special Issue on Spintronics, vol. 54, No. 5, May 2007.

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- Link to 2007 ITRS Interconnect Chapter
- Link to 2008 ITRS Update Table (download FOCUS_B.xls)

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METROLOGY, INSPECTION & FAILURE ANALYSIS

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Ehrenfried Zschech
Sr. Manager, Center for Complex Analysis; AMD Fab 36 LLC & Co. KG

More than ever before, the dramatic productivity enhancement of IT requires applications with significantly increased electrical and optical functionality. The respective micro- and nanoelectronic products will rely both on the continuous shrinking of feature sizes as well as the introduction of new materials and design concepts. In the following two papers, two highly reputable scientists – Alain Diebold and Lothar Pfitzner – each reflect the key challenges to metrology and yield enhancement strategies for future technology nodes as outlined in the ITRS, and they explain their personal views on the need of advanced analytical techniques for CD metrology, in-line defect inspection and contamination control. These tasks are essential for process control, yield improvement and the necessary product reliability.

Advanced lithography processes and such resulting devices as downsized traditional planar transistors or 3D FinFET structures require complex structure information, i.e., CD measurements that provide line shape and sidewall angle simultaneously. In addition, new high-resolution analysis techniques are needed to characterize high-κ metal gate stacks and strained silicon channels. For metal/low-κ interconnect stacks, the characterization of locally modified dense and porous dielectric material with high spatial resolution is one of the major challenges. As mentioned by Alain Diebold, R&D is needed to be prepared for process control of carbon-based materials like diamond-like carbon, fullerene-based thin films, graphene and carbon nanotubes in the long-term range.

In-line defect detection at high capture rates and contamination control are essential topics that need intensive development efforts for future technology nodes. In addition, the detection of small nonvisual defects and process variations will require new approaches and advanced analytical techniques. One promising, very sensitive technique for fast in-line detection of nonvisual defects and inhomogeneously distributed contaminations will be surface potential spectroscopy.

Both these papers demonstrate that manufacturing at extraordinary scales, new thin film materials and new device structures will require advanced analytical techniques and respective data analysis procedures for metrology, contamination control as well as defect inspection and review. These tasks drive the need to improve the efficiency of existing analytical methods as well as to explore and to implement additional analytical techniques for next-generation technology nodes. I trust you will be stimulated by these papers to reflect on your metrology and yield enhancement strategies for future IC fabrication.

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Advanced Material Solutions From Entegris

Using the ITRS as a guide, suppliers such as Entegris develop specific technology roadmaps to ensure the indirect materials used in semiconductor processes effectively support future technology nodes. The result is a technology roadmap that establishes drivers and requirements that help define the development of consumables and other components.

At the highest level of the ITRS is the establishment of device technology by design guidelines and year. For the indirect material supplier, establishing material drivers that will be required for consumable parts in equipment and fabs is a critical step to meet the overall device design rules. Examples of these requirements are size and the number of particulates measured in the chamber, useful product lifetime, flow rates and pressure drops in process liquids, gases and air. Each of these requirements lead the material supplier in a direction of material development with these specific goals in mind.

Entegris has implemented an advanced materials science strategy to enable future technology development through the introduction of high-purity, low-erosion graphite, dense silicon carbide for plasma etch, carbon-nanotube enhanced polymers, high-purity uniform silicon and carbon-based coatings to increase yields and equipment utilization, nanoscale filters and environmental chambers to protect reticles and next-generation devices. Entegris has aligned its applied development projects to meet the challenges of the semiconductor industry and provide solutions for current and future technology nodes.

ITRS CHAPTER: Yield Enhancement

Lothar Pfitzner
Fraunhofer IISB

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The Yield Enhancement chapter of the International Technology Roadmap for Semiconductors defines the difficult challenges in the short-term (≥22 nm) and long-term (<22 nm) range, with information on defect budgets needed to obtain acceptable yields on semiconductor devices. What a huge number of possible yield distracting events we have to deal with, even though the chapter limits its focus on front end processing is depicted in Figure 1, where major contributions to yield reduction are shown. To achieve high early yields and fast yield ramps, aggressive yield enhancement strategies must be developed. It is a significant challenge to adopt the yield enhancement strategies into all future nodes, where yield learning and yield improvement again start, to some extent, from scratch.

The key challenges of yield enhancement were adapted to the latest developments and challenges recognized by the 2008 Yield Enhancement International Technical Working Group. The most important one will be the detection of multiple killer defects and the signal-to-noise ratio. It is a challenge to detect multiple killer defects and to differentiate them simultaneously at high capture rates, at low cost of ownership and at high throughput. Furthermore, it is a substantial difficulty to identify small, but yield-relevant defects under a vast amount of nuisance and false defects. As a new challenge, however with some lower priority, the requirement for 3D inspection was identified. This necessitates inspection tools with the capability to inspect high aspect ratios but also to detect nonvisuals such as voids, embedded defects and subsurface defects. In general, the demand for high-speed and cost-effective inspection tools remains, and the need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases. E-beam inspection seems not to be the solution for all those tasks anymore.

Other topics challenging the Yield Enhancement community are prioritized as follows in the near term:

- **Process Stability versus Absolute Contamination Level:** Including the Correlation to Yield Test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield data. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.

- **Wafer Edge and Bevel Monitoring and Contamination Control:** Defects and process problems around wafer edge and wafer bevel are identified as causing yield problems. Currently, the monitoring and contamination control methods require intensive development.

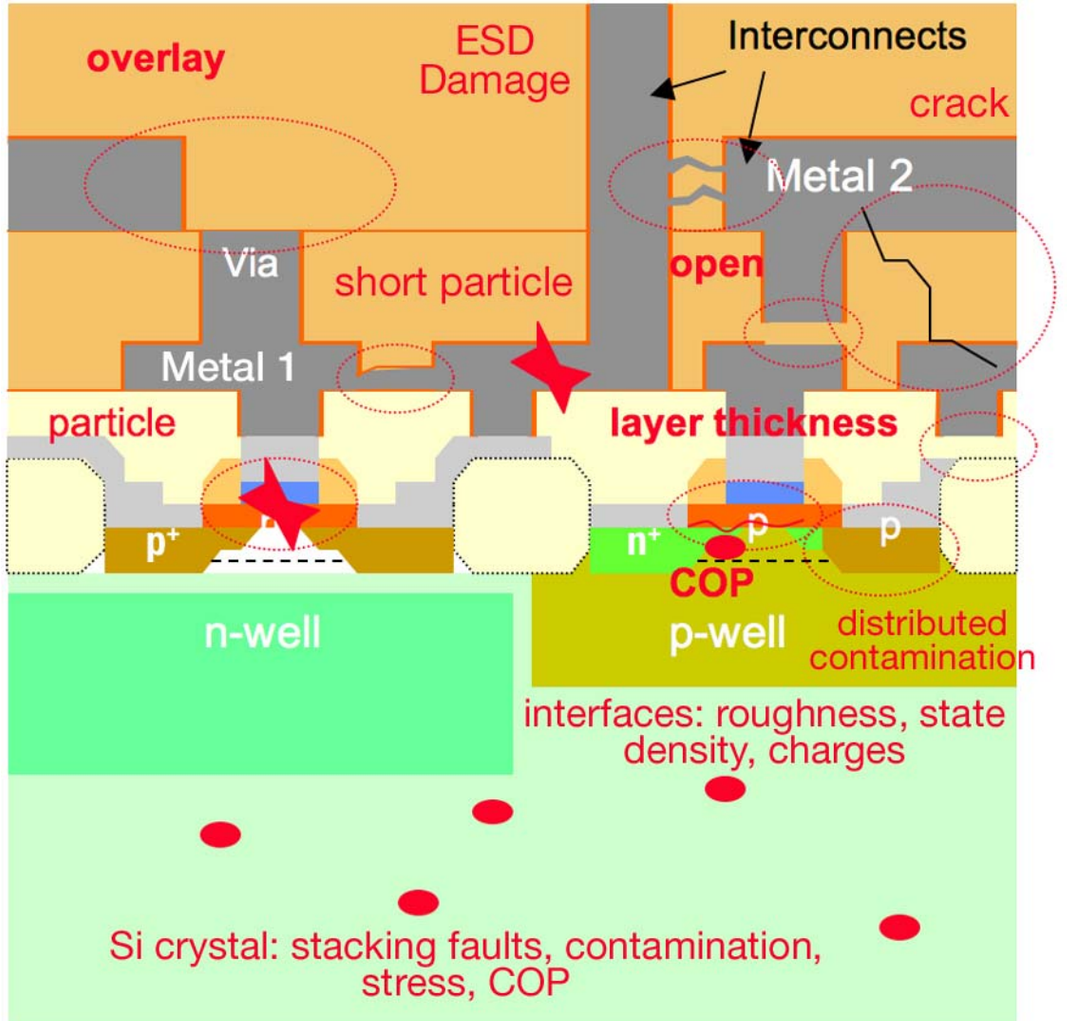

Figure 1. Schematic of Some of the Yield Distracting Faults, Contamination and Technology Problems

In the long term, the following key challenges are currently identified:

- **Nonvisual Defects and Process Variations:** Increasing yield loss due to nonvisual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them extremely sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.

Increasing yield loss due to nonvisual defects and process variations requires new approaches in methodologies, diagnostics and control.

- **In-line Defect Characterization and Analysis:** Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding new methods for data interpretation and ensuring quality.
- **Development of model-based design manufacturing interface:** Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultrathin film integrity, impact of circuit design, and greater transistor packing, to name just a few.

Regarding the structure, the Yield Enhancement chapter consists of three subchapters: *Defect Budget and Yield Model, Defect Detection and Characterization* and *Wafer Environment and Contamination Control*. The major activity during 2008 was the control and update of the tables provided by these subchapters. The changes are summarized as follows:

- ***Defect Budget and Yield Model:*** This update includes the recalculation of the defect budgets based on the values for the current technology generation's critical dimensions to maintain compatibility with ORTC. The changes result from important updates of DRAM chip size and the change of the scaling trends. Up to now, the transfer to "Flash" as a technology driver was not performed. The ITWG requires a solution to access updated particle-per-wafer pass data or particle control limits to supply data on defects, and data on tolerable particle-per-wafer pass (PWP) to equipment suppliers and integrated device manufacturers. For the long-term challenge, for the development of model-based design manufacturing interface (design for manufacturability, DFM), the following issues must be discussed in the near future: 1) The majority of models should be operated at the design stage; for example, Optical Proximity Correction, Well Proximity, Stress Proximity and CMP must be treated that way. 2) The amount of available models seems to be rapidly increasing – not just the accuracy of models, but also the opti-

mization of the trade-off between those models might be requested.

- ***Defect Detection and Characterization:*** The corresponding tables in the Yield Enhancement Chapter were checked carefully against the latest developments for defect inspection and detection. The subchapter was aligned with the latest requirements from the discussions with the *Lithography* and *Front End Processes* ITWGs. The conversion of the tables to "Flash" requirements that was finalized as "Flash" now involves the most advanced technology and therefore qualifies as the most aggressive driver for inspection and review equipment specifications. In one table, specifications for edge line measurement were added. The other table was extended for the required specifications for SEM and optical review following bevel and edge inspection. This change especially emphasizes the importance of yield impact and the requirement for root cause analysis of bevel- and edge-related/caused defects.
- ***Wafer Environment and Contamination Control:*** Discussions with the Interconnect and Front End Processes ITWGs resulted in the identification of selected FEOL and BEOL thin film chemical precursors that are currently used in high-volume manufacturing processes. Several of these precursors were included in an update of the table, along with a first identification of critical quality parameters to support high-yield manufacturing. The UPW (Ultra Pure Water) section of the table summarizing data on Wafer Environment and Contamination Control highlights the inability of particle metrology in UPW to support the targets established by the Front End Processes defect targets. Further work is needed to understand the particle deposition from UPW and to specify organics in UPW. Significant progress in the understanding of metal deposition from UPW will be incorporated into the table in the 2009 revision. In the AMC (Airborne Molecular Contamination) section, specifications for metrology environments have been added. The chemical section has continued providing guidance to understand the impact of organic contaminants. A concept for *AMC Integration and a Total AMC Concept* is under development.

Summarizing the progress in the Yield Enhancement chapter, the tables offer an updated set of data, key challenges were identified and measures to improve the 2009 revision activities were taken.

Contributors to the Yield Enhancement Chapter:

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Lothar Pfitzner holds an M.S. (Dipl.-Ing.) degree in materials science and a Ph.D. (Dr.-Ing.) in electronics engineering, both from the University of Erlangen-Nuremberg, Germany. Since 1985, he has been heading the Semiconductor Equipment and Manufacturing Methods department of the Fraunhofer Institute of Integrated Systems and Device Technology (IISB) in Erlangen, performing research and development in the field of Advanced Equipment Control and Advanced Process Control. Since 2004, he has also been leading the Yield Enhancement Interna-tional Technical Working Group of the ITRS. ■

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ITRS CHAPTER: Metrology

Alain Diebold,[1] Stephen Knight[2]
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The metrology community continues to be challenged by the acceleration of new materials and processes. These challenges are compounded by shrinking feature size and new device structures such as FinFETs. In 2008, the Metrology Technical Working Group concentrated on metrology for advanced lithography processes and metrology for front end processes. Double patterning, space double patterning and double exposure create additional measurement requirements that continue to be the topic of research and roadmap review. In this article, we cover both the 2008 updates and review the general needs for all areas of metrology. Especially important is the area of Beyond CMOS metrology. The Metrology TWG expects an expanded interest in metrology for 3D interconnect in 2009. The 2008 summer meeting provided a forum that emphasized the emerging materials, devices, processes, and metrology for Beyond CMOS.

Advanced Lithography Metrology

In 2007, the Metrology Roadmap started evaluating CD metrology in terms of measurement uncertainty instead of precision. Although the ITRS always considered tool matching (e.g., determining if the CD-SEMs used for measuring gate level give the same answer), measurement uncertainty includes all forms of uncertainty, including accuracy. When tool matching is included, CD measurement capability does not meet the uncertainty requirements for isolated gates for logic for 45nm 1/2 pitch. There are known solutions for the 45nm 1/2 pitch for dense lines. Overlay metrology also requires improvement for single layer processes. All of this assumes that one is measuring traditional transistors, essentially planar structures. However, newer, more three-dimensional structures such as the fin of a FinFET mean that CD must be measured on the sidewall of a fin structure.

In 2007, the Metrology Roadmap started evaluating CD metrology in terms of measurement uncertainty instead of precision.

This issue has not received the necessary research and development activity.

Advanced lithography processes being developed to extend immersion DUV lithography below the 45nm 1/2 pitch received the majority of the Metrology TWG's attention in 2008. Several TWG members are diligently working to provide metrology for spacer double patterning processes. In Figure 1, we show three advanced lithography processes: double exposure, double patterning and spacer double patterning. The general metrology needs for advanced lithography are discussed in Table 1. The biggest issue for CD metrology is that all forms of double patterning result in two distributions of CD, line shape, and sidewall angle. Scatterometry or optical CD requires a library of ellipsometric (or in some cases, polarized reflectometry) responses to the features in the grating test structure. The two sets of CD are a significant challenge to CD measurement. Scatterometry provides an average sidewall angle from the 2D line shape. Another issue is whether or not CD-SEM or scatterometry can achieve the uncertainty requirements for sidewall angle.

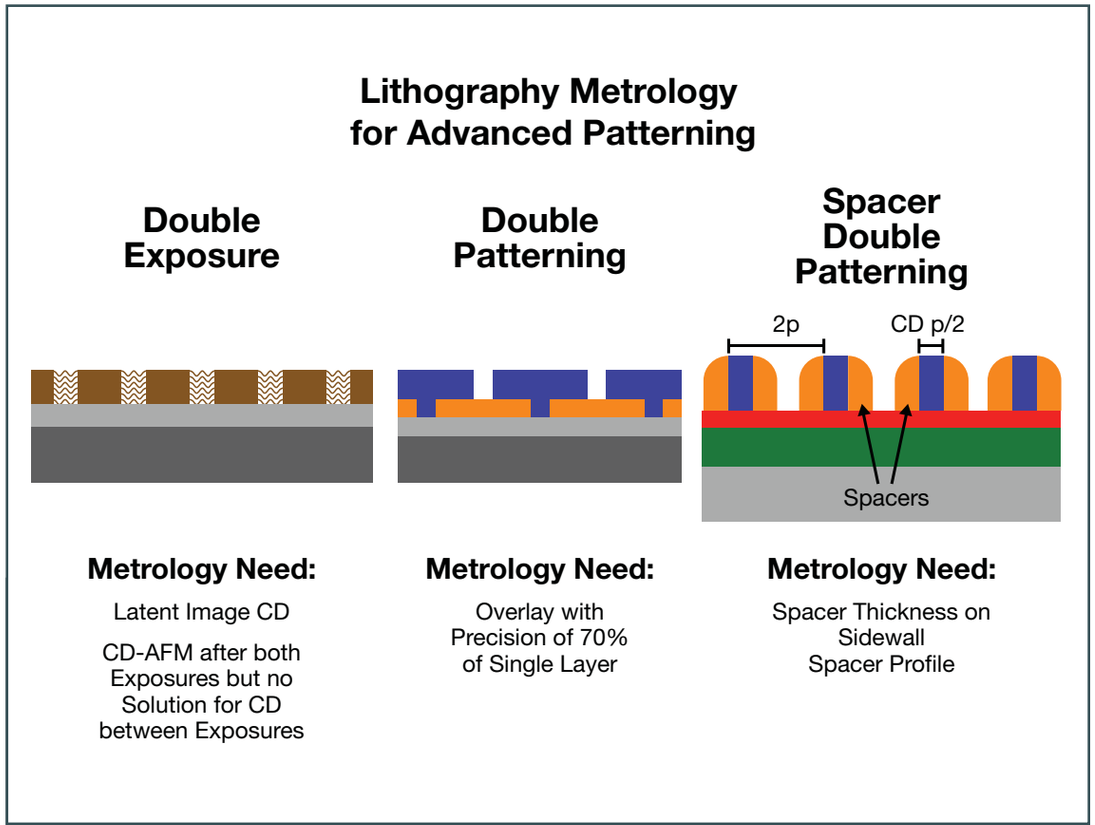

Figure 1. The Metrology Needs for Advanced Lithography Processes

Front End Processes

There is a notable diversity in transistor technology. There are many different processes for increasing carrier mobility. Although transistors based on high-k and metal gate materials are being manufactured, most of the industry is working to introduce these materials. In addition, 2008 activities included a review of the introduction of new substrate materials such as fully depleted SOI (ultrathin SOI). The next generation of transistors will again use a diverse set of materials. During 2008, the Metrology TWG worked with FEP TWG to understand the timing of new FEP materials and processes. R&D for high-k metrology continues to be of great interest to the semiconductor industry.

Double Exposure	Double Patterning	Spacer Double Patterning
32/22nm 1/2 Pitch		
For alignment, need to measure latent image in 1st exposure	Sidewall Angle (SWA) and Height Accuracy for odd and even lines	Spacer Sidewall Thickness Uniformity across entire field
2 populations of CD, SWA, height and pitch		
More unknown requirements?	How trapezoidal is profile of pattern for each of the patterns?	
	Overlay at resolution (i.e., with targets at device size): what is overlay at target vs. at device level?	SWA of odd and even lines
	Phase Shift Mask: influence of CD on overlay (feature-level mask metrology)	Need 3D line shape
Mask image placement metrology	Mask image placement metrology	Spacer thickness uniformity of final layer
	Mask CD uniformity metrology	Mask CD uniformity metrology

Table 1. Metrology TWG evaluation of metrology requirements for advanced patterning. The coloration matches the ITRS; thus, with further development, most measurement needs can be met.

During 2007, members of the Metrology TWG proposed new measurement requirements for stress in the lab and in the fab. Most measurement methods were laboratory-based and required long analysis times. In 2008, the limits of each measurement method were discussed along with some proposed new methods. The challenges for stress metrology include measurement spot size and the problems associated with measuring the stress of a buried layer in the 3D transistor. Most methods work well when applied to an unpatterned wafer. In addition, sample preparation for TEM may result in a measurement that does not reflect lattice strain found in the full 3D transistor structure. Multi-technique comparisons are a critical means of understanding the benefits and limitations of each method.

Interconnect Metrology

Over the past several years, the Interconnect TWG has reported on the variety of low-k materials used in IC manufacture. With the introduction of air gap low k, changes in low-k metrology center around the introduction of new materials. Porosity measurement is again becoming a hot topic. A complete description of metrology for 3D interconnect is difficult to assemble due to great diversity of approaches to 3D. Measurement of wafer bonding and alignment as well as the quality of through silicon vias and the metal fill are all critical metrology needs. The high aspect ratios and opaque materials all require methods not typically used in wafer metrology. IR microscopy and acoustic microscopy both allow imaging through silicon.

Metrology for Beyond CMOS

The approaching needs for metrology for Beyond CMOS resulted in increasing interactions between the Metrology TWG and the Emerging Research Materials and Emerging Research Devices TWGs in 2007 and this year. The interest in graphene provides a useful topic for discussion of Beyond CMOS metrology. Graphene is a so-called soft material, which means that it is easily damaged by electron microscopy. Joe Stroscio and colleagues at NIST have used STM to image graphene layers on SiC, including defects below the layer. Raman spectroscopy can detect the difference between single and multilayer graphene. Solutions to this issue include operating transmission electron microscopes at voltages well below 100 keV instead of at 200 or 300 keV. The spatial resolution is greatly reduced, even for the aberration-corrected microscopes. We emphasize the important link to multi-slice image simulations. The necessary operational conditions for imaging defects and other structure in graphene aid experimental work and provide correct image interpretation. One key challenge is imaging multilayer graphene.

Porosity measurement is again becoming a hot topic. A complete description of metrology for 3D interconnect is difficult to assemble due to great diversity of approaches to 3D.

Microscopy must become more capable of observing phenomena such as spin. Methods such as ballistic electron emission microscopy (BEEM) and scanning electron microscopy with polarization analysis (SEMPA) have already imaged different spin states in Beyond CMOS materials.

Nanoscale dimensions impact all areas of metrology. One example of how quantum effects change routine metrology is ultrathin SOI and small diameter nanowires. From the practical point of view, the optical constants (dielectric function) used to measure thin single crystal films of silicon change, meaning that metrology requires new optical constants for these thin films. The error in film thickness metrology increases as film thickness decreases. After carefully ruling out film stress, one finds that quantum confinement shifts the E_1 critical point. Light is strongly absorbed by silicon at photon energies around the E_1 critical point. It is important to note that the E_1 critical point has a strong excitonic character, while the E_2 critical point, which does not have strong excitonic character, does not shift. Calculation of the band structure of silicon nanowires requires inclusion of excitonic effects. Understanding device properties as well as optical and electrical measurements requires calculation of the band structure.

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The 2008 International ITRS Metrology TWG included:

Soobok Chin, Hyun Mo Cho, Alain Diebold, Thomas Hingst, Kazuhiro Honda, Masahiko Ikeno, Eiichi Kawamura, Chul Hong Kim, Steve Knight, Bart Rijpers, Yuichiro Yamazaki

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John Allgair, Chas Archie, Bill Banke, Meredith Beebe, Ben Bunday, Soobok Chin, Hyun Mo Cho, Alain Diebold, Mike Garner, Dan Herr, Thomas Hingst, Richard Hockett, Kazuhiro Honda, Masakazu Ichikawa, Masahiko Ikeno, Eiichi Kawamura, Chul Hong Kim, Steve Knight, Mario Kobrinsky, Isao Kojima, Sumio Kuwabara, Jack Martinez, Fumio Mizuno, Kazuo Nishihagi, Akira Okamoto, George Orji, Ingrid Peterson, Noel Poduje, Bart Rijpers, J.H. Shieh, Vladimir Ukraintsev, Brad Van Eck, Victor Vartanian, Andras Vladar, Yuichiro Yamazaki

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See bio on page 10.

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Steve Greathouse
Global Process Owner, Microelectronics;
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This issue of Future Fab is focused on the ITRS programs, directions and scope.

The International Technology Roadmap for Semiconductors, known throughout the world as the ITRS, has a 15-year history of forecasting the semiconductor industry's future technology requirements. These future needs drive present-day strategies for worldwide research and development among manufacturers' research facilities, universities and national labs.

For anyone who might have attended the ITRS yearly meeting that was co-located with SEMICON in San Francisco in July, it was evident from the first presentation that the themes of the 2008 ITRS programs were centered around the phrase "More than Moore." There were several discussions on how much further CMOS products can be pushed before they hit their physical limit.

While a majority of silicon-based technologies do follow Moore's law, there are many silicon products that do not. Some examples are Sensor/Actuators, RF, MEMS, Power/HV, Passive, Bio-chip/bio-systems, System in a Package (SIP), solid-state (LED) lighting, micro-fluidics, nanotechnologies and several others.

Many nonsilicon-based products will also benefit from the "More than Moore" advances because of techniques and materials being put in place to support this treadmill. These include micro-miniaturization technologies for mechanical devices, self-assembly techniques and handheld products.

In this Assembly, Test & Packaging Technologies section of Future Fab, there are two articles that discuss the ITRS focus areas: The article by W. R. Bottoms and W. T. Chen, covering the Assembly & Packaging chapter, outlines many of the packaging technologies in production and discusses those being planned for future products. These include wire bonded, flip chip and through-via stackable products. Wafer-level package, SiP and nanotechnologies are also discussed.

The article by Roger Barth of Numonyx, Inc., covering the Test & Test Equipment chapter, outlines many of the device and manufacturing trends encountered in the test world. He introduces many of the items that will be revamped in the 2009 roadmaps to keep Test up with the "More than Moore" requirements.

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ITRS CHAPTER: Test & Test Equipment

Roger Barth
Numonyx, Inc.

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Introduction

Test is the process used to validate the specifications of an integrated circuit so that there is high confidence of operation in the final application. Depending on the specific IC design and health of the process technology, on average, 60 to 95 percent of the die on the wafer will be good. The remaining devices are bad and must be separated out during the manufacturing process. The intent of the Test and Test Equipment ITRS 15-year roadmap is to align integrated circuit equipment suppliers, chip designers and chip test manufacturers on test requirements.

Background

The first ITRS test roadmap was published in 1999, but was preceded by Semiconductor Industry Association (SIA) test roadmaps in 1994 and 1997. The early SIA roadmaps focused on logic test and the use of Built in Self Test (BIST) and Design for Test (DFT) to achieve low cost of test. The 1999 ITRS roadmap added mixed signal devices, microcontrollers, and discrete and embedded roadmaps for DRAM and Flash. Since that first ITRS roadmap, sections have been added for mechanical handling and contacting of packaged units and wafers, device reliability screening and burn-in, test for System on Chip (SoC) and System in Package (SiP), cost of test considerations, RF and analog device test. Information has also been included for specialized devices such as LCD display drivers and imaging devices that are produced in very high volumes and contained in many mobile communication and computing devices. The ITRS test roadmap has grown from 28 pages with nine tables in 1999, to 63 pages with 15 tables in 2008, but despite the size increase, every effort has been made to keep the chapter both a source of information and an easily understood tutorial for new readers. There are approximately 40 contributors to the roadmap in any given year, but during the last 10 years, more than 100 contributors from Europe, Asia and the Americas have enabled the roadmap to take the form it has today.

The ITRS test roadmap has grown from 28 pages with nine tables in 1999, to 63 pages with 15 tables in 2008.

The Test Technology Working Group (TWG) maintains close alignment to the Systems, Design, Assembly and Packaging, Interconnect and Wireless chapter TWGs.

Drivers

Device and manufacturing trends drive changes in the test roadmap. Device technology trends are primarily smaller transistor sizes, new circuit designs that have increased performance, smaller package form factors and reduced operating power. Manufacturing trends are driven by the need to continuously reduce cost.

Key Device Trends

- *Device interface bandwidth and clock speed increases* are driven by technology scaling and the consumer need for higher device performance with lower power and a smaller form factor. By 2022, the typical MPU chip will have 10 billion transistors and a clock speed of 14 GHz.
- *Increased integration* as seen in SoC and SiP devices for consumer and mobile applications. Integrating the controller, memory, signal processor and I/O in a single die or in a single package results in a smaller form factor.
- *Integration of nondigital and digital on the same silicon.* (Why have a bunch of wires when they can be eliminated via wireless communication such as Bluetooth, Wi-Fi, cell phone, etc.?)
- *Package form factors that will be smaller, thinner and lighter* in the future than they are today. A package need not be much larger in all dimensions than the silicon area for the device. Smaller packages stimulate new development in mechanical handling.

Manufacturing Trends

- *Device customization during the test process* allows use of a single silicon design to satisfy multiple customer requirements by loading operational code or enabling permanent configuration of options.
- *Distribution of the test flow over multiple manufacturing test steps* may lower the overall cost of testing a product, but will increase production complexity. A single tester that can test every function of every product during a singe test insertion may be convenient, but is much more costly than using testers that are specialized and allow high utilization of all tester resources.
- *Dynamic flows that allow real-time modification* of the test flow based upon yield or previous pass/fail on devices in the same lot can reduce overall test cost.
- *Feedback to manufacturing* is inherently important to drive lower manufacturing cost. An electrical fail signature can be analyzed to adjust the manufacturing process to obtain greater yield.

Difficult Challenges are constraints that must be considered when developing a new product design and test plan. These include:

- *Cost of test* must follow Moore's Law, which states that the cost of an integrated circuit will decrease on a regular basis. Per transistor, test cost must also continue to decline at the same rate as the cost of making a transistor.
- *Increased yield through yield learning* is required to decrease overall cost of

existing products and provide specific feedback for manufacturing process adjustments and design changes to eliminate or reduce specific faults or failure modes.

- *Detecting systemic defects* is becoming more difficult as lithography line widths continue to shrink and the number of mask layers continues to increase. Electrical test fail signatures, along with data mining, are vital to identifying yield-limiting structures.
- *Screening for reliability* is for detection of potential product field failures before the product leaves the manufacturing line. Elimination of field failures can result in higher customer satisfaction and lower product cost.

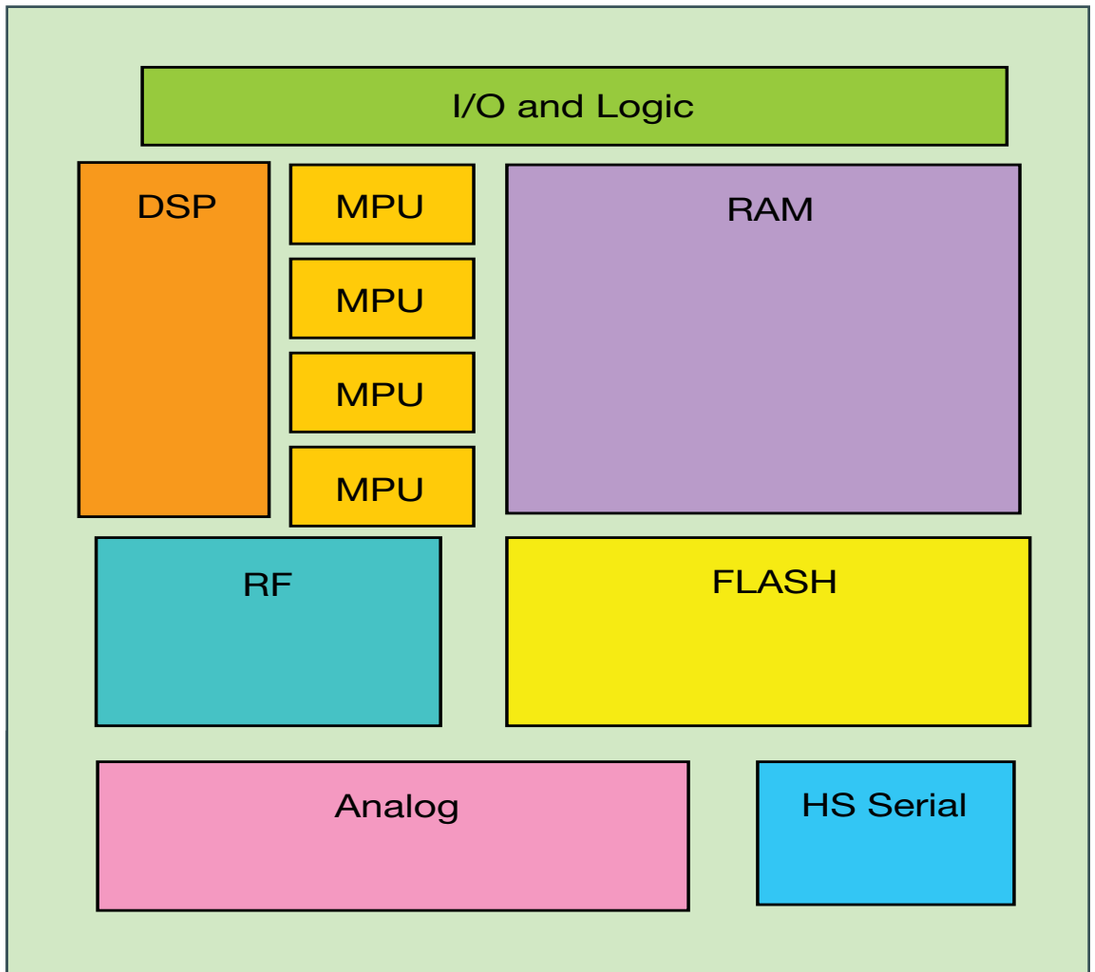

Figure 1. Typical SoC With Multiple Cores

Key Test Chapter Sections

The test chapter is broken into a number of independent sections based upon test focus areas. This arrangement allows readers to focus on a specific area of interest. The sections are:

- *Test parallelism* is dependent on the type of device being tested and is a careful balance of cost and capability to perform testing. Full wafer test and high-parallelism packaged test is becoming standard on many memory devices, but microprocessors, SoC, and mixed signal devices see limits on test parallelism due to device power, tester function complexity or measurement capability.
- *The Mixed Signal* devices section contains test issues, device bandwidth, noise and jitter requirements for analog signal digitizers and generators.
- *Burn-in* covers the power and frequency requirements to screen reliability failures for high-performance microprocessor and mixed signal devices under both wafer-level and unit-level test burn-in conditions.
- *Probing of wafers and handling of packaged die* face challenges due to decreasing size and pitch for die pads and package balls or leads and an increase in the number of pads and balls or leads over time. Key challenges for mechanical handling are defined in the hander, prober, probecards and contactor sections and tables.

Full wafer test and high-parallelism packaged test is becoming standard on many memory devices.

- *SoC* devices contain multiple logic, memory, mixed signal, etc., design cores, each of which drives specific DFT features in order to control overall test cost (Figure 1). SoC devices are generally much more complex to test than individual cores because each of the cores may have its own unique DFT scheme.
- *MPU and consumer Logic* devices are similar but vary in the number and types of cores and challenges for test. Test data volume is dependent on the number and types of unique cores or core-type structures and is a key driver of test cost.
- *Memory* encompasses DRAM, NAND and NOR Flash and SRAM both for discrete and embedded applications. Input/output (I/O) performance, data retention properties and device read/write latency are key distinctions between the various memory families.

2009 Directions

While only minor table modifications were made in 2008, the 2009 roadmap will include some major revisions. DFT sections in both the Test and Design chapters will be updated, aligned and partitioned between the two chapters such that the Test chapter will include the requirements for low-cost test, and the Design chapter states the implementation methodology. The DFT roadmap section has not undergone a major revision since 2003. Gigahertz interface DFT advancements will also be reflected. Adaptive test methods to reduce overall test cost will get increased focus.

The ITRS roadmap has been evolving from traditional CMOS device types to the

"More than Moore" device concept that can encompass CMOS and non-CMOS technologies. SiP devices present testing challenges that must be solved as SiP-driven solutions are a leading indicator of where "More than Moore" will drive the industry over the next decade. The extreme case of SiP is a 3D silicon structure where multiple die are designed to replace a single large and complex die, and then the "multiple die" are mounted on top of each other during the assembly process. 3D device structures will require many vias to connect signals between the die, so an effective test partitioning strategy is needed.

A change in the roadmap of one team has a ripple effect to other teams, which results in a continuous evolution of future direction and challenges.

Final Words

Test is only one of 16 ITRS focus area roadmap teams. A change in the roadmap of one team has a ripple effect to other teams, which results in a continuous evolution of future direction and challenges. Resolution of the challenges outlined in the various chapters does not eliminate the need for the roadmap, as each successful elimination of a barrier provides opportunity to identify new challenges that will need to be added to the roadmap and resolved.

Test Chapter Contributors

Rob Aitken, Ken-ichi Anzou, Dave Armstrong, Davide Appello, Roger Barth, Mike Bienek, Phil Burlison, Yi Cai, Mouli Chandramouli, Wendy Chen, Calvin Cheung, Steve Comen, Dennis Conti, Jack Courtney, Koichi Eguchi, Shawn Fetterolf, Yasuo Fujii, Anne Gattiker, Atul Goel, Kazumi Hatayama, Hisao Horibe, Hisao Horibe, Koji Isodono, Shuichi Ito, Sridhar Kannan, Takuya Kobayashi, Akitoshi Kumada, Amit Majumdar, Prasad Mantri, Peter Maxwell, Jerry McBride, Peter Muhmenthaler, Phil Nigh, Yasumasa Nishimura, Sejang Oh, Mike Peng Li, Bill Price, Brad Robbins, Paul Roddy, Mike Rodgers, Yasuo Sato, Ulrich Schoettmer, Rene Segers, Tetsuo Tada, Wataru Uchida, Jody Van Horn, Erik Volkerink, Tom Williams, Koorosh Zaerpoor, Yervant Zorian

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ITRS CHAPTER: Assembly & Packaging

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The electronics industry is nearing the limits of traditional CMOS scaling. Predictions that Moore's Law has reached its limits have been heard for years and have proven to be premature. However, we are now nearing the basic physical limits to CMOS scaling and the price-elastic growth of the industry can no longer continue based on Moore's Law scaling alone. New materials and new device architectures are in development that will eventually provide a path to increased density, increased performance and lower cost beyond the capability of CMOS-based circuits. There will, however, be a time gap between the slowing of traditional CMOS scaling and the introduction of a new generation of device architectures and electronic materials that can support the continued drop in cost per function associated with Moore's Law. Assembly and Packaging innovations are driving dual technology trends in the industry:

- Equivalent scaling through functional diversification
- Density increase through 3D packaging

This industry technology landscape is well-described by the phrases "More Moore" and "More than Moore." They are discussed in detail in the ITRS Assembly & Packaging chapter to be found on the ITRS website.

This functional diversification, often referred to as "More than Moore," is accomplished through integration of multiple circuit types using System on Chip (SoC) and System in Package (SiP) technology. The most important of these, as the electronics industry becomes ever more dominated by the consumer, will be System in Package. SiP technology enables the efficient use of three dimensions through innovation in packaging and interconnect technology. The result will support continued increase in functional density and decrease in cost per function as we begin to reach the limit of current technology.

The Assembly & Packaging technology base builds from the state of the art in single chip packaging, with its advanced wirebond and flip chip processes. This base has been expanding with a proliferation of new package innovations and new package types driven by the demands of the consumer-dominated marketplace. Emerging technologies combined with this base include wafer-level packaging, die stacking, package stacking, through silicon vias (TSV), 3D packaging, printable circuits, thinned wafers and both active and passive embedded devices. Combining these technologies into SiP devices provides a mechanism for cost-effective incorporation of functional diversification. This

technology enables the continued increase in functional density and decrease in cost per function required to maintain the growth of electronics markets.

SiP technology is rapidly evolving from specialty technology used in a narrow set of applications to a high-volume technology with wide-ranging impact on electronics markets. The broadest adoption of SiP to date has been for stacked memory/logic devices and small modules integrating mixed signal devices and passives components for mobile phone applications. Numerous concepts for 3D SiP packaging are now emerging, driven largely by the demands of portable consumer products. Figure 1 shows the major categories of SiP technology emerging as solutions to today's market requirements.

There are many advantages of SiP, and importance varies with different applications. They include:

- Small and custom form factors
- Decreased weight
- Reduced power consumption
- High-functional density
- High-frequency operation
- Large memory capacity
- High reliability
- Low package cost
- Low development cost compared to SoC
- Rapid time-to-market
- Wireless connectivity (GPS, Bluetooth, cellular, etc.)

SiP technologies enable integration of components and technologies from different areas. SiP technologies are becoming the primary architecture for high-value, system-level products for the all-important consumer arena. With the growth of the design and manufacturing infrastructure, the technology will proliferate into electronic products in all major markets. A white paper on System in Package has been published on the ITRS website. This white paper describes in depth the multi-faceted technologies and difficult challenges associated with SiP.

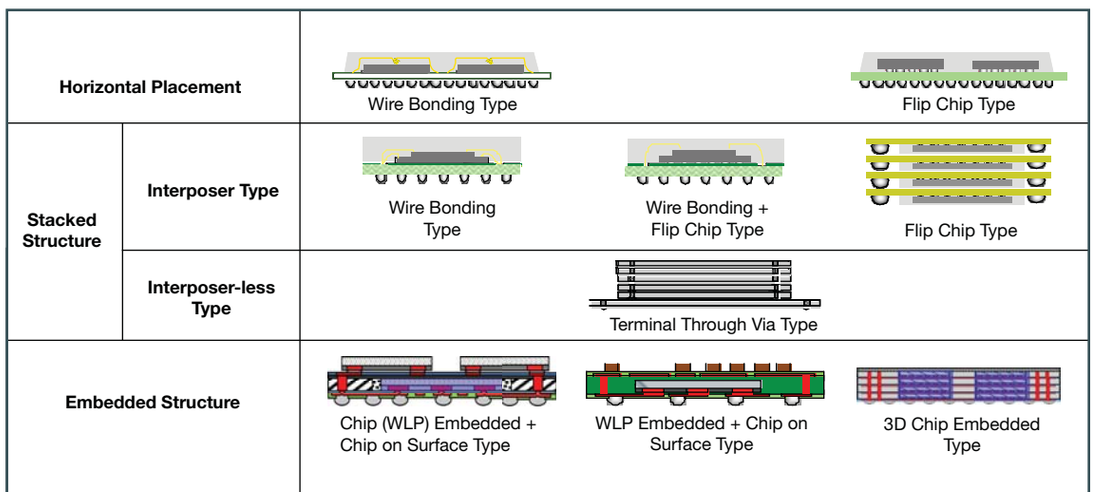

Figure 1. Innovation in SiP Architectures

Wafer-level packaging (WLP) is an emerging technology where all elements of a package are within the boundary of the die and all packaging processes are done before singulation of the wafer into individual circuits. The development of WLP is motivated by the recognition that wafer-level processing technology, i.e., parallel processing on the wafer, offers many advantages over traditional packaging. Wafer-level CSP (WLCSP) is the first generation of wafer-level packaging product introduced into the marketplace. This technology was originally based upon the established technology and manufacturing infrastructure of flip chip wafer bumping processes and equipment. WLPCSP technology with and without a redistribution layer (RDL) is used for a wide variety of products. They are mainly being used in portable consumer products where small size, thickness and weight are differentiators. The manufacturing technology and high-volume infrastructure has enabled widespread implementation of WLCSP in the marketplace today. Innovations in WLP address the need to increase performance and functionality while reducing size, power and cost of the system. This technology will provide significant cost reductions as it matures and production volume increases.

The combination of WLP and wafer/die stacking approaches leads to a large number of variations in WLP technology. The highest levels of integration are achieved through 3D packaging. Die stacking has been used for consumer products such as

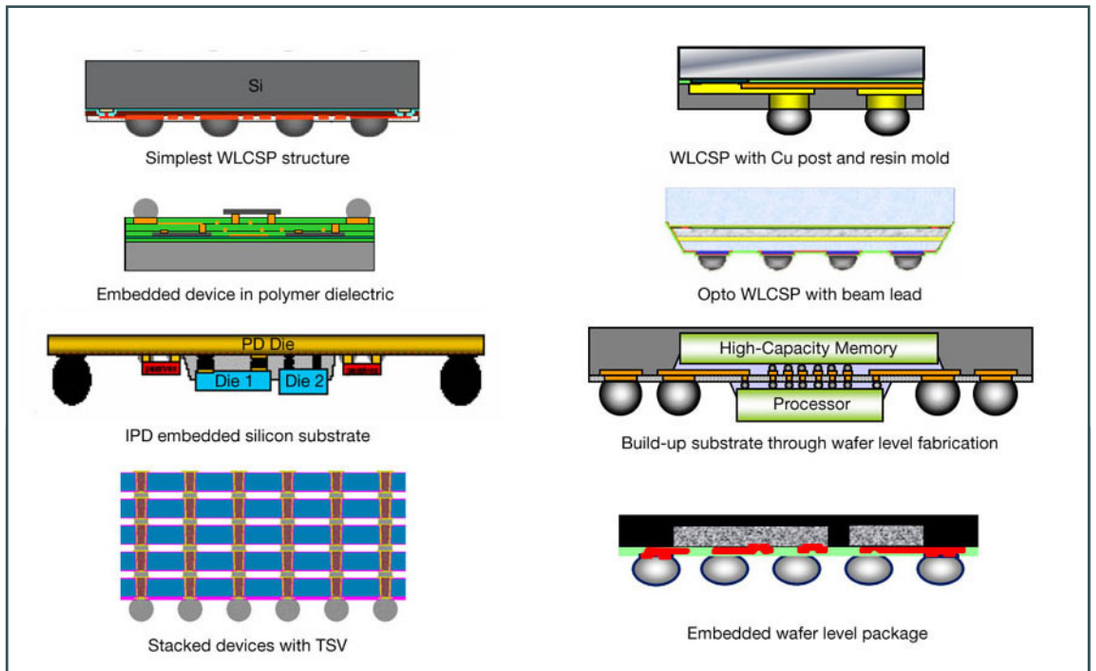

Figure 2. Examples of Wafer-Level Packaging Innovations

cell phones for several years with wire bonding used to connect the stacks to the package substrates. An important new technology is the use of through silicon vias (TSVs) to allow more-efficient die stacking and 3D integration. These developments lead to more-complex packages for both single and multi-die wafer-level packages, as shown in Figure 2.

Innovations in SiP and WLP technologies depend upon the integration of progress in materials and equipment made in all segments of the industry. The successful integration of all of these elements provides a rich portfolio of capabilities in the era of "More Moore" and "More than Moore." A schematic representation of the next-generation advanced SiP package is illustrated in Figure 3.

Some of the advanced packaging elements in this package include:

- Stacked die
- Wafer-level packaging
- Through silicon vias
- Embedded components
- Wafer thinning
- Wafer-to-wafer bonding
- Die-to-wafer bonding
- New materials

In this decade, most of the packaging materials have been changing due to regulatory RoHS requirements for green materials as well as needs for performance, form factor and function. They include bonding wire, solder systems, molding compounds, thermal interface materials, underfill materials, diebond adhesives and so on. In particular, the escalating cost of gold has spurred great motivation for copper wire to replace gold wire in wirebonded packages across the industry. Developments of new materials and new materials system include:

- Nanotubes
- Nano Wires
- Macromolecules
- Nano Particles
- Nano composite materials

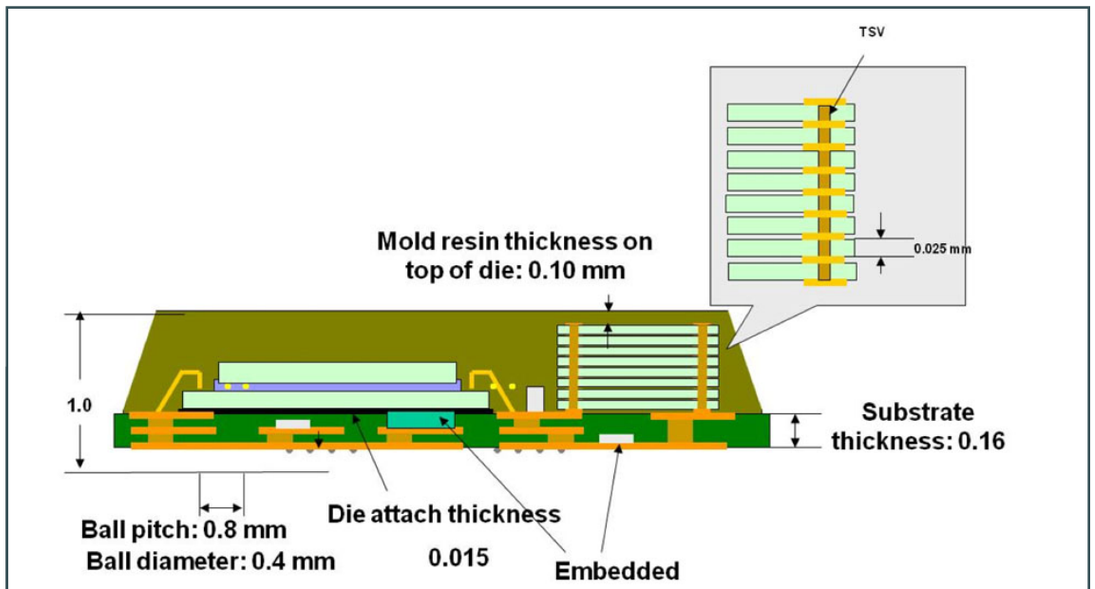

Figure 3. Example of Next-Generation SiPs

The ITRS Assembly & Packaging chapter addresses packaging technologies for specialized functions and applications including:

- Optoelectronics packaging
- RF and millimeter wave packaging
- Medical and bio chip packaging
- MEMS device packaging
- Electronics in textiles and wearable electronics
- Automotive electronics
- Solar cell packaging

Innovations in Assembly & Packaging have been accelerating as packaging becomes a major enabler for a large class of products in the consumer-driven marketplace. Many important issues remain that require continued development. In the ITRS Roadmap chapter, difficult challenges for the near-term time frame (>22nm) as well as the longer-term time frame have been described in some detail. The difficult challenges for the near term have been categorized below:

- Impact of BEOL including Cu/low κ
- Wafer-level CSP
- Co-design and simulation tools
- Embedded components
- Thinned die issues
- Gap between chip and package cost trend
- High-current density packages
- Flexibility requirements for packages
- 3D packaging

The packaging research landscape has been changing alongside the changing business models in the electronic industry. The System in Package white paper, mentioned earlier in this article, contains a listing of global research institutes and university research groups currently engaged in Assembly & Packaging research.

Acknowledgments

The ITRS Assembly & Packaging Roadmap was developed by 60 individuals from Europe, Asia and the United States who worked diligently through the year. We thank these members of the Assembly & Packaging Technical Working Group for their invaluable contributions to the ITRS 2008 Update and, for many of them, their leadership and guidance during several years of contribution to the ITRS Roadmap.

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W. T. Chen

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