# Future Fab

## INTERNATIONAL

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# Welcome to the latest issue of Future Fab ...

Before you delve into the virtual pages of our latest issue, we wanted to have a quick rant. Do you know what really annoys us here in the hallowed halls (ahem, office) of Mazik Media, the home of Future Fab? The fact that so many think that the semiconductor industry is yesterday's news, that it's done, dusted and no longer of interest. It's rare to hear, see or read about our amazing business outside of the handful of publishers that are left clinging to life in this industry. Mark Zuckerberg got a whole Hollywood *film* made about him and his face(book), and yet he and everyone else in the dot-com world owe their existence to the innovators of the "traitorous eight" of Shockley Labs fame, and if you don't know what we're talking about, shame on you!

Well, we're not going to take this laying down! What does this mean to you, our loyal readers? Well if you *really* want to know, send an email to iwanttoknowwhatyoureupto@mazikmedia.com and we'll add you to a list of insiders.

We have big plans that are going to move us onto a different stage, literally. Watch this space ... but in the meantime, enjoy edition 41 in this, our 16th proud year of existence!

Venimus, vidimus, venimus rabiem nos reflexae!

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# EDITORIAL PANEL

Biographies of Future Fab's Panel Members
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Welcome to our new Panel Member – Mark McClear

**Mark McClear**
**Global Director, Applications Engineering, Cree LED Components**

Mark McClear is responsible for LED lighting applications development and Cree's Application Engineering Technology centers worldwide. He holds a B.S. in electrical engineering from Michigan State University and an MBA from Babson College, and has 11 issued and published U.S. patents in electronics, LED and solid state lighting.

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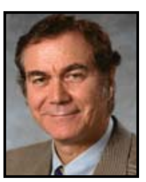

**Paolo A. Gargini**
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Dr. Paolo Gargini is also responsible for worldwide research activities conducted outside Intel for the Technology and Manufacturing Group by consortia, institutes and universities. He received doctorates in electrical engineering and physics from the Universita di Bologna, Italy.

**Michel Brillouët**
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Michel Brillouët joined CEA-Leti in 1999, where he managed the silicon R&D. Prior to joining CEA-Leti, he worked for 23 years in the Centre National des Télécommunications (France Telecom R&D Center), where he held different positions in micro-electronics research. He graduated from École Polytechnique.

**Alain E. Kaloyeros**
**Senior Vice President, CEO and Professor, College of Nanoscale Science and Engineering; University at Albany**

Alain E. Kaloyeros has authored/co-authored over 150 articles and contributed to eight books on nanoscience, holds 13 U.S. patents, and has won numerous academic awards. He received his Ph.D. in experimental condensed matter physics from the University of Illinois, Urbana-Champaign, in 1987.

**Gilbert J. Declerck**
**Executive Officer, imec; Member of the Board of Directors, imec International**

Gilbert J. Declerck received his Ph.D. in electrical engineering from the University of Leuven in 1972. He has authored/co-authored over 200 papers and conference contributions. In 1993, he was elected fellow of the IEEE. Since July 1, 2009, Dr. Declerck has been executive officer imec and a member of the board of directors of imec International.

**Didier Louis**
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### Rohan Akolkar
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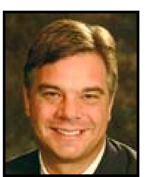
Dr. Akolkar received the Norman Hackerman Prize of the Electrochemical Society in 2004, and numerous Intel Logic Technology Development awards. He has authored more than 40 technical papers, invited talks, and U.S. patents in the area of electrodeposition.



### Thomas Sonderman
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Thomas Sonderman obtained a B.S. in chemical engineering from the Missouri University of Science and Technology in 1986 and an M.S. in electrical engineering from National Technological University in 1991. He is the author of 43 patents and has published numerous articles in the area of automated control and manufacturing technology.

### Christo Bojkov
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Alain's research focuses on the impact of nanoscale dimensions on the physical properties of materials. He also works in the area of nanoelectronics metrology. Alain is an AVS Fellow and a senior member of IEEE.

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Shishpal Rawat holds M.S. and Ph.D. degrees in computer science from Pennsylvania State University, University Park, and a B. Tech. degree in electrical engineering from the Indian Institute of Technology, Kanpur, India.

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Jon Candelaria has over 34 years' experience in the electronics industry in a wide variety of engineering and managerial roles. He received his BSEE and MSEE from the University of New Mexico.

### Yannick Le Tiec
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### Daniel J.C. Herr
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Dr. Herr is a pioneer in collaborative nanotechnology research. He is professor and chair of the Nanoscience Department at the new Joint School for Nanoscience and Nanoengineering in Greensboro, North Carolina. Until recently, Dr. Herr served as the director of Semiconductor Research Corporation's Nanomanufacturing Sciences area. He received his B.A. with honors in chemistry from Wesleyan University in 1976 and his Ph.D. from the University of California at Santa Cruz in 1984.

### Steve Greathouse
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Steve Greathouse has published many articles on technical topics related to semiconductor packaging, failure analysis and lead-free packaging. He has a B.S. in electronic physics from Weber State University with advanced studies in material science and computer science.

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Liam Madden is responsible for foundry technology, computer aided design and advanced package design. He earned a BE from the University College Dublin and an MEng from Cornell University. Madden holds five patents in the area of technology and circuit design.

### William T. Chen
**Senior Technical Advisor, ASE (U.S.) Inc.**

Bill Chen is the co-chair of the ITRS Assembly and Packaging International Technical Working Group. He was elected a Fellow of IEEE and a Fellow of ASME. He received his B.Sc. at University of London, MSc at Brown University and Ph.D. at Cornell University.

### Yayi Wei
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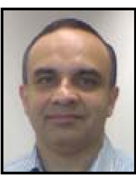
Dr. Wei investigates advanced lithography processes and materials. He has over 16 years of lithography experience, including DUV, 193 nm, 157 nm, 193 nm immersion, EUV and E-beam lithography. Dr. Wei has numerous publications and holds several patents in the field of lithography.



### Pushkar P. Apte
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Dr. Pushkar P. Apte's strategy consulting firm focuses on the high-tech industry. He received his master's and Ph.D. from Stanford University in materials science and electrical engineering, and his bachelor's degree in ceramic engineering from the Institute of Technology, Varanasi, India.

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The Berlin University of Technology is an institution for research and development in the areas of device simulation, technology, characterization and reliability. Christian Boit received a diploma in physics and a Ph.D. in electrical engineering on power devices, then joined Siemens AG's Research Laboratories for Semiconductor Electronics in Munich and has been a pioneer on photoemission.

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Dr. Edelstein played a leadership role in IBM's industry-first "Cu Chip" technology in 1997, in the introduction to manufacturing of Cu/Low-k insulation in 2004. He received his B.S., M.S., and Ph.D. degrees in applied physics from Cornell University.

### Sitaram R. Arkalgud
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Sitaram R. Arkalgud has over 20 years of R&D and manufacturing experience within the chip industry. He has a Ph.D. and a master's degree in materials engineering from Rensselaer Polytechnic Institute, and a B.S. in metallurgical engineering from Karnataka Regional Engineering College, Surathkal, India.

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Janice Golda manages an organization responsible for creating strategies and working with Intel's lithography, mask and metrology suppliers and subsuppliers to deliver equipment meeting Intel's roadmap technology, capacity and cost requirements. She is a member of the Berkeley CXRO Advisory committee, is Chairman of the Board for the EUV LLC and holds one U.S. patent.

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Warren Savage has spent his entire career in Silicon Valley, working with leading companies, where he focused on building a global scalable semiconductor IP business. In 2004, he founded, and still leads IPextreme in the mission of unlocking and monetizing captive intellectual property held within semiconductor companies and making it available to customers all over the world. He holds a B.S. in computer engineering from Santa Clara University and an MBA from Pepperdine University.

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# EDITORIAL PANEL

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Stephen Buffat is responsible for the startup and operation of Lockheed Martin's nanotechnology facility and operation in Springfield, Mo. He has authored or co-authored numerous articles on photolithography, etch and 300 mm surface preparation process technologies.

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After graduating in physics from the University of Milan, Davide Lodi started working in 1997 for STMicroelec-tronics as a process engineer. After becoming the manager of Wet Processes and Metrology Engineer-ing at the NVM R&D Agrate site, he moved to Numonyx, which was acquired by Micron in 2010.

**Peter Ramm**
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Peter Ramm received his physics and Dr. rer. nat. degrees from the University of Regensburg. He has authored or co-authored over 100 publications, including three book chapters and 23 patents.


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# FUTURE VISIONS & CURRENT CONCERNS

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**Alain E. Kaloyeros**
Senior Vice President, CEO and Professor
College of Nanoscale Science and Engineering; University at Albany

"The best way to predict the future," it has been said, "is to invent it." Such is the case with manufacturing, which relies on ongoing innovation to enable advancements in reliability, efficiency and cost.

Few sectors reflect this reality better than a technology-heavy industry like nanoelectronics. But how long can innovation alone, particularly as it has been manifested over the past 47 years in the form of Moore's Law, continue to support the fundamental economics that drive the continued pursuit of smaller and faster devices? In this context, most industry leaders would agree that lithography has provided many of the greatest challenges and rewarding solutions with respect to the technical viability and associated economics of continued device scaling in the sub-100 nm device era.

Parsing the economic and technical aspects of dimensional scaling of integrated circuits is an overarching theme in this edition's Future Visions & Current Concerns section.

From an economic perspective, imec's Phillip Christie carries out a refresher on the manufacturing model within Gordon Moore's "Moore's Law" paper from 1965. In his article, he makes a number of thought-provoking and compelling conclusions regarding the ultimate cost benefits of continued device scaling, especially as it relates to the concomitantly increasing costs of patterning as devices shrink.

Looking more directly at the processing and manufacturing aspects of scaling, AZ Electronic Materials' Geoff Wild offers a novel perspective on an alternative to conventional lithographic technologies. He echoes the issue of the exponentially increasing cost of lithography with time, and suggests that, if current trends continue, the cost-per-patterning toll by 2020 will be approaching half a billion dollars. This prohibitive capital cost will continue to marginalize all but the largest chip manufacturers, causing further erosion in market competition. Mr. Wild discusses directed self-assembly as a potentially cost-effective solution for nanoscale patterning that relies on the composition of applied block copolymers to precisely define surface structures.

*This introduction was co-authored by Alain E. Kaloyeros, Ph.D.; Eric T. Eisenbraun, Ph.D., CNSE associate professor of nanoscience; and Steve Janack, CNSE vice president for Marketing and Communications.*

FUTURE VISIONS & CURRENT CONCERNS

# Moore's Law, Madmen and Economists

**Phillip Christie**
imec

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The economist Kenneth Boulding is famously quoted as saying "Anyone who believes exponential growth can go on forever in a finite world is either a madman or an economist." So engineers who are neither obviously mad nor practitioners of the "dismal science" have learned to live with the surprising longevity of Moore's Law with what amounts to an intellectual shrug of the shoulders. This is highly rational behavior, since history has shown that predicting the end of Moore's Law is essentially not at all cool.

While accepting that scaling devices below the atomic scale is clearly going to be a challenge, there appear to be no insurmountable technological barriers to the continued health of Moore's Law in the medium term. However, Moore's Law is self-evidently not the driver of technological change but rather a consequence of a particular set of economic incentives that make it extremely profitable to continue to increase the number of components on a chip every couple of years. The purpose of this article is to identify these incentives and to speculate on what might happen if these incentives change and how the industry might evolve to accommodate them.

Moore's original 1965 paper[1] made two key assumptions. The first was that the cost per chip was nearly independent of the number of components[2] on the chip. In other words, the cost per component was nearly inversely proportional to the number of components.

This creates a powerful incentive for a chip company to drive down this complexity curve until, as stated by the second assumption, the smaller distance between components rapidly leads to decreased yields and this overwhelms the cost advantages of putting more components on a chip. This results in an optimum component count at minimum cost for a fixed technology. This is illustrated in Figure 1, which has been generated using the same manufacturing and defect models used in Moore's paper, and where the resulting optimum number of components per chip at minimum cost for a given technology node is indicated by a circle. This graph (which in its original form contained data for only two nodes) was used by Moore to infer a doubling of the component count every two years which, in various modified forms, later became identified as Moore's Law.

Viewed from this perspective, the key economic principle driving Moore's Law is that each successive technology node succeeds in controlling defect densities, thereby increasing the maximum number of components per chip that can be achieved at minimum cost. A corollary is that, if the cost of a chip is determined only by its processing costs, then the costs associated with masks, design effort and processing equipment must be assumed insignificant.

Unfortunately, what is often referred to as Moore's Second Law (more accurately referred to as Rock's Law), says that these non-recurring costs are also rising exponentially with each node. The only way to ride the Moore's Law curve is to amortize the non-recurring cost overhead over larger and larger numbers of wafers, or to use increasingly bigger wafer sizes. In effect, the continuation of Moore's Law requires the demand for a product to be infinite.

To gain more insight into the consequences of finite demand for products, we can add a term to Moore's model that accounts for non-recurring costs. The method is quite general, but to provide a specific example, we shall consider mask costs.

Due to the limitations of optical lithography, the ratio of mask costs to wafer processing costs (that is, the ratio of non-recurring to recurring costs) has increased by a factor of 10 as we have transitioned from 0.5 µm (500 nm) technology to 28 nm technology. Moore's model, however, refers to costs per component, and while processing costs per

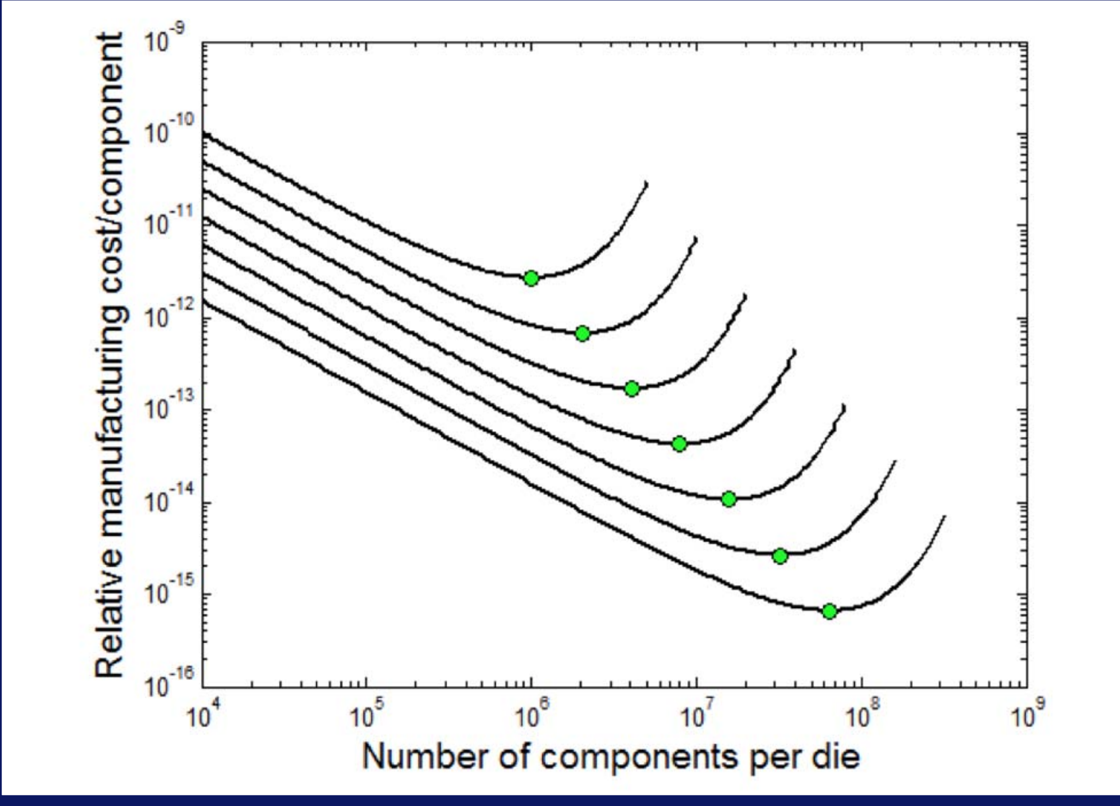


Figure 1. An Extension of the Manufacturing Model Proposed in Moore's 1965 Paper[1] to Illustrate the Manufacture of Chips at Minimum Cost

component have been falling appropriately, the mask costs per component have remained approximately constant. If this constant, non-recurring amount is added to the manufacturing cost in Moore's model, then we obtain the sequence of curves shown in Figure 2. These data have been generated by assuming that the non-recurring mask costs have been spread over 10,000 wafers and that the area of a chip at each node is constant. The result is that there is no benefit in transitioning to a new technology node when the processing cost per component becomes comparable to the mask cost per component.

In this model, there are only three ways to continue to follow Moore's Law and increase the number of components per chip with each new technology node: 1) spread the non-recurring costs over an increased number of wafers and so effectively lower the non-recurring cost "floor"; 2) use bigger wafers; and 3) the most heretical option is to produce components at a higher than minimum cost.

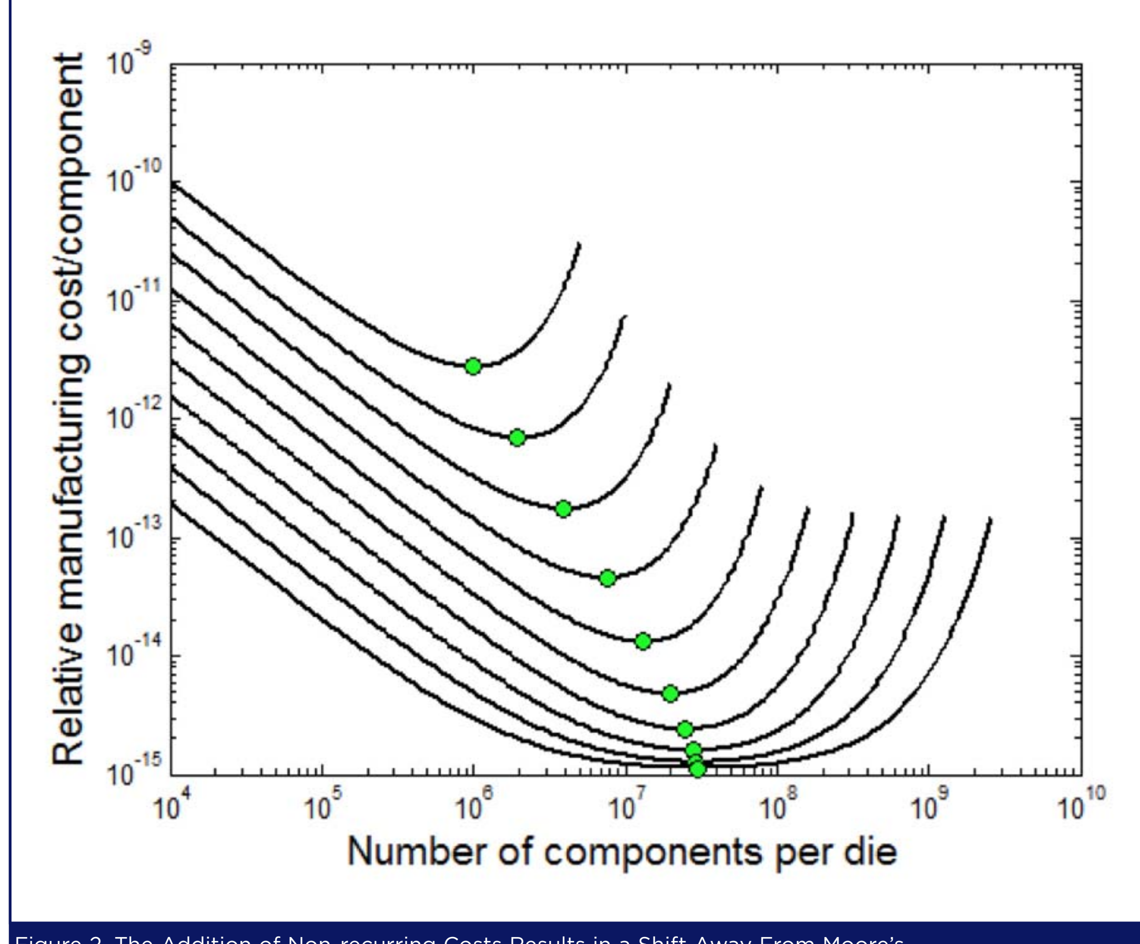


Figure 2. The Addition of Non-recurring Costs Results in a Shift Away From Moore's if Constrained by Minimum Cost

The strategy of processing more and more wafers has pushed Moore's underlying infinite demand requirement to its limits. For the most aggressive technology nodes, there are fewer and fewer products that can be sold in enough volume to be economically viable. This has made it ever more difficult for smaller businesses, and even medium-sized businesses, to take advantage of the improved performance of the latest technology nodes. The second strategy of increasing the wafer size was last performed at the 130 nm node, but marshalling the required industry investment to implement a transition from 300 mm to 450 mm wafers looks like it might happen, at the earliest, in 2015. But, as for the first option, only a dwindling number of products that can be sold in the huge volumes required to hit the minimum cost point will benefit from it.

The third option will result in a startlingly new business experience for the majority of companies. By following this strategy, their new product will have more components (at the same area), at possibly faster clock rates and reduced power, but it will cost more to reach economically viable production volumes. For these companies, Moore's Law will have passed through a minimum price point. Should we worry about this?

Some insight may be gained from the auto industry. Figure 3 shows 100 years of average car prices[3] expressed in 2010 dollars. The phase of exponentially falling average manufacturing cost per car lasted for 40 years until 1940. A smaller data set for the Ford Model T (which may be interpreted as representing the minimum car cost, also converted to 2010 dollars) also exhibits a dramatic price reduction phase that lasted until it passed through a minimum price point after which it stopped production in 1927. Due to a lack of published data, it is a point for speculation as to whether the price of the most expensive cars with the biggest profit margins has ever passed through a minimum price point! It is not the purpose of this article to assert the economic similarities between the automotive and semiconductor industries, as clearly there are very large differences. Our only goal is to postulate that a minimum price point does not necessarily imply the end of growth but that some adjustment to long-term business models may be required to ensure continued profitability.

So might we be approaching a minimum price point in the semiconductor industry? It is still very early in the adoption cycle to make concrete predictions, but there is some evidence that the transition to 32/28 nm technologies will not result in the cost savings that have been experienced historically.

In another example of the durability of Moore's original paper, he writes:

*"Clearly, we will be able to build such component-crammed equipment. Next we ask under what circumstances we should do it. [...] It may prove more economical to build large systems out of smaller functions, which are separately packaged and interconnected."*

Clearly, this second assembly approach lost out to the much more attractive economics of large-scale integration, but what are we to make of the emergence of 3D die stacking and interposer strategies that seem to be gaining headway today? This has been referred to in many articles as moving Moore's Law to the third dimension, but the higher assembly costs

of these techniques make it difficult to accept that they qualify for the minimum cost criterion that drives Moore's Law.

An interesting conjecture about passing through a minimum price point is that it results in the end of technology commoditization. This concept provided the rationale for companies transitioning to a fab-lite strategy that essentially regarded wafer capacity as a commodity to be traded, like wheat or iron ore. In a scenario where chip prices are rising due to finite product demand, foundries – like Japanese car manufacturers in earlier decades – can gain market share by offering increased production flexibility with ever-more-targeted options to offset the advantages that the mega-volume customers currently have in early access to leading-edge technology. Some evidence for this is that the number of options offered with each new technology node has been growing rapidly, and at the 28 nm node, even a high-performance option targeted for mobile devices is on offer from a foundry. Several of these options come with additional extended threshold voltages (ultra-low and ultra-high), as well the possibility of the low-cost tuning of device characteristics by selecting several nm-scale offsets (both positive and negative) to transistor gate lengths.

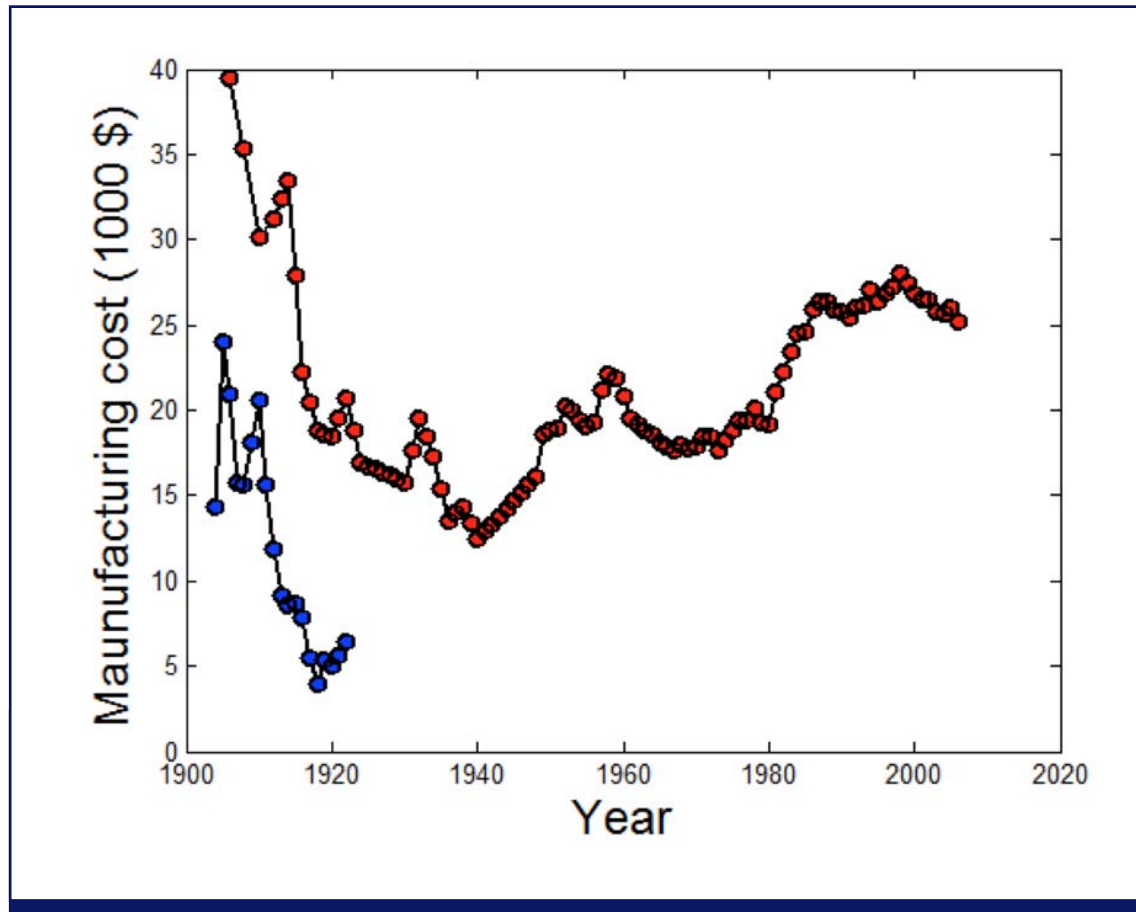


Figure 3. Manufacturing costs for cars expressed in 2010 dollars. Red circles indicate average costs, blue circles indicate Ford Model T prices.

In a post-minimum price-point world, the costs and risks associated with flexible, targeted manufacturing need to be carefully controlled. It only makes sense if the customer – meaning the company designing the marketing for the product produced by the foundry – has a good grasp of how different technology choices affect performance. The foundry customer must be able to assess how the multiple technology choices offered by the foundry affect the performance of the product during the early design phase. This level of knowledge that can be supported within large companies may prove to be a big challenge for the small and mediums-sized businesses that will benefit most from this strategy.

The closer coupling between design and technology also makes it harder to shop around. Guaranteeing access to limited, tailored wafer capacity will create large incentives for foundries to lock in customers. This may even lead to upfront payments to ensure product delivery. In this scenario, the fabless and fab-lite customers become heavily invested in their own foundry access, a model that has been termed "foundry-lite."

The idea of rising prices with each new technology node will take some getting used to. It will require much better communication between the producers and consumers of technology. But these changes will not necessarily stop the growth and profitability of the chip industry, unless you subscribe to the views of madmen or economists.

## Endnotes

1. The original article by Gordon E. Moore, "Cramming more components onto integrated circuits," *Electronics*, pp. 114-117, April 1965 has been reprinted in *Proc. IEEE*, vol. 86, No. 1, pp. 82-85, January 1998.
2. In this article, the use of the word "component" in Moore's original paper is continued and implies the smallest design component that could represent a simple logic gate, such as an inverter with two transistors, a SRAM memory bit with six transistors or an individual transistor.
3. U.S. Department of Energy, Vehicle Technology program. The data have been expressed in 2010 dollars using the GDP deflator.

## *About the Author*

***Phillip Christie***

Phillip Christie has over 25 years' international experience in IC technology research and development. Based in the Brussels area at imec, a world-leading center for nanotechnology research and development, he is responsible for foundry technology assessment, tactics and strategy for small/medium businesses and fabless/fab-lite companies. Phillip is a regular speaker at conferences, with an extensive portfolio of published articles and peer-reviewed research papers. ■

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The semiconductor market continues to be hyperefficient in meeting ever-evolving technology and consumer demands. This efficiency improvement and ability to incorporate change has been seen across all aspects of the semiconductor manufacturing supply chain, literally from the ground up. Even facility design and build has stepped up to meet highly compressed work schedules and adjusting to change while ensuring facilities are equipped for truly next-generation requirements.

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# Lithography 2020: Top Down Vs. Bottom Up

**Geoff Wild**
AZ Electronic Materials

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## Abstract

As the costs of lithography continue to escalate for future generations, a viable and complementary alternative is emerging in the form of directed self-assembly ("DSA"). In lithography, all the information for the patterning is transmitted "top down" from the mask, but cost scales with complexity. The DSA approach uses a "bottom up" chemical approach, similar to that used in nature, to drive complexity with a potentially compelling cost of ownership. This article reviews the opportunity and current status of the work.

By 2020, CMOS technology may have reached its physical limit, and we may be producing devices based on new designs and new materials, such as graphene or nanotubes. While we do not know with certainty what we will be making, it is a safe bet it will be made by some form of lithography. EUV lithography will have ironed out the bugs by 2020, but at a high cost: Extrapolating the historical exponential increase in the cost of exposure tools leads to a sticker price of $300-500 million per tool (Figure 1). By 2015, it is estimated that 30 percent of layers will have to use some form of advanced patterning: either multiple patterning, or EUV; by 2020, that number will have risen to well over 50 percent. For the 8 nm node or for smaller devices, it may even be necessary to use EUV in combination with multiple patterning, an even-more-frightening cost perspective. We may be able to develop the technology needed for this kind of process/tool combination, but the question is whether the economics can ever support it in mass production. There is a growing feeling that "something has to give" – that lithography is in need of a new and lower-cost paradigm.

The current lithography processes can be thought of as a "top down" approach: All the information needed to make a chip layer is encoded in a mask and transferred in the exposure step. With increasing amounts of information, this top-down approach bumps up against the limits of physics and becomes exponentially more expensive. In contrast, systems in nature often use a "bottom up" approach, in which components of a structure have built-in "chemical intelligence" and self-assemble into the final functional structure. In a bottom-up approach, the cost of a structure can rise linearly, or even less than linearly, with the amount of information it contains.

Today, the most advanced technology that uses a bottom-up approach for semiconductor applications is the directed self-assembly (DSA) of block copolymers. In block copolymers, the long, connected strings of monomer A and monomer B (i.e., … AAAAA – BBBBB …) prefer to interact with their own kind rather than with the other monomer, resulting in phase separation. Since the two strings are chemically bound, they cannot move too far away from each other, and the block copolymers therefore spontaneously self-assemble into a number of defined 3D phases that depend only on their chemical composition (Figure 2). Of these phases, the hexagonal rod and lamellar phases bear a striking similarity to the contact hole and line/space patterns made by photolithography, if they are oriented perpendicularly to the wafer surface. This vertical orientation can be achieved by coating the wafer surface with a material that has equal affinity to both A and B phases – a neutral underlayer.

Even with a neutral underlayer, however, the self-assembled patterns are not immediately useful for chip-making. This is because they will not naturally assemble in the right spot on the wafer, nor in the

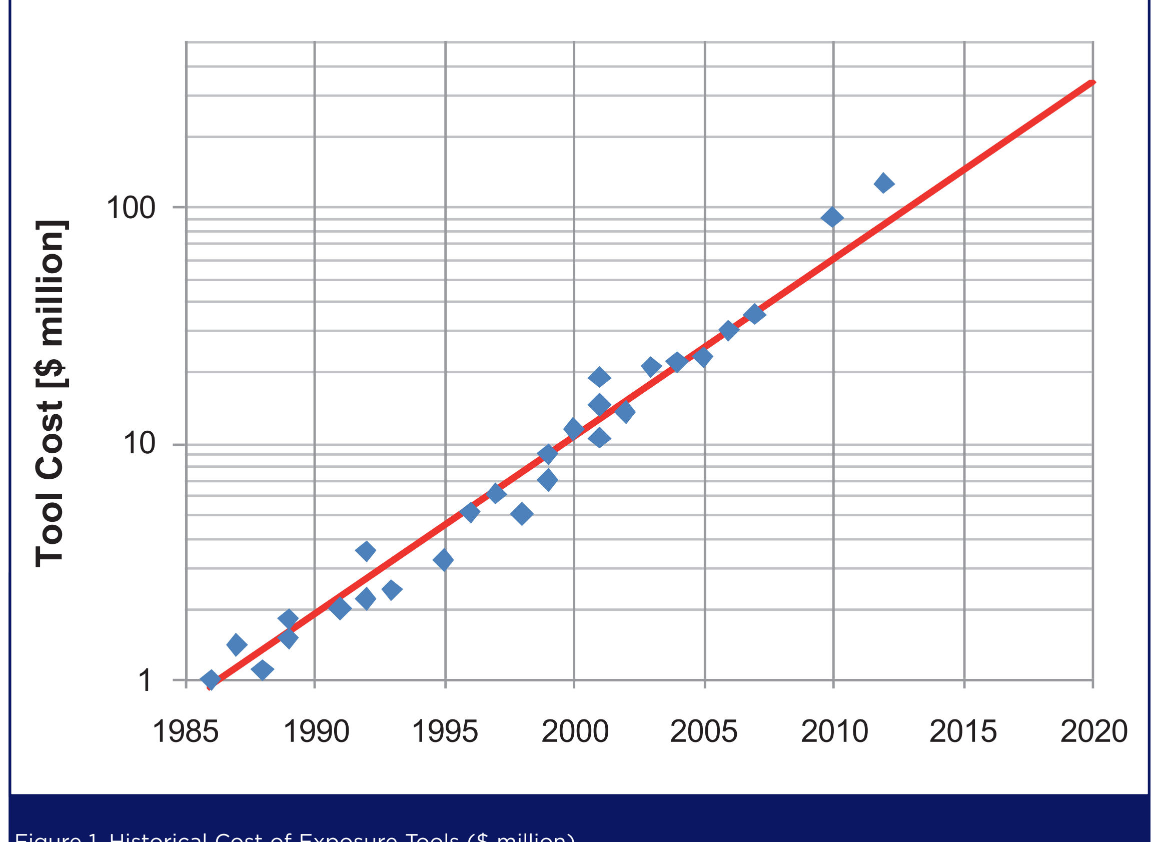


Figure 1. Historical Cost of Exposure Tools ($ million)

desired chip layout. For example, a lamellar phase on a neutral underlayer will arrange itself in a fingerprintlike pattern that is useless for chip-making (Figure 3). Directed self-assembly solves this problem by providing guide structures to which the patterns can align themselves. In the example of Figure 3, the guide structures are lines traditionally patterned by 193 nm immersion lithography, and their size and spacing is chosen so that four lamellae pairs can fit into the space previously occupied by one guide structure. Etching away block B selectively yields a 13 nm line/space structure that has four times the frequency of the guide line. This is much smaller than can be achieved by immersion lithography and is a significant challenge to make with EUVL.

Higher-frequency multiplication factors of six and more are possible, as is the option of pinning more than one lamella to the guide structure, which could expand the use of existing 193 nm immersion tool sets to the 8 nm node (Figure 4). DSA at these feature sizes will require development of new polymers; however, compared to, for example, changing the EUV wavelength to 6.7 nm, this is a comparatively simple and cheap development task.

Beyond line/space frequency multiplication, DSA processes can also provide contact hole multiplication and rectification, with the latter being of particular interest for contacts made by EUV lithography, which suffer from low CD uniformity due to shot noise. The cost of the DSA process, not counting the formation of the guide structures, is almost independent of feature size, requiring only the coating and annealing of the neutral underlayer and block copolymer, and an etch step. The economics of DSA patterning compares therefore very favorably with that of multiple patterning and EUVL processes.

This low-cost/high-performance promise of DSA has recently led to a surge in interest from both industry and academia.

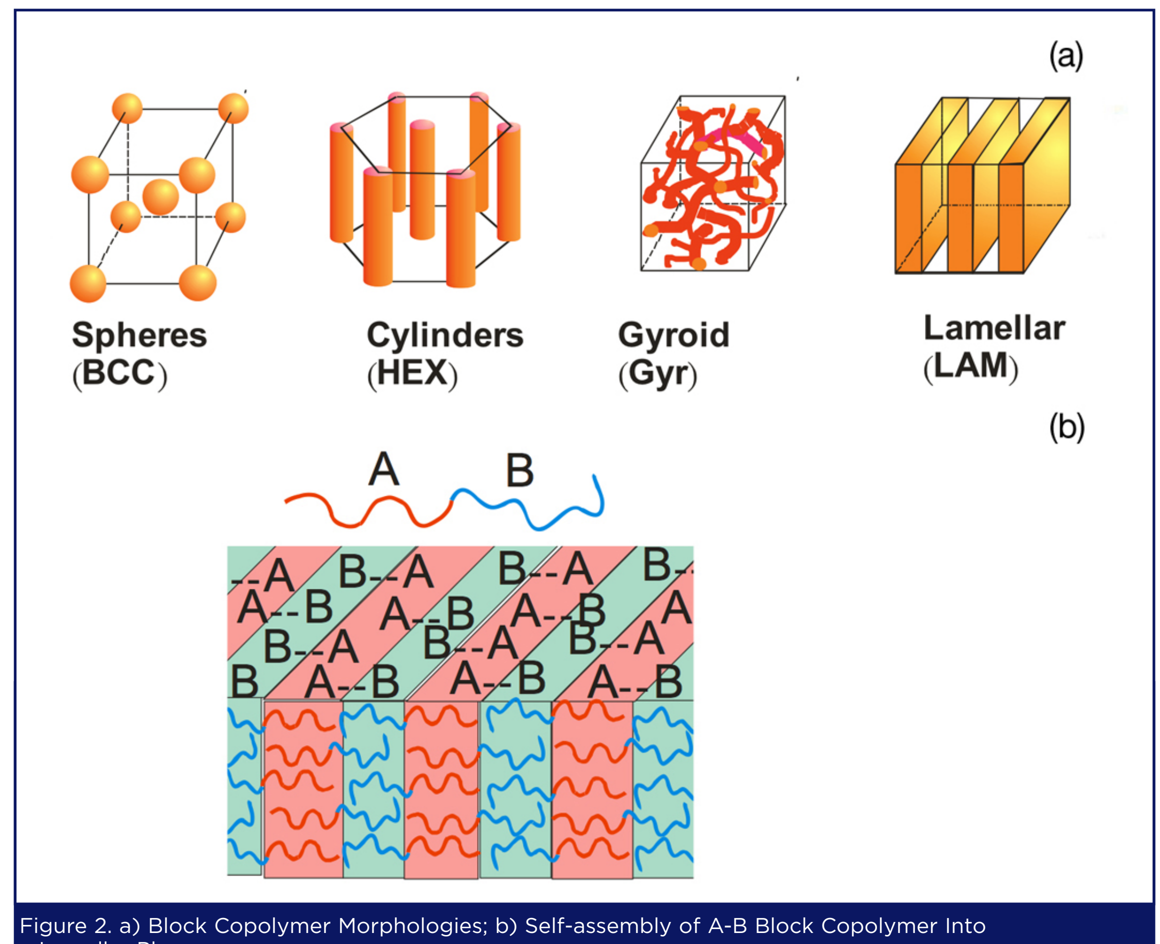


Figure 2. a) Block Copolymer Morphologies; b) Self-assembly of A-B Block Copolymer Into a Lamellar Phase

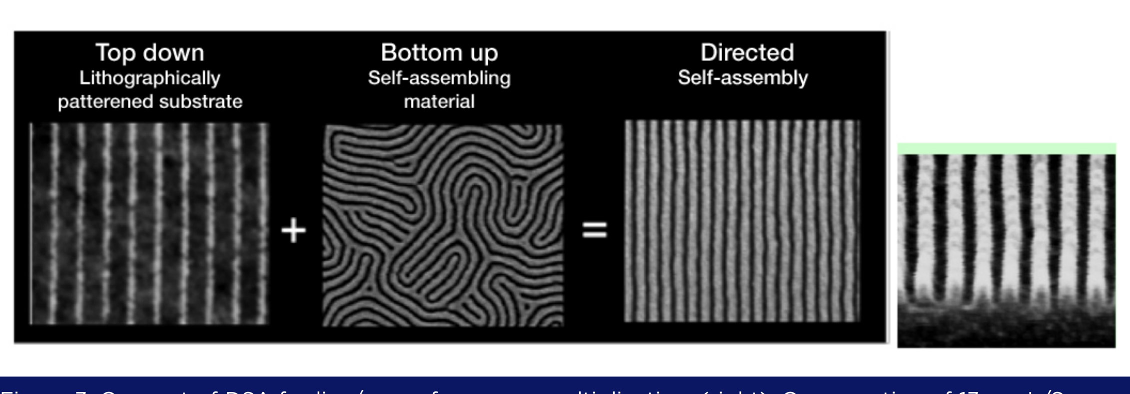


Figure 3. Concept of DSA for line/space frequency multiplication. (right): Cross section of 13 nm L/S patterns made with DSA using 193 nm immersion guide structures (after dry etch). *Courtesy of IBM*

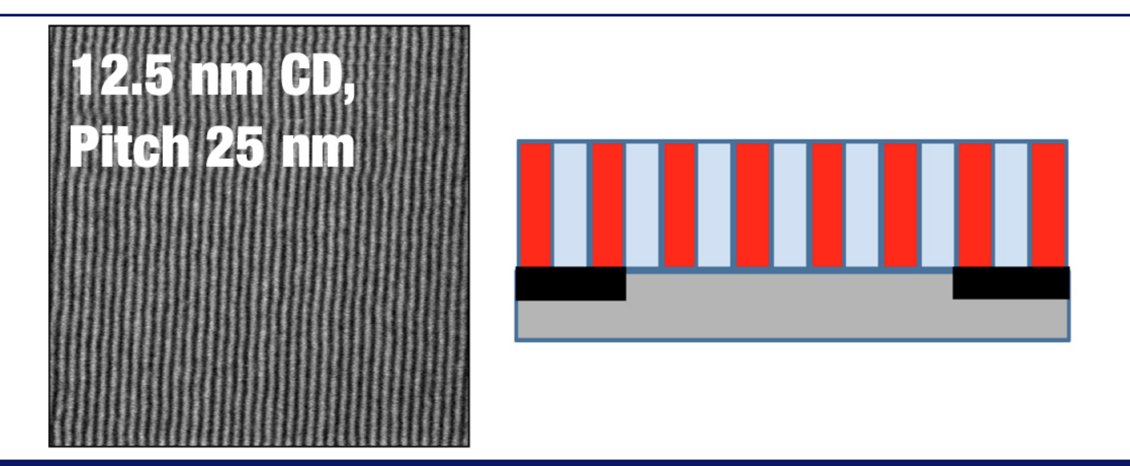


Figure 4. 12.5 nm L/S DSA structures on guidelines patterned with 193 nm dry lithography (35 nm lines/150 nm pitch - 6x pitch division with guide structure width 1.5 $L_0$). The same approach can enable the use of 193 nm immersion lithography for the 8 nm node (24 nm guide structure, 120 nm pitch).

Promising results have already been obtained on one of the main questions about DSA – whether its thermodynamics and kinetics can lead to defectivity levels commensurable with chip-making. A joint IBM/AMAT full wafer study found no immersion specific defects and was able to place an upper limit of <25 DSA-specific defects per wafer; about the same level that was seen for immersion lithography five years ago. While much work still needs to be done before DSA is ready to enter manufacturing, so far, research has not identified any roadblocks that would stand in the way of it becoming a mainstream chip-making technology well before 2020.

In 2010, we began a significant R&D effort for the commercial development of DSA materials at our Branchburg, N.J. facility, in partnership with IBM's Almaden Research Center. As part of this joint development project, AZ has full access to IBM's DSA technology and worldwide licenses to their patent portfolio. IBM has long been a leader in DSA, and AZ has built on their know-how to develop reproducible and performing materials and processes that can meet the demands of high-volume manufacturing. Today AZ's DSA materials stand ready for process learning in future advanced semiconductor applications. With the benefit of 20-20 foresight, my prediction is that the bottom-up paradigm will become an integral part of semiconductor manufacturing.

## About the Author

**Geoff Wild**

Geoff Wild is currently the CEO and president of AZ Electronic Materials. He was previously the divisional director of Johnson Matthey Electronics, and then president of AlliedSignal Electronic Materials (now part of Honeywell). Mr. Wild was the CEO of Nikon Precision Inc. from 2002 until 2007, and then CEO and president of Cascade Microtech Inc. from 2008 until 2009. He is also a nonexecutive director of Materion Corp. and was previously a non-executive director of E-Ink Corporation and Axcelis Inc. ■

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# CHIP ARCHITECTURE & INTEGRATION

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**Warren Savage**
Chief Executive Officer, IPextreme

One of the key lessons from the industrial revolution was that standardization enables markets to grow at explosive rates. Standardization radically altered the landscape of transportation (standard railroad gauges), warfare (interchangeable parts in Winchester rifles) and production (Henry Ford's assembly line). Indeed, even the distribution method of electricity involved a pitched battle between Nicola Tesla (AC) and Thomas Edison (DC) as to what standard would be adopted for the power grid we still use today.

As it was 100 years ago, standardization today allows industries to grow in important new directions by incorporating the combined wisdom of the technical community into a format that the future can be built upon. Because of the globalization of our economies, these technical standards have a faster and more widespread effect than ever before.

In the following paper by Karen Bartleson of Synopsys, you will see the important role that standards play in the semiconductor market today. Important new standards are continuously required to enable new efficiencies in design, interchange, quality and connectivity that will be required for the industry to keep pace with the relentless demand of consumers and to capture the ingenuity of our engineers.

CHIP ARCHITECTURE & INTEGRATION

# Semiconductor IP Standards: More Important Than You Think

**Karen Bartleson**
Synopsys

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## What Are Technical Standards?

Standards are abundant in today's world, and they are quite diverse. There are standards for health and safety, standards for measurement and even standards for human behavior. The type of standard that is most apparent in the semiconductor industry is the technical standard. A technical standard is defined in Wikipedia as "an established norm or requirement about technical systems. It is usually a formal document that establishes uniform engineering or technical criteria, methods, processes and practices."

Modern system-on-chips (SoCs) depend heavily on technical standards. Design descriptions are written in standard languages. Design intent, such as low-power management, is written in standard formats. A design database, such as OpenAccess, is at the heart of the process for custom and analog design. Electronic design tools interoperate with each other, configured into sophisticated flows, using industry standards from formal committees and those that arise as de facto standards.

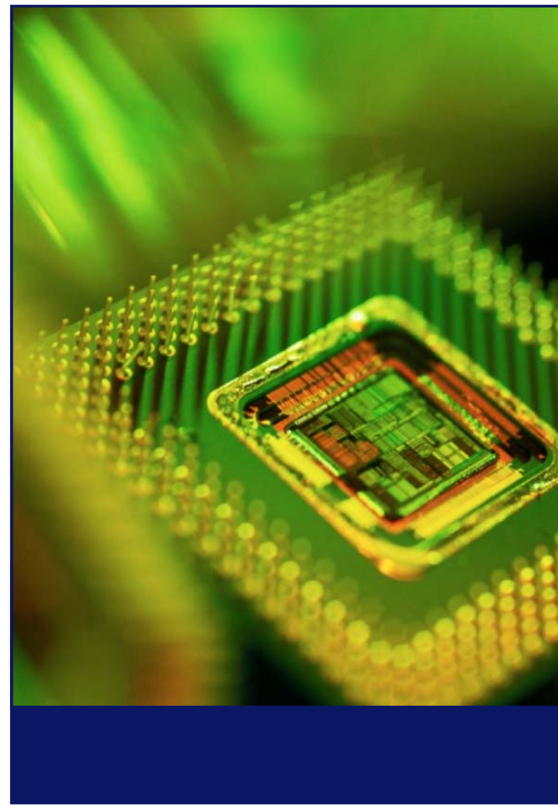
SoCs are not designed from scratch. They start with building blocks known as semiconductor IP. Within the industry, the blocks are called simply "IP," not to be confused with Internet Protocol or intellectual property in the general sense. IP blocks, too, rely on standards long before they find their way into an SoC.

## The Importance of Standards for IP

At the beginning of an IP's life, standards come into play. The IP is designed and verified using standard hardware description languages like Verilog and SystemC. The IP is then sold as a design written in Verilog (or other HDL) accompanied with a testbench in SystemC (or other language). Additional information, warranties and so on also come with an IP product, but standards form the fabric of the IP. A positive result of using a standard to design an IP is that it can be readily interoperable with other IP and parts of the SoC that use the same standard.

The IP can also implement a standard. This is particularly true for interface IP. Interfaces have become household words by now, such as USB and Ethernet. (Well, maybe Ethernet isn't a household word unless your household is composed of geeks.) An SoC – or a less complex "regular" integrated circuit – often needs some type of common method for communicating with the outside world. The most effective way to implement an interface standard is to buy an existing IP. Designing your own USB interface might be a fun challenge, but probably not worth the time and effort. There are many USB IP vendors that will be happy to save you the time and effort, for a price, of course.

The burning question, then, is how do you know if the IP you want to purchase has the level of quality that you need? Again, standards can help. The standard officially known as "1734-2011 - IEEE Standard for Quality of Electronic and Software Intellectual Property Used in System and System on Chip (SoC) Designs" was created for this purpose.



From the IP vendor's perspective, there is a need to protect the "source code" of the IP's design. When an IP is represented in a standard language, the design might easily be seen and understood. It would be harmful, if not devastating, to the IP owner's business to have a competitor reverse-engineer and clone the IP. The legal system could be called upon in this case, but it's better to prevent it from happening in the first place. There is a standards project under way in the IEEE Standards Association called "P1735 - Recommended Practice for Encryption and Management of Electronic Design Intellectual Property (IP)" that has the goal of addressing this need in addition to other IP interoperability challenges.

Possibly the most important role that standards play in the IP arena is allowing the IP to "talk" to other IP and custom-designed portions within an integrated circuit or SoC. This was the original charter of the Virtual Socket Interface Alliance (VSIA). The alliance was formed among a group of interested electronic design automation vendors and customers. At the time, they viewed an advanced circuit design as if it were a PCB with sockets into which IP and other design parts would be plugged into. They specified standards – existing ones and ones that needed to be developed – that would allow the IP and other parts to interface and communicate with each other. As the industry moved forward, the standards were employed and evolved so that SoCs could become a reality. Eventually, VSIA declared its mission had been accomplished, its standards were transferred to the IEEE Standards Association and its doors were closed.

## Two Prime Examples

Today there are numerous standards that benefit IP developers and customers. There are many effective standards and several organizations addressing the standardization needs and challenges of IP development and integration.

A prime example is the standard called IP-XACT, more formally known as “1685-2009 - IEEE Standard for IP-XACT, Standard Structure for Packaging, Integrating, and Reusing IP within Tool Flows.” A second, and quite obvious, example is USB.

IP-XACT was originally developed by the SPIRIT Consortium (Structure for Packaging, Integrating and Re-using IP within Tool-flows). When SPIRIT merged with Accellera, a premier standards-setting organization in the electronic design automation industry, work on IP-XACT continued within Accellera. After ratification by Accellera, IP-XACT was transferred to the IEEE Standards Association for formalization under this ANSI-accredited standards-development organization.

IP-XACT is an XML schema for describing IP in a way that is language- and vendor-neutral. There are several standard design languages being used for IP descriptions today: C, C++, Verilog, VHDL, SystemVerilog, SystemC, e, OpenVera and PSL. IP-XACT enables interoperability and reuse of IP by employing XML, which is simply plain text. Interestingly, XML is a standard itself, from the World Wide Web Consortium (W3C), with far-reaching use throughout the Internet and far beyond the IP marketplace.

The drivers behind IP-XACT are: improving time to market; needing to manage ever-increasing complexity; and having to reduce the cost of development and verification for integrated circuit design. Time to market is a nice way of saying “whoever gets there first makes the most money.” Think of how complex electronic products have become – mobile devices, tablets, “the Internet of everything” – and it’s obvious why managing complexity is imperative. Reducing costs is another nice way of saying “making more money.” Standards aren’t always recognized as helping companies make more money, but it’s true.

One of the best examples of a hugely successful IP standard is the USB (universal serial bus) interface standard. Implementation of USB in products is visible in practically every electronic product on the market today, from smartphones to televisions to servers.

The USB standard was developed by a special, nonprofit corporation called the USB Implementers Forum Inc. Currently, there are almost 700 member companies in the USB-IF from all around the world. The USB-IF promotes market adoption, enhancement and compliance of the USB standard. In order to license the USB logo for use with a product, which indicates that the product is compliant with the standard, the vendor must pass testing requirements at a USB-IF compliance workshop or at a certified test lab. Because IP (called “silicon building blocks” by the USB-IF) is as much a product as something like a tablet is, the USB-IF calls out and specifies testing requirements explicitly for IP.

Not only is the USB-IF concerned with the standard – that is, the USB specification itself – but also with both hardware and software compatibility. Electrically speaking, devices, connectors, hubs and peripherals must work together, the same way that power outlets do. Software in an operating system must be leveraged so the OS can be used with a variety of PCs and peripherals. These concerns affect everyone including hardware suppliers, software developers and IP creators.

## How You Can Participate

Standards organizations thrive on participation from people and companies that know the value of standards and want to ensure the standards are effective, usable, adopted and maintained. Consumers and suppliers both play a role in creating good standards. In the case of IP standards, it’s also a business-to-business (B2B) involvement, as the end-customer – the consumer – probably doesn’t care how standards are created or what their technical merits are.

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They simply want the products they buy to work well.

As a designer of integrated circuits and electronic products that embody IP, you want to be sure that IP standards are implementable and testable. As a supplier of design automation tools, you know that standards must be clearly defined and readily supported by your products. The best way to ensure good standards is to participate in their creation and maintenance.

Standards organizations welcome your participation with open arms. Joining is almost always a straightforward step. Websites give information about membership and any fees that might be required. (Standards development – like any product – can't happen without funding.) Each organization has a set of bylaws and/or policies and procedures that you should read before joining. Then, bring your expertise, enthusiasm and business acumen to the table, where you'll ultimately be rewarded with robust standards to propel your industry forward.

## About the Author

***Karen Bartleson***

Karen Bartleson is senior director of Community Marketing at Synopsys, responsible for interoperability, standards and social media programs. She was elected president of the IEEE Standards Association for 2013-2014. Karen authored "The Ten Commandments for Effective Standards" and "The Standards Game Blog." ■

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# MANUFACTURING: FABS, SYSTEMS & SOFTWARE

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**Thomas Sonderman**
Vice President, Manufacturing Systems Technology; GLOBALFOUNDRIES

In the design and implementation of manufacturing control systems, it can be said that there has been an appreciation for the need to understand the functionality to be delivered by those solutions. As continued development of factory automation progresses to more integrated and holistic fab solutions, however, there is commensurate need to understand the effect of a given solution on the overall manufacturing environment. Effective development and implementation of systems and software must therefore understand the larger set of manufacturing performance indicators in truly gauging the impact of any given solution. The authors of the following two papers illustrate this need to fully appreciate the increasing scope of solution development and impact.

Ignizio and Garrido discuss the particular impact of variability at the unit process level on simulation of fab capacity and cycle time. The inherent challenge presented is in accurately modeling these fab metrics without a sufficient understanding of the magnitude and sources of variability at the unit operation level. This has implications for the modeling methodology itself, but also in the interpretation of the results and the subsequent actions to be taken to improve fab capacity and cycle time.

Kabitzsch et al. present discussion from the 11th European AEC/APC Conference, and discuss the evolution of this conference into a European Advanced Process Control and Manufacturing Conference. As has been evident in the evolving conference program, interest in the discussion of APC solutions is extending in scope to evaluate their fuller impact to manufacturing. To this end, the authors highlight the expanded program that includes a Manufacturing Effectiveness and Productivity section to more completely discuss the costs and benefit associated with APC solutions.

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# Automated Measurement Devices Measure Critical Parameters in Semiconductor Fabrication Processes/Equipment

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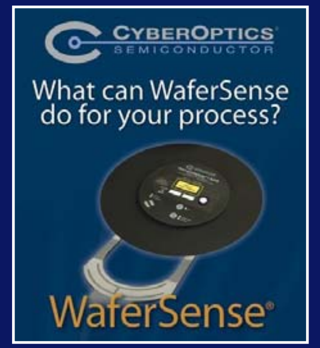

# Advanced Process Control Goes Manufacturing: APCM Conference in Europe

**Klaus Kabitzsch,[1] Michael Klick,[2] Andreas Steinbach,[3] Alan Weber[4]**
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[3]Von Ardenne Anlagentechnik GmbH [4]Alan Weber & Associates

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## Abstract

Manufacturers, suppliers and the scientific communities of semiconductor, photovoltaic, LED, flat panel, MEMS and other relevant industries are invited to the 12th European Advanced Process Control and Manufacturing conference, taking place at MINATEC Grenoble on April 16-18, 2012.

Beyond the established topics of equipment and process control on unit process and fab level, the new agenda also includes current challenges and future needs of manufacturing effectiveness.

## Contributions of the 11th European AEC/APC Conference at a Glance

The 11th European Advanced Equipment Control/Advanced Process Control conference took place in Dresden, Germany, April 4-6, 2011. More than 160 attendees listened to 10 keynotes and invited talks, 29 oral presentations, 22 posters and two tutorials. Organizers managed a sophisticated trade-off between an expanded area of topics and the need for detailed scientific exchange. Two parallel sessions on unit process and factory-level control enabled an emphasis on methodologies and IT infrastructure.

The conference last year highlighted new APC strategies, including less reactive and more predictive approaches at the factory level, as well as new ideas principally based on increased process understanding for process control at the unit process level. Enhanced equipment quality assurance (EEQA) as a new approach is now within the scope of APC: Its major target is to increase productivity and manufacturability by focusing on equipment characterization. Process control in LED manufacturing was shown to be a new and fast-growing APC applications area. General trends were also discussed, as a number of contributions dealt with higher APC effectiveness through increased process understanding.

The program was well balanced between the traditional APC approaches on the one hand, and new needs, problems and methodologies on the other, e.g., talks on fab logistics and performance (A. Gellrich).

The session on plasma processes (seven talks) comprised different approaches for understanding plasma instabilities in order to avoid yield loss in manufacturing (N. Urbansky), and advanced plasma diagnostics that will be required in the future for robust plasma process models, e.g., for virtual metrology (VM). An important contribution from the session on thermal processes and implant (three talks) was a systematic comparison of control methods at the equipment level (D. de Roover). Another interesting example in the metrology session (four talks) was a study of optimal metrology sampling strategies (A. Subramanian). Other sessions were devoted to lithography (two talks) and APC applications (two talks).

A second part of the talks dealt with fab-level requirements and methodologies, IT infrastructure, etc. The session on data analysis, modeling and visualization (seven talks) covered a wide range of topics, from anomaly detection in time-series data (J. D'Amour) to model stability in adaptive VM (A. Dementjev). A session on IT infrastructure (four talks) included talks on very fast databases (W. Benn) to new standardization approaches for sensor interfaces in manufacturing (D. Suchland).

## APC Embraces Manufacturability

A number of high-quality keynotes and invited talks focused on more strategic

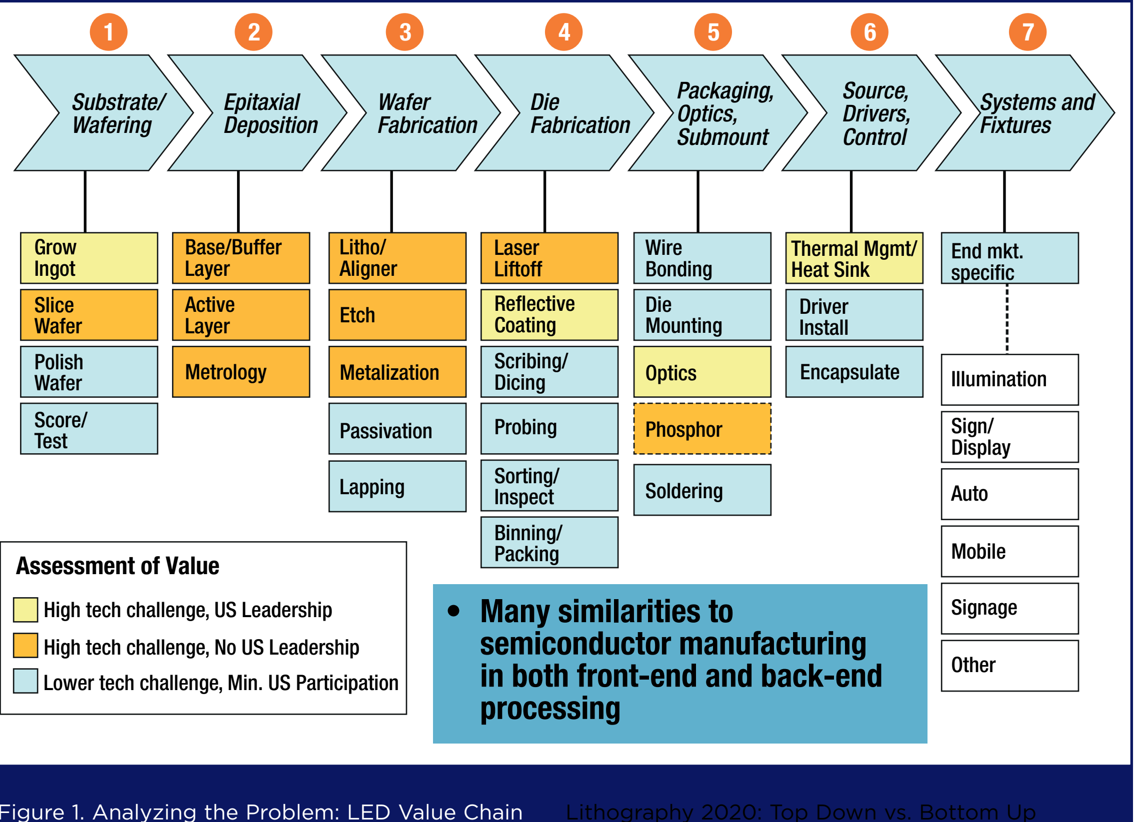


Figure 1. Analyzing the Problem: LED Value Chain

Lithography 2020: Top Down vs. Bottom Up

objectives, future trends and visionary ideas. Semiconductor manufacturing is a very complex process chain, so the approach for understanding and control of these processes must be deeply interdisciplinary.

In contrast to the traditional heuristic approaches, future-unit process-level APC systems will take into account the specific properties of the process. This requires robust and simple process models based on process understanding, including models of the equipment and its key components. These reflect the important properties of the process and enable a first-level data selection and compression – with completely different models and parameters from litho to PECVD or CMP.

APC at the fab level will continue to use effective standard algorithms, including data projection methods such as PCA. Here the effectiveness is much higher when it is based on validated, pre-processed data from process-level APC.

Equipment models are the core part of ISMI's EEQA program, and consequently, were also the main focus of this conference, beginning with the tutorials dealing with general and RF equipment models. In two of the invited talks, this was discussed in the context of equipment health monitoring (invited talk, G. Crispieri, keynote Alan Weber), and finally referenced as one of the future trends in APC methodology related to updates of the ITRS (J. Moyne). Here a better and more detailed understanding of equipment properties is the target for increase in productivity, while also directly addressing the issues of chamber matching and improvement of fab ramp-up.

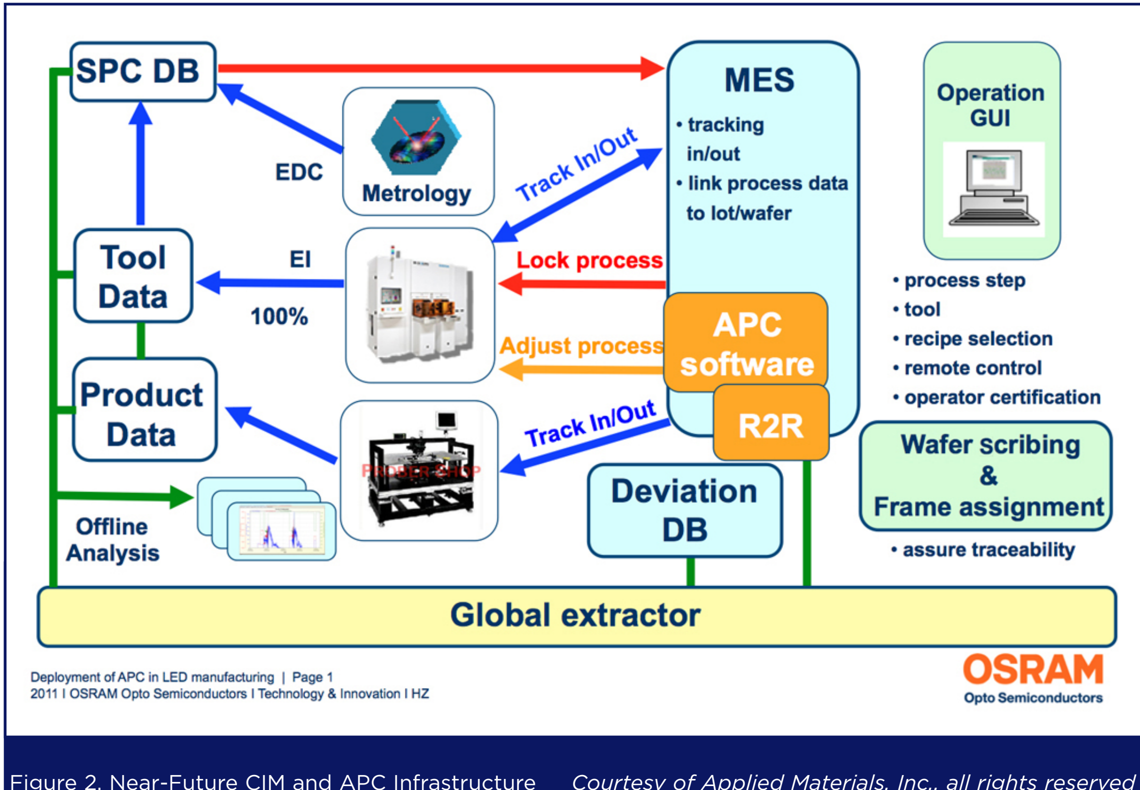


Figure 2. Near-Future CIM and APC Infrastructure *Courtesy of Applied Materials, Inc., all rights reserved*

For APC at the fab level, deeper understanding of yield dependencies will be the core area over the next few years. We have to consider not only the static behavior of equipment or process models, focusing on methods like correlation or PCA; dynamic behavior becomes even more important in the coming years. This will enable a better view of the future behavior of equipment and the entire fab. As a result, accurate prediction of yield, equipment states and maintenance needs will be more feasible.

For both unit process and fab-level systems, feedback control should not always be the dominant choice. Model-based feed-forward control will become much more important in the next years, in combination with better prediction capabilities across different time horizons ("less reactive, more predictive"). However, this will require far better process models (static and dynamic) than we have today, because feed-forward control also opens the doors to optimization-based control systems.

## APC in LED Manufacturing

This year, LED manufacturing was the hot topic in new APC applications. Two talks discussed this application area from the supplier (J. Moyne, Applied Materials) and user (H. Zull, OSRAM) points of view. Both talks have shown very impressively that APC methodology must always fit the process chain and address the economic requirements for cost saving, which is driven mainly by the LED manufacturers. Solutions at the unit process level – well established in silicon wafer manufacturing – cannot be transferred without adaptation. This holds true for APC both at the unit process and fab levels.

## Benefit Calculation of APC Projects

One of the more interactive sessions was a lively panel discussion on APC ROI (return on investment). The panel included seasoned participants from across the value chain, including device makers, equipment suppliers and APC software suppliers. This breadth of coverage ensured that none of the factors in the ROI formula would be discounted, underscoring the principle that for an implementation project to be viable, the benefit must accrue to all the stakeholders.

Some of the key insights include: 1) ROI for many projects is not emphasized, because APC investments are now considered strategically vital, and no longer an optional technology; however, ROI can still be useful for ranking potential process/productivity improvement projects after a fab is running; 2) FDC can be well justified during fab ramp-up in addition to full production, because the earlier the equipment is characterized, the more quickly the processes can be stabilized and qualified; 3) too often we forget the manpower savings in ROI calculations, since we assume the avoidance of scrap wafers is the largest benefit; but when you have limited staff, the "opportunity cost" of tying up a process or equipment engineer on a problem that could have been avoided with an FDC or preventive maintenance solution can be significant; and 4) fabs are starting to recognize and consider the "hidden" cost of internal solutions when making buy vs. build decisions for APC software; while this is welcome news for commercial software suppliers, there aren't that many left to hear it.

## 12th European APCM Conference

The 12th European Advanced Process Control and Manufacturing conference will take place at MINATEC Grenoble on April 16-18 this year. Beyond the established topics of equipment and process control on unit process and fab level, the new agenda also includes current challenges and future needs of manufacturing effectiveness. About 80 oral presentations and posters of topics such as semiconductor, photovoltaic, LED, flat panel, MEMS and other relevant industries are expected.

1. Advanced Process Control on Unit Process Level
   - APC applications at unit processes
   - Unit process control methods
   - Tool and sensor data analysis
   - Maintenance & tool optimization
   - Enhanced equipment quality assurance (EEQA)
2. Advanced Process Control on Fab Level
   - Fab-level process control methods
   - Virtual metrology
   - Yield management
   - Factory data analysis
   - IT infrastructure
3. Manufacturing Effectiveness and Productivity
   - Unit process & equipment productivity
   - Factory productivity and automation
   - Factory modeling, simulation and optimization
   - Cost optimization and end-of-life equipment issues
   - Environment and green manufacturing

The keynote of Jeremy Read (vice president, Applied Materials) will focus on prediction as the future enabler for quality management across the semiconductor manufacturing application space. In this talk, a cohesive manufacturing automation prediction infrastructure and strategy will be presented. Key elements of that strategy including predictive maintenance, virtual metrology (sensor fusion), predictive scheduling and predictive yield will be highlighted in terms of what these technologies can offer and what we have achieved with them to date. The potential impact of these technologies today and in the future in areas such as quality management and process control for specific applications (e.g., automotive) will be explored, as well as challenges in implementation such as the culture change associated with getting the necessary algorithmic solutions accepted on the factory floor in order to move from a reactive to predictive paradigm. Further, an ultimate vision will be presented of the future factory environment with intra- and inter- factory prediction systems in place enabling this new predictive paradigm in manufacturing.

The increasing role of APC in the ITRS, and challenges, opportunities and synergies of 450 mm wafers are further key aspects of the upcoming conference.

Traditionally, this conference has also always been a platform of training and education. As in 2011, there will be again two tutorials; the first one will focus on data analysis, multi-dimensional visualization and geometric process control, demonstrating parallel coordinates and the synergistic technologies of multi-dimensional visualization and geometric process control they have spawned in the solution of ostensibly complex problems drawn from a spectrum of engineering (as well as other) disciplines.

The second tutorial deals with APC and corrective, preventive and then predictive maintenance; and how maintenance methodology, supported by advanced process control, opens new equipment engineering and manufacturing opportunities for cycle time, cost and yield.

Beyond the industry exhibition, the European APCM conference offers an excellent opportunity for user group meetings, which are organized by the companies themselves, in coordination with the conference.

For further information, please see www.apcm-europe.org.

## Endnote

1. N. Patibandla et al. DOE SSL Manufacturing R&D Workshop; April 2010

## *About the Authors*

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Klaus Kabitzsch received his diploma and a Ph.D. (1982) in electrical engineering and communications technology. He subsequently worked in the industry in the area of control of machines and equipment. After 1989, Dr. Kabitzsch worked at the universities of Leipzig and Dresden and focused his research on sensor networks, distributed systems, real-time software and automation. He became professor and head of the department of Technical Computer Sciences in 1993 at the Dresden University of Technology. Dr. Kabitzsch's current projects focus on the automation domain, component-based software design, design tools for networked automation, energy and quality management, data analysis, advanced process control and predictive technologies.

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Michael Klick is CEO of the Plasmetrex GmbH, a plasma process control solution provider. He received his diploma in technology of electronic devices in 1987 and his Ph.D. in plasma physics from Ernst-Moritz-Arndt-University Greifswald in 1992. Dr. Klick has over 15 years' experience in nonlinear modeling of industrial RF plasmas and development of plasma sensor systems for etch and deposition in semiconductor and PV manufacturing. He holds several patents in this area. Dr. Klick has been working on the qualification of process and maintenance personnel since 2003, and gives regular lessons for students about industrial plasma technology at the Ruhr-University Bochum. Assessment, modeling, and RF and plasma chamber matching for plasma tools in manufacturing are his current key activities.

**_Andreas Steinbach_**

Andreas Steinbach is working on process development at Von Ardenne Anlagentechnik GmbH, a worldwide leading manufacturer of equipment for industrial vacuum processes of plasma and electron beam technologies. He received his diploma for physics in 1983 and his Ph.D. in physics from Dresden University of Technology in 1990. Dr. Steinbach has over 25 years' experience in industrial plasma processes for etch and deposition in semiconductor and thin film manufacturing, and holds several patents in this area. Since 1998, he has been working on process control in semiconductor and thin film technology. From the beginning in 2000, Dr. Steinbach was one of the leading heads organizing the European Advanced Process Control and Manufacturing Conference.

**_Alan Weber_**

See bio on page 7. ■

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MANUFACTURING: FABS, SYSTEMS & SOFTWARE

# Fab Simulation and Variability

**James P. Ignizio,[1] Hernando Garrido[2]**
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## Abstract

Simulation, specifically *discrete event simulation*, is widely employed throughout the manufacturing sector – particularly in semiconductor and photovoltaic fabs – for prediction and assessment of factory performance. Of special interest is fab *cycle time* and *capacity*. Whether it be a proposed, ramping or mature fab, it is vital to have accurate estimates of facility performance. Conventional wisdom among simulation personnel is that – once a detailed fab simulation model has been developed – the model should be run for a period of one to possibly two years of simulated time so as to reach the "steady state" performance of the simulated fab. This process is repeated a number of times and the average of the results are employed in the decision-making process (e.g., should more or fewer tools be used?). Again, conventional wisdom holds that such a process is sufficient to establish accurate estimates of fab performance. That assumption is challenged in this paper.

## Introduction

Decision-making depends upon predictions. Some predictions are subjective, based on little more than guesses. Others are developed through a more analytical process. Whether subjective or analytical, *predictions are made on the assumption that a given future event, condition or performance metric is indeed predictable.* As will be discussed, however, the validity of any prediction depends – in large part – on *knowing what we don't know*. More specifically, it is vital to know the source and amount of variability existing within each segment of the fab.

In the semiconductor and photovoltaic (PV) industries, predictions are made at both the *macro level* (e.g., future state of the economy, competition, demand for a new product and cost of silicon) and *micro level* (e.g., predicted plant capacity, yield and cycle time). In this paper, our focus will be at the *micro level*; i.e., predictions of fab performance.

Consider a fab, either operational or to be built. Two performance metrics one *should* want to predict are fab *capacity* (e.g., maximum *sustainable* wafer flow rate) and fab *cycle time* (i.e., time between entry of a job into the fab and its departure). Under the assumption that our predictions are accurate, decisions such as the capacity of each workstation (a.k.a., "tool set") may be made. Poor predictions, however, may lead to either insufficient or excess capacity. The cost of either error is significant.

## Methods for Performance Prediction

The three most common approaches for prediction of production line performance are via spreadsheets, queuing models, and simulation. Spreadsheets ignore variability, as well as the complex interactions between workstations, and – despite their popularity – this "quick and dirty" approach to prediction poses a significant risk.

Queuing models *do* consider variability and, to a limited degree, workstation interactions. They have, however, two significant limitations. First, *they only deliver predictions of the **steady state** of the facility* – while ignoring the "ups and downs" encountered prior to reaching that state. Second, while queuing models have been constructed for small factories or segments of larger facilities, their development for something as massive and complex as a semiconductor fab would require a heroic effort (and one would still be left with just a prediction of the facility's steady state).

Most, if not all, semiconductor and photovoltaic firms employ simulation models when attempting to predict fab performance. The outputs of the simulation of a *detailed* model of a fab provide forecasts that are commonly accepted and acted upon. The four most widely acknowledged drawbacks of simulation, however, are: the time and effort required to construct a model; time and effort devoted to "care and feeding" of the model; time and effort

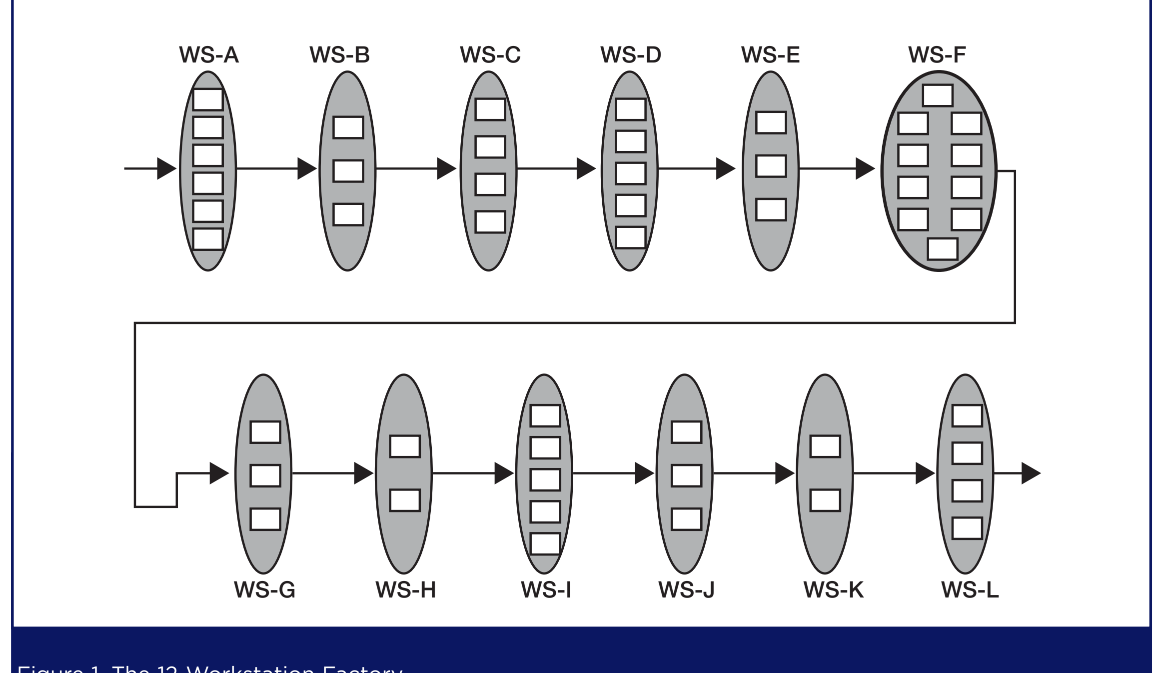


Figure 1. The 12-Workstation Factory

necessary to collect supporting data; and the extensive amount of training and practice required to gain a reasonable degree of proficiency in the art and science of simulation.

Based on our (real-world) experience, it may take a year or more just to construct a valid fab simulation model before being able to conduct the experiments necessary to support fab performance prediction. As mentioned, conventional wisdom throughout the semiconductor and PV industry holds that one should run the model for one or two years of *simulated time* in order to reach *steady state*. Just one single simulation run, however, may require a day or more to conduct. And one run is hardly enough to obtain predictions with any degree of confidence.

Because of the amount of time consumed by each simulation, firms may (and often do) rely on the output of relatively few experiments. They assume this is sufficient to obtain accurate predictions of fab performance at steady state. This is an assumption the author disputes – whether one is dealing with a massive, complex fab or even a much simpler, much smaller factory devoted to the production of less complex products – as shall now be illustrated.

| 12 Workstation Facilities | | |
|---|---|---|
| Workstation | Process Rate (jobs/day) | Utilization |
| A | 24.0 | 83% |
| B | 30.0 | 67% |
| C | 32.0 | 63% |
| D | 20.5 | 98% |
| E | 28.5 | 70% |
| F | 25.0 | 80% |
| G | 33.0 | 61% |
| H | 20.4 | 98% |
| I | 26.0 | 77% |
| J | 30.0 | 67% |
| K | 20.4 | 98% |
| L | 40.0 | 50% |

Table 1. Process Rates and Utilization

## Illustration: The 12-Workstation Factory

For purposes of illustration, consider an exceptionally simple factory consisting of just 12 workstations wherein:

- The facility services a single product, flowing through the factory at a constant rate of 20 jobs per day.
- There is zero transit time between workstations, no rework and no reentrancy.

This factory is depicted in Figure 1. Each ellipse represents a workstation and each rectangle within an ellipse is a machine. Thus, in WS-A (i.e., workstation A) there are six machines. ***If we believe that simulation delivers accurate predictions of fab performance, then it should certainly provide accurate predictions of the performance of this tiny facility.***

Table 1 lists a portion of the data for this factory. As may be seen, it contains three constraints (workstations *D, H* and *K* – each with utilizations of 98 percent). [Readers who wish to examine the complete data set, as well as actually "run this factory" via a queuing model, may do so at www.mhprofessional.com/ignizio.]

Assume we wish to predict average job cycle time (a particularly important measure). Since this factory is so small and simple, a queuing model (e.g., the one referred to in the URL previously cited) may be used to predict cycle time *at steady state*. The result for this facility is ***90.42 days***. Shouldn't we then expect a detailed simulation model of the same factory to reach essentially the same results if run for a "sufficient" amount of simulated time?

Since simulation models of semiconductor fabs are run for one or two years of simulated time, it would follow that, *if conventional wisdom is indeed valid*, this should be more than enough for our exceedingly simple 12-workstation factory to reach its steady state. To determine this, a detailed discrete event simulation model of the 12-workstation factory was constructed using the ExtendSim® simulation platform.

## Simulation Plots

The plot of Figure 2 provides a small, but representative sample of the numerous runs made. The horizontal axis represents simulated days (from 1 to 730 days) and the vertical axis is the cycle time in days. The predicted cycle time ***after two simulated years*** ranges from 35 to 64 days – ***nowhere near the true steady state value of 90.42 days***. Stated another way, even after two years of simulated time, the factory has yet to reach steady state (and, in fact, will not do so even after ***10*** *simulated years*).

The primary reason for the poor prediction of the 12-workstation cycle time may be summed up in one word: ***variability***. The impact of variability is further amplified via the high level of utilization of the three constraints. The important point, however, is that these outcomes are a result of the degree and types of variability encountered in ***real-world*** fabs and factories – ***as opposed to the more modest levels of variability inserted into the simulation models so often employed in the manufacturing sector***.

To further investigate this point, consider the same 12-workstation model wherein

Figure 2. Cycle Time Over 2 Years of Simulated Time – ***Using Actual, Measured Factory CoVs***

the *only* changes are made to the variability about factory starts and effective process times. More specifically, the coefficients of variability (CoVs) have been changed to unity – the values most typically employed in factory simulation models. Of course, if we reduce factory CoVs (e.g., variability of factory starts and variability of effective processing times), then the steady state cycle time will also decrease – substantially. A queuing model will, in fact, indicate that the steady state cycle time achieved *simply by reducing variability* will be 9.2 days – a 90 percent reduction in cycle).

Running simulations of this version of the 12-workstation factory results in the plots shown in Figure 3. The simulated time is now *10 years*. Clearly, in this instance the factory does reach its steady state. In fact, it reaches a steady state cycle time of between roughly nine and 9.5 days – but not until roughly 1,500 simulated days (about four years) of simulation!

## Interpretation and Conclusions

The results achieved by reducing factory variability, either in a real or simulated fab, reveal three extremely important points:

- Substantial reductions in the cycle time of real-world fabs may be achieved through the reduction of sources of factory variability – an approach that is most often far less expensive and time-consuming than via the introduction of new machines or personnel (as is most typically done) to reduce the utilization of constraint workstations.
- Factory simulation models that fail to include the ***actual*** variability inherent in the ***actual*** factory invariably overestimate the performance of the fab being simulated (i.e., overestimate the factory's velocity and capacity).
- Of the numerous factory simulation models we have been privy to, rarely if ever was the true level of facility variability employed. Instead, the variability values employed were much less than that measured in the actual factory.

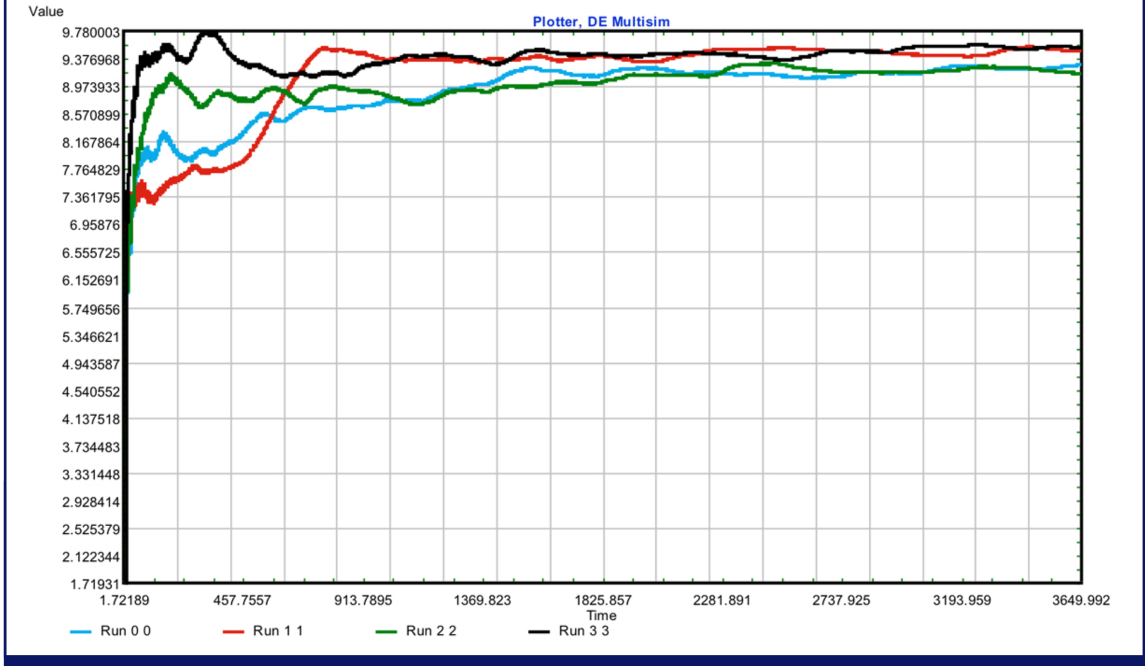


Figure 3. Cycle Time Over 10 Years of Simulated Time – ***With CoVs reduced to 1.0***

This returns us to the original thesis of this paper; i.e., the validity of any prediction depends – in large part – on *knowing what we don't know*. We simply should not expect to develop reliable, accurate predictions of fab performance if we do not know:

- the actual degree and extent of variability within the actual, real-world fab;
- or appreciate the specific manner in which variability impacts fab performance; particularly, such sources of variability as job interarrivals at a given workstation, variability about machine downtimes, variability about the effective process rates of machines, and the impact of clustering fab starts and preventive maintenance events.

Most firms (at least of which we are aware) do not even collect the data pertaining to the above sources of variability. Instead, classical probability distributions are employed along with textbook values of probability distributions in their simulation or queuing models. As just one example, a typical fab simulation will employ coefficients of variability (the ratio of standard deviation to the mean) on the order of 1.0 or even less. When, however, these sources of variability are accurately measured in real-world fabs and factories, we often see CoV values as high as 8.0 (and sometimes more).

The variability values (CoVs) for the simple 12-workstation model listed previously are not atypical – nor do the results obtained for that model differ that much from the costly, time-consuming simulation models of semiconductor or PV fabs. We have, in fact, collected the data necessary to determine the coefficients of variability within real-world facilities, including, most recently, those observed in a 300 mm semiconductor fab. Not surprisingly, ***the results obtained via simulation when the actual values of variability were used differed substantially from those achieved via the use of the far more modest values typically employed in fab simulation models.***

Returning once again to the theme of this paper, far too many firms do not appear to know what they do not know. What they do not know is all the sources, and their true values, of variability within a fab. Consequently, performance predictions and predictability are too often but an illusion – despite the amount of time and effort devoted to their simulation models.

## References


1 Ignizio, James P., "Optimizing Factory Performance," McGraw-Hill, 2009

2 McGraw-Hill website: www.mhprofessional.com/Ignizio


## About the Authors

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James P. Ignizio is founder and CEO of The Institute for Resource Management. He is the author of 10 books and more than 350 publications. Dr. Ignizio's short courses in manufacturing science, artificial intelligence and applied operations

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research have been attended by several thousand industrial and governmental personnel over the past 30 years.

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Moshe Preil is commended for his excellent summary article in this section, which asserts, "Throughout the history of microlithography, advances in resist chemistry have been as important as advances in exposure tool technology. To maintain this impressive history of technology enablement, we must be sure we are aiming at the right targets ahead of us, not behind us."

In 2009, the International Technology Roadmap for Semiconductors (ITRS) Lithography International Technology Working Group (Litho ITWG) identified the following among its most difficult challenges: <2.8 nm (3σ) overlay; high sensitivity resists, with <22 nm ½ pitch resolution; low defectivity, i.e., <0.01 10 nm particles/cm²; and <1.3 nm (3σ) line width roughness. Based on these requirements, that year's Exposure Tool Potential Solutions roadmap noted the Lithography ITWG's consensus that there exists "no proven optical solution beyond the 22 nm node." However, this Working Group identified directed self-assembly as a lower-probability potential patterning solution for the 16 nm DRAM ½ pitch node and beyond.

In the 2011 ITRS revision, the Litho ITWG's 2018 projected requirements specify 12-16 nm ½ pitch resolution and a more relaxed overlay requirement of <3.2 nm (3σ). The corresponding 2011 potential tool solutions table now conveys a more evolutionary projection of future lithographic technologies. However, with the continued exponential growth of fab, exposure tool, and mask costs, a key question remains as to whether the current nanoelectronics fabrication paradigm is sustainable.

This article provides compelling indirect justification regarding the strategic need for new families patterning materials and processes that augment and extend current methods. The success of extensible and manufacturable nanopatterning depends on approaches that circumvent or compensate for current lithographic limitations. The path forward must navigate through the apparent trade-off in conventional top-down lithography between three critical and interdependent chemically amplified resist performance factors: resolution, throughput and line edge roughness.



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## Proven Solutions Through Evolution

Nikon Corporation has been one of the world's leading optical companies for more than 90 years. Nikon developed the world's first production-worthy step-and-repeat photolithography tool in 1980. Since then, over half of all integrated circuits printed have been manufactured on Nikon steppers and scanners.

Nikon has a long-established precedent of leading the industry through innovation and the continuous evolution of our proven lithography solutions, providing photolithography systems spanning the range of resolutions required by today's IC manufacturers. From high-throughput i-line steppers to advanced immersion ArF scanners for 22 nm applications and beyond, Nikon delivers exceptional performance with the lowest cost of ownership, and the most comprehensive customer support of any manufacturer.

In 2007, Nikon shipped the industry's first 1.30 NA immersion scanner, the NSR-S610C, for 45 nm half-pitch production. Later that year, Nikon also introduced the NSR-S310F and NSR-S210D non-immersion scanners. These systems were evolutions of the S610C immersion platform that incorporated Tandem Stage technology to provide optimal performance and cost of ownership for dry lithography applications.

Then, in 2009, to meet the stringent requirements for 32 nm double patterning and provide extendibility to next generation applications, Nikon introduced the NSR-S620D immersion scanner, which is based on the innovative *Streamlign* platform. This was followed in 2011 by the NSR-S320F, an evolutionary *Streamlign* platform-based system designed to deliver exceptional performance and productivity for the most critical dry ArF applications. Most recently, Nikon began shipping the NSR-S621D immersion scanner. This latest evolution of the proven *Streamlign* platform fully satisfies the aggressive overlay and throughput requirements of high-volume immersion double patterning applications at 22 nm and beyond.

Next generation lithography techniques continue to evolve, but IC makers need solutions today that will keep them on their aggressive technology roadmaps. With a history of innovation and evolutionary lithography solutions, Nikon will be there to ensure you maintain your production timelines.

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LITHOGRAPHY LANDSCAPE

# Optimum Dose for EUV: Technical vs. Economic Drivers

**Moshe Preil**
GLOBALFOUNDRIES

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## Introduction

Pre-production EUV exposure tools have now been delivered to the first customers with target insertion points below 20 nm. However, resists capable of producing usable patterns at these resolution levels remain to be proven. Meeting the simultaneous requirements of resolution, sensitivity and line edge roughness (LER) remains a serious challenge.[1] Compounding the difficulty of this task are the extreme sensitivity requirements being driven by the tool suppliers, in large part due to low source power and the overriding need to maintain high throughput. Putting the need for speed first leads to serious compromises in resist chemistry and performance. In this paper, we will model the driving forces behind the throughput targets and the resulting dose requirements. We will then show how the resulting low doses lead to shot noise problems and a resulting penalty in resist performance.

## Economic Drivers: How Cost per Function Drives Throughput Requirements

The semiconductor industry has enjoyed decades of unparalleled success by following one simple metric: The cost per function must always go down over time. In fact, this is the essence of Moore's Law – not only must lithography drive feature size shrinks, it must simultaneously improve productivity and lower cost. Figure 1 shows a graph of leading-edge exposure tool cost over time. The exponential growth has been remarkably constant; tool cost has doubled every 4.2 years for the past three decades. Fortunately, the tools themselves have become more productive at an even faster rate; the rate of productivity doubling is roughly once every three years. The resulting capital cost per megapixel has therefore declined steadily over time (Figure 2), reaching roughly 10 cents per megapixel today.

Any new tool must run at a sufficiently high throughput to keep the cost per function on a downward trend. For tools with low power sources, this drives a requirement for very-low-dose resists. Figure 3 shows the tool cost per million pixels for EUV systems at various projected throughputs. It is clear that EUV will not cost less than \$0.10/Mpixel unless throughput exceeds 100 WPH. Given the limited source power, this drives the need for very fast resists. Published EUV roadmaps call for doses of 10-15 mJ/cm².

## Early DUV Resists: Lessons We Should Learn

Early DUV tools, based on Hg arc lamps or very early excimer lasers, operated under similar constraints. Due to limited source power, early DUV resists were targeted in the 1-5 mJ/cm² range, orders of magnitude less than the existing g- and i-line resists. This led to the invention of acid catalyzed resists, which are now the standard for high-performance production resists, but at the time they were both novel and incredibly unstable.[2] Heroic efforts by Ito, Willson, Frechet and colleagues resulted in formulations with sensitivities below 1 mJ/cm² but with virtually no stability for processing. These systems suffered from excessive sensitivity to poisoning by airborne molecules (amines), making them unusable for cost-effective manufacturing.

By 1991, the next-generation excimer lasers with power output of around 4 watts were available with greatly enhanced component lifetimes, producing on the order of 100 mW/cm² at the wafer plane. The first truly production-worthy DUV resist, APEX-E, was sampled by IBM to other users in 1993. Operating in the 10-40 mJ/cm² range depending on PEB temperature, APEX-E was still subject to poisoning by environmental contaminants, but at a controllable level. This resist and its successors – notably IBM ESCAP – took advantage of the higher dose to add base quenchers, enabling higher contrast and greater resistance to

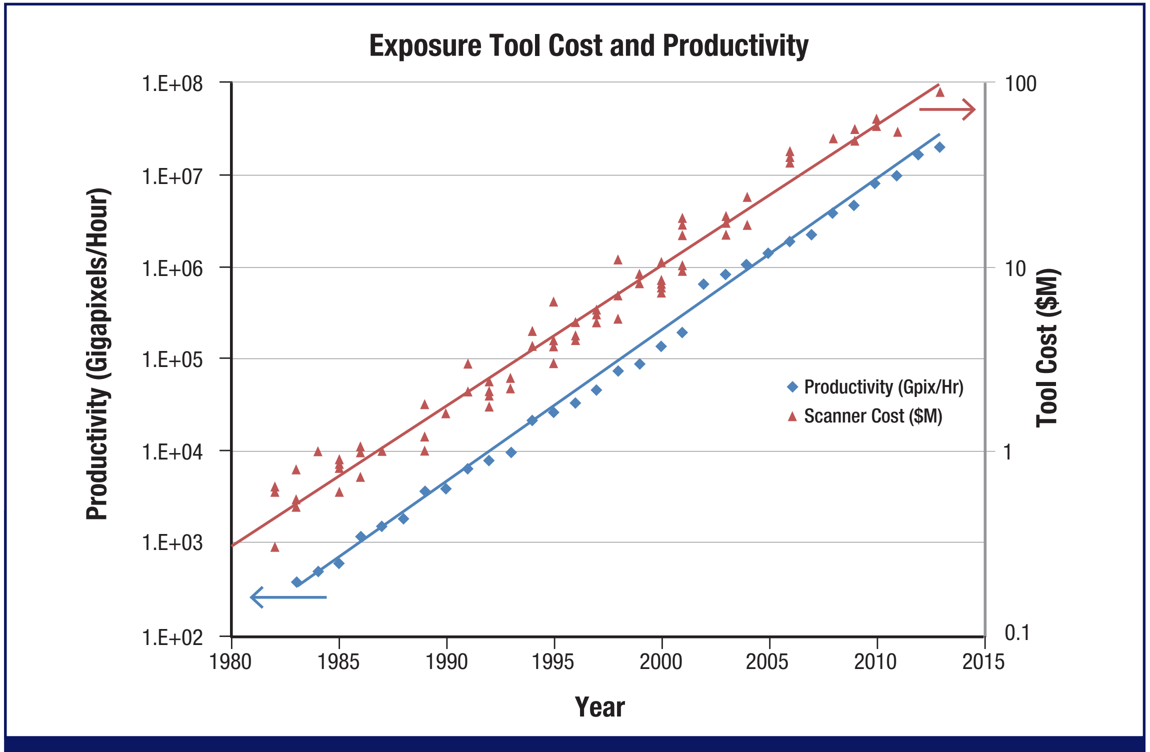


Figure 1. Exposure tool cost and productivity vs. year of introduction. Data from multiple suppliers and users. Exponential fit shows cost doubling every 4.2 ± 0.2 years while productivity doubles every 3 years.

contamination, and the high-dose/lower-PEB combinations led to more stable processes.

Fifteen years after the initial attempts at ultra-sensitive resists, systems operating at 20-50 times higher doses finally made DUV viable for production. Research into a huge number of dead-end chemical formulations pursued in the interim filled many volumes of conference proceedings but never resulted in production-worthy resists.

## EUV Resist: Implications of Shot Noise on Dose

The exposure process consists of a series of stochastic processes: the exposure itself, which consists of a finite number of photons per unit volume; the probability that any given photon will be absorbed and generate a photoelectron to initiate a cascade or lower-energy electrons, which in turn have a probability of being captured by a PAG molecule to generate photoacids; the diffusion and catalytic amplification of the photoacid molecules; and the development process. Numerous papers have studied different aspects of the stochastic chain in detail.[3,4] These complex models require a wide range of physical and chemical inputs and are well beyond the scope of this paper. For our purposes, we will focus on the first step in the chain; namely, the shot noise inherent in low-dose exposures with high-energy photons.

Due to the limited power of 13.5 nm sources and the low transmission of the reflective optical chain, EUV power at the wafer plane will be seriously limited even if the sources eventually meet the roadmap targets of 100-500 watts. To specify a cost-effective throughput target of 100 or more wafers per hour, the target dose commonly mentioned is 10-15 mJ/cm$^2$. Since the energy per EUV photon is over 14 times greater than for 193 nm, this low dose results in photon numbers where shot noise can be significant.

To compute the shot noise, we need to determine an effective area over which to integrate the photon flux. The area of interest is actually much smaller than the effective pixel size (minimum resolution squared). Even when exposing a fairly large area of many tens of nanometers, the large number of photons striking the middle of the structure does not play any role in the development of the resist profile at the edge of the pattern. A better approximation of the region of interest is to look only at those photons that will play a role in defining the developed resist edge, a region defined by the resist blur.[5] The blur region is strongly coupled to resolution and is generally on the order of one-half of the minimum feature.[6] We will refer to this interaction range as the ambit. Increasing the blur will increase the number of photons per unit area at the resist edge, reducing LER, but at the cost of resolution.

Figure 4 shows the shot noise ratio computed for different doses and ambits. For a Poisson distribution, the variance equals the mean, so the noise ratio is just (√N)/N, where N is the number of photons in the ambit. Since the number of photons goes as the square of the ambit, the ratio goes as 1/(ambit); the number of photons is linear with dose, so the ratio goes as 1(√dose). Note that this is a 1-sigma value. To estimate the full width of the noise distribution, we should really consider 3 sigma as the parameter of interest.

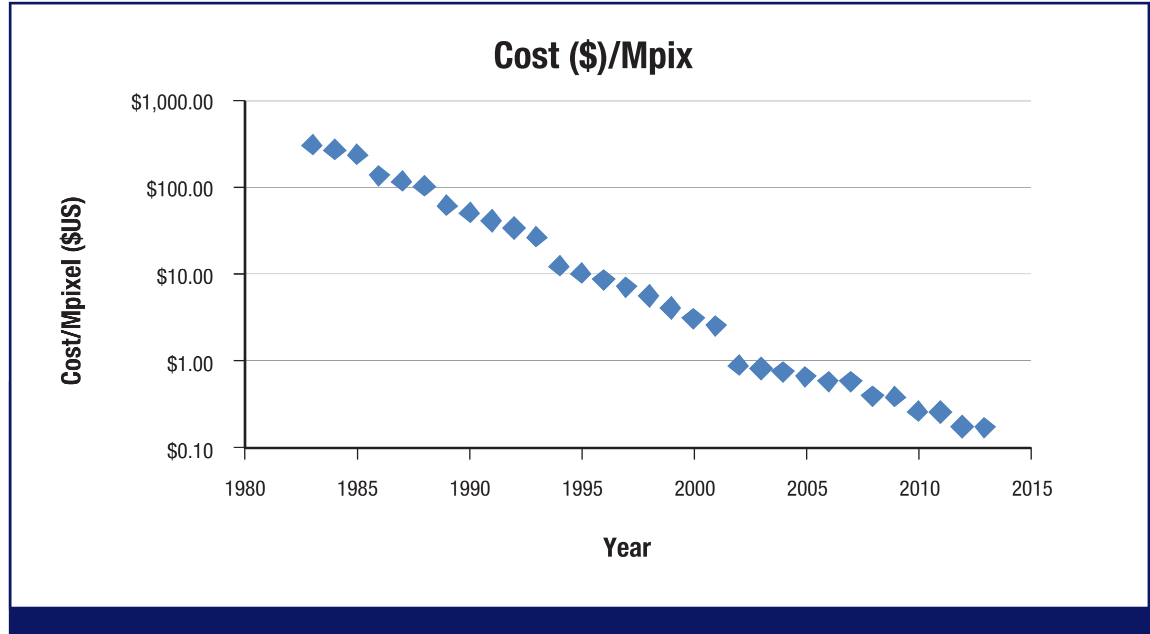


Figure 2. Cost per megapixel over time. Discontinuous jumps indicate wafer size changes. Cost declines over time as productivity outpaces rate of tool cost growth.

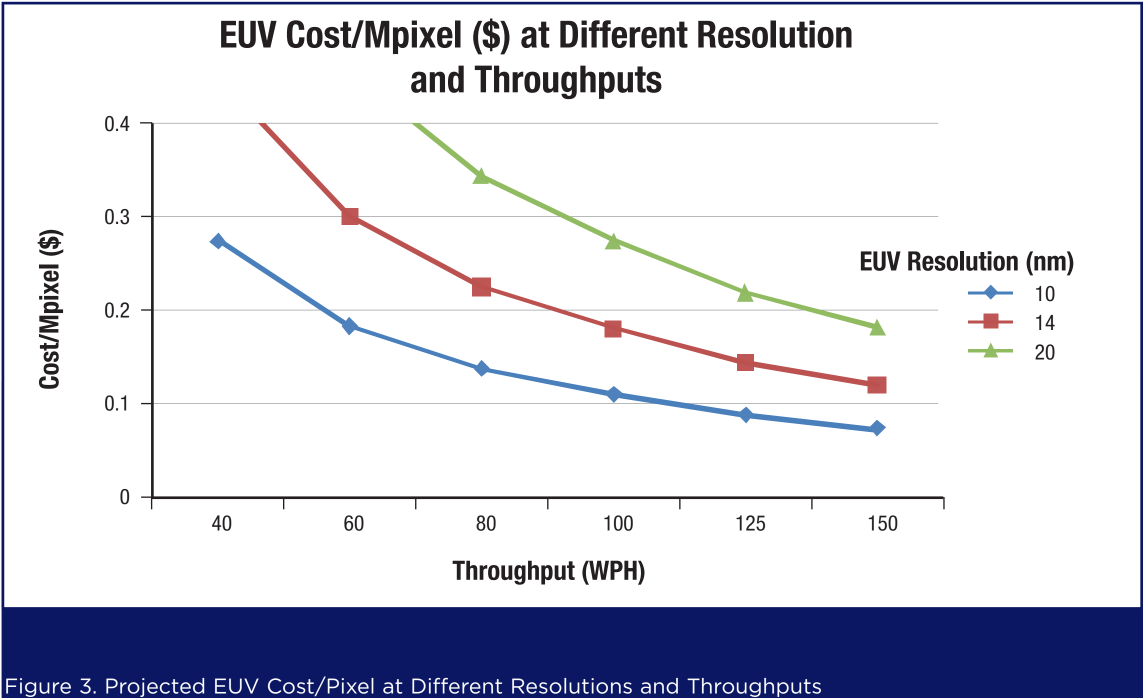


Figure 3. Projected EUV Cost/Pixel at Different Resolutions and Throughputs

For a 10 nm ambit and a dose of 15 mJ/cm², each 100 nm square unit area would receive a nominal exposure of just over 1,000 photons; 3*noise ratio is over 9 percent, rendering 10 percent total CD control problematic. To keep 3*noise ratio below 5 percent would require a dose of at least 50 mJ/cm². As the need for better resolution drives the blur down to the 5 nm level, 3*noise ratio of even 7.5 percent would require a dose of 100 mJ/cm². This calculation simply counts photons. In a real resist system, not all of the photons are absorbed in reactions that generate useful photoelectrons, making the shot noise in the resist even worse. It is clearly advantageous to have higher quantum efficiency and PAG loading to generate more photoacids and increase the chances of a single photon setting off a lithographically useful reaction, but amplification cannot undo the initial photon noise; it can only keep it from getting worse in the ensuing stochastic processes.

Photon noise does not necessarily translate directly into LER. Diffusion and other averaging processes may help reduce LER, but at the cost of longer-range CD uniformity, MEEF, resolution or exposure latitude.[7,8] For example, if the development process smoothed the line edges, the LER would improve but the location of the edge would vary. The relationship between CD uncertainty and LER can be summarized as:[9]

$$\sigma_{CD} \sim \log(L_c) \times \sigma_{LER} \quad (1)$$

Filtering can reduce $\sigma_{LER}$ but it also increases the correlation length $L_c$ and therefore the longer-range CD uniformity error. As with any system with a noisy input, filtering is possible but at the expense of fidelity.

The current champion resists have roughly 20 nm resolution and 3 nm LER at doses in the range of 10-20 mJ/cm²; resolution has been pushed down to 16 nm but only by increasing the dose over 30 mJ/ cm². These LER values are at least 50 percent worse than even the basic shot-noise model would suggest. Clearly, current resists are not shot-noise limited. Other stochastic processes, including the impact of out-of-band radiation, must also play a major role. As these other variations are reduced by increasing resist absorption, higher PAG loading and other means, the photon shot-noise limit will remain. Other, more mathematically rigorous studies have gone into far greater detail of the exact impact of shot noise on LER.[3-5] To date, there has been no definitive conclusion on the ultimate limit of LER vs. dose and the trade-off between LER, CDU and exposure latitude through modifications of the resist chemistry. The general scaling of photons vs. blur suggest that the limit will not be achieved without a significant increase in resist dose.

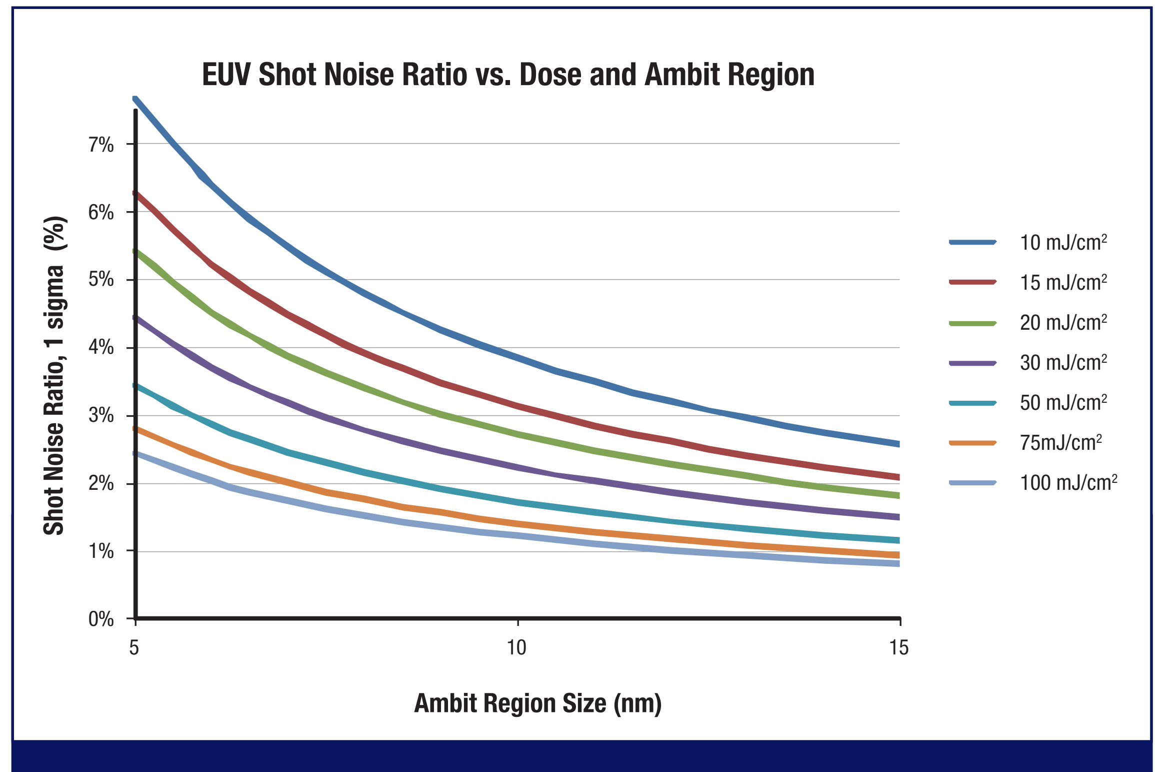


Figure 4. Shot Noise Ratio for 13.5 nm Photons as a Function of Dose and Effective Interaction Region Within the resist (ambit), Which Should Typically Be on the Order of 1/2 to 1/3 of the Minimum CD

## Conclusions

The doses currently being targeted for EUV based on throughput and cost considerations appear to be too low to achieve acceptable LER and overall CD performance. The shot noise due to the low number of photons is not yet the limiting factor in resist performance, but it sets a clear floor.

We have seen in our discussion of early DUV resists how unrealistic dose targets imposed by source limitations led to extensive delays in achieving production-quality materials. As we look ahead at the sub-20 nm nodes, we do not have the luxury of chasing the wrong target for too much longer. If there is a path to a better resist that breaks away from current formulations but at the cost of higher dose, history and physics suggest that we should not reject these ideas out of hand simply because they are too slow.

The other lesson we have learned time and again in this industry is that we always need to aim ahead of the short-term target to develop successful processes. Resists in development today should ideally be targeting the 14 nm or even 10 nm nodes. Since shot noise only gets worse as we try to print smaller features, resist development should look at the real dose requirements of the next node, not the past nodes. Throughout the history of microlithography, advances in resist chemistry have been as important as advances in exposure tool technology.[10] To maintain this impressive history of technology enablement, we must be sure we are aiming at the right targets ahead of us, not behind us.

## Acknowledgments

This paper is an abridged version of a paper presented at the SPIE Advanced Lithography Symposium in February 2012. The themes presented in this paper have evolved over time and benefited greatly from discussions with the members of the Strategic Lithography Technology group at GLOBALFOUNDRIES, especially Tom Wallow and Keith Standiford, as well as Chris Mack, Mark Neisser and others.

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Moshe Preil is the manager of Emerging Lithography and Tools, part of the Strategic Lithography Technology department at GLOBALFOUNDRIES. He has over 25 years of experience in both the fab and supplier sides of the industry, working in various lithography, process control and yield management positions. Previously at AMD, Dr. Preil was involved in the early development of deep-UV technology. He earned his Ph.D. in physics from the University of Pennsylvania, working on optical and electron spectroscopies of novel graphite-based compounds. Dr. Preil has published numerous journal papers and has been issued 10 U.S. patents. ■

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# FRONT END OF LINE

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**Didier Louis**
Corporate and International Communication Manager; CEA-Leti

Low-power consumer electronics require fast circuit operation for demanding applications with complex functionality and low-power consumption for long battery life.

In the first paper in this section, Christine Gottschalk of ASTeX reports on the importance of the quality of ultrapure water, and more particularly, on the level of dissolved oxygen for controlling silicon oxide formation on the silicon wafer surface at the gate-stack level, for example.

The point of use of UPW or water chemical mixtures is the main point of control, additionally with permeation protection of tubing material to assume low oxygen concentration and contamination during the wet processes.

Experimental results by using an adapted detoxification unit system and good tubing-type materials have been given. Oxygen concentration below 1 ppb has been reached.

In the second paper in this section, researchers from IBM report the use of fully depleted silicon on insulator (FDSOI) structures as the main candidates for further scaling MOS devices (below 20 nm) and for addressing the performance needed for advanced technology nodes. Simply described, the FDSOI device structure is planar, so the devices are relatively simple to build and the measurement tools and techniques, as well as elementary process steps, can be used without modifications for planar FDSOI devices. They also have many attractive features as an easy path to realize multiple threshold transistors.

Attention must be paid toward Si film thickness uniformity, as it can cause Vt variation in thin body transistors. Thickness variation must be controlled and maintained below +/- 0.5 nm.

All the results reported indicate very good management of variability, scalability and drivability by using planar FDSOI technology.

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# The Challenge to Reduce Dissolved Oxygen for Advanced Processing

**Christiane Gottschalk**
ASTeX GmbH, a subsidiary of MKS Instruments

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## Abstract

Controlling oxide formation on the wafer surface is one of the reasons for reducing residual dissolved oxygen (DO) levels in ultra-pure water as well as in dilute hydrogen fluoride. As the feature size in semiconductor manufacturing continues to decrease, the quality of water and the dissolved oxygen content are becoming increasingly more critical. For certain processes, a point-of-use deoxification step has become necessary. Challenges to decrease and maintain the low level of $O_2$ will be discussed.

## Introduction

As semiconductor processing changes due to smaller dimensions and new architectures, new fabrication strategies are emerging. These include novel approaches such as gate-last versus standard gate-first integration and new materials such as high-k and metal gates. The industry has focused on controlling oxygen in back end of line as well as recently in front end of line applications, to inhibit, for example, galvanic corrosion or to ensure stable hydrophobic surfaces. Many presentations during the last ECS conference in Boston covered this topic, focusing on a common sense approach of necessary control and reduction of the level of dissolved oxygen.[1-4]

Control of the oxygen concentration in ultra-pure water (UPW) thus appears as a new critical process requirement at the gate-stack level, during epitaxial growth steps and during the contact cleaning step for improved performance. In diluted hydrogen fluoride, for example, control of the oxygen content is mandatory, e.g., for stable hydrogen-terminated surfaces.

UPW in new semiconductor fabs is typically deoxified to a level below 5 ppb. From the point of delivery (POD: outlet of final filtration in UPW plant,[5]) to the point of use (POU: inlet of wet bench bath, spray nozzle or connection point to piping that is used for other chemicals,[5]), however, oxygen diffuses back into the water. As a result, for critical processes, a POU deoxification of UPW and chemical mixtures of reducing agents becomes necessary. A variety of challenges, which will be discussed below, must be considered to achieve the required low dissolved oxygen concentration level.

## Experimental and Theoretical Approach

Deoxification experiments were done with a system consisting of two contactors in serial-using nitrogen ($N_2$) as a purging gas in a counter-current mode (Figure 1). A pump before the liquid outlet was used to increase the pressure to the necessary level.

To predict the expected oxygen level behind the unit, a model was created that covers desorption as well as permeation (for details see [4]), as these two effects in particular must be considered.

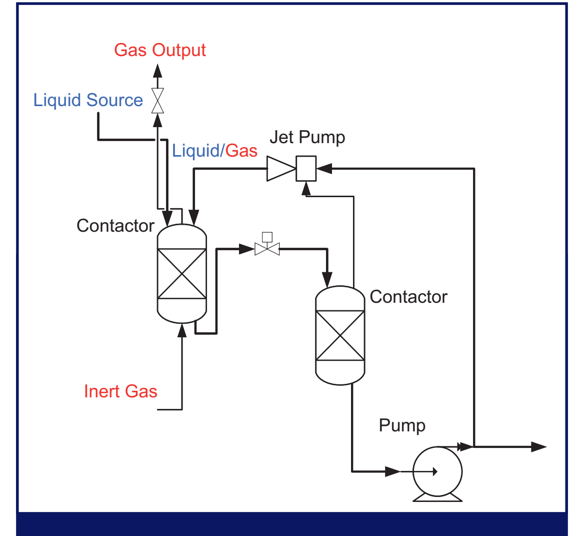


Figure 1. Deoxification Setup (patent applied for)

### Desorption

The outlet oxygen concentration achieved in liquid is highly dependent on the oxygen content of the inert purging gas: The higher the grade, the cleaner the purging gas and the lower the outgoing concentration. The saturation concentration, as a function of the oxygen content in $N_2$, marks the physical/chemical limit for this method (Table 1).

### Permeation

The permeation of gases through polymers is a well-known effect.[7] Permeation involves the adsorption of the gas on the tubing surface, the diffusion through the tubing material, desorption and finally absorption into the liquid. The oxygen permeation through tubes for liquids depends directly on the tubing type, as can be seen in Table 2.

Perfluoralkoxy (PFA) turned out to be the "worst" material for oxygen permeation, while polyvinylidene fluoride (PVDF) showed the best results. In the case of deoxified mixtures with HF, PVDF is unsuitable due to the high permeation rate of HF (HF permeation

| Grade | Maximum $O_2$ Gas Content[6] | $O_2$ Saturation Concentration |
|---|---|---|
| 4.6 | 5 ppm | 0.22 ppb |
| 5 | 3 ppm | 0.13 ppb |
| 6 | 0.5 ppm | 0.02 ppb |
| 7 | 0.03 ppm | 0.001 ppb |

Table 1. Purging Gas $N_2$ at Different Grades, its Maximum Specified Oxygen Content and the Resulting Saturation Concentration of Oxygen in Water at 20 °C and Ambient Pressure

coefficient: 6.19 $10^{-1}$ $cm^4$ $m^{-2}$ $min^{-1}$ $bar^{-1}$ [9]). This leads back to PFA tubing material.

The verification of the model was done by comparing calculated and measured data. It was shown that with the chosen setup, oxygen concentration below 1 ppb was attainable and the experimental data were in good alignment with the calculated values (see Figure 2).

## The Practice

With the help of the model, the dimension and the configuration of a necessary deoxification unit can be calculated and – important for the process – the increase of the oxygen level at the POU can be predicted.

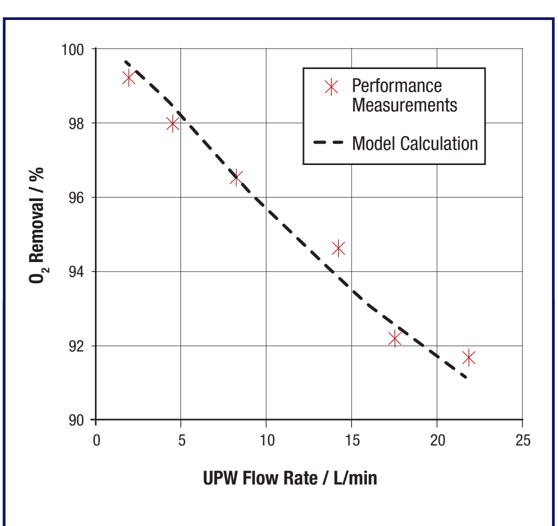


Figure 2. Comparison of Model Calculation vs. Experimental Data

As an example, Figure 3 shows a setup for diluted HF including chemical mixing, buffer tank, recirculation loop and deoxification system with double-contained flushed tubing to the POU. The oxygen concentration was calculated after different steps and for the complete setup, assuming that HF has a similar oxygen saturation point as water and that the acid is $O_2$ saturated. The mixture of HF to UPW was 1 to 100, and the tubing length behind the deoxification system was 10 m.

It can be seen that with the help of the deoxification unit, a DO of less than 1 ppb can be achieved. Without the double containment between the deoxification unit and POU, the DO will increase by a factor of greater than 60.

Ideally, at least the final deoxification step for chemicals and UPW should be integrated or in close proximity to the tool. A mini-environment with reduced oxygen content around the connecting tubing will allow longer distance. Inside the tool, the process environment should be enclosed with a controlled low oxygen level.

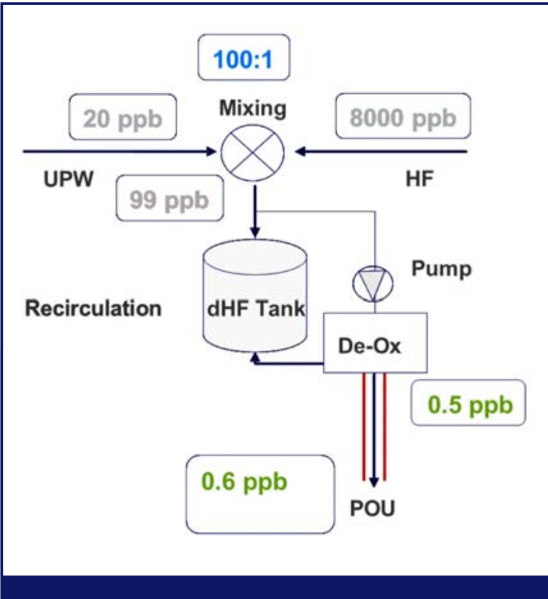


Figure 3. Setup With Calculated Oxygen Content With $N_2$ Flushed Double-Contained Tubing

| Tubing Material | PFA | FEP | PE | PP | PVDF |
|---|---|---|---|---|---|
| $O_2$ Permeation Coefficient[8] | 2.42 $10^{-2}$ | 1.67 $10^{-2}$ | 7.86 $10^{-3}$ | 3.04 $10^{-3}$ | 2.85 $10^{-4}$ |

Table 2. Permeation Coefficient Depending on Tubing Type, $O_2$ at 22 °C [$cm^4$ $m^{-2}$ $min^{-1}$ $bar^{-1}$]

## Summary and Conclusion

POU deoxification is only one of the measures necessary to achieve controlled, low-oxygen concentrations in process fluids. Additional measures must be taken to avoid oxygen contamination of process water. The demand for ultra-low oxygen concentration in UPW and precisely mixed chemicals requires a new approach for deoxification. The permeation of oxygen through the tubes used for liquids in the semiconductor industry is becoming a limiting factor in low-oxygen applications. Thus, only the combination of deoxification units near the tool, together with a permeation protection between the deoxification unit and the POU, can ensure applications with oxygen in the low ppb level.

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Christiane Gottschalk obtained her Ph.D. in the area of chemical engineering in 1996, with the topic "Advanced Oxidation Processes." She joined MKS Instruments – ASTeX Berlin in 1997 and is currently director of Advanced Product Development, responsible for ozone business. ■

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# FDSOI for Next-Generation System on Chip Applications

**Bruce Doris, Kangguo Cheng, Ali Khakifirooz**
IBM Research at Albany NanoTech

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Conventional device scaling is nearing its limits as gate lengths approach physical dimensions of beyond 25 nm. Historically, the transistor size has shrunk while maintaining good electrostatics, which, simply put, is the ability to turn the transistor off. The conventional approach to transistor scaling is to thin the gate dielectric, increase the channel doping, form shallower junctions and reduce the power supply. Unfortunately, these scaling elements have limitations. In fact, the level of channel doping now needed to turn transistors off creates excessive junction leakage and, ironically, increases the tendency for the transistor to be in the "on" state when it is intended to be in the "off" state. Fully depleted devices rely on thin Si channels to control the electrostatics and enable the transistor to be turned off even at very small gate-length dimensions.

FDSOI has many attractive features. Design migration from conventional architecture layouts from previous nodes to FDSOI architecture layouts is straightforward, since the FDSOI device structure is planar. The history effect observed in partially depleted SOI is not present in FDSOI.[1] Therefore, there is absolutely no need for circuit designers to consider history effects when designing with FDSOI transistors. In addition, FDSOI offers an easy path to realize multiple threshold voltage transistors that are needed for all practical circuit applications. FDSOI architecture features an independent back gate that can be used to intentionally and precisely adjust threshold voltages. Back-gate implants can be used to adjust the threshold voltage by 30-70 mV, depending on buried oxide (BOX) thickness. N-type doping in the back gate for pFETs enables a Vt shift relative to pFETs with p-type doping in the back gate. A similar Vt shift is achieved for nFETs with p-type doping relative to nFETs with n-type doping for the back gate. Additionally, back-gate biasing is another way to intentionally and precisely control the threshold voltage for FDSOI devices. This is a particularly important feature, since the multi-Vt approach for FDSOI enables threshold voltage adjustment completely and entirely without the use of channel implants. The fact that no channel implants are needed to adjust the threshold voltage results in superior low-voltage operation without the need for complex circuit-assist elements.

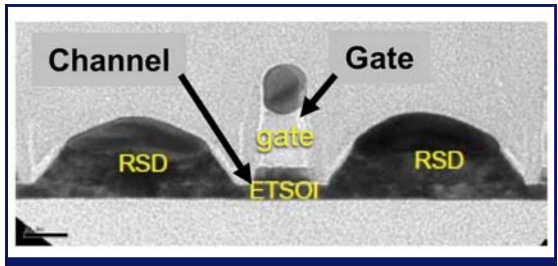


Figure 1. FDSOI Transistor With 25 nm Gate Length, 6 nm Channel Thickness and Raised-Source Drain

The planar FDSOI device is relatively simple to build, and most of the measurement tools and techniques as well as process tools and processes used for conventional devices can be used without modification for the planar FDSOI device. A cross section of an FDSOI transistor is shown in Figure 1.

Channel thickness uniformity requirements are especially demanding for planar FDSOI devices. Si thickness variations cause Vt variations in thin body transistors.[2] Figure 2 shows the dependence of Vt variation on silicon thickness uniformity. Vt variation in excess of about 25 mV is not acceptable. Therefore, silicon thickness variation must be controlled and maintained below +/- 0.5 nm.

Fortunately, the Si film thickness is straightforward to measure and optimize since it is planar. It has recently been shown that the silicon thickness can be controlled in a manufacturing process environment to well within the tolerance needed for planar FDSOI.[3] Figure 3 shows the progress that has been made in realizing appropriate starting wafers for FDSOI applications.

In conventional devices, Vt is modulated by halo dose. However, halo implants increase electric fields as well as coulomb

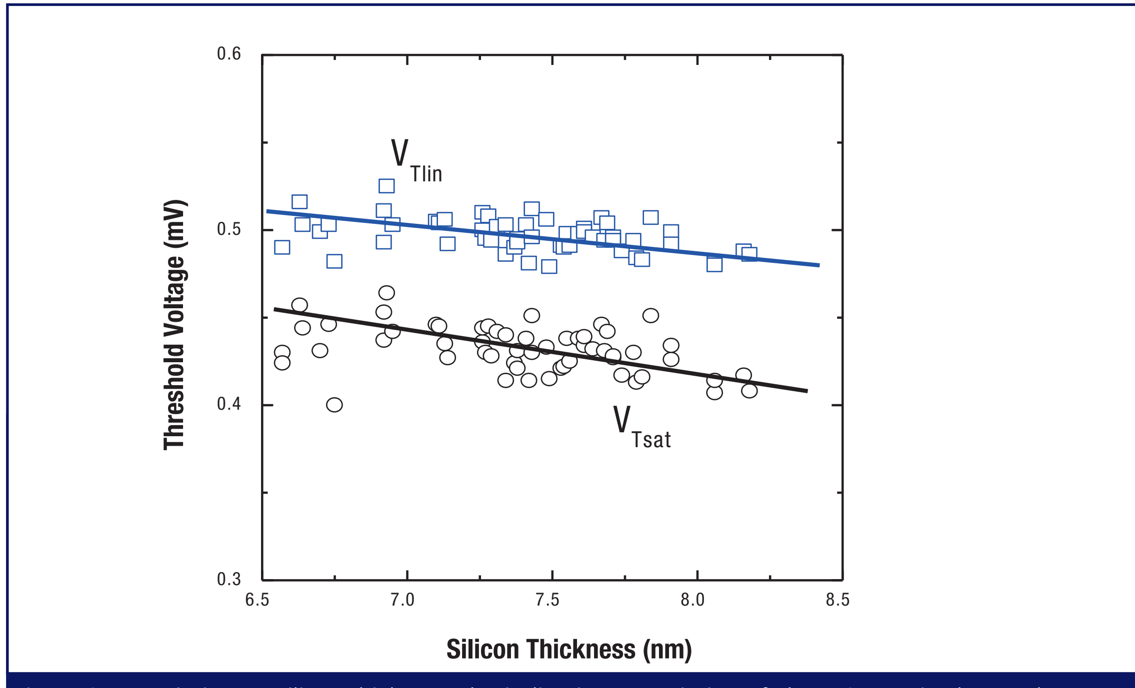


Figure 2. Vt variation vs. silicon thickness plot indication Vt variation of about 25 mV is observed for 1 nm silicon thickness variation.

scattering, and cause excessive random doping fluctuations. Ideally, the use of channel implants is avoided for FDSOI. Devices with no channel doping operate at lower effective fields where mobility is significantly higher. The undoped channel FDSOI device also enables superior SRAMs because random dopant fluctuations from the halo are eliminated. SOC chip designs require FETs with multiple Vts or "off" current targets ($I_{off}$), although halo is not desired for FDSOI. Therefore a new approach to multi-Vt or multi $I_{off}$ is needed that does not depend on channel doping.

As previously stated, the FDSOI device features an independent back gate. Therefore, $I_{off}$ for planar FDSOI devices can be controlled by using back biasing, as shown in Table 1.[4] Back-gate implants can also change $I_{off}$. The combination of back-gate implants and back-gate bias can cover the $I_{off}$ space needed for SOC. In addition to meeting the requirement for multiple $I_{off}$ targets, it has been shown that planar FDSOI can support all the auxiliary devices needed for SoC applications.[5]

The past several technology generations have relied on mobility enhancement techniques to achieve performance targets. Thus, FDSOI CMOS may require mobility enhancements to meet performance objectives. On the other hand, aggressive gate pitch for next-generation nodes degrade the enhancements from embedded stressors and stressed liners. Mobility enhancement can also be achieved through alternate channel materials and surface orientations. These approaches to mobility enhancement do not degrade with gate pitch and may be needed for future applications. Figure 4 shows that significant mobility improvement can be achieve for thin channel devices through channeling engineering, although integration may be challenging.[6]

| back bias | $I_{on}$ (μA/μm) | $I_{off}$ (nA/μm) | DIBL (mV/V) | SS (mV/dec) | GIDL (pA/μm) |
|---|---|---|---|---|---|
| -2V | 525 | 0.1 | 68 | 90 | 4 |
| -1V | 602 | 0.63 | 68 | 89 | 5 |
| 0V | 682 | 3.69 | 70 | 91 | 7 |
| 1V | 759 | 19.9 | 71 | 91 | 14 |
| 2V | 833 | 126 | 71 | 90 | 20 |

Table 1. Various $I_{off}$ targets can be achieved by adjusting back bias in planar FDSOI devices without degradation to other device parameters.

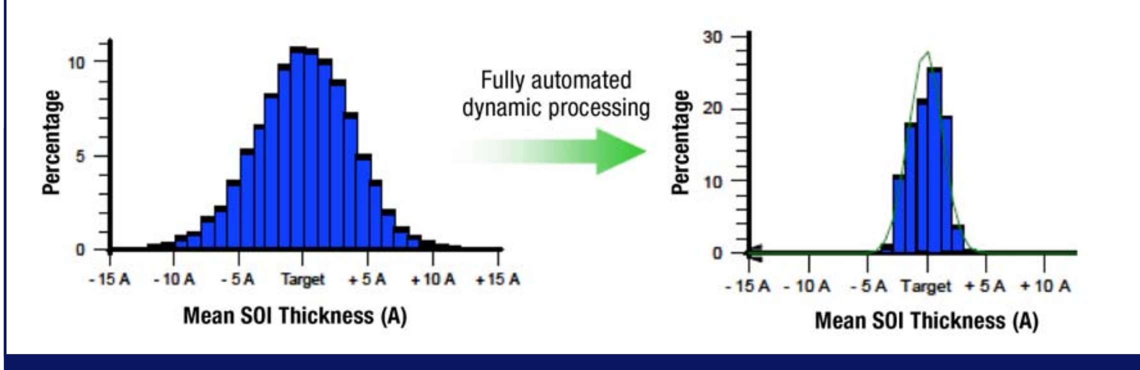


Figure 3. Mean Si thickness variation can be controlled to the tolerance needed for FDSOI applications (+/- 5A).

Today's low-power consumer electronics demand fast circuit operation for applications with complex functionality and also require low power consumption for long battery life. Figure 5 shows that planar FDSOI ring oscillators, a benchmark for circuit performance, at 20 nm node dimensions are dramatically faster even at lower operating voltages compared to a conventional 28 nm node technology.[7]

An enormous investment in tooling and yield learning is needed to implement new transistor architecture in a manufacturing line. Therefore it is extremely important for any new device architecture to be viable for more than one generation of technology. Figure 6 shows that planar FDSOI can be scaled to smaller gate lengths by thinning the channel thickness. Drain-induced barrier lowering (DIBL) is a measure of the ability of the gate to turn the transistor off. The figure shows that by thinning the channel from 6 nm to 3.5 nm, the same DIBL can be achieved at smaller gate length. Another method to scale transistor size for FDSOI devices is by using back bias. Figure 6 shows that the same DIBL can be achieved at significantly smaller gate-lengths by applying a back bias. The back bias required to improve the DIBL depends on the BOX. Lower back-bias voltage is needed for thinner BOX thicknesses. It is important to note that both channel thinning and back biasing to improve DIBL at smaller gate lengths does not degrade performance, as shown in the $I_{on}$ and $I_{eff}$ vs. $I_{off}$ plots that both measure performance. Thus, FDSOI is scalable and therefore could be used for multiple generations.[8]

SOC applications need high drive currents. Circuit speeds are not entirely determined by on-current ($I_{on}$) characteristics.

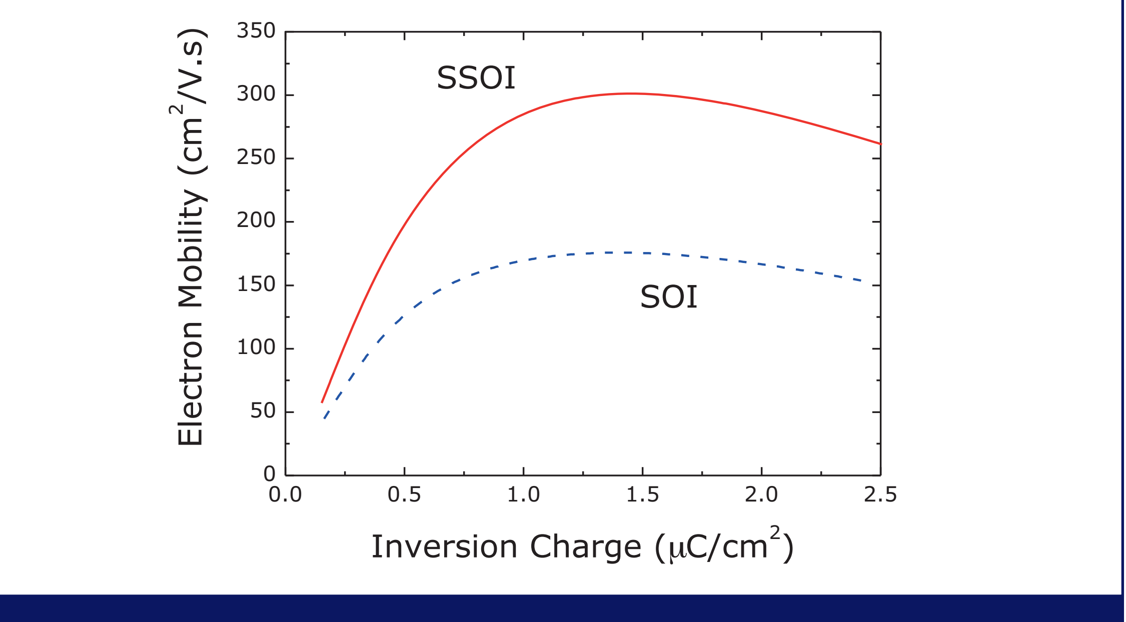


Figure 4. Electron Mobility vs. Inversion Charge Density for SOI and SSDOI Demonstrating Significant Improvement for SSDOI Channels

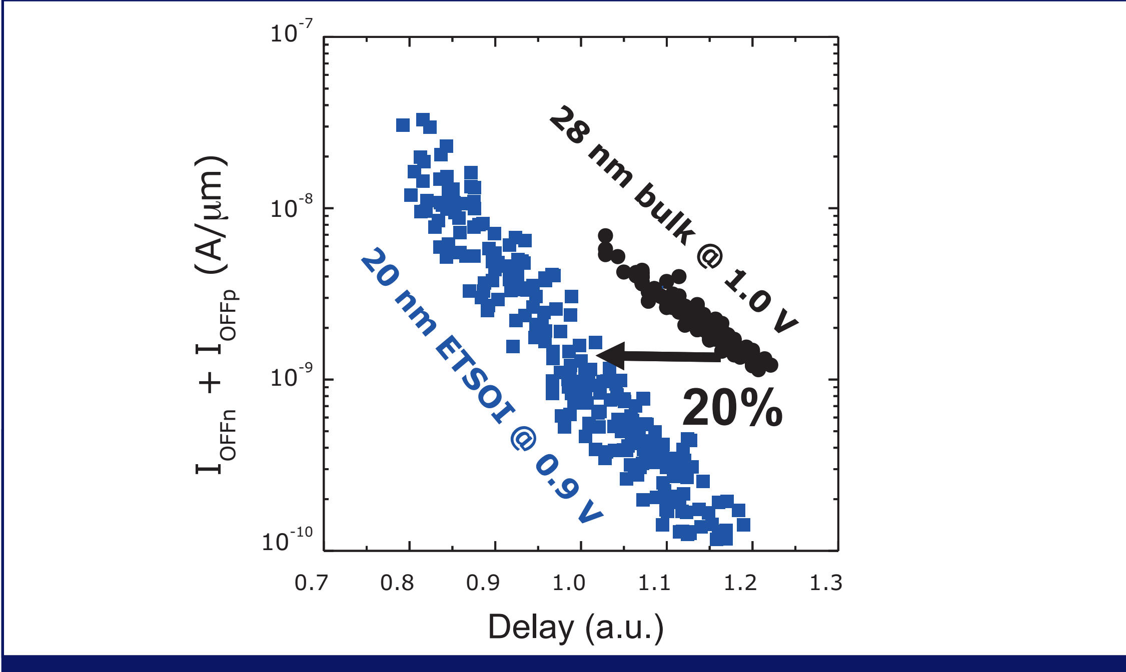


Figure 5. Planar FDSOI circuits operating at 0.9 V with 20 nm node dimensions are 20% faster than 28 nm node circuits with conventional transistors operating at 1.0 V.

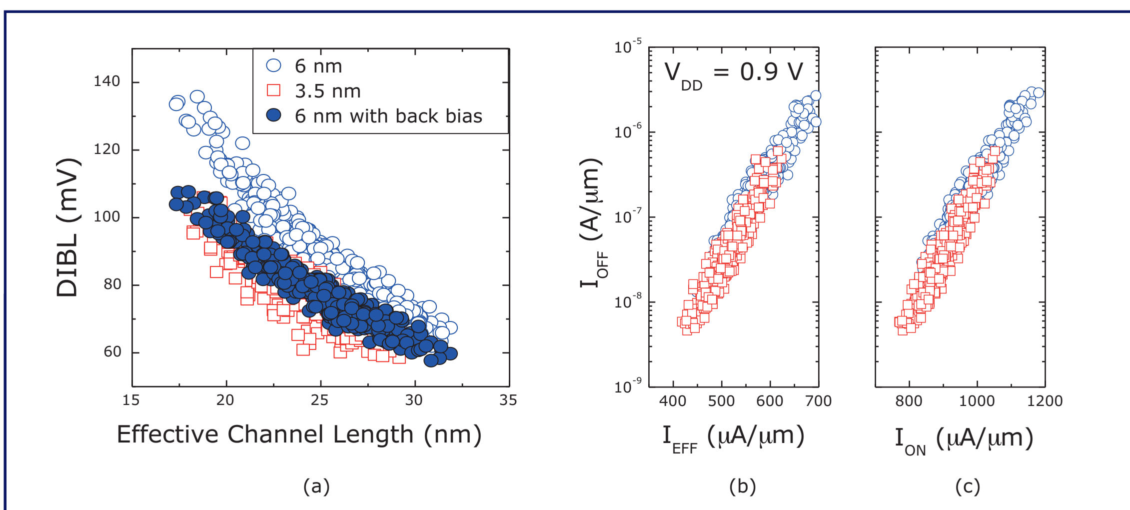


Figure 6. Planar FDSOI nFETs with 6 nm channel thickness compared to planar FDSOI with 3.5 nm channel thickness showing significant scaling with the thinner channel a) with no loss of $I_{eff}$ b) or $I_{on}$. Back bias of the FDSOI nFETs with 6 nm channel can also be used to achieve scalability a).

A more accurate metric to predict circuit performance is the effective current ($I_{eff}$), which is an average of the voltages that the drain gate of the transistor experiences during normal circuit operation. Fully depleted devices typically have much better DIBL compared to conventional transistors, and DIBL has a strong influence on $I_{eff}$. Thus, FDSOI devices can have very competitive $I_{eff}$. Figure 7 shows nFET and pFET $I_{on}$-$I_{off}$ plots demonstrating planar FDSOI performance.

| | FDSOI | Bulk[8] | PDSOI[9] |
|---|---|---|---|
| *Gate Pitch (nm)* | 100 | 112.5 | 130 |
| *$L_G$ (nm)* | 22 | 35 | 26 |
| N/P DIBL (mV) | 80/130 | 140/180 | - |
| *$I_{OFF}$ (nA/μm)* | 100 | 100 | 100 |
| N/P $I_{on}$ (mA/μm) | 1.4/1.2 | 1.62/1.37 | 1.55/1.22 |
| N/P $I_{eff}$ (mA/μm) | 0.82/0.68 | 0.86/0.74 | - |
| N/P $I_{dlin}$ (μA/μm) | 175/255 | 231/240 | - |

Table 2. Benchmark of planar FDSOI data relative to previous high-performance technology data. Bulk,[9] PDSOI.[10]

Table 2 shows a benchmark of the data in Figure 7 compared to previous work in high-performance technologies and indicates that planar FDSOI transistors have comparable $I_{eff}$ and $I_{on}$ for a given $I_{off}$. Moreover, the FDSOI devices can achieve this level of performance at significantly smaller gate lengths. Not only does the smaller gate length speed up circuit performance in CV/I metrics, but the smaller gate length is also a necessity to meet gate-pitch requirements (the distance between gates) for 20 nm node-and-beyond technologies.

## Conclusions

Alternate device architecture is needed for next-node technology. Fully depleted devices offer many advantages over the current conventional device architecture. Planar FDSOI is scalable and can deliver performance needed for advanced technology nodes.

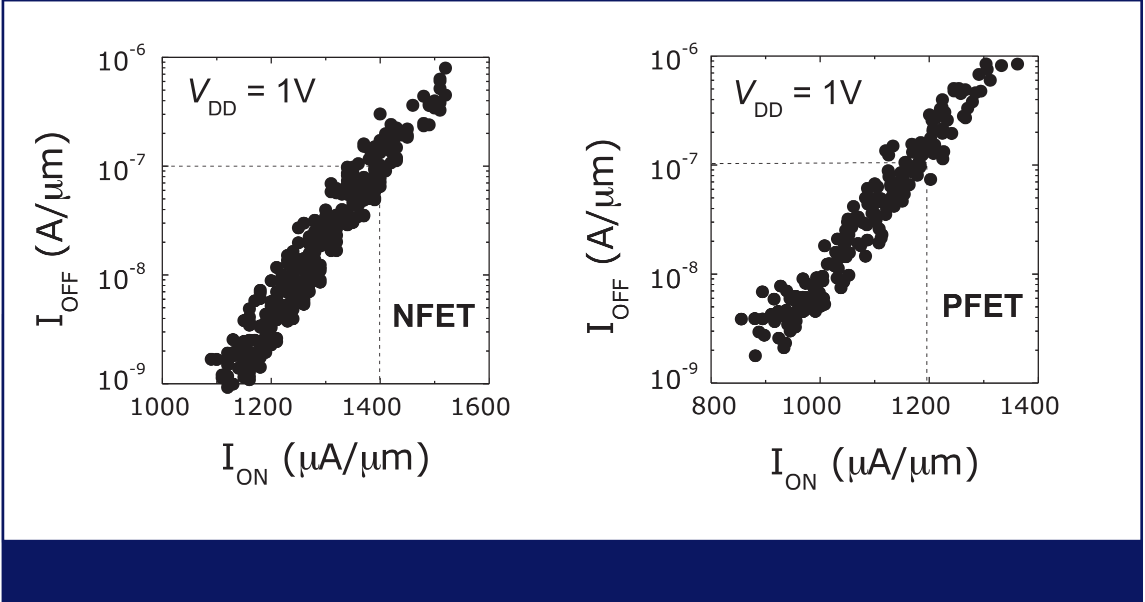


Figure 7. nFET and pFET $I_{on}$ vs. $I_{off}$ for high-performance planar FDSOI devices at $V_{DD}$ = 1 V

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## Tomographic imaging for nanoelectronics

As integrated circuit features continue to shrink, interconnect lines, contacts and vias require characterization of the complete structure. Tomographic imaging provides a very useful means of viewing the 3D shape of these structures. Large features such as through silicon vias (TSVs) require X-ray methods.

An example of the power of tomographic X-ray microscopy can be found in Figure 3 from the Metrology Chapter on the 2010 ITRS. The ability to observe voids inside the copper TSV structure provides a powerful means of characterizing copper deposition processes. On-chip interconnect has much smaller feature sizes, and as device sizes shrink, the ability to use TEM to image the entire metal structure increases.

Just as with the tomographic imaging of TSVs, electron tomography of copper interconnect is used for process characterization. Tomography is not the only advanced means of characterizing device structures, characterization of grain size and texture is important. Dark-field TEM imaging has long been used for this sort of analysis, and advances in detector technology enable large-area, low-angle annular dark field imaging of grain structure. The ability to study grain structure over a large area is considered key to process learning. Mapping of X-ray fluorescence signals and electron energy loss signals also provide important new information. We hope to highlight advances in X-ray detector technology for TEM in a future issue.

The following article in Future Fab's Metrology section highlights the importance of advanced imaging techniques for nanoelectronics research, development and manufacturing. Frieder H. Baumann's article describes three TEM imaging methods for interconnect characterization: electron tomography for 3D characterization; low-dose electron energy loss spectroscopy (EELS) mapping for ultra-low-k; and very low angle annular dark field (VLAADF) imaging for grain size analysis.

METROLOGY, INSPECTION & FAILURE ANALYSIS

# Advanced TEM Imaging Analysis Techniques Applied to BEOL Problems

**Frieder H. Baumann**
IBM Microelectronics Division

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## Abstract

In the last few decades, transmission electron microscopy (TEM) has made enormous progress. Not only has the spatial resolution advanced far into the sub-Angstrom realm, but sophisticated new analytical methods have also been developed. This paper will show by means of three examples how this progress is used for back end of line (BEOL) characterization. First, we will show how 3D imaging using electron tomography allows the complete reconstruction of nano-meter-sized interconnect structures in the memory of a desktop computer. Secondly, low-dose spectroscopy and subsequent noise reduction is shown to allow characterization of radiation-sensitive intermetal dielectrics. Third, STEM imaging in a special electron-optical alignment is demonstrated to allow unprecedented Cu grain imaging in interconnects, enabling determination of grain size distributions with hitherto unseen precision.

## Introduction

Some of the key factors for the tremendous progress of the art of electron microscopy in the last two decades have been the improvement of the electron optics, the advancement in computing power (at the TEM tool and off-line) and the introduction of the CCD camera for image and spectroscopy recording.

In the area of electron optics, the introduction of lens correction systems (correcting the spherical aberration $C_S$) has pushed the spatial resolution far into the sub-0.1 nm regime. $C_S$-corrected TEM tools are commercially available from several vendors, and are slowly but surely becoming the standard for high-resolution imaging applications.

The dramatic increase in computing power and data storing capability has enabled us now to run a complete TEM session fully automated. This allows for very long and/or tedious data acquisition procedures, as we will see in the electron tomography section.

The introduction of the CCD camera did far more than redeem the microscopist from hours in the darkroom to develop photo plates: The CCD camera, with its linear response to the electron dose, transformed the art of electron microscopy into a quantitative science, allowing electron energy loss spectroscopy (EELS), energy filtered imaging, electron crystallography and much more.

In this article, we will show how three modern TEM characterization techniques can help the BEOL development engineering team to understand and improve the processes and integration schemes: The techniques are electron tomography for 3D characterization; low-dose EELS mapping for ultra-low-k (ULK) materials; and VLAADF (very low angle annular dark field) imaging for grain size analysis.

## Electron Tomography in the BEOL

Electron tomography for BEOL applications is mostly done in scanning transmission electron microscopy (STEM) mode. In order to prevent strong contributions from Bragg-reflections of the materials involved, the STEM images are recorded with a high angle annular dark field detector (z-contrast mode).[1] This also ensures a monotonic dependence of the signal with increasing density, a necessary condition for successful 3D reconstruction.[2]

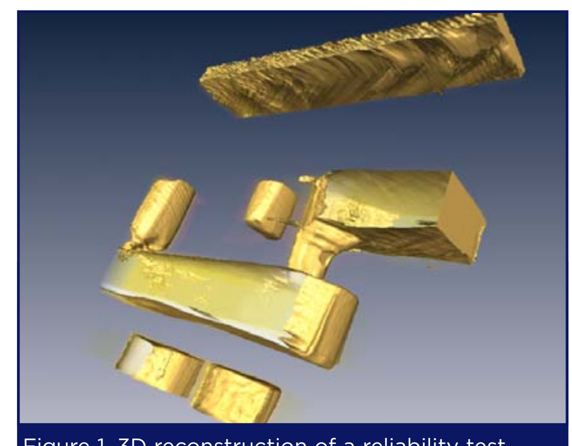

Figure 1. 3D reconstruction of a reliability test structure from the 45 nm node technology (2x level). The width of the center lines is 100 nm. Note the void (round crater) in the side wall of the via, which can eventually become a reliability concern.

The tomogram is recorded as follows: The sample is tilted around a fixed axis from -70° to + 70° in steps of 1° or 2°, and STEM images are recorded at each step. Any deviation in imaging conditions between two steps (image shift, focus shift, beam tilt, dynamic focus, etc.) is automatically adjusted by the software running the TEM during the tomogram acquisition.

After the acquisition, the images are aligned with respect to each other. Then, the images are concatenated to form a simple movie. By watching the movie, the human brain "reconstructs" the 3D nature of the imaged object. In many cases, the movie is sufficient to show the 3D nature of the object and to understand the nature of the object at hand.

Alternatively, the imaged object can be reconstructed as a virtual object in the computer. This is usually achieved by mathematical methods such as weighted back-projection or algebraic techniques like SIRT (simultaneous iterative reconstruction technique).[2] The reconstruction is computationally very intensive; only in the last decade has it been able to be employed in mainstream laboratories.

In the BEOL, electron tomography is usually employed to investigate the origin of voids in Cu, to examine if seed layers are contiguous, to understand the nature of "shorts" and "opens," and to characterize the overall geometry of the interconnects in 3D. Figure 1 shows such a full 3D reconstruction of a Cu interconnect structure. The data set consisted of 70 images recorded between -67° and +67° tilt angle. The 3D model was calculated using the SIRT technique with 20 iterations. This virtual object can now be tilted and rotated on the screen of the computer, and can be looked at from

any angle and in any direction. Of special interest in this case was the void found in the side wall of the via, which appears as a crater in the 3D reconstruction.

Three-dimensional tomography can also be used to measure step coverage of barrier and seed layers, as demonstrated in a recent paper in this journal.[3]

## Low-Dose EELS Mapping for ULK Characterization

During process steps like reactive ion etching or wet cleaning of modern intermetal dielectrics, the composition of the dielectric can change by out-diffusion of certain constituents. One prominent example is the loss of carbon from the ULK due to RIE interaction. To monitor the C concentration in the dielectric, high-resolution electron probe techniques like EELS profiling in STEM mode have been employed. Recently, however, the probe itself has been observed to change the composition of the ULK material, leaving a trace, or even holes, in the examined area. Naturally, this form of radiation damage renders the examination useless.

To mitigate the radiation damage per unit area, we are forced to reduce the electron dose by a factor of up to 25, resulting in a loss of signal of the same amount. We can partly recover the signal by measuring a map, and then averaging a couple of adjacent lines in the map (see Figure 2). Still, the signal-to-noise ratio is not high enough to give useful answers.

A dramatic increase in the signal-to-noise ratio can be achieved by employing a mathematical procedure called principle component analysis (PCA).[4] In PCA, the observed variables are reduced to a smaller number of principle components that will account for most of the variance (in this case: signal) in the observed variables. This technique reduces the noise significantly without compromising spatial or energetic resolution.

By employing both the averaging of adjacent lines in a low-dose map and the noise reduction using statistical analysis, we are able to monitor the carbon concentration in our ULK materials without introducing any radiation damage (Figure 2). As can be seen in Figure 2e, no C-depletion toward the metal lines is observed, and thus the full capacitance savings of the ULK is retained.

It is worth noting that noise reduction using data mining methods like PCA are often also used to “clean up” noisy X-ray or EELS maps,[5] making the PCA part of the TEM tool chest.

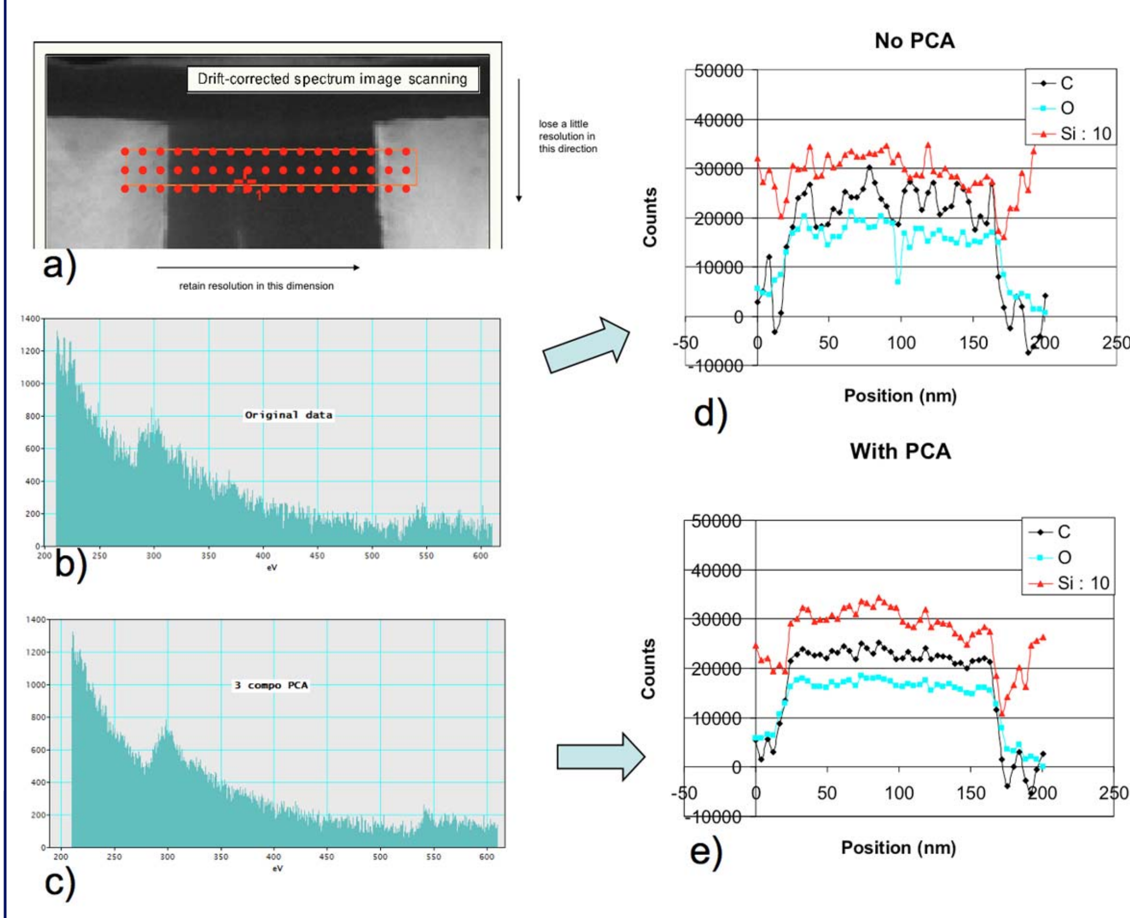


Figure 2. a) To reduce the electron dose, the material is mapped using an ultra-low dose beam. The signal is then summed up in the vertical direction to produce a 1D profile across the dielectric; b) the EELS spectra near the C edge after averaging in the vertical direction are still very noisy; c) PCA noise reduction analysis drastically reduces the noise in the EELS spectra. Now the O edge can also be detected; d) shown are the raw EELS counts for the three elements Si, C and O in the dielectric. The data shown in (b) (no PCA) still produce very noisy profiles; e) after reducing the noise using PCA (c), profiles with very little noise can be obtained.

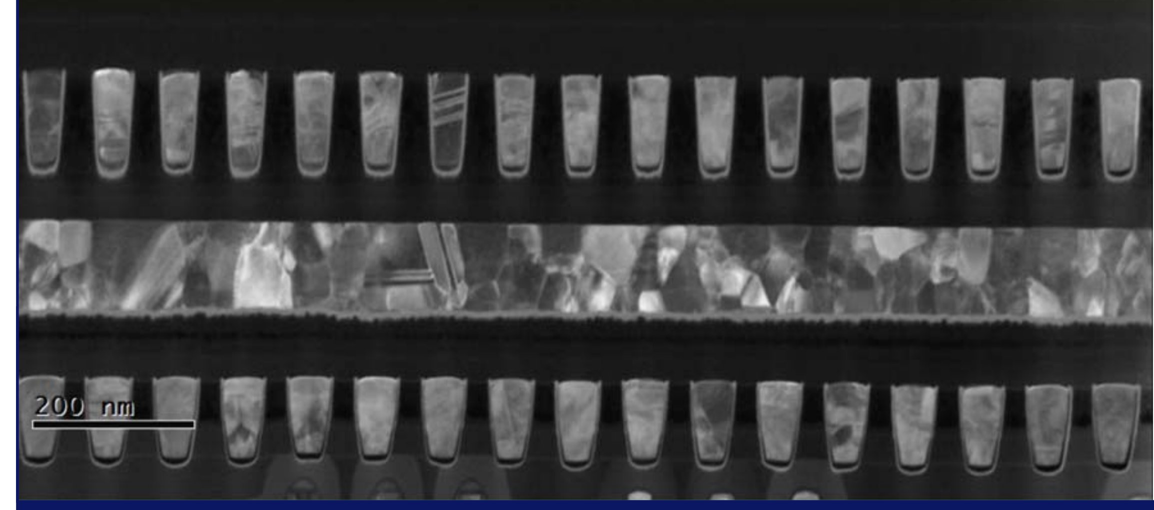


Figure 3. Very low angle annular dark field STEM (VLAADF-STEM) image of a modern interconnect stack. The imaging conditions are optimized to enhance contrast due to orientation differences. Each grain can be easily delineated by the naked eye. Just a few images like these per sample allow to map and analyze large numbers of grains to obtain grain size distributions of high fidelity.

## Grain Mapping in Cu Interconnects

The size of the Cu grains in the metal lines plays an important role in mechanical, electrical and reliability characteristics of current VLSI circuits. Unfortunately, the determination of grain size distributions of modern interconnect structures has always been a tedious and labor-intensive task. Since FIB and SEM methods run out of resolution, TEM techniques have to take over.

Traditionally, sets of TEM dark field images recorded under different beam tilt or sample tilt conditions have been recorded and analyzed to get grain size information. Only recently, STEM methods have emerged that are able to provide very good grain contrast in a single image. This is achieved by aligning the microscope in VLAADF mode,[6] which minimizes z-contrast and favors diffraction contrast (Figure 3). In this fashion, many grains can be imaged simultaneously in one STEM image. Thus, a few STEM images can provide data of hundreds of grains, leading to enhanced statistics and thus higher confidence levels in the grain size distributions. Using this technique, we were able to use grain size distributions to optimize the processing conditions, and tooling, for the liner seed deposition.

It should be emphasized that this technique only determines the grain size. Mapping the orientations of the grains toward each other is much more elaborate, but can also be done using the TEM.[7]

## The Future

TEM has come a long way, from merely imaging the devices, to develop into a versatile tool, able to almost completely characterize all aspects of modern FEOL and BEOL structures. No other technique combines reasonable elemental sensitivity with very high spatial resolution like TEM does.

Three-dimensional imaging using electron tomography has reached the mainstream now and will become a standard technique for advanced BEOL problems. The next steps in 3D imaging will be dual-axis tomography to eliminate the "missing wedge," and elemental mapping in 3D using EELS and/or EDX maps.

Characterization of the ULK dielectric will become more and more important. Ultra-low-dose techniques to determine the chemical composition and porosity are in development and are already showing initial results.[8]

The latest generation of analytical TEM tools equipped with novel X-ray detectors allows acquisition of X-ray maps in just a few minutes, compared to hours in tools just a few years older. Therefore, elemental mapping is now almost as fast as STEM image acquisition. The possibility of very fast X-ray mapping (including even light elements) will make the vision of "TEM color photography," with one color for each element, a reality in the very near future.

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Frieder H. Baumann, a native of Namibia, studied physics in Bielefeld and Goettingen, Germany, where he earned his master's degree and Ph.D. in physics from the University of Goettingen. He was a member of the technical staff for 14 years at Bell Laboratories in New Jersey, focusing on advanced electron microscopy, process simulation, and optical MEMS design and fabrication. After Bell Labs, he joined Philips Semiconductors in Hamburg, Germany, leading the process and device simulation efforts for discrete bipolar devices. Since 2006, he has been a senior engineer in IBM's Microelectronics division in East Fishkill, N.Y., and works on device characterization and physical failure analysis using advanced electron microscopic techniques. ■


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## Who invented 3D integration?

Recently I found a blog called "Who Invented the Through Silicon Via (TSV) and When?" where it noted that in 1958, the Nobel laureate William Shockley filed a corresponding patent introducing through semiconductor vias – calling them "deep pits." Indeed, Shockley was involved in the first *realization* of a transistor, but it should be mentioned that a transistor *concept* was already patented 1925 by Julius Edgar Lilienfeld. So, who invented the transistor? Correspondingly, one explicit inventor of 3D integration cannot be manifested – and of course, 3D integration is much more than the drilling and filling of TSVs ...

On the other hand, a few pioneering teams involved in the realization of 3D integration can certainly be named. The concept of 3D IC was claimed in 1964 by R.W. Haisty, R.E. Johnson and E.W. Mehal of Texas Instruments Inc., and the patent of through connections for connecting circuits on both sides of the semiconductor wafer was filed in 1964 by M. Smith and E. Stern of IBM. In 1989, M. Koyanagi and colleagues at Tohoku University demonstrated 3D IC integration by *wafer bonding*. Corresponding *die-to-wafer stacking* technologies for KGDs, which are significant for 3D integration of heterogeneous systems, were developed by Fraunhofer Munich (patents filed in 1994 by P. Ramm and R. Buchner). And certainly you can call the author of the following article, James Jian-Qiang Lu from Rensselaer, one of the inventors of 3D integration: Since the late 1990s, in fact, he has made distinctive contributions in this research area, with more than 150 publications covering 3D integration platforms, technologies and design. I am proud to say that James Lu, together with Philip Garrou and me, authored the overview chapter "Three-Dimensional Integration" in the recently published "Handbook of Wafer Bonding" (Wiley). One of his articles, "3D Integration: Why, What, Who, When?" can be found in Future Fab International, Issue 23 (2007).

James Lu's article in the following section represents an outstanding overview on this emerging technology in the past five decades, as well as showing the current developments toward commercialization.





# 3D Hyper-Integration: Past, Present and Future

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## Abstract

Three-dimensional (3D) hyper-integration has recently been recognized as an emerging technology to lead to an industry paradigm shift due to its tremendous benefits. The concepts of 3D integrated circuits were conceived almost five decades ago. Worldwide academic and industrial research and development were actively conducted in the last decade; products and prototypes toward volume production have been demonstrated. Wide adoption still faces major technical and business challenges, but it holds a promising future for smart-systems applications.

## Introduction

3D integration is an emerging technology that vertically stacks and interconnects multiple materials, technologies and functional components to form highly integrated micro-nano systems. This is expected to lead to an industry paradigm shift due to its tremendous benefits in performance, data bandwidth, functionality, heterogeneous integration and power.

3D integration is currently seen as the leading candidate to extend the benefits of Moore's Law to future IC technology nodes and to provide "More than Moore" solutions in the post-CMOS era (Figure 1). By means of stacking and connecting function blocks vertically, 3D technology can overcome some physical, technological and economic limits encountered in planar ICs to extend Moore's Law life. The most critical component in 3D integration is the through strata via (TSV) or through silicon via (TSV); a massive number of short TSVs can electrically connect multiple strata of ICs and/or devices vertically, enabling high performance, high functionality, compact heterogeneous systems with high data bandwidth and speed, and low power consumption and manufacturing cost.[1-4] This article attempts to briefly review some important developments in the past five decades, as well as provide some perspective on 3D hyper-integration for future smart systems. It is by no means comprehensive, but hopefully it will shed some light on the research and development of 3D hyper-integration. Critiques and comments are welcome.

## 3D Integration: Past and Present

With the technology development of 3D integration in the past five decades, we may consider roughly four periods of time:

- 1960s to 1970s: Generation of 3D integration concepts

- 1980s to early 1990s: First wave of 3D technology research
- Late 1990s to 2000s: Second wave of 3D technology R&D toward commercialization
- 2010s to future: Third wave of 3D technology for smart systems

### Generation of 3D Integration Concepts

3D is not new. We have always been living in a 3D world. Humans have created 3D buildings for thousands of years. Elec-tronics were created in 3D in their early stages. Not long after the first integrated circuit (IC) was invented by Jack Kilby in 1958, the 3D integration idea was conceived. Evidence can be found from the following patents:

- R.W. Haisty et al. (Texas Instruments Inc.), "Three-Dimensional Integrated Circuits and Methods of Making Same," U.S. Patent No. 3,613,226, filed on Aug. 18, 1964 and granted on Oct. 19, 1971. A continuation of the application originally filed in 1964 was filed in 1971 with the same inventors and same patent title; the patent was granted on July 24, 1973 with U.S. Patent No. 3,748,548.
- M.G. Smith and E. Stern (IBM), "Methods of Making Thru-Connections in Semiconductor Wafers," U.S. Patent No. 3,343,256, filed on Dec. 28, 1964 and granted on Sept. 26, 1967.
- B.L. Kravitz and H. Winsker (United Aircraft Corp.), "Integrated Circuit Modules," U.S. Patent No. 3,370,203, filed on July 19, 1965 and granted on Feb. 20, 1968.

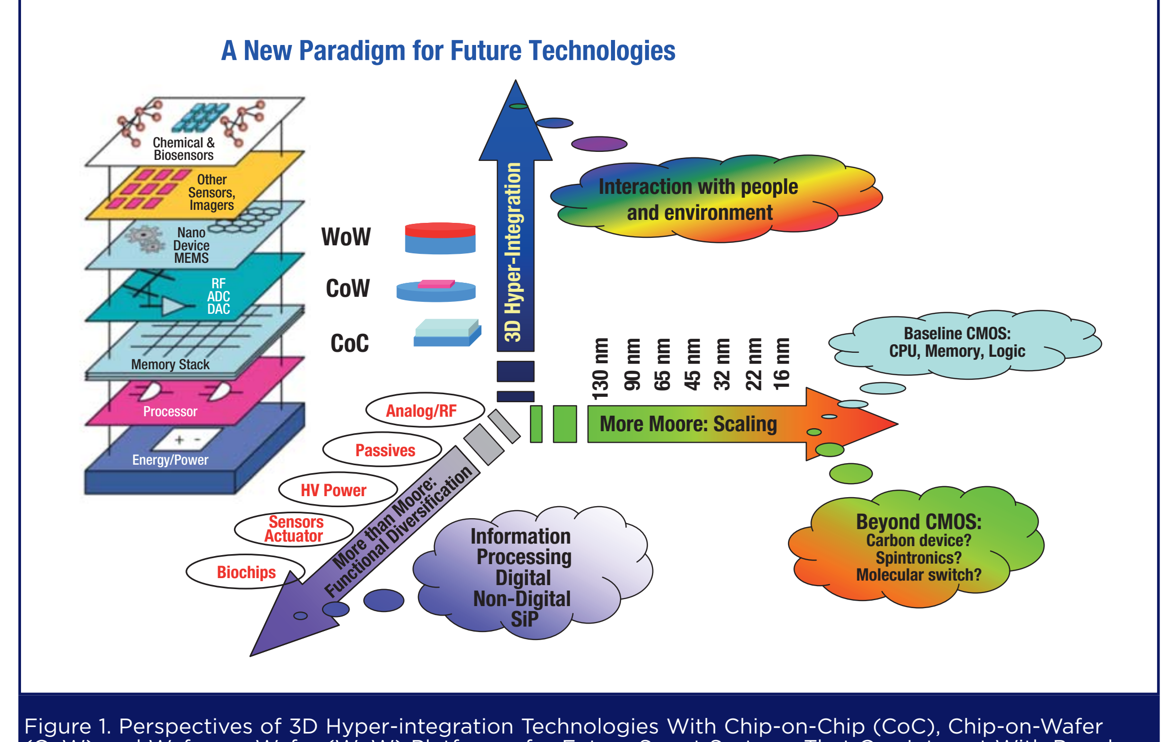


Figure 1. Perspectives of 3D Hyper-integration Technologies With Chip-on-Chip (CoC), Chip-on-Wafer (CoW) and Wafer-on-Wafer (WoW) Platforms, for Future Smart Systems That Can Interact With People and the Environment

### First Wave of 3D Technology Research

Active 3D integration research started in early 1980s, with more patents and technical papers published.

- T.R. Anthony (General Electric Co), "Implantation of Electrical Feed-Through Conductors," U.S. Patent No. 4,368,106, filed on July 21, 1981 and granted on Jan. 11, 1983. This patent and a paper by the inventor, which was published in IEEE Trans. on Components, Hybrids, and Manufacturing Technology in 1982, described the laser drill and copper electroplating to form feed-throughs for interstrata electrical connections.
- M. Yasumoto et al. (NEC, Japan), "Process of Fabricating Three-Dimensional Semiconductor Device," U.S. Patent No. 4,612,083, filed on July 17, 1985 and granted on Sept. 16, 1986. In this patent, no TSV was needed.
- M.J. Little and J. Grinberg (Hughes Aircraft Company), "3-D Integrated Circuit Assembly Employing Discrete Chips," U.S. Patent No. 5,032,896, filed on Aug. 31, 1989 and granted on July 16, 1991. In this patent and its related publications, the thermomigration of aluminum through silicon to form signal paths through silicon wafers was used and further developed.
- Y. Tomita et al. (Matsushita Electric Industrial Co.), "Three-Dimensional Stacked LSI," U.S. Patent No. 5,191,405, filed on Dec. 19, 1989 and granted on March 2, 1993. In this patent, the interlayer via-hole wiring to power IC was introduced.
- J.L. Gates (Hughes Aircraft Company), "Method of Making a 3-Dimensional Circuit Assembly Having Electrical Contacts that Extend through the IC Layer," U.S. Patent No. 5,489,554, filed on Feb. 4, 1994 and granted on Feb. 6, 1996.
- P. Ramm and R. Buchner (Fraunhofer, Munich), "Method of Making a Three-Dimensional Integrated Circuit," U.S. Patent No. 5,563,084, filed on Sept. 22, 1995 and granted on Oct. 8, 1996.

The last two patents described 3D integration technologies closer to present practices. A number of technical papers were published in this period of time. Some research efforts on 3D integration technology and circuit design were documented in two books:

- S.K. Tewksbury, Chapter 12, "Silicon Wafer Hybrids," Wafer-Level Integrated Systems: Implementation Issues, Kluwer Academic Publishers, 1989.
- M.J. Little and J. Grinberg, Chapter 6, "The 3-D Computer: An Integrated Stack of WSI," Wafer Scale Integration, ed., E.E. Swartzlander, Kluwer Academic Publishers, 1989.

However, it seems that it was a failed practice, without any commercially viable 3D products in the market in this period of time. The author believed that the major reason for this failed practice was a lack of demand and supporting technologies. It was a wonderful time period for 2D-IC commercial products, following Moore's Law of exponential growth in IC chips for computer technology, leading to the revolution of information technology.

### Second Wave of 3D Technology R&D Toward Commercialization

In 1997, IBM announced its six-level copper interconnect technology, which opened a new chapter of interconnect technology for improving the IC performance.

In 1998, a multi-university research center, Interconnect Focus Center (IFC), was created, with major funding from

Semiconductor Research Corporation (SRC) and the U.S. Defense Advanced Research Projects Agency (DARPA). The overarching goal was "to discover and invent new interconnect solutions that will meet or exceed ITRS projections." Major participating universities in IFC were Georgia Institute of Technology (GIT), University at Albany (UAlbany), Massachusetts Institute of Technology (MIT), Rensselaer Polytechnic Institute (RPI) and Stanford University. Thanks to the leadership and vision of the center director, Prof. J.D. Meindl, 3D integration was established as the IFC flagship program.[4] Also, thanks to Prof. A. Kaloyeros, UAlbany and RPI received significant funding from the New York State Office of Science, Technology and Academic Research (NYSTAR, now "New York State Division of Science, Technology and Innovation") for 3D integration research. Many aspects of 3D integration design and technologies were investigated and reported directly to major semiconductor companies and in a number of journals and international conferences. The research outcomes from the IFC 3D programs planted the seed for the second wave of 3D integration technology.[1-4]

The major driving force was "interconnect limits on performance of gigascale integration (GSI)," where demand to "go vertical" results from the need to drastically reduce the long interconnects on 2D chips. The second important reason 3D integration could become a successful practice is that it became feasible to develop the four key 3D technologies: wafer alignment, wafer bonding, wafer thinning and inter-strata interconnection, because they had been actively researched and developed for micro-electro-mechanical systems (MEMS) in the 1990s.

In 2003, Dr. D.I. Radack of DARPA created the first major 3D IC program (DARPA BAA 03-25, Three Dimensional Integrated Circuits); articulated a clear technology vision based on 3D heterogeneous integration; recruited the best researchers from universities, national labs and semiconductor companies; and formed a new 3D research community. The legacy of this successful program resulted in DARPA funding several other large 3D programs. Results from these efforts have greatly contributed to a wider understanding of 3D integration and 3D infrastructure development.

A number of academic institutions, industrial consortia and semiconductor companies across the globe started research and development in 3D integration. Results were reported in journals, conferences and books.[1, 5-8] More patents were applied and granted. A set of critical 3D processes and equipment for alignment, bonding, thinning and inter-strata interconnection (such as TSVs) were developed [1, 5-7].

Since TSV became the heart of 3D integration recently, it is worth mentioning some of the development (to the author's knowledge) as follows:

- The term "TSV" was used for the first time by Prof. L. Schaper and his student in their paper presented in the IMAPS International Conference on Advanced Packaging and Systems (ICAPS), Reno, Nevada, March 11, 2002.[9]
- The first patent using the term TSV: C.L. Rumer and E.A. Zarbock (Intel), "Through Silicon Via, Folded Flex Microelectronic Package," U.S. Patent No. 6.924,551 B2; filed on May 28, 2003 and granted on Aug. 2, 2005.

The term TSV was widely accepted, probably after Dr. K. Lee (Samsung Electronics) presented his world-first, eight-NAND stack functional sample at the 3rd International Conference of 3-D Architectures for Semiconductor Integration and Packaging in November 2006, and Dr. C.-G. Hwang (president and CEO of Samsung Electronics) gave his keynote of "New Paradigms in the Silicon Industry" at the IEEE International Electron Devices Meeting (IEDM) in December 2006.

### *3D-TSV R&D and Business*

Currently we are moving into the third wave of 3D integration. 3D-TSV technology has been actively developed by a number of academic institutions, government labs, industrial consortia and semiconductor companies around the world. Several corresponding full-3D processing flows have been demonstrated, with a number of approaches investigated. Particularly, after the use of TSVs for image sensors, TSV technology is getting into prime time for TSV silicon interposers (e.g., Xilinx's giant FPGAs), wide I/O applications (e.g., 3D DRAMs) and heterogeneous products for low-power, high-performance and small-factor smart-system integration.

Infrastructures (equipment, ECAD tools and standards) are being rapidly established. Several consortia are working with semiconductor companies to develop 3D-TSV technologies and define ecosystems.

## 3D Hyper-Integration Perspectives

With a number of companies announcing their timelines and roadmaps for 3D products, the focus of research and development turns to thermal-mechanical-electrical reliability of 3D TSV integrated systems, and the design of 3D systems with particular consideration of thermal issues.

Development of 3D integration will move from chip-on-chip (CoC) platforms to chip-on-wafer (CoW) platforms. Cu TSV technology in particular is close to maturity and is gearing up for volume production of wide I/O 3D DRAMs and for giant FPGAs with TSV Si-interposers, while image sensors using TSVs have been in the market for a few years. Once the infrastructure and ecosystem are in place, 3D IC technology development and applications will continue advancing in the coming years in an evolutionary, instead of revolutionary, fashion, from CoC to CoW and wafer-on-wafer (WoW) platforms (Figures 1 and 2). The author believes that a good set of solutions for processing integration, thermal-mechanical stress, yield and test, as well as cost reduction, will be developed for 3D hyper-integration of future smart systems for computing, information technology, mobile and mixed-signal applications, biomedical devices, and power and smart lighting applications.

3D hyper-integration provides a viable path to a future paradigm combining powerful computer technology with many applications, so that future smart systems can easily interact with people and the environment. Such systems can be smart information/communication systems (for cloud computing, handheld devices, wireless communications, etc.), smart-sensing control systems (for automobile transportation, avionic system, drones, etc.), future LED-based smart-lighting and new energy systems, smart biomedical systems (for diagnosis, surgery, drug delivery, health sensing/monitor, or brain-computer interfaces (BCIs), etc.), just to name a few. The future promises to be an exciting time. Our daily lifestyle and even our

culture may be dramatically changed with proliferation of this 3D hyper-integration technology.

## Acknowledgments

The author would like to thank many colleagues and students who supported and contributed to the 3D integration research. The author's 3D research programs have been supported by SRC, GRC, MARCO, DARPA, NSF, APAR-e, NYSTAR, SEMATECH, IBM, Freescale Semiconduc-tor, Tezzaron and EVGroup over the years.

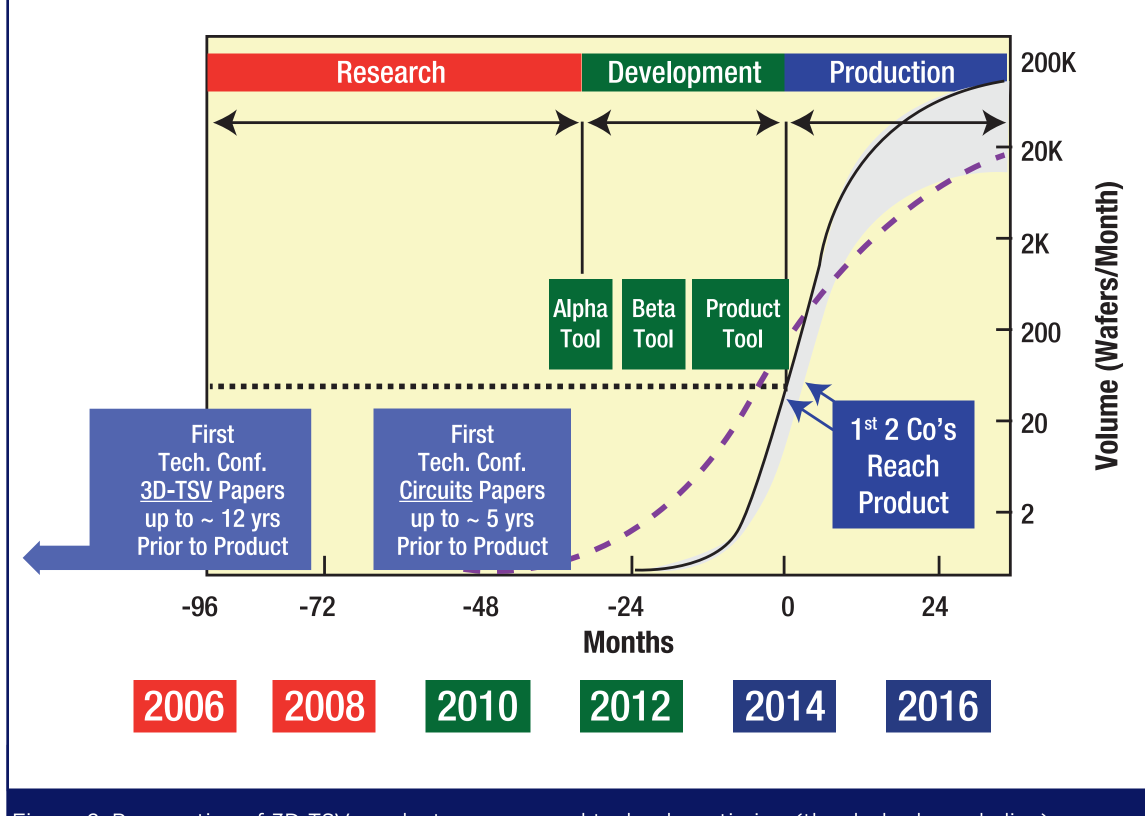


Figure 2. Perspective of 3D-TSV product ramp-up and technology timing (the dashed purple line). Unlike traditional 2D IC products (the solid line and shadow), there will be a number of 3D-TSV products gradually introduced with a relatively smaller volume ramp-up rate (the dashed purple line) due to the complexity of 3D technology and ecosystem.

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## *About the Author*

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James Jian-Qiang Lu is an IEEE fellow and an IMAPS fellow and life member. He has been working on 3D hyper-integration technology since the late 1990s at Rensselaer Polytechnic Institute in the Electrical, Computer and Systems Engineering department. James has more than 200 publications in the micro/nano-electronics area from theory and design to materials, processing, devices, integration and packaging. His particular interest is 3D hyper-integration of smart systems. ■

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Electronic devices like smartphones and mobile devices require IC packages that are small and thin in order to meet consumer demands for more functionality within an increasingly limited space. The smallest packaging format is wafer-level CSP, where the package is the die with ball grid array solder balls attached to the active surface of the die. A feature of this package is that the number of the I/O of the die cannot exceed the number of BGA balls the die surface area is able to accommodate. One way to expand the I/O capability is to surround the die with molding compound, thereby increasing the area available for circuitry and pads for BGA solder balls. This is commonly known as wafer-level fanout package (FOWLP). eWLB, originally developed by Infineon, is a prominent example of FOWLP.

This following paper describes a study of physical design and materials selection to manage the BGA solder ball board reliability. Two reliability risks are considered: thermal cycle fatigue; and drop impact. The authors selected two lead-free solder ball compositions and studied the dopant effect. It is interesting to follow the studies of intermetallic (IMC) formation and the effect of the assembly process (cooling) for thermal cycle tests and for drop impact tests. The authors found two solder compositions that perform the best among the six solder candidates in their evaluation.

Next for consideration is the effect of package thickness and the effect of distribution layers in this eWLB package. The authors employed finite element stress simulation for comparison with experimental data. While it is intuitively obvious that thinner package and multiple RDL layers would decrease ball shear stress driving thermal cycle fatigue, it is important to understand quantitatively the level of reliability improvement. It is gratifying that there is good correlation between simulation and experimental data.

This is an interesting paper describing design and materials considerations in the development of the emerging FOWLP package family.





# Design for Board-Level Reliability Improvement in eWLB Packages

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## Abstract

eWLB (embedded wafer-level BGA) is a key advanced package because of the advantages of higher I/O density, process easiness and integration flexibilities. It facilitates integration of multiple dies vertically and horizontally in one package without using substrates. Thus, recently eWLB development is moving forward to the next-generation packages of 3D integrations to meet the market demands. eWLB consists of diverse materials and structures built in a reconstituted wafer. As the volume increases, structural design as well as selection of materials becomes more important in determining process yield and long-term reliabilities. Therefore, it is necessary to investigate the key design factors affecting the reliability comprehensively.

In this paper, the influences of materials characteristics and structural designs on the board-level reliability will be demonstrated. Since the requirements for improving performances of drop and thermal cycling on boards are sometimes a trade-off, it is important to find the optimal design parameters to meet both reliability performances. Therefore, constructive analysis has been performed by examining every design factor both in a component level and in a board level. The reliability study was carried out in depth by experimental approaches as well as through thermomechanical simulations.

As a result, the most influential factors for reliability turned out to be relevant to the solder joint design, such as solder compositions and dielectric mechanical properties. On the other hand, the different structural design allows the life to be prolonged by providing increased resistance to the crack propagation and also by making the entire package body more flexible.

## Introduction

In recent years, trends in consumer products have been dramatically changing to handheld products, such as smartphones, tablet computers, thin laptop computers and so on. To meet product requirements, technologies tend to be developed in order to close the interconnect gap and to add multiple functional

chips for different features in a similar system footprint with a reduced package size.

Conventional wafer-level package (WLP) has a fan-in structure to fulfill the integration with high I/O counts. Hence, WLP extends its technology to new areas to deliver high-volume applications across multiple wafer diameters for various end-market products, such as passive, RF, memory as well as logic ICs and MEMS. For meeting all requirements coming from diverse devices, a fan-out type of package is needed.

In this point of view, eWLB is a package that will satisfy the abovementioned challenges, because it offers additional space for routing higher I/Os in addition to the silicon chip area, which is not possible in conventional WLP or WLB.[1]

eWLB technology involves a wide range of factors. Besides physical constraints such as package footprint and height, other parameters include I/O density, a particular challenge for small chips with a high pin count. In order to make the best use of the advantages of fan-out structures, designs of eWLB packages take materials and structural design selections into cautious consideration. eWLB has combinations of different materials in discontinuous structures with Si dies and mold compound. Thus, the design needs to be drawn to make the heterogeneous structure as continuous as possible.[2]

### *Materials Design for Reliability*

Figure 1 shows the schematic structure of eWLB in a cross-sectional view. The chip is embedded inside a mold compound in a wafer level, and a redistribution layer is formed over the heterogeneous surface of a combination of Si and mold compound, which enables forming additional I/O patterns on the fan-out area that is on a mold compound. In such a structure, the passivation layer as well as buildup RDL and solder balls are sitting on both Si and mold compound. But as the material properties of Si and the mold compound are quite different in a micro scale, there are many silica fillers contained in the mold compound formula to make its mechanical properties similar to Sis in a local area. At the boundaries between the different materials, there might be an abrupt change in material properties, which may impact the reliability of eWLB. Therefore, solder compositions should be carefully made to overcome such a unique characteristic.

Fanout area (molded)
Chip
Redistribution layer (RDL)
Dielectric
Solder Ball
Solder Stop

Figure 1. Schematic of Cross-Sectional View of eWLB Packages

### *Solder Ball Composition*

In general, SAC solder balls are better in temperature cycles on boards (TCoB) than PbSn. Mechanical properties of SAC solders are varying as a function of Ag content. Higher Ag-contained SAC has higher shear stress, which results in longer life in TCoB. On the other hand, lower Ag SAC is beneficial for drop performance, because it is softer and more ductile than higher-Ag SAC. In the mobile products, the drop performance gets more important together with thermal cycles. As the package size becomes smaller and thinner, the drop performance becomes more critical and more dependent on the solder compositions. It has been reported that some additives into SAC alloy improve the drop performance by making stronger interface on pads and controlling intermetallic compound (IMC) thickness and morphologies. Therefore, the effect of micro alloying with Ni, Fe, Co, Sb, Ti, etc., has been studied to optimize the robust package design.[3-5] The common consensus in typical package type is that lower Ag tends to be beneficial for better drop performance but adverse for TCoB. Some additional Ni or Sb is helpful in resolving this contrary trend.

Interestingly, this trend does not work well in the drop performance of eWLB packages. SAC305 performs equivalently as SAC107 or SACN (shown in Table 1).

| Solder Balls | JEDEC | |
|---|---|---|
| | First Failure (# of cycles) | Characteristic Life (# of cycles) |
| SAC305 | 70 | 689 |
| SACN | 34 | 413 |
| SAC107 | 65 | 654 |

Table 1. Drop Test Results as a Function of Solder Compositions

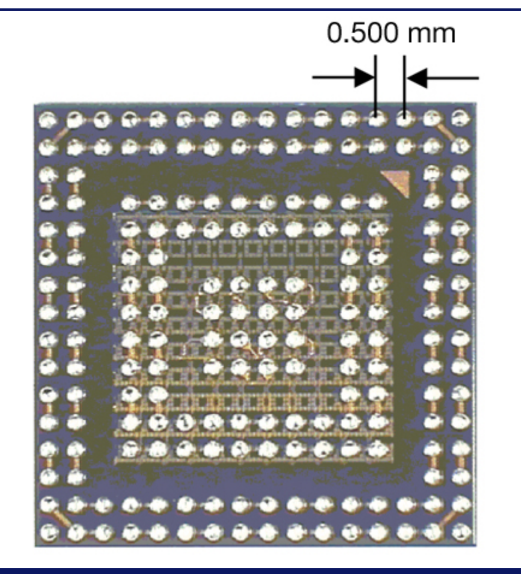



Figure 2. Test Vehicle Configurations in a Bottom View

| Item | Description |
|---|---|
| Package size | 8 x 8 x 0.475 mm |
| Die size | 5 x 5 mm |
| Backside protection layer thickness | 0.025 mm |
| Bump count | 192 |
| Bump diameter/pitch | 0.300/0.500 mm |

Table 2. Test Vehicle Dimension Used in This Study

The effect of impurities of SAC305 solder balls on the mechanical properties of eWLB has been further investigated. Figure 2 describes the test vehicles used in this study and Table 2 lists the dimension of the test vehicles. The solder compositions are listed up in Table 3 in a ppm level.

The ppm level difference in impurity presences is not so obviously detectable through characterizations. Here, we have tried to check the undercooling temperatures of SAC305 alloys because more impurities may offer more nucleation sites affecting the undercooling (supercooling). Differential scanning calorimetry (DSC) was employed to measure undercooling temperatures. Undercooling temperature is defined as the difference of onset temperatures in heating and cooling of alloys. Ten mg of solder balls were used for the measurement. Heating was up to 250 °C at 6 °C/min and cooling down to room temperature at the same rate of 6 °C/min. Figure 3 shows DSC plots of A and D SAC305 solders. The cooling peaks occur in different temperatures in two types of SAC305, leading to having different undercooling behaviors (shown in Table 4). The degree of undercooling influences the solder reflow process profile as well as the interfacial reactions at the joints. A higher degree of undercooling may require a slower cooling rate to lower temperature and create thicker and bigger intermetallic grains and consume more Cu pads. This causes changing in solder joint mechanical

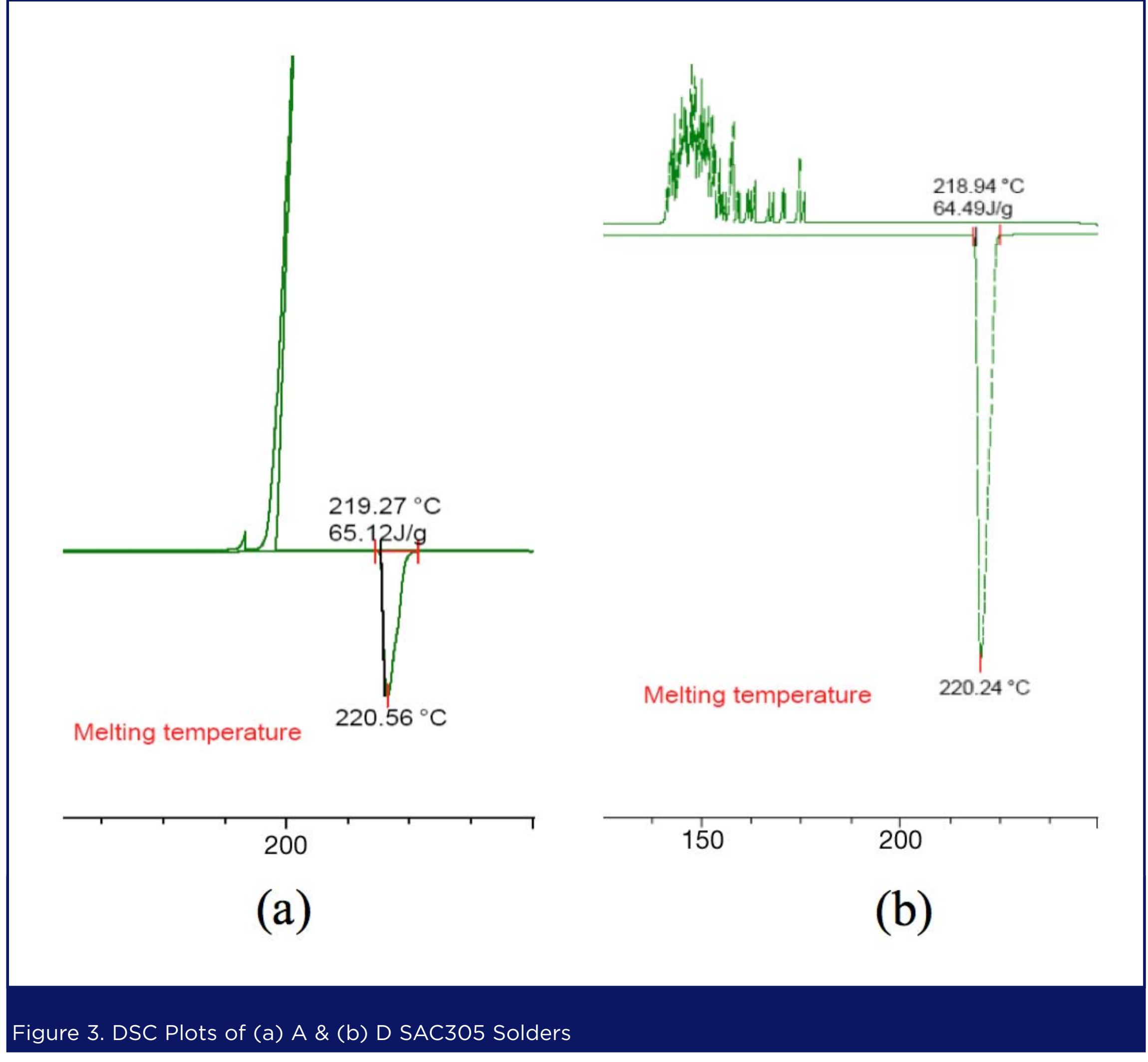
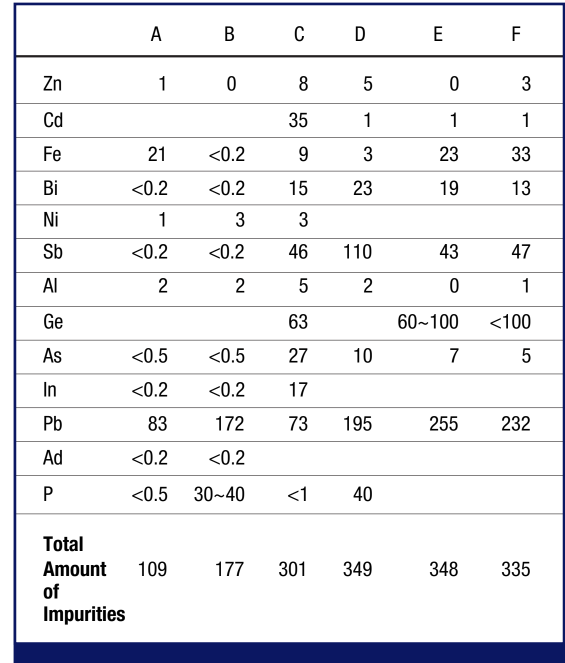


Figure 3. DSC Plots of (a) A & (b) D SAC305 Solders



| | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| Zn | 1 | 0 | 8 | 5 | 0 | 3 |
| Cd | | | 35 | 1 | 1 | 1 |
| Fe | 21 | <0.2 | 9 | 3 | 23 | 33 |
| Bi | <0.2 | <0.2 | 15 | 23 | 19 | 13 |
| Ni | 1 | 3 | 3 | | | |
| Sb | <0.2 | <0.2 | 46 | 110 | 43 | 47 |
| Al | 2 | 2 | 5 | 2 | 0 | 1 |
| Ge | | | 63 | | 60~100 | <100 |
| As | <0.5 | <0.5 | 27 | 10 | 7 | 5 |
| In | <0.2 | <0.2 | 17 | | | |
| Pb | 83 | 172 | 73 | 195 | 255 | 232 |
| Ad | <0.2 | <0.2 | | | | |
| P | <0.5 | 30~40 | <1 | 40 | | |
| **Total Amount of Impurities** | 109 | 177 | 301 | 349 | 348 | 335 |

Table 3. Impurity Levels of 6 Different SAC305 Solder Balls (in ppm scale)

| | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| Undercooling (°C) | 24 | 49 | 57 | 21 | 17 | 40 |

Table 4. Undercooling of Various SAC305 Solders

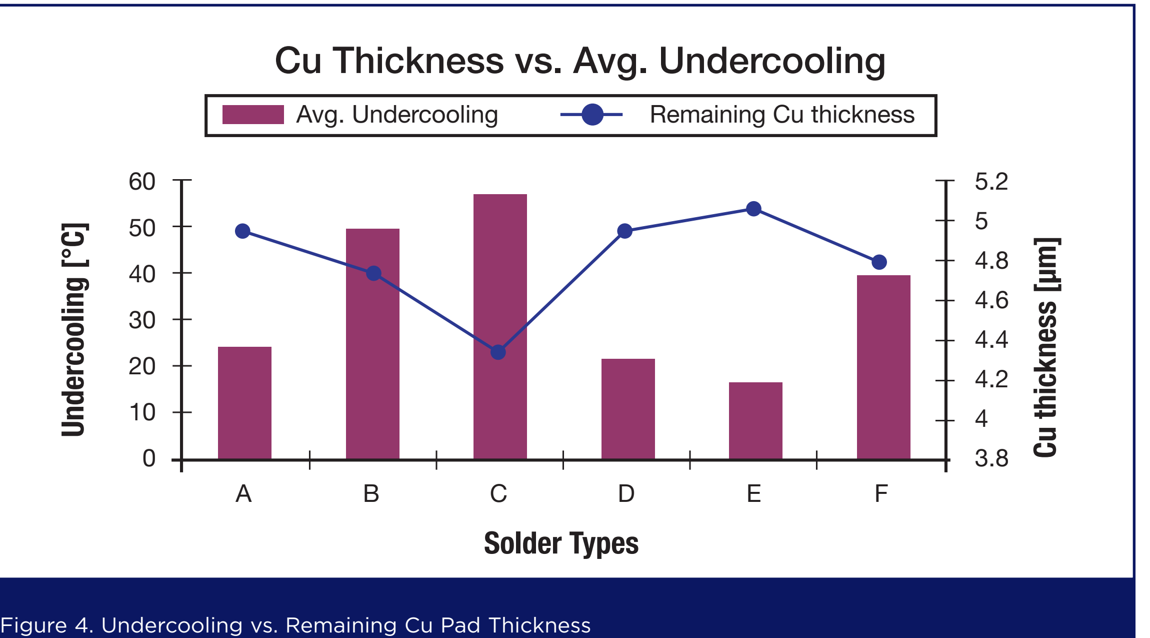


Figure 4. Undercooling vs. Remaining Cu Pad Thickness

properties. It should be monitored so as to control uniform solder joint formations in a reflow process.

However, a higher undercooling and a thicker IMC layer are not always correlated with each other. This is because some impurities may suppress excessive IMC growth while they increase the degree of undercooling. The degree of undercooling is able to be matched with the remaining Cu pad thickness, as shown in Figure 4. A higher degree of undercooling leaves thinner Cu pads due to longer duration in the liquidus zone prior

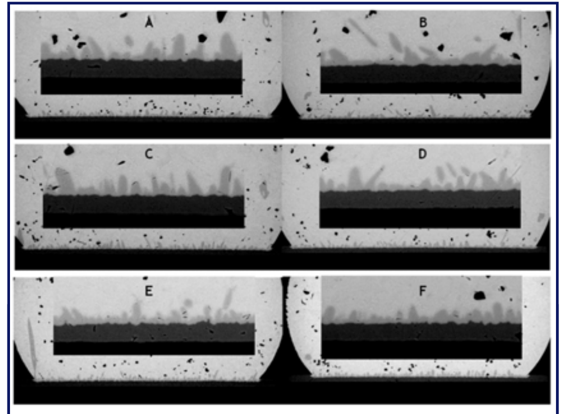


Figure 5. SEM Micrographs of 6 Types of Solder Joints After Reflow

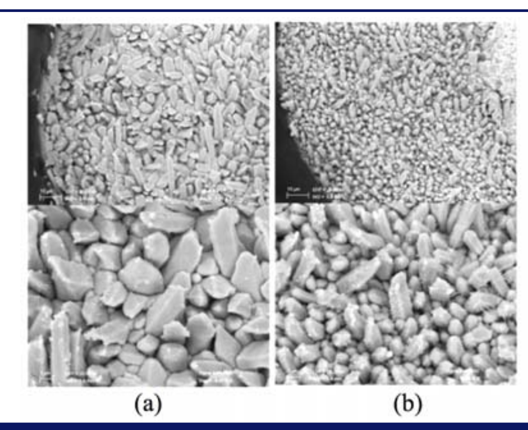


Figure 6. IMC Grains Morphologies in the Top View of (a) D Solder Joint; and (b) E Solder Joint After Reflow

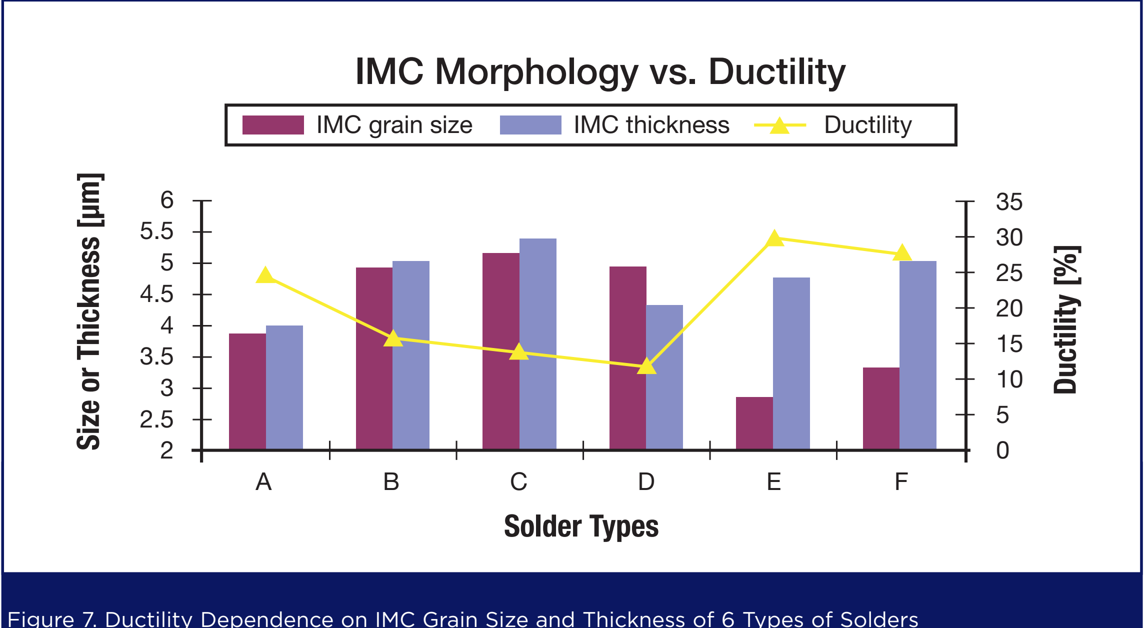


Figure 7. Ductility Dependence on IMC Grain Size and Thickness of 6 Types of Solders

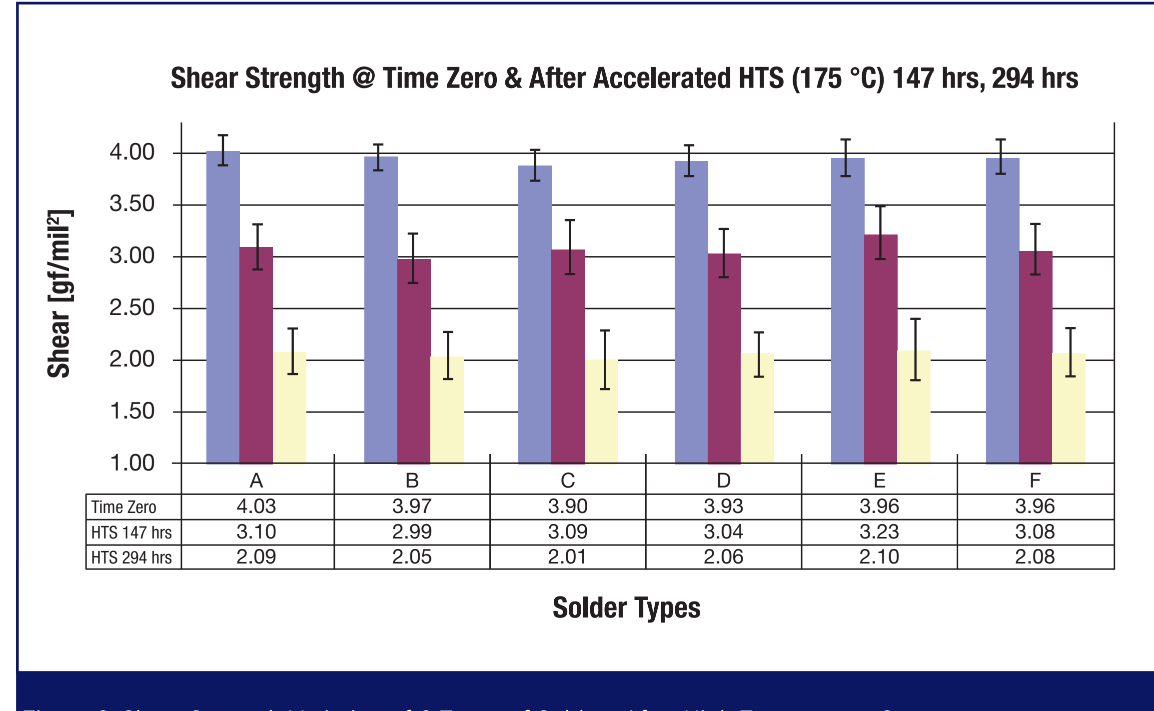
to solder solidification, which makes more Cu dissolution into liquid solders.

Figure 5 shows the interfacial microstructures of six types of solder joints. It is clearly observed that the IMCs form differently in all joints. IMC formations are showing diverse behaviors as well. In Figure 6, there are grain morphologies taken from the top view of solder joints after removing the solder matrix completely by chemical etching. IMC grain sizes appear much larger in D joint than E joint. The grain size as well as the thickness of IMC determines the solder joint reliabilities, which are shear strength, high-speed shear strength and Kirkendall void formations.

Figure 7 explains the relationship between IMC morphologies and joint ductility. Solder joint ductility was measured after high speed shear tests at a rate of 1 m/sec. The fracture energy was measured and converted into joint ductility. It turned out that the ductilities of A, E and F joints are higher than the others. It is more likely to be related with both IMC thickness as well as grain sizes. In A, D and E joints, IMC grows rather more moderately than others. More importantly, smaller grain sizes are governing joints ductilities, which is preferable for a better drop performance.

Figure 8 shows the shear strength variation after high-temperature storage at 175 °C for 294 hours. Shear strength values are decreasing regardless of solder types, which means that shear test cannot be a good measure to distinguish the solder joints properties in detail.

Through all investigations, A and E have demonstrated desirable properties to achieve a good drop performance. They




| | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| Time Zero | 4.03 | 3.97 | 3.90 | 3.93 | 3.96 | 3.96 |
| HTS 147 hrs | 3.10 | 2.99 | 3.09 | 3.04 | 3.23 | 3.08 |
| HTS 294 hrs | 2.09 | 2.05 | 2.01 | 2.06 | 2.10 | 2.08 |

Figure 8. Shear Strength Variation of 6 Types of Solders After High-Temperature Storage

are: having a lower degree of undercooling; an IMC layer composed of thinner and smaller grains; high shear strength and higher ductility in a high-speed shear test. As a result, A and E were confirmed as candidates for a good combination with Cu pads in an eWLB test vehicle.

To verify the effectiveness of A & E SAC305 solders, a drop test was carried out based on JEDEC standards (1500 g, 0.5 m sec, half-sine pulse). It was found that both solders revealed first failure at 101 drops in drop tests, as shown in Figure 9. A test was done up to 200 drops. Failure analysis showed the fails at the interface of the component side in both cases. It is regarded as normal failure mode.

As a result, drop reliability of eWLB can be improved remarkably by choosing the correct solder composition. For the selection of solder composition, we need to evaluate the solder alloys by screening from impurity levels, undercooling and ductility measured by high-speed shear test.

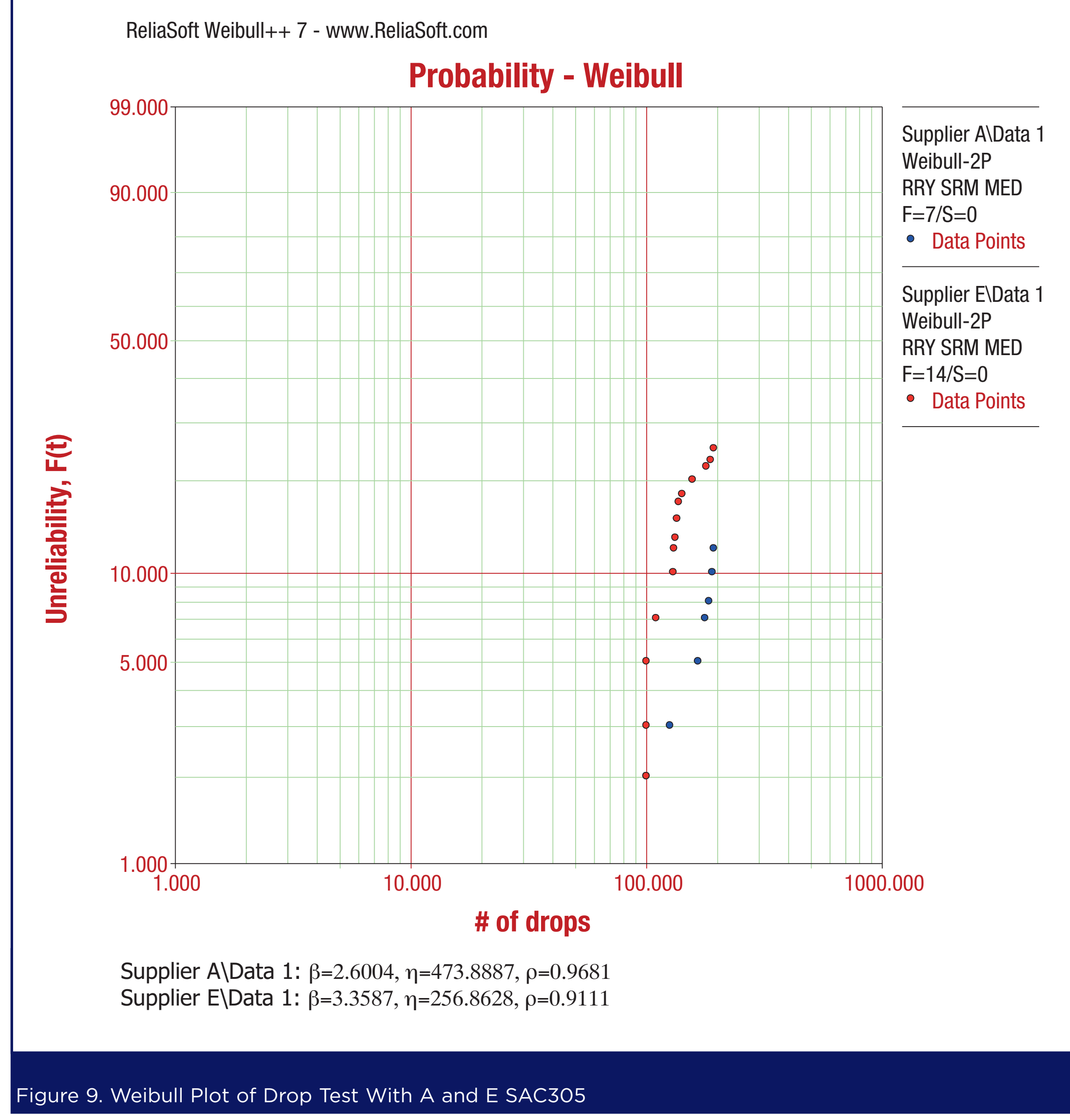



Figure 9. Weibull Plot of Drop Test With A and E SAC305

### *Structural Design for Reliability*

In addition to the items listed in Table 2, there are more dimensional factors affecting TCoB life. They are: package thickness; passivation thickness; number of buildup layers in RDL; passivation opening sizes in the solder joints; and so on. Among them, the most influential design factors from the empirical data are package thickness and number of RDL layers. Therefore, it was theoretically studied by means of simulation approach.

As a variance, standard and thinner package thicknesses, 475 µm vs. 275 µm with one and two layers of RDL were evaluated. Two testing conditions were taken into consideration in the simulation study, which were one or two cycles per hour in thermal cycles. The parameters used in this study are summarized in Table 5.

In this simulation, a constitutive equation is assumed with the Anand model from Chang et al. The CTE value of FR4 is assumed to be 16.0 ppm/°C and CTE of PCB = 16.6 ppm/°C . The simulation results in Table 6 are derived from the strain energy calculated from the equation based on the Anand model.[6]

The increment in number of RLD layers from one layer to two layers increases TCoB life 16~24 percent. In addition, a decrease in package thickness from 475 µm to 275 µm helps to prolong TCoB life by 7~9 percent.

| Leg # | Package Option | Pkg Thk (mm) | # of RDL | Cycle Rate (cph) |
|---|---|---|---|---|
| 1 | 1L Nom eWLB | 0.475 | 1 | 1 |
| 2 | | | 1 | 2 |
| 3 | 2L Nom eWLB | 0.475 | 2 | 1 |
| 4 | | | 2 | 2 |
| 5 | 1L Thin eWLB | 0.275 | 1 | 1 |
| 6 | | | 1 | 2 |
| 7 | 2L Thin eWLB | 0.275 | 2 | 1 |
| 8 | | | 2 | 2 |

Table 5. Evaluation Legs used with Variation in Testing Conditions with a Temperature Range from -40 °C to 125 °C

| Leg # | Predicted Characteristic Life (Cycles) | | |
|---|---|---|---|
| | Solder Bump @Pkg Corner | Solder Bump @Die Corner | Measured Char. Life (Cycles) |
| 1 | 789 | 949 | |
| 2 | 877 | 1017 | 954 |
| 3 | 917 | 1130 | |
| 4 | 1026 | 1225 | |
| 5 | 925 | 1034 | |
| 6 | 1026 | 1095 | |
| 7 | 1151 | 1213 | |
| 8 | 1292 | 1304 | 1430 |

Table 6. Predicted Characteristic Life as a Function of Package Thickness, Number of RDL and Number of Cycles per Hour in Testing

A combination of two-layer RDL and a thinner package is expected to maximize the effectiveness about ~30 percent longer TCoB life. A slight change in the design factors enables obtaining a longer life in TCoB with the same materials set.

## Summary

In this study, eWLB design factors affecting board-level reliabilities were investigated through experiments and simulation. In a material design, solder compositions play important roles in determining reliabilities. Even impurities of solder balls improve drop performances significantly by making better interfacial properties with smaller intermetallic compound grains and thinner intermetallic layer. The simulation study was performed to understand the dimensional effect on the BLRT performances in the eWLB. Reducing the package thickness and increasing the RLD layers can improve TCoB life.

Therefore, the design parameters of materials as well as structural dimensions need to be thoroughly studied to achieve the best performance in the BLRT. In the right design, performance can be improved by ~30 percent in TCoB life.

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