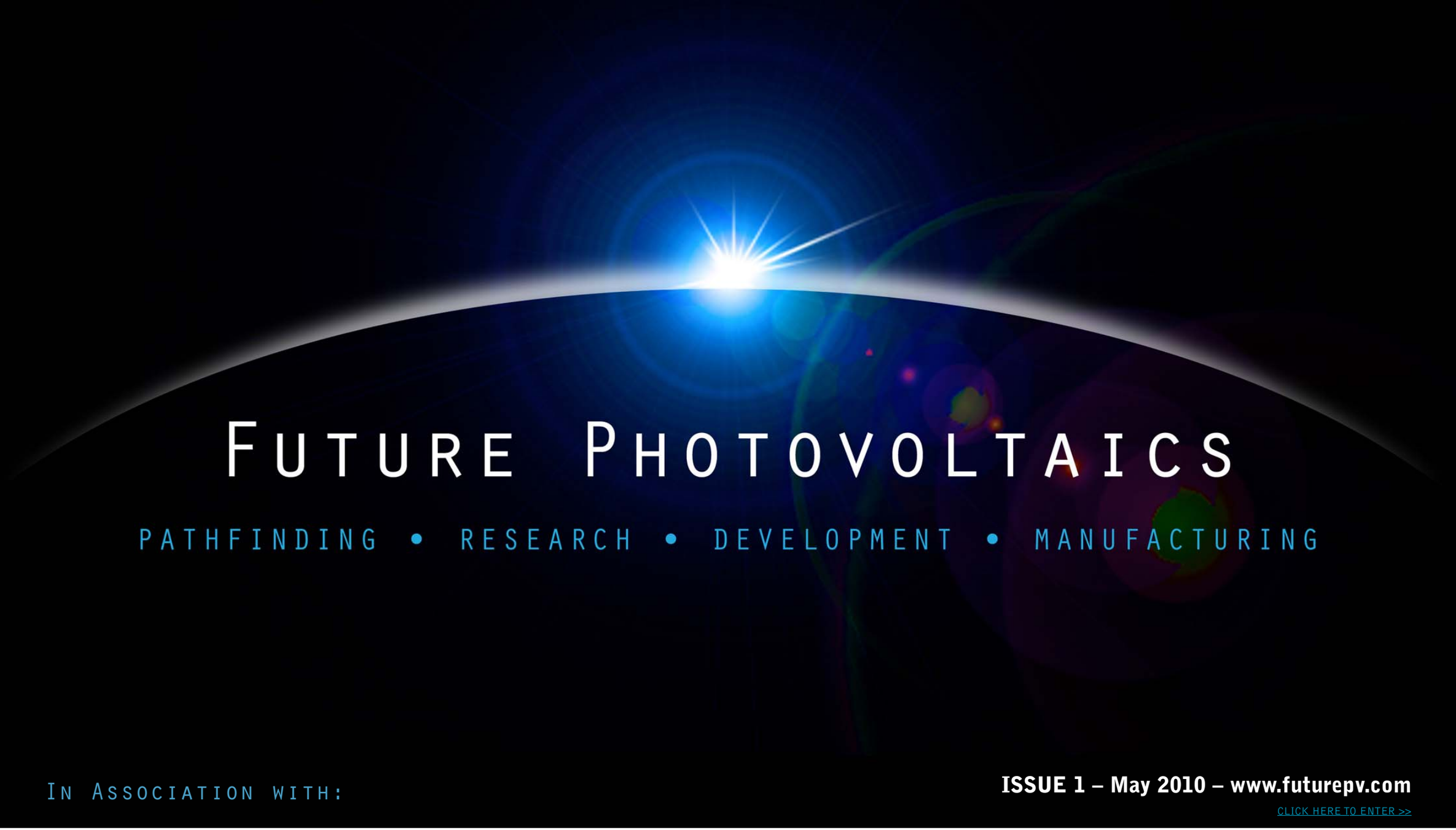

Future Photovoltaics

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Welcome...

... to this, the first issue of Future Photovoltaics - the photovoltaic industry's first FREE 100 percent digital technology journal built by members of the industry for the industry. Our primary aim with FPV is to bridge information gaps - research to manufacturing, cell fabrication to module construction, academia and commercial entities. The Mazik Media editorial model is unique in mainstream publishing and hopes to bring the industry's various social groups closer together. Over the coming issues, we hope to continually improve FPV and evolve it as the PV industry itself evolves.

With our unique open nature, we're always open to our readers' suggestions. Please feel free to write to us at converse@mazikmedia.com with any comments or suggestions; your input is highly valued.

In the meantime and with this inaugural issue, we want to extend special thanks:

We would not be anything without our Editorial Board and our partners, so firstly, a massive THANK YOU to them all. Secondly, we'd like to thank our sponsor companies and all the contributors to this debut edition - all worked tirelessly to very tight deadlines and we hope you'll agree that the content is first rate. Last but by no means least, we'd like to thank certain individual members of the PV community for their aid in helping us make the right connections and for giving of their time to help educate us on the intricacies of this unique industry:

Guy Beaucarne - Dow Corning
Craig Hunter - Intermolecular
Tim Woodward - Nth Power
Craig Cornelius - Hudson Clean Energy Partners
Kevin Lally - Tokyo Electron Ltd.
Steve Eglash - Consultant
Henri Chavrel - Air Liquide
Lauren Poole - Consultant

We hope you enjoy this first issue of Future Photovoltaics and we look forward to receiving your feedback!

The Future PV team

CONTENTS

"The photovoltaic market is dominated by solar cells …" Els Parton, Jef Poortmans - p48

<< PREVIOUS PAGE | NEXT PAGE >>

CONTENTS

"Optical measurement of film thickness is a challenge..." Alain C. Diebold - p112

METROLOGY, TEST & FAILURE ANALYSIS

PHOTOVOLTAIC SYSTEMS

EDITORIAL PANEL

For the full version of the following biographies, please click here

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<< PREVIOUS PAGE | NEXT PAGE >>

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<< PREVIOUS PAGE | NEXT PAGE >>

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FUTURE VISIONS & CURRENT CONCERNS

Click here to return to Table of Contents

Wim C. Sinke
Staff Member Solar Energy
Energy Research Centre of the Netherlands

Photovoltaics on its way to full maturity

Photovoltaics has benefited tremendously from knowledge, technologies and experience in the semiconductor chip industry. This is especially evident for early photovoltaics, in the '50s to (roughly) the '80s of the 20th century. One could even argue that the semiconductor industry gave birth to photovoltaics. As the photovoltaic sector developed, it became clear, however, that the technologies needed for downscaling of dimensions and increasing of speed of integrated circuits are quite different from those required to enhance cell and module performance and decrease cost per square meter of device area. Photovoltaics thus largely went its own way and introduced technologies and manufacturing practices that were specific to photovoltaics.

This certainly worked well for a period of time and has enabled the development of a wealth of different types of cells and modules and a drastic reduction of manufacturing costs. To a certain extent this can be seen as the period of exploration and divergence – a child finding its own way and becoming independent.

Now that the photovoltaic sector is gradually coming of age, it becomes clear that it can still (or rather, again) learn from the semiconductor industry. Further growth can no longer be based on such a wide spectrum of technological approaches and company-specific roadmaps. Of course, individual companies need to distinguish themselves from competitors by their products, but it is impossible to develop successful products from technology scratch. This is far too costly and/or too slow for companies to stay in business. Moreover, the lack of globally accepted process and product standards makes it difficult to design advanced yet economical production lines and to address a broad range of markets with a limited number of products. This now starts to hamper rapid further cost reduction and market growth.

In this issue of Future Photovoltaics, two well-known successes of the semiconductor chip industry – Moore's Law and global standardization – are shown to have important potential parallels with the photovoltaic industry. In other words, the photovoltaic industry sector may benefit from the experiences and practices that made the semiconductor industry the miracle of the 20th century. If translated and applied well, they may make the photovoltaic industry the miracle of the 21st century.

Standards Can Take PV to Its Gold Medal Game

Brent Nelson
National Renewable Energy Laboratory

Abstract

Standards could help the PV industry move to the next level of competition in the Energy Olympics. The PV industry can learn from the standards that made winners out of the semiconductor chip industry. The challenge is bringing together the complex interests that make up the PV industry, in a timely and mutually beneficial endeavor.

In early 2010, countries from all over the world competed for the gold medal in the Olympic Games. In a similar way, the photovoltaics industry is competing in an international competition to reach its gold medal game – outcompeting conventional electricity generation to obtain wide-scale market penetration. Standards will help the industry to reach that level of competition, but standards tend to develop by default rather than by a proactive process. The question is, will conventional electricity generation technologies, particularly coal, continue to win the competition until PV de facto standards emerge, or can the PV industry get to the podium faster by working together to develop standards?

The PV industry has few standards now to support the manufacturing process or to help achieve cost reduction and process efficiency goals. The semiconductor industry was in the same place decades ago when it recognized the need for standards. The creation of standards helped the semiconductor industry progress along Moore's Law of technological advancement. PV can learn from the semiconductor industry's experience.

Winning Lessons From the Chip Industry

PV and traditional semiconductor businesses have a lot in common. Both use similar materials: semiconductors, metals and insulators. Their deposition, processing and measurements are done using similar equipment. Both require the ability to incorporate innovations and to rapidly scale up, which requires high up-front capital costs to get into the game at any scale.

By developing standards for areas outside their core technology, semiconductor companies were able to focus on what made them special as a technology. For example, standards allowed the semiconductor industry to focus on the

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research and development of improved transistors that were 1,000 times more powerful than their predecessors. Semiconductor companies could then remain focused on Moore's Law, which led to processors as small as a grain of rice and the widespread adoption of semiconductor technologies in markets around the world.[1]

Figure 1 – The PV industry shares many similarities with the semiconductor industry in terms of technology and manufacturing challenges. Shown here are wafer solar cells being sorted at a BP Solar manufacturing facility in 2008.

The PV industry lacks a unified communication standard between production equipment and the shop floor. When the semiconductor industry faced the same challenge in the 1980s, the industry's trade organization, Semiconductor Equipment and Materials International (SEMI), brought companies together to create the SEMI Equipment Communication Standards/Generic Equipment Model, which resulted in a reduction of the cost required to automate a factory, increasing throughput and efficiency. The industry did this because a lack of standards was stated as a major roadblock to efficient manufacturing. More standards quickly followed.[2]

Standards also allowed semiconductor companies to move away from a vertically integrated business model, meaning they focused on everything from silicon feedstock to shipping out products. By creating standards, semiconductor companies were able to spread out the cost and risk. If one area of the supply chain was disrupted, they were able to pull supplies from several sources and reduce the risk of going bankrupt because of one weak link in the chain. Standards meant companies could spend their time and money on research and development and other core business areas.

At one point, IBM was vertically integrated. The company made its own resistors, circuit boards, PCs, mainframes and software. The structure led to a large cumbersome company that had to divest in order to survive. IBM PCs were a success because a big company championed their development, yes, but they also kept costs down by making modular parts that they could get from multiple vendors. IBM even outsourced its operating systems, giving birth to Microsoft. IBM's original market of 240,000 units would never have expanded worldwide had they tried to do everything internally. Many computer companies that tried to stay vertically integrated didn't survive. Some, like Apple, did survive, but settled for a smaller market share.

Many PV businesses are vertically integrated in the same way as early semiconductor companies: They manage everything from feedstock generation to solar cell fabrication to module manufacturing and installation. As the market grows, PV companies will find standards for things like specifying material quality, environmental health and safety considerations, tool communications, module sizes and connections, deployment schema, and other generic areas. The standards will greatly assist their ability to deal with multiple vendors and customers all over the world. They will also reduce supply and deployment (investor) risk, lower costs, increase reliability, improve efficiencies and help PV be a competitor in the Energy Olympics.

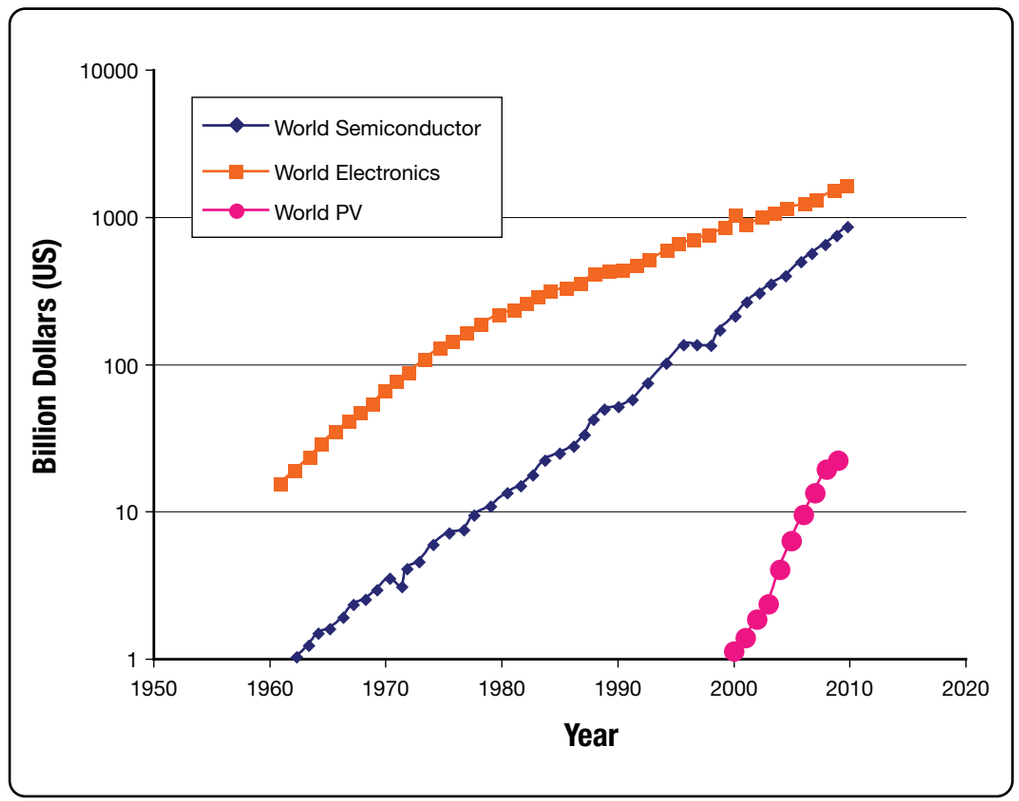

Figure 2 – Industry Growth Perspective

Source: Compiled with data available from www.iciknowledge.com, Paul Maycock (PV News) and eia.doe.gov

<< PREVIOUS PAGE | NEXT PAGE >>

The Standards Challenge

Unlike the semiconductor industry, the challenge to creating standards for the PV industry is its unique technologies. For one, the semiconductor industry is focused on one base material, silicon, and only one basic form, the circular wafer. The PV industry uses many semiconductor elements besides silicon, including cadmium telluride, gallium arsenide and related materials, copper indium gallium diselenide, and even silicon in various forms (single crystal, multi-crystal, amorphous, and nanocrystalline). In terms of material handling, while the IC industry did debate on wafer diameters and thicknesses, it was still a round wafer. The PV industry has many material handling form factors, including round wafers, square wafers, rectangular wafers, various sizes of glass substrates (up to 2.2 m x 2.6 m) and even foils of various size made of plastic and stainless steel. Because these different material technologies require different processes and the material handling requirements vary with material form factors, it is difficult for equipment manufacturers to supply multiple tools across the industry, keeping factory costs up.

The U.S. Department of Energy, the National Renewable Energy Laboratory, the National Academy of Sciences, SEMI and the Semiconductor Manufacturing Technology (SEMATECH) association are working with companies on developing PV standards and roadmaps. The work has revealed some recurring themes. Most companies involved in supporting manufacturing (i.e., equipment, factories, feedstocks, etc.) and those in related fields (i.e., insurance, installation, regulators, etc.) want standards. However, cell and module manufacturers are much more cautious. Due to the low internal[3] cost of electricity generation by fossil fuels (the competition), the less developed state of the PV industry and the tremendous success of its diverse technology portfolio, it is difficult for individual PV companies to find the time, resources or motivation to collaborate on roadmaps and standards. It is difficult for them to engage in activities that may require them to retool an entire shop floor to meet a standard, lose a competitive advantage or risk venture capital interest by being seen as unoriginal. In addition, these groups cite the 35 percent growth rate per year as evidence that standards may not be possible or needed for this type of technology. After all, PV has a multitude of applications including field-mounted, building-integrated and concentrated, so why worry about standards when one size doesn't fit all?

Timing Is Everything

Just as in the Olympic Games, when it comes to standards, timing is everything. The semiconductor industry has a great sense of timing. It learned early on that standardizing too early is a mistake, but so is standardizing too late. When cost pressures forced all IC companies to seek lower costs, the timing was right for standards.

According to a recent SEMI PV Group survey, the timing is right for the PV industry to standardize module sizes, substrate sizes, chemicals, automation, equipment integration, performance testing, permitting, installation and inspection. Executives in the crystalline silicon PV industry are working closely with SEMI's PV Group to create standards for silicon in some of these areas. The SEMI Standards Program has created standards committees in Europe, Japan, North America and Taiwan to allow companies to collaborate in a precompetitive environment on topics such as PV wafer and cell transport, single-substrate tracking, equipment-to-equipment communication, solar grade silicon feedstock, connector ribbon, minority carrier lifetime, transparent conductive oxide, cell specification templates, impurity test methods, process chemicals and gases, cell and module vibration test methods, cell appearance, and cell defect detection. Efforts are now under way to standardize

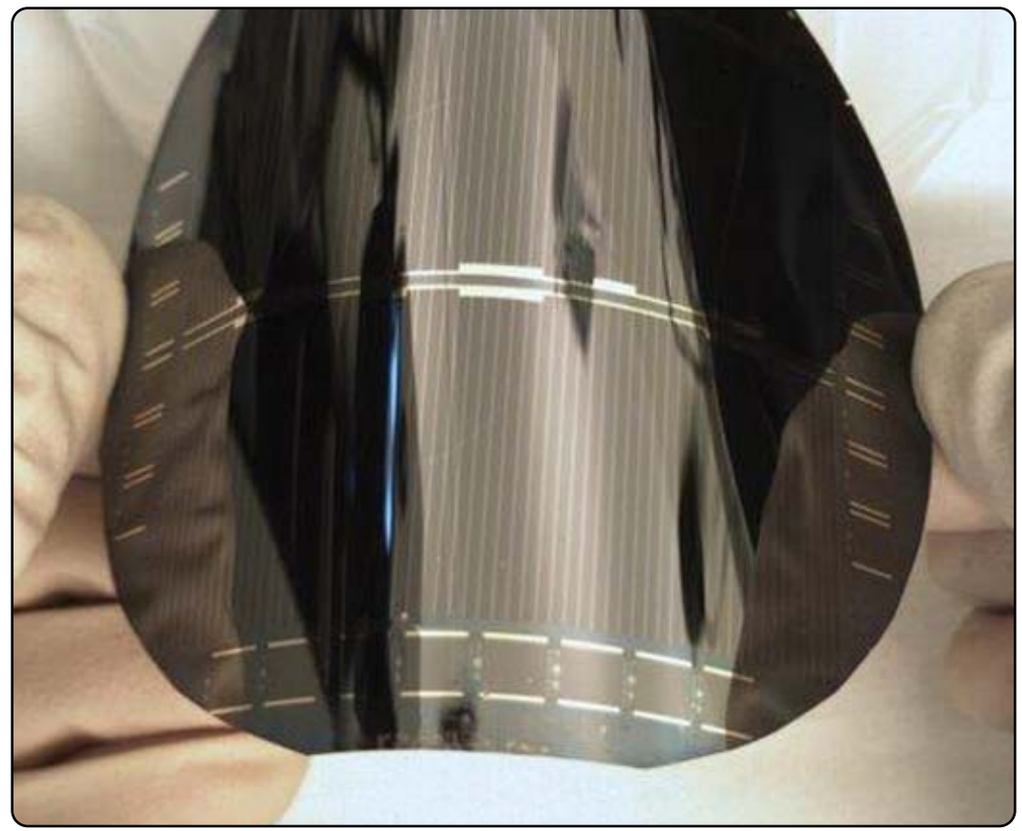

Figure 3 – To create standards, the PV industry must overcome unique challenges, such as bringing together the complex group of technologies that make up PV. Shown here is a solar cell made by MicroLink Devices that uses gallium arsenide instead of silicon and concentrator technology to maximize efficiency and reduce costs.

<< PREVIOUS PAGE | NEXT PAGE >>

thin-film substrate size and create classification criteria for crystalline silicon solar cells in Japan and Taiwan. In Europe, several new activities gained approval to start. Most notably, a PV wafer and cell carrier effort led by Q-Cells, and a solar grade silicon feedstock specification standards project, driven by several silicon manufacturers including Wacker, PV Crystalox, Hemlock and REC Group.[4]

It may be too early to standardize for companies involved in thin-film technologies. So far, their participation in standards activities has been limited, and the big players feel their products are the standard. The SEMI PV Group has identified four areas that don't threaten anyone's intellectual property or differentiating technologies that could jump-start the standards process. These are:

- Analytical test methods, which tell the industry what is important to measure and how to measure it;
- PV equipment interface specifications, which define how to get data out of tools and make it easier for tools to talk together;
- PV gases and chemical purity, which tell the industry what gases and chemicals are good enough to make solar materials; and
- PV facilities, which could lead to safer manufacturing plants that produce a high yield at low cost.

The PV industry will continue to bump into the issue that cell and module manufacturers are resistant to having standard cell structures and module sizes. The size issue may end up working itself out in the market with winners and losers. Whether or not such standards are developed collaboratively or in the marketplace, roadmapping efforts may have to answer these questions as part of the process:

- Should the industry create one roadmap for everyone or a different roadmap for each technology? (Like the Olympic Games, have different rules for different sports.)
- Is there a middle ground; that is, should the industry create material handling roadmaps (i.e., roadmaps for wafers, high-temperature foils, low-temperature foils, and glass)?

Summary

Lack of standards and roadmaps for the PV industry is a major roadblock to accelerated market growth. As the industry grows, more companies will jump on board. The development and widespread adoption of standards by PV companies can reduce costs, foster technological innovation and meet growing demand – all of which are required to win the gold in the energy game.

Besides the two major benefits of reducing costs and improving manufacturing processes, standards can also benefit the PV industry by removing barriers to market entrance by new companies, facilitating workforce development and fostering cooperative research and development. From a big picture perspective, with coal being the largest competitor, the most pressing question remaining is, will the environment even survive the game if the PV industry waits for these standards to evolve naturally or is the need more imminent?

To find out more about SEMI's standards activities, visit www.pvgroup.org. Have comments or suggestions for the author? Send them to: Brent.Nelson@nrel.gov.

Endnotes

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☞Click here to return to Table of Contents

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<< PREVIOUS PAGE | NEXT PAGE >>

Click here to return to Table of Contents

Enabling Our Customers to Reach the Lowest Cost of Ownership

The Meyer Burger group offers a unique technology and product portfolio, covering all the important technologies from solar silicon to solar module. The group is dedicated to enable its customers to reach the lowest cost of ownership and thus to reach grid parity faster.

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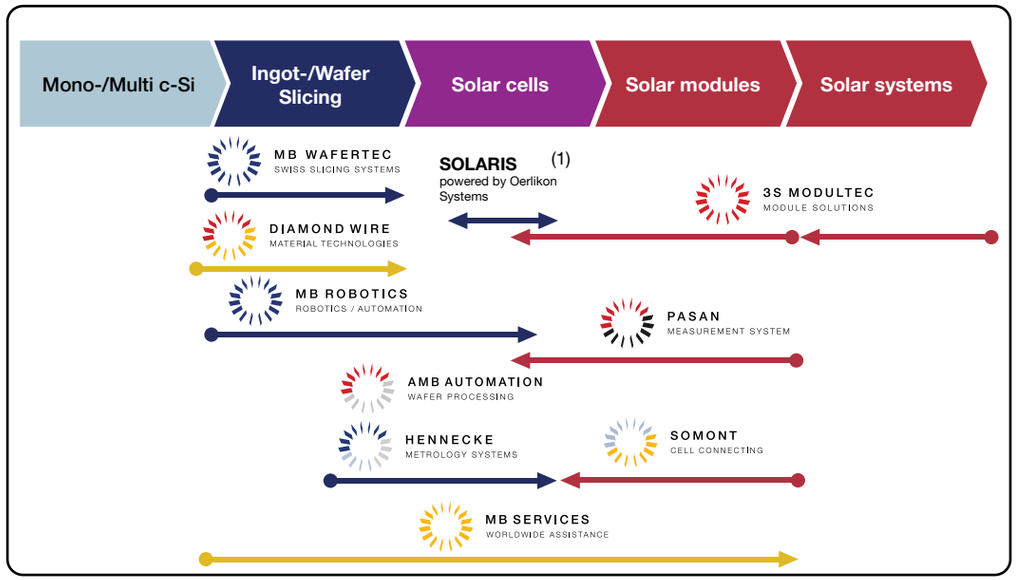
Meyer Burger Technology Ltd is the first global technology group in the solar industry that covers the most important technologies of the photovoltaic value chain, from solar silicon to entire solar systems. The group offers fully integrated manufacturing solutions, comprising machines and automation systems, critical consumer goods, process expertise and local services from a single source. The combination of these core competences is unique in the industry and will enable the significant reduction of costs along the entire production chain, with the aim of achieving faster grid parity for solar power. The companies are the perfect fit in terms of their technology portfolios and geographical presence, and have a global distribution and service network that is unique in the industry.



Meyer Burger Swiss Solar Systems: a unique technology group

Safeguarding and expanding the existing expertise and market know-how in the individual technology and production centers remains a key priority within the group.

Strong global distribution network

The way the companies complement each other is also apparent in the regional distribution centers. The merging of the distribution networks and anticipated cross-selling benefits will increase sales volumes, accelerate global expansion and further strengthen the new Group's presence in its key markets in Europe, Asia and the U.S. With its technology portfolio and strong geographical presence, the new Group will command a powerful global distribution and service network that is unique in the industry.

<< PREVIOUS PAGE | NEXT PAGE >>

Moore's Law of Photovoltaics

Stuart Bowden, Christiana Honsberg, Dieter Schroder
Arizona State University

Abstract

Advanced civilizations require energy – commonly produced today from fossil fuels using *yesterday's sunshine* in the form of vegetation converted to unsustainable coal, oil and gas, and subsequently converted into electricity via electromechanical machinery. The convergence of environmental, social and technical issues highlights the need for new approaches to electricity generation. Photovoltaics (PV) uses *today's unlimited sunshine* to generate energy that is sustainable in perpetuity. However, despite PV's many advantages, today it contributes only a small fraction to total electricity generation. In order for PV to contribute substantially to total electricity generation, it must achieve sustained growth rates of over 40 percent over four orders of magnitude in production volume. Integrated circuits (IC) have achieved such sustained growth rates, famously expressed as Moore's Law. Recasting Moore's Law for photovoltaics shows that PV has the technical characteristics to achieve similar sustained growth rates as the IC industry.

Introduction

Most electricity is generated today with electromechanical machinery, much as it has been since the concept of the electric generator by Faraday in 1832 and the first AC generator by Tesla in 1892. Such generators have served us well, but little has changed in the fundamentals. It was not until 1941 that solid state physics and quantum mechanics were applied to electricity generation through the invention of silicon solar cells at Bell Labs.[1]

Quantum mechanics, the major scientific advance of the 20th century, and semiconductor devices (diodes, transistors, integrated circuits), have had an enormous, transformative impact on society. Lighting, almost entirely controlled by incandescence in the past, has been partially replaced by fluorescence and will be replaced by electroluminescence through light-emitting diodes (LEDs). Displays, which previously used cathodoluminescence in cathode ray tubes, are now almost entirely based on flat panel displays with pixels controlled by thin-film transistors and backlighting by LEDs. The field of communications is controlled by semiconductor devices, through the use of lasers and photodetectors in fiber optics and ICs in wireless communications. While PV is central to satellite power generation, it has made only a minor contribution to terrestrial power generation.

Our present energy systems face "a series of great opportunities disguised as insoluble problems":[2] climate change, uneven geographical distribution, national security and long-term resource supply. PV offers many benefits as a sustainable energy source, including large solar resource, high efficiency and low environmental impact (both in terms of emissions and of water use). Further, PV has high-ideal efficiencies (higher than cogeneration, thermal cycles or solar thermal systems). PV is a robust and reliable technology, and the Bell Labs cell of 1954 still generates power.

Contrary to popular view, solar cells have a **higher energy density** (energy delivered over the lifetime of a device per unit mass of material) than most other energy technologies.[3] The energy density is an important parameter for power generation as it relates the necessary material quantity to generate a given amount of power. It is also a measure of how much material needs to be mined to generate today's and tomorrow's power. Figure 1 shows the energy density of the most common "fuels" used today for power generation. Coal, oil and natural gas have a density of 30-50 MJ/kg. Reactor

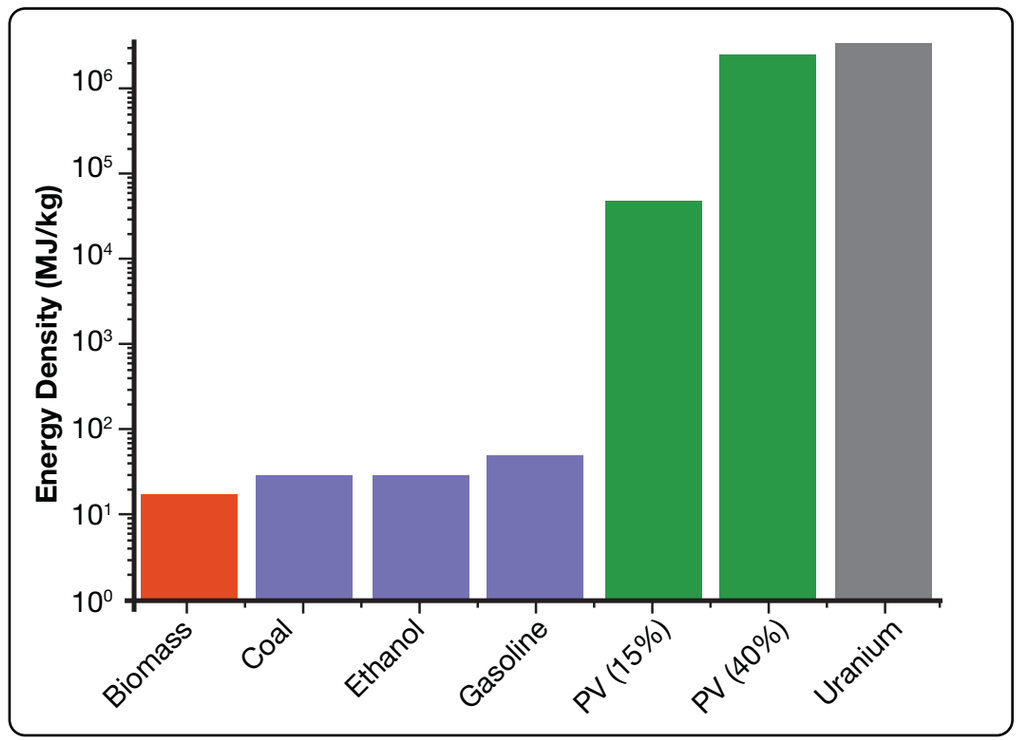


Figure 1 – Energy Density for Common Energy Technologies[4]

<< PREVIOUS PAGE | NEXT PAGE >>

grade uranium has a significantly higher density of 3.46×10^6 MJ/kg. Solar cells come in at a surprisingly high value in the mid 10^4 to the 10^5 MJ/kg range. The high-energy density of solar cells is due to their small volume and their expected life of 20 years. The calculation for the solar cell power density use is – cell efficiency of 15 and 40 percent, cell thickness 200 µm and 2 µm, sunshine for 6 hours/day and 20-year life – all lead to the high values of 5.05×10^4 MJ/kg and 1.35×10^5 MJ/kg.

PV Growth Rates

As shown in Figure 2, photovoltaics has grown at an average compound annual growth rate (CAGR) of 40 percent for over a decade,[5] and even with recent economic setbacks causing slowed growth, it is expected to grow again at 40 percent CAGR in 2010.[6] The photovoltaic experience-cost curve shows the cost of modules decreasing by 20 percent for every doubling of cumulative volume, resulting in many photovoltaic technologies achieving the long-standing cost target of $\$1/W_p$. The present challenge is to continue the photovoltaic growth rate of 40 percent so that photovoltaics can make a significant contribution to world electrical production.

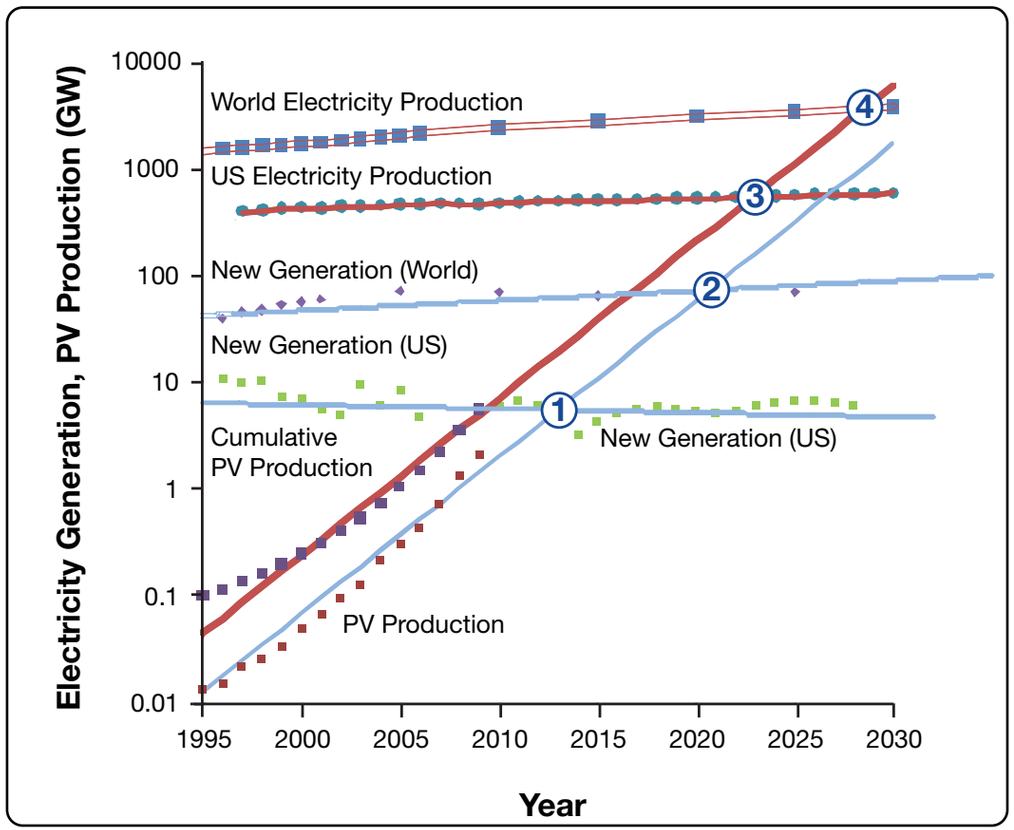


Figure 2 – The rapid growth of photovoltaics of 40 percent CAGR and the slower growth of electricity production of 1.5 percent in the U.S. and 3.5 percent worldwide.[7] The numbered points are described in the text.

A 40 percent growth rate is a necessary and sufficient condition to allow large-scale contributions of photovoltaics to the world electricity grid. Figure 2 illustrates the impact of 40 percent growth curves. Because the PV industry is growing more rapidly than the electricity market, sustained growth allows substantial contributions to the electricity industry in a short time frame. To allow for a direct comparison between photovoltaic production and conventional electricity sources, the photovoltaic production figures normally given in terms of watts peak (W_p) have been divided by a factor of six, corresponding to a yearly production of 1500 kWh/kW, which is typical of the continental U.S. The numbered points in Figure 2 show:

1. In the next five years all ***new*** U.S. electricity production capacity could be met with photovoltaics (although it requires the U.S. to absorb world production).
2. In 10 years, all ***new*** world electricity production could be photovoltaics.
3. Within 15 years, photovoltaic production could meet the entire electrical generation of the U.S.
4. In just over 20 years, the entire world electricity production could be met by photovoltaics.

In practice, the development of an affordable, practical, large-scale photovoltaics industry would increase the electricity market. For example, shifting some of the transport sector to electricity, using electricity to address water issues, or increasing electricity access to the 1.5 billion people (one-fourth of the world's population) presently without access to electricity.[7]

Achieving Rapid Growth and Continuous Improvements: Moore's Law

While PV has demonstrated continuous cost reductions and growth rates of over 40 percent for two decades, it must continue to do so in a broad range of locations sustained over five orders of magnitude change in cumulative production capacity. Cost alone is not a predicator of growth, since it ignores many issues, such as the impact of efficiency and unforeseen barriers related to large-scale production. For example, historical 40 percent growth rates are not predominantly limited by cost; subsidies have maintained the market to the point where manufacturers are challenged to provide PV modules, and even resulted in short-term price increases as manufacturers were sold out several years in advance. "…buying out the experience curve" (i.e., providing subsidies until PV reaches grid parity) is estimated at a total worldwide cost of $60 billion to $160 billion over a 10-year period.[8,9]

The rapid development of ICs is famously expressed as Moore's Law, which describes the doubling every 18 months of the transistor count per unit area. The enabling feature of Moore's Law

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is the existence of a parameter that drives both improved performance *and* reduced cost, circumventing the nearly ubiquitous trade-off between performance and cost in many industries. In ICs, the enabling technical parameter is the gate length, where a shorter gate both improves computer speed and reduces costs by allowing more transistors on a silicon wafer. As formulated for ICs, Moore's Law does not translate to PV[10] since neither efficiency nor module area scale by large factors. While the PV experience curve is often cited as evidence of a "Moore's Law" effect,[11-13] the experience curve does not by itself demonstrate the positive feedback between higher efficiency and reduced cost.

While not directly translatable, the technical features that made Moore's Law possible have analogs in photovoltaics. For example, the analog to transistors/cm^2 is W/cm^3 (where cm^3 corresponds to the volume of material in the solar cell). The volume is the relevant parameter rather than surface area (as in transistors) both

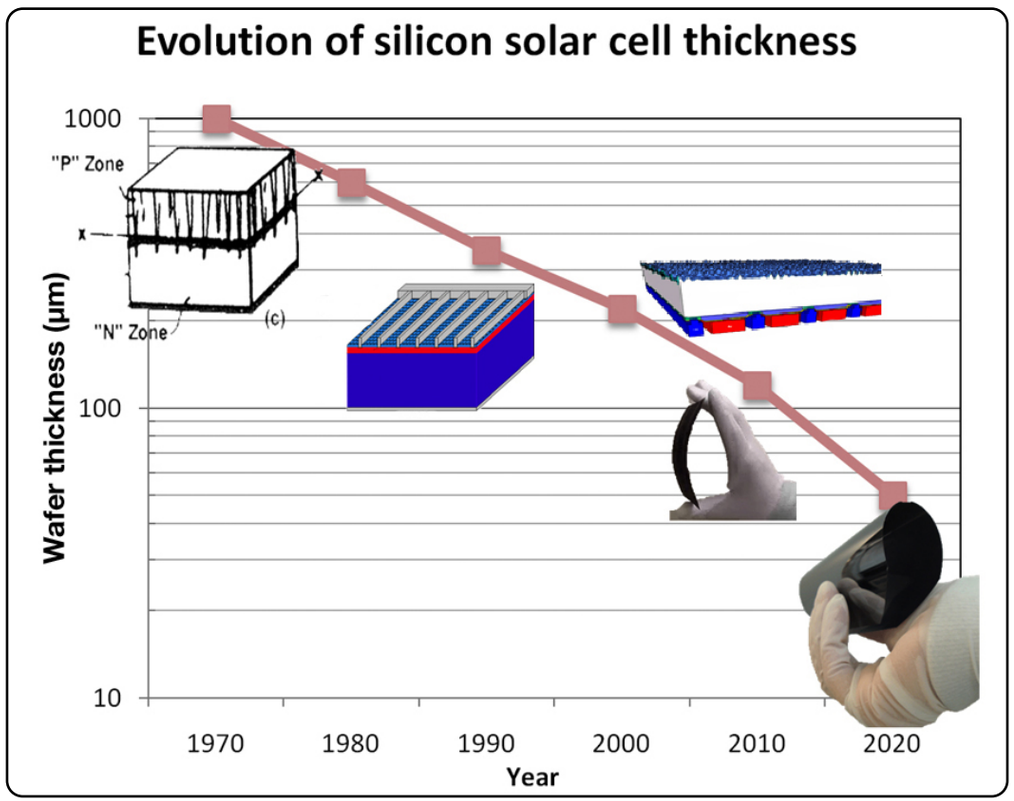

Figure 3 – Evolution of Solar Cell Thickness, Showing Move From 1000 µm to Ultra-Thin Wafers

because PV costs are dominated by material volume in large-scale production and because performance relates to material volume (e.g., in real devices, both absorption and recombination relate to material volume). There are two approaches to decreasing material volume while increasing efficiency: decreasing solar cell thickness and increasing concentration. A thinner solar cell enables higher W/cm^3 by increasing the efficiency (assuming light trapping) and by decreasing material use, making solar cell thickness an analog to gate length in transistors. Plotting the evolution of silicon solar cell thickness (Figure 2) shows the beginning of a "Moore's Law" for PV, where silicon solar cell thickness has decreased from 1,000 µm in early solar cells, to a typical value of 200 µm today, with new wafer technologies as thin as 20 µm,[14] and some solar cells as thin as 2 µm.[15] Interestingly, the change in thickness is numerically similar to the change in gate length in ICs, which decreased from about 5 µm in 1975 to under 50nm today. The combination of increased efficiency, thinner wafers, concentration and other effects will enable a five-order of magnitude improvement in W/cm^3, similar to that experienced in transistors/cm^2 in Moore's Law.

In PV, as in the IC industry, Moore's Law represents *potential* for growth through intensive, focused collaboration and innovation, rather than an intrinsic property realized through evolution. In ICs, speed is not improved by smaller gates unless parasitics are controlled, voltages are scaled and photolithography allows shorter for transistors. Similarly, in solar cells, efficiencies will decrease unless surfaces are improved, yields are maintained and wafer handling and defects are addressed. While the industry is still in its early stages, gains in performance and affordability are achieved through optimization and economies of scale, but continual advances – even beyond those originally predicted possible – are achieved through innovation. The PV industry is at a critical juncture, reaching the limit of evolutionary improvements. Its need for the next decade is collaborative, innovative solutions, driven by a roadmap.

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[<< PREVIOUS PAGE](#) | [NEXT PAGE >>](#)

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Jef Poortmans
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The need to look beyond business as usual

With a view to forecasting the future of photovoltaics, the PV industry and R&D community are currently involved in many roadmap exercises. A majority of these studies assume that photovoltaics will grow by slowly evolving, more than by rolling out breakthroughs and innovative technologies. Thus, for the coming decade, the forecasts mainly emphasize gains through scaling and manufacturing. The goal, eventually, is to bring the costs of photovoltaic systems down by a factor of two.

From an industrial point of view, this is perfectly understandable. However, these forecasts might lead us to underestimate the potential of future breakthroughs – breakthroughs that will be essential for this highly promising industrial sector of renewable energy, especially if we want to reduce photovoltaics costs even further, say, with an additional factor of two.

The two papers in this issue of Future Photovoltaics are a perfect illustration of novel ideas that may eventually lead to further breakthroughs.

The paper of Gupta et al. from Sandia National Laboratories outlines a marriage between microsystems and photovoltaic cell expertise. Their ideas open up the avenue for the smart exploitation of self-assembly as a way to produce highly efficient PV modules and, eventually, full systems.

The paper of Hunter et al. from Intermolecular, Inc. deals with alternative material systems. These could make non-Si thin film cells a sustainable approach by avoiding the use of scarce materials such as indium. Next to the fundamental study of materials, a particularly attractive element in this paper is the combinatorial approach that is used to verify the relevant properties of a broad range of material compositions. This method may improve the learning speed by one to two orders of magnitude. Approaches as these are deemed to play a growing role in the further rollout of photovoltaics.

Microsystems-Enabled Photovoltaics: A Path to the Widespread Harnessing of Solar Energy

Vipin Gupta, Jose Luis Cruz-Campa, Murat Okandan, Gregory N. Nielson
Sandia National Laboratories

Abstract

If solar energy is ever going to become a mainstream power source, the technologies for harnessing sunlight have to become cheaper than all other forms of energy, be easy and quick to install, and work more safely, reliably and durably than present-day grid power. Our research team is striving to make this happen by utilizing microdesign and microfabrication techniques used in the semiconductor, LCD and microsystem industries. In this article, we describe microsystems-enabled photovoltaic (MEPV) concepts that consist of the fabrication of micro-scale crystalline silicon and GaAs solar cells, the release of these cells into a photovoltaic (PV) "ink" solution, and the printing of these cells onto a substrate using fluidic self-assembly approaches. So far, we have produced 10 percent efficient crystalline GaAs cells that are 3 µm thick and 14.9 percent efficient crystalline silicon cells that are 14 µm thick. The costs associated with this module assembly approach in conjunction with optical concentration can be well below $1/Watt$_{peak}$ while retaining the superior conversion efficiency and durability of crystalline silicon and III-V materials.

Our Vision

With the emerging electrification of personal transportation, decentralization of energy generation in places that lack a reliable electricity grid, growing concerns about atmospheric emissions from fossil fuel use, and ever-increasing global demand for electricity, there is an insatiable need for point-of-use technologies that generate electricity in a clean way.

Our group is striving to make microsystems-enabled photovoltaics (MEPV) the most efficient, versatile and inexpensive way to provide that electricity. We envision high-concentration, sun-tracking MEPV for power utilities; low-concentration, flat-plate MEPV for horizontal rooftops; and flexible, integrated MEPV for sloped rooftops, vehicles, gadgets and the human body.

Many things have to be accomplished before photovoltaics become a ubiquitous technology: reducing the amount of necessary high-cost semiconductor material, developing highly efficient cells, achieving long-term durability and reliability, using low-cost packaging substrates, creating scalable high-speed assembly processes, and establishing fast methods to install and wire the grid-connected circuitry.

Several groups across the world,[1-4] including ours, have developed prototype small and ultrathin photovoltaic cells that reduce PV material use dramatically. These ultrathin cells perform nearly as well as thick ones[4-6] that are much thicker than what is necessary for photoelectric conversion simply to minimize breakage during cell processing, handling and assembly.

Figure 1a depicts the normalized cell efficiency (efficiency/potential efficiency) vs. the cell thickness. It shows that ultrathin cells can substantially decrease the cost associated with the use of silicon material while retaining 90 percent of the potential conversion efficiency. This graph assumes a single light pass through

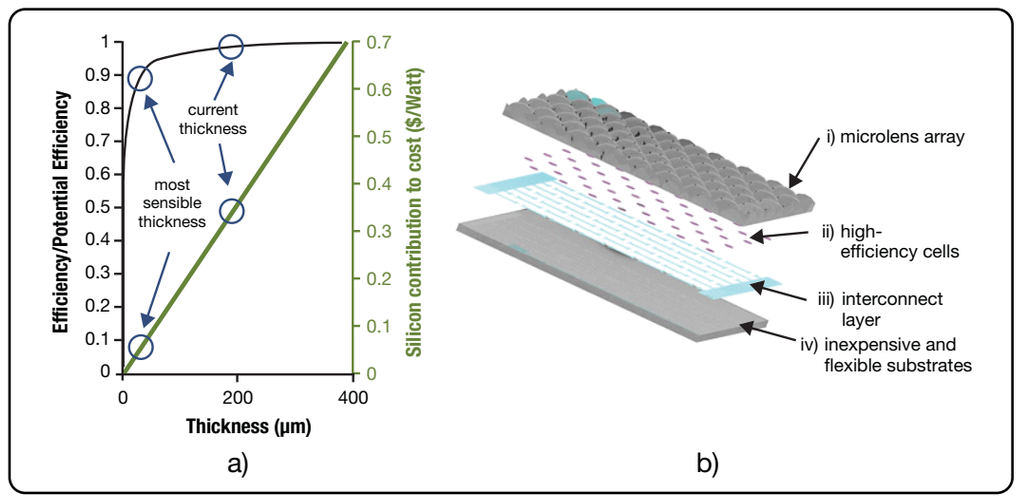

Figure 1 – a) Cost and potential conversion efficiency in silicon solar cells as a function of thickness; b) the microsystems-enabled photovoltaic module concept showing the four distinct layered components

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the cell; adding back reflectors and light trapping structures would further enhance the conversion efficiency and make the knee of this curve move to thicknesses below 10 µm.[6]

Our method integrates multiple technologies in an effort to produce an inexpensive module. Figure 1b shows the four main parts of our approach: i) a microlens array that concentrates the light onto the cells; ii) the ultrathin, small and highly efficient solar cells; iii) an interconnection layer; and iv) the entire system encapsulated in flexible substrates.

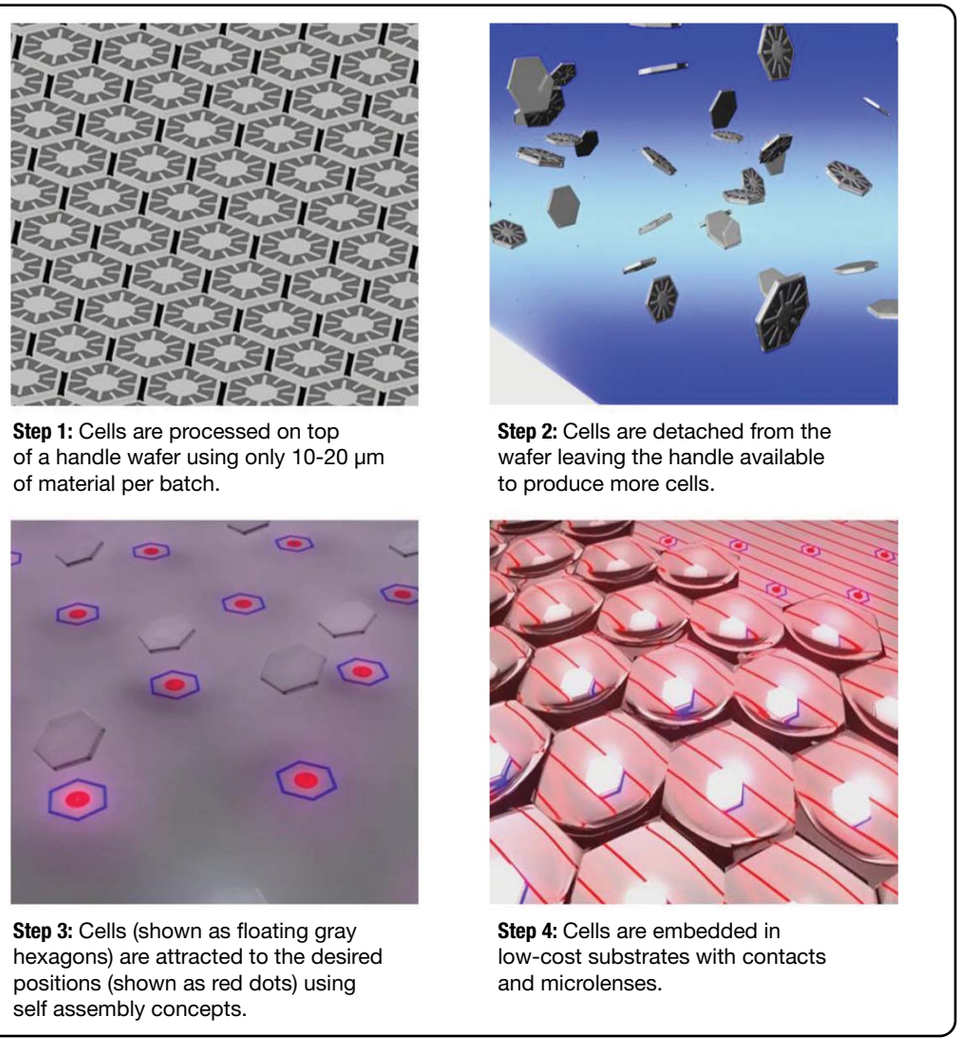

Figure 2 – Process to Create Photovoltaic Sheets of Micro Cells From Cell Liftoff to Final Assembly

Benefits of our Approach

Our approach uses tiny solar cells that are 14-20 µm thick and 250 µm to 1 mm in lateral dimensions. This method enables three main ways of reducing the PV module costs[7]: by making the cells with a small lateral dimension, by creating ultrathin cells and by using micro-concentrators. The small lateral size enables better use of the available wafer area (i.e., reduction in edge die loss), increases area usage through the production of hexagonal cells, and gives semiconductor manufacturers the flexibility to use any wafer size. Thinning the cells reduces semiconductor material costs, improves carrier collection and potentially achieves higher open circuit voltages. The small size also enables the cells to be processed with IC fabrication tools, allowing near-ideal cell performance (>20 percent for c-Si, >40 percent for III-V multijunction cells). Finally, micro-optical elements concentrate sunlight onto each cell, further reducing the need for high-cost semiconductor materials. All together, this three-pronged approach decreases the need for high-cost materials, reduces overall system cost and increases conversion efficiency per gram of utilized PV material.

Another advantage of our method is that it utilizes mature technology, tools and techniques used in the production of microelectronics and microsystems. This enables the production of micro solar cells with consistent IV parameters, high efficiencies and superior robustness compared to conventional large-area thin cells. All of the manufacturing steps (patterning, diffusion, passivation and metalization) are done while the micro cells are still attached to the substrate wafer to facilitate handling. Then, thousands of ultrathin micro cells are detached from the wafer by means of a sacrificial layer or an anisotropic etch (liftoff technique) and released into a solution. Only 15-25 µm of the handle wafer is consumed in each batch and the rest is left available to be reused and produce another lot of micro cells. Each substrate wafer (e.g., c-Si, GaAs, Ge) thus has the possibility of being reused many times rather than being consumed in a single fabrication run.

The micro size subsequently requires novel and workable parallel self-assembly methods[8] to place the cells onto designated spots. These assembly concepts use energy minimization approaches to make arrays of the cells on inexpensive substrates. The cells can be embedded in low-cost flexible materials that produce virtually flat modules. Figure 2 shows the procedure used to create PV sheets using this technology.

In addition to the benefits obtained at the cell level, there are multiple advantages at the module and system level due to the scale of the cells. Small cell size allows the use of inexpensive refractive optics[2] instead of Fresnel optics, giving better optical efficiencies; reduced thickness and small lateral cell size simplifies the management of thermal loads on the PV modules (which is particularly important for optical concentrating designs); the microscale PV concentrator makes high-accura-

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cy and high-bandwidth tracking possible, thereby reducing tracking cost and complexity as well as providing pointing accuracy during windy conditions (due to the high-speed response of the tracker)[7,10]; and finally, small form factor (i.e., thin) concentrator modules with integrated in-plane trackers can be flat mounted at the point of use for the generated electricity.

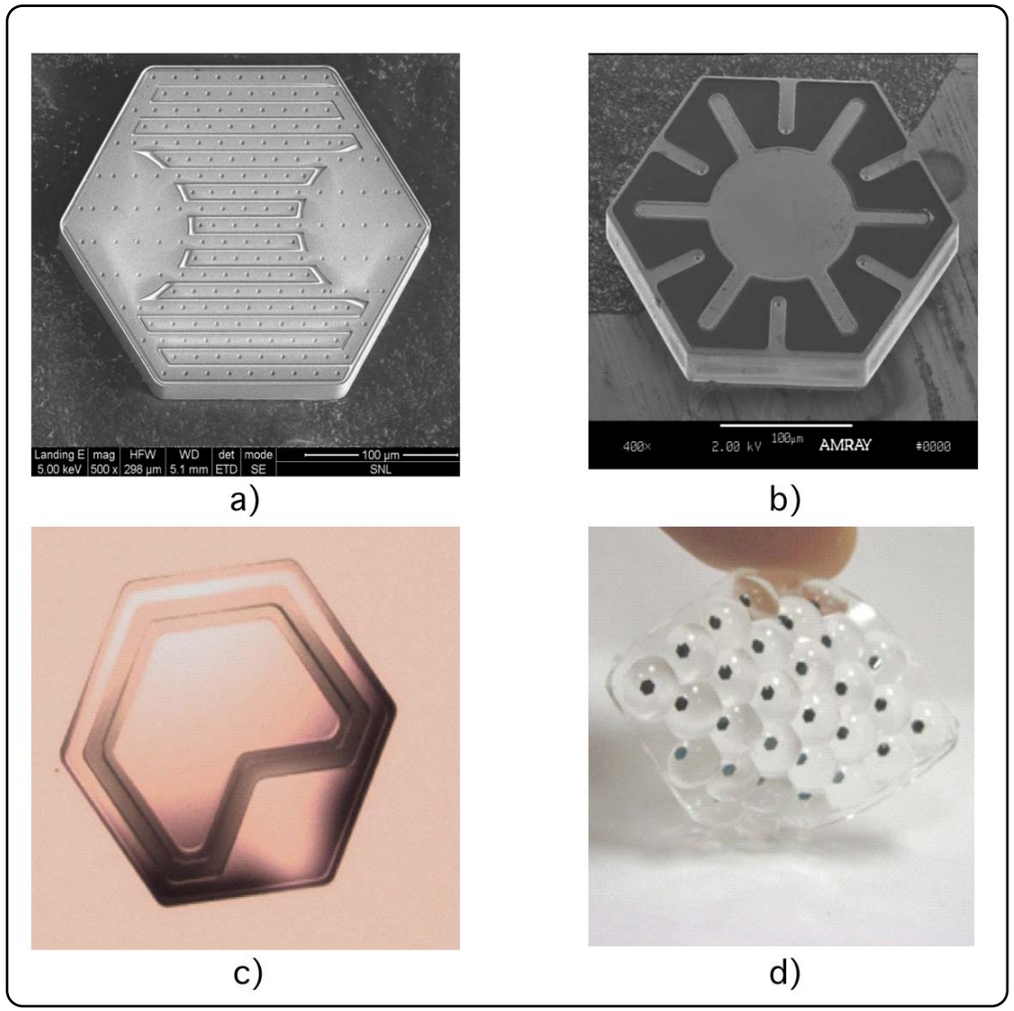

Figure 3 – Pictures of our released solar photovoltaic cells: a) Scanning electron microscope (SEM) image of a 250 µm wide silicon solar cell released through an anisotropic KOH under-etch with lateral interdigitated fingers; b) SEM of 250 µm wide silicon solar cell released using a buried silicon dioxide layer with radial contacts; c) 250 µm GaAs solar cell released using a buried AlAs layer; d) flexible mechanical model with embedded cells and micro optics

Our Results to Date

Our technique produced ultrathin solar cells with lateral dimensions ranging from 250 µm to 1 mm. We have utilized a variety of materials, approaches and designs, including single crystal silicon in (111) or (100) crystallographic orientations and single-crystal GaAs. The approaches differ in the chemistry and technique used to detach the wafers from the cell: (111) oriented silicon wafers require a potassium hydroxide (KOH) anisotropic etch that undercuts the cell, while (100) oriented silicon wafers make use of a buried silicon dioxide sacrificial layer. In the case of GaAs cells, the release sacrificial layer used is AlAs.

The designs of our solar cells include: i) a silicon back-contacted radial pattern; ii) a silicon back-contacted interdigitated format; and iii) an ultrathin, single-junction GaAs cell with back contacts. Figure 3 shows optical and scanning electron microscope (SEM) images from the finished cells using the different materials, approaches and designs as well as a mechanical model with the cells embedded in an inexpensive, flexible substrate with an integrated microlens array.

In order to explore the commercial potential of MEPV technology, a cost analysis was carried out assuming a solar flux of

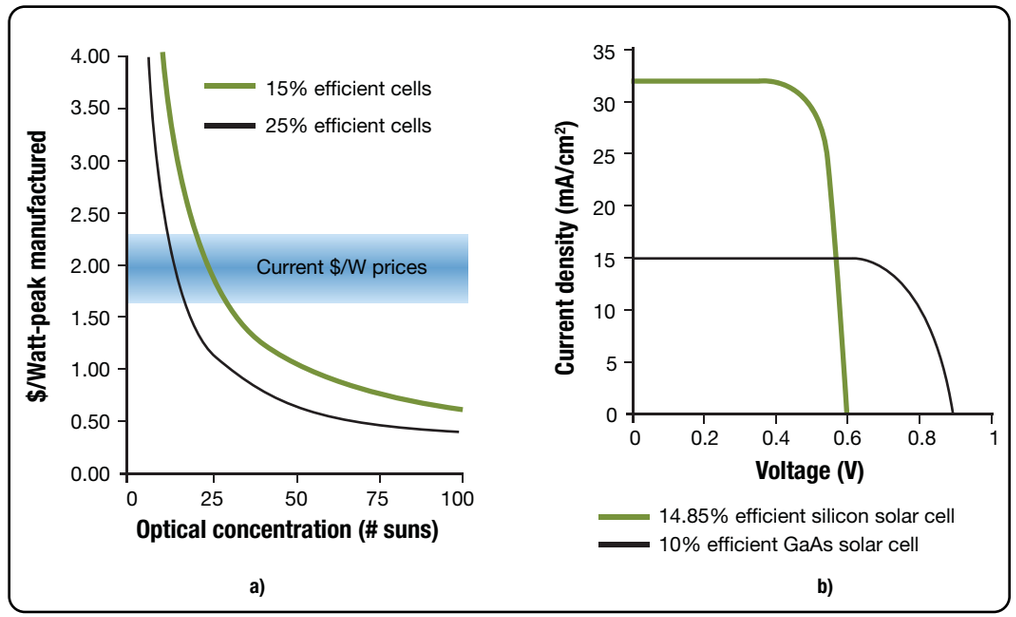

Figure 4 – a) Cost analysis of our technology: $/Watt vs. concentration for different cell efficiencies assuming a $25/m² assembly cost; b) experimental J-V measurement curves of our micro cells

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100mW/cm^2, a process cost of $150/wafer, a wafer diameter of 200 mm, a $25/m^2 assembly cost, and 95 percent overall cell process yield. This analysis revealed that the costs of our technology approach could be well below $1/Watt$_{peak}$ by using moderate concentration (below 50x) and massive parallel assembly. Figure 4a graphically shows the results of these calculations.

So far, our technology has produced 14.9 percent conversion efficiency for 14 µm (13.7 +/- 0.38 µm) thick cells made from crystalline silicon and 10 percent conversion efficiency for 3 µm thick cells made of GaAs.[11] This level of performance is comparable to the conversion efficiency in available commercial silicon-based modules with PV cells that are 10-15x thicker. Figure 4b shows the current density-voltage curves (J-V) for two of our cells. Both cells were tested with a solar simulator normalized to 1000W/m^2 using a silicon reference solar cell.

Conclusions

In the United States, solar energy generation, including photovoltaics, presently produces 0.1 percent of the energy used for electricity, heating and transportation. If PV adoption is to grow at a compounded annual growth rate of 40 percent per year and thereby become a 40 percent contributor to the U.S. and global energy portfolio within one human generation,[12] a series of technology breakthroughs are needed in PV cell development, assembly, installation, operation and end-of-life retirement.

The microsystems-enabled photovoltaic concepts described in this article show one technology pathway to realizing this vision. The 10 percent efficient, 3 µm thick crystalline GaAs cells along with the 14.9 percent efficient, 14 µm thick crystalline silicon cells developed by our team suggest that there are breakthrough possibilities along this pathway. Combining these experimental results plotted in Figure 4b with the parallel self-assembly approach illustrated in Figure 2 as well as the cost analysis shown in Figure 4a, there appears to be a reasonable probability of developing a MEPV manufacturing approach that is as low or perhaps lower in U.S. dollar per Watt-peak cost than all other forms of energy, including PV thin film technologies.

Contrary to the popular belief espoused by futurist thinker Tom Friedman, the world is not flat.[13] It is filled with the various shapes and curved contours of natural terrain, large manmade structures, portable electronics, vehicles and the human body. All of these prospective PV hosts are becoming ever more ready to adopt efficient, versatile and inexpensive photovoltaic devices for powering important things. Microsystems-enabled PV can provide those devices, and our research team is committed to doing our part to develop the technological means of making it so.

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<< PREVIOUS PAGE | NEXT PAGE >>

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Optimization of Earth-Abundant Photovoltaics Through High-Productivity Combinatorial Technologies

Tony Chiang, Jian Li, Craig Hunter, Michael McElfresh
Intermolecular, Inc.

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Introduction

Increasing demand for environmentally friendly, sustainable renewable energy sources has driven significant investment in thin film (TF) photovoltaic (PV) devices. The long-term goal of providing a meaningful percentage of global energy supply will eventually drive the need for low installed-cost (<$1/$W_p$) photovoltaic systems that exclusively employ earth-abundant materials. A number of earth-abundant direct band gap semiconductor materials have the potential to enable both high efficiency and extremely low cost in very-large-scale production (100+ GW), yet relatively little attention has been devoted to their development and characterization.

Among all thin film PV technologies, $Cu(In_x,Ga_{1-x})Se_2$ (CIGS) and CdTe are the only two that have reached volume production with >10 percent stabilized module efficiencies. Solar cell production volume must ramp tremendously in the coming decades to meet sharply growing global energy needs that are expected to double to 27 TW by 2050. However, the supply of indium, gallium and tellurium may inhibit annual production of CIGS and CdTe panels to <100 GW.[1] Both the price and availability of indium and gallium are increasingly uncertain due to competing demand from other industries, including flat panel displays, LEDs and a number of other semiconductor device applications. Anticipated aggregate demand for gallium in 2030, for example, is expected to be six times the current global supply.[2] Moreover, indium prices have already exhibited tremendous volatility in accordance with LCD production cycles. Location of these raw material resources is also a concern for PV companies in many geographies, as China controls a significant portion of the global supply of gallium (83 percent) and indium (60 percent),[2] and has recently signaled willingness to restrict export of strategic raw materials.[3] In short, efforts to develop high-efficiency thin film PV devices using more widely available raw materials are critically important if thin film PV is to play a meaningful role in the future global energy supply.

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Copper-zinc-tin-sulfide (CZTS, Cu_2ZnSnS_4) kesterites are one type of "earth abundant" material system that is garnering increasing interest from the PV community. IBM recently announced a champion 9.66 percent conversion efficiency $Cu_2ZnSn(Se,S)_4$ (CTZSS) solar cell,[4] a tremendous advancement over the previous record CZTS cell of 6.7 percent efficiency.[5] While the IBM approach has some drawbacks,[6] the sharp efficiency improvement over a very short period of time illustrates the potential of CZTS-type materials for PV as well as the benefit of placing a focused effort on their development. Nevertheless, there still exists an enormous gap between demonstrated efficiency and the 32 percent theoretical single-junction efficiency for this class of devices.[7]

The current immaturity of thin film PV devices that exploit earth-abundant materials represents a daunting challenge in terms of the time-to-commercialization. That same immaturity also suggests an enticing opportunity for breakthrough discoveries. A quaternary system such as CZTS requires management of multiple kinetic pathways, thermodynamic phase equilibrium considerations, defect chemistries and interfacial control. The vast phase space to be managed includes process parameters, source materials choices, composition and overall integration scheme. In addition, the back contact layer, buffer layers and the transparent conducting layer greatly expand the phase space for development of a device. Traditional research and development methods are ill-equipped to address such complexity, and the resulting slow pace of development is a major reason why it takes so long to move from concept to volume production for any new material system.

Combinatorial-based rapid device prototyping methods pioneered by Intermolecular, Inc. permit fabrication, comprehensive characterization, and analysis of hundreds of unique solar cells on a weekly basis, systematically and comprehensively exploring alternative device structures, process integration schemes and materials compositions at speeds that would otherwise be impossible using traditional methods and systems. This capability applied to earth-abundant thin film PV research and development would cut the development cycle dramatically and bring commercial production of these devices much closer to reality.

CZTS PV Devices

Cu_2ZnSnS_4 (CZTS) is a compound semiconductor that derives from the chalcopyrite structured I-III-VI_2 compound CIGS, where indium/gallium is substituted by zinc/tin and selenium by sulfur. The substituted elements in CZTS are comparatively order(s) of magnitude more abundant and correspondingly much cheaper than CIGS elements. CZTS has been reported to have a direct band gap between 1.45 and 1.6 eV, which is very close to the optimum value of an absorber layer of a solar cell.[8-11] Additionally, the absorption coefficient of CZTS is on the order of 10^4 cm^{-1}, making it an attractive candidate for a thin film solar cell absorber.[12]

A standard CZTS device structure (see Figure 1), would require deposition of four primary layers on a substrate: a back contact (typically Mo); an absorber layer (CZTS); a buffer layer (e.g., CdS or ZnS); and a front contact (typically ITO or Al:ZnO). The wide range of options associated with each material and deposition process provides an opportunity to reduce manufacturing costs and increase cell efficiencies.

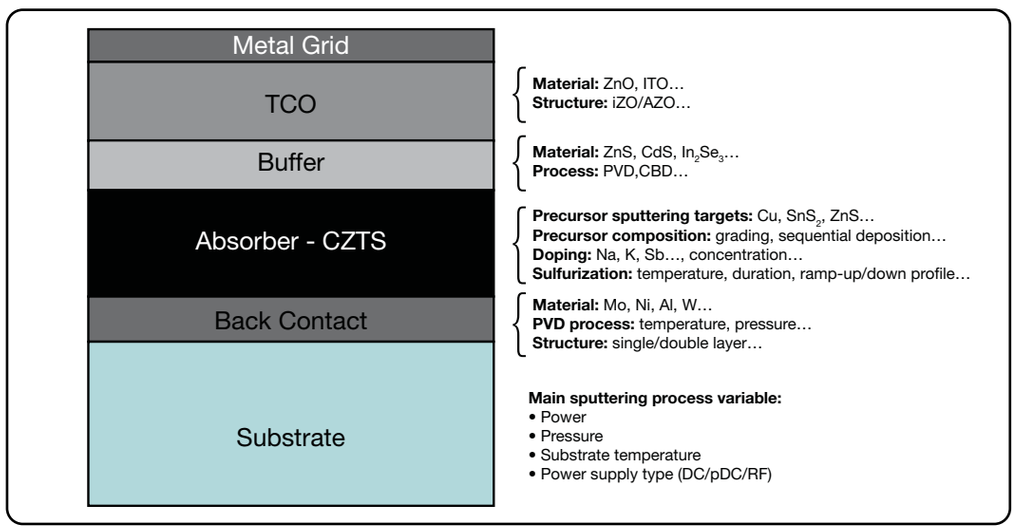

Figure 1 – Key Material/Deposition Process Variables Illustrating the Large Process/Material Space for CZTS Device Optimization

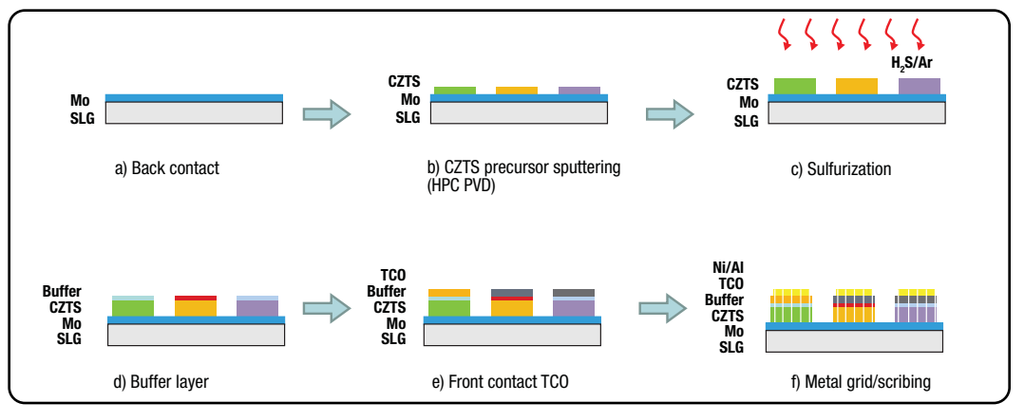

Figure 2 – A High Productivity Combinatorial (HPC) Work Flow for High-Throughput CZTS Solar Cell Development and Optimization

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Various techniques have been used so far for depositing the critical CZTS absorber layer. These techniques include electron beam deposition followed by sulfurization,[12-14] hybrid sputtering,[15] vacuum evaporation with sulfurization,[16] sol-gel followed by H_2S annealing,[17] pulsed laser deposition,[18] sputtering followed by sulfurization,[5,8] single-step RF sputtering,[18] electroplating [20,21] and spray pyrolysis.[22]

For the absorber layer, the fundamental physical properties of CZTS/CZTSe such as ground state structures and optical properties are still far from well understood. The band gap of CZTSe reported in the literature,[23-25] for example, is much lower than the theoretically predicted value.[26] The stable chemical potential region for the formation of stoichiometric quaternary CZTS is predicted to be small due to competing secondary phases such as ZnS. Also, p-type doping in CZTS is more difficult than in the ternary compounds such as $CuInSe_2$.[7]

Intermolecular HPC Work Flow for CZTS

Intermolecular has developed and successfully used high-productivity combinatorial (HPC) work flows in the semiconductor industry to increase R&D learning rates by 100x or more. Comprising custom-built HPC processing equipment, electrical-test vehicles, characterization suites and customized software for design-of-experiments, automated execution and data management/analysis (informatics system), each component of the work flow is designed to provide fast and efficient exploration of the materials process space and integration into device structures. Intermolecular's unique HPC systems and methods dramatically accelerate each stage of working with a new PV material: discovery, development, optimization and manufacturing scale-up.

While there are many approaches to depositing CZTS, the relative immaturity of the devices coupled with the general lack of fundamental understanding of these materials favor the use of mature and repeatable deposition techniques that allow the researcher maximum compositional and uniformity control and flexibility. Intermolecular proposes to start with a CZTS work flow leveraging its proprietary HPC sputtering and wet processing platforms developed over the past five years for acceleration of advanced semiconductor research and development for integrated circuits. A program recently started at Intermolecular focused on CIGS optimization uses analogous methods, and some early results are shared below.

In the simplest HPC CZTS process flow as shown in Figure 2, the incoming glass would start with an already-deposited molybdenum back contact (later iterations of this flow could involve combinatorial exploration of lower-cost back-contact materials as integrated into various device compositions).

The glass would be cleaned and loaded into an Intermolecular Tempus™ P-30 combinatorial PVD (sputtering) chamber to deposit site-isolated, uniform CZTS precursors (e.g., Cu/Zn/Sn, or Cu/ZnS/SnS) as shown in Figure 2b. Figure 3 shows the Intermolecular HPC sputtering chamber in more detail, with its unique capability to deposit sequenced and simultaneous co-sputtered uniform films under a variety of conditions in a site-isolated manner. A novel dual rotary stage (see Figure 3b) and aperture system enables site-isolated thin films to be deposited on a given substrate at a set of specified locations. Co-sputtering allows a variety of compositions to be deposited using four completely independent sputter sources. The spacing between the substrate and the sputter target of each gun can also be independently controlled. The tool supports four different process gases so that depositions can be done using

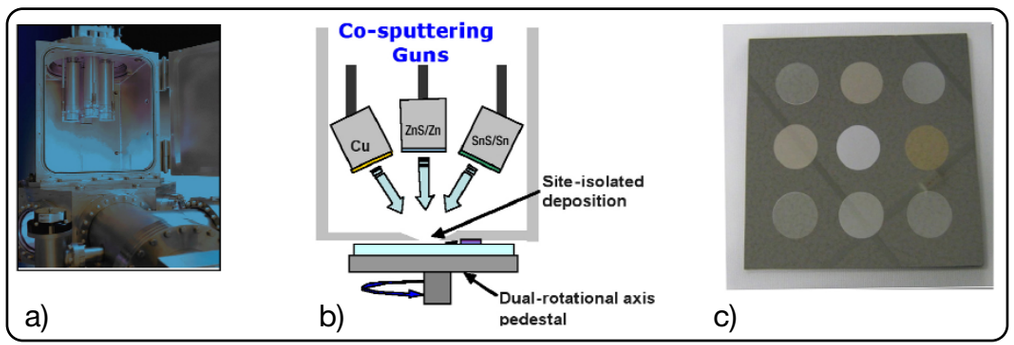

Figure 3 – a) Photograph of an HPC P-30 PVD chamber; b) schematic view of proposed CZTS precursor co-sputtering (up to 4 sputter sources available); and c) top view of a 5" x 5" Mo-coated soda-lime glass substrate with site-isolated CIG sputtered films

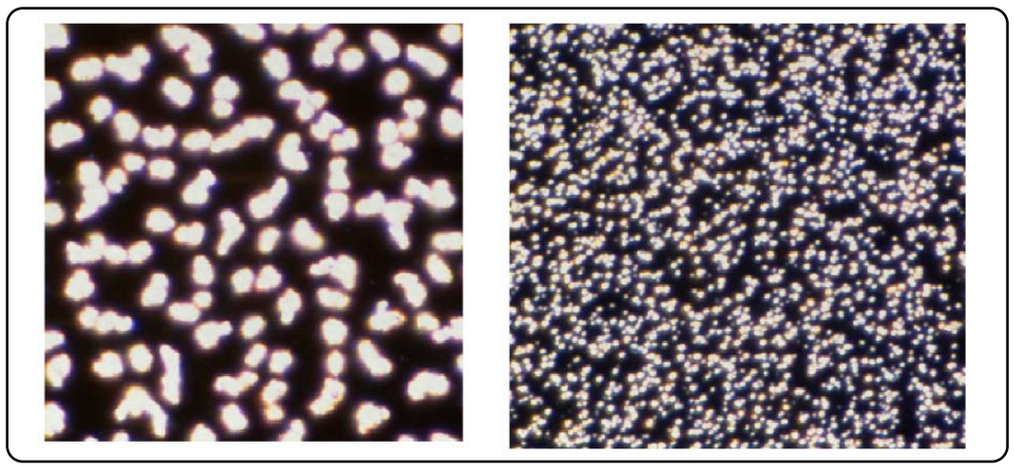

Figure 4 – Morphology changes with deposition parameters, as shown in these plan views with equal magnification of two CIG films deposited on the same Mo back contact. The nominal nodule size is reduced by approximately an order of magnitude. Thickness and composition are fixed.

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reactive sputtering. The power sources for the sputter guns can be DC, pulsed DC or RF.

The P-30 chamber allows deposition of site-isolated regions, typically 10 mm to 30 mm in diameter, without angular artifacts and with excellent within-spot and spot-to-spot uniformities. As a result, arrays of different complex multi-layer stacks and graded pre-reacted absorber layers can be deposited on a single substrate (see Figure 3c). The result is the ability to rapidly build up unique CZTS stacks with excellent control over film composition, deposition parameters and thickness.

When HPC sputtering methodologies were applied to a baseline CIGS device system using Cu, CuGa and In targets, deposition rates for each material increased linearly with sputtering power and were in the 1 to 5 Å/s range for nominal target powers up to a few hundred watts. Co-sputtering allowed for the precise control of film stoichiometry within uniform binary and ternary layers for complex stacking experiments. Since co-sputtering provides additive fluxes from multiple sources, the net deposition rates are the sum of the individual fluxes, and the resulting stoichiometry is a function of the relative fluxes. Site-to-site and within-site repeatability and uniformity has been excellent at ~2 to 3 percent thickness and sheet resistance variation for the materials sampled.

Figure 4 shows an example of the large difference in resulting film morphology that can be derived through control of sputtering recipe parameters. Cu-In-Ga pre-reacted absorber layer films were deposited under varying conditions in the HPC P-30 chamber, keeping the thickness and composition fixed. The morphology changed dramatically, from nominally ~1 to 10 µm nodule size (left) to an order-of-magnitude reduction in nodule size (right), due only to changes in the sputtering recipe. With proper control, the nodule size can be further reduced and morphology improved such that AFM measurements show merely 10nm RMS surface roughness.

The inherent complexity of the interaction of, and interdependencies between, materials, process and device presents an enormous obstacle to rapidly advance novel PV materials. Often phase stability is found only in a narrow window and even small changes in material composition can significantly influence device results. For example, researchers have shown that sodium doping, intentionally or indirectly via out-diffusion from the soda lime glass substrate, can boost CIGS efficiency significantly. Yet the fundamental mechanism driving this behavior is still not well understood even today. Using the HPC P-30 chamber, doping studies for CZTS can be systematically and controllably explored using the fourth sputtering source.

As illustrated in Figure 2c, following deposition of the precursor materials, the proposed CZTS flow would require cells to be submitted to sulfurization in a high-temperature furnace (500 to 600°C) in an H_2S gas or sulfur vapor environment. Each of the nine areas on the substrate would have a unique CZTS precursor stack, and all of them would then be subject to the same sulfurization process. Sulfurization for CZTS is analogous to post-selenization used in the two-step CIGS process flows in which a ternary CIG layer is reacted with selenium to form the final desired absorber layer.

A buffer or "window" layer deposited on the p-type CZTS layer (see Figure 2d) forms the p-n junction and may serve to minimize surface recombination. CdS by chemical bath deposition is often the material and process of choice, but Cd-free buffer layers (e.g., ZnS) are of high interest, and may be applied by sputtering, wet processing or atomic layer deposition (ALD). Top contact transparent conductive oxides (TCOs) would typically be deposited by sputtering as shown in Figure 2e. Indium tin oxide (ITO) is often used due to its conductivity, optical transmission and durability, but some form of doped ZnO is likely to prove a lower-cost, acceptable performance alternative. Utilizing Intermolecular's HPC tools (the Tempus™ F-20 for wet processing, the P-30 for sputtering and the A-30 for ALD) opens opportunities to rapidly conduct cross-product studies across the layers of a CZTS cell. For example, the researcher may choose to deposit three absorber materials across nine site-isolated spots, and then deposit unique TCOs in each of the three repeat cells, thereby having a 3 x 3 matrix in a single run.

To complete the cell, as illustrated in Figure 2f, a top-layer metal grid is deposited using sputtering or evaporation with shadow masks. The cells are then defined with mechanical or laser scribing, with the cells now ready for testing.

Each substrate prepared in this fashion would contain at least nine unique sets of CZTS solar cells – each set in some way different from the others in terms of materials, composition, process, process integration or device structure. Temperature is the only global variable during processing of a single substrate, but would

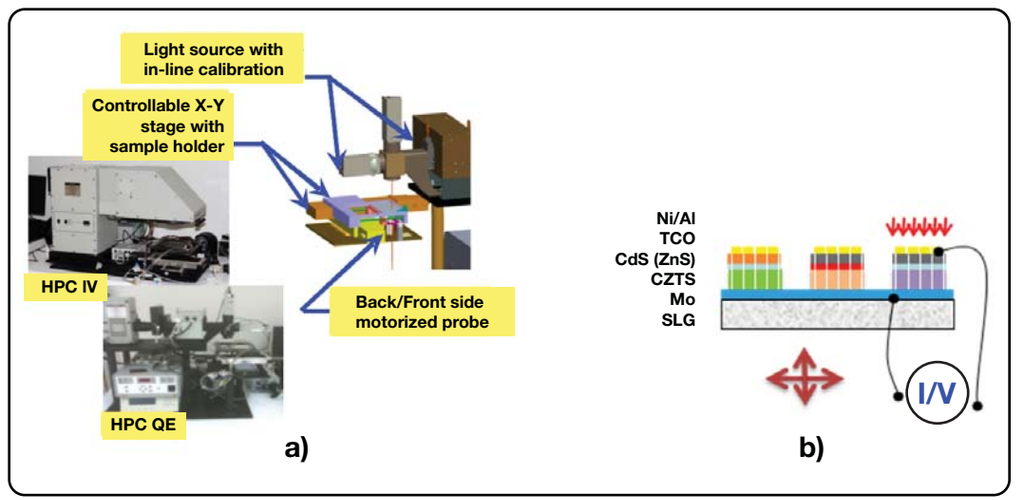

Figure 5 – a) Integrated HPC current-voltage and quantum efficiency (IV/QE) metrology tools with controllable X-Y stage and automatic probing; b) schematic view of high-productivity solar cell characterization with HPC IV/QE tools

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easily be varied from substrate to substrate. Each set (the circles shown in Figure 3c) can be scribed into eight 5 mm x 9 mm CZTS cells to provide multiple points of information for each unique experiment. At full-scale development, it is expected that four to six such substrates, each containing 72 solar cells, will be prepared each day.

Manual testing of the resulting ~300 to 400 solar cells generated each day would be impractical and unreliable. For this reason, Intermolecular developed an automated HPC current-voltage and quantum efficiency (IV/QE) testing system (as shown in Figure 5a) to measure and characterize each cell in a high-throughput fashion (see Figure 5b). Substrate and superstrate thin film solar cells as well as traditional crystalline silicon solar cells can be prepared and measured in this manner. All data from the process parameters, process history, design-of-experiments and finished solar cell results are captured in the Intermolecular Informatics database to facilitate analysis of results.

Across a single year, an HPC work flow would permit exploration and comprehensive characterization of more than 10,000 permutations on the CZTS solar cell.

Conclusions

Thin film materials such as CZTS appear to offer the potential for abundant and inexpensive PV solar energy generation. HPC work flows provide the ability to rapidly and efficiently explore and optimize CZTS materials for integration into a complete solar module. Intermolecular's existing HPC sputtering and wet processing tools enable development work flows that would permit rapid and comprehensive exploration of photovoltaic devices, including those employing novel material systems such as CZTS.

The ongoing goal is to optimize a full CZTS solar cell, requiring the full characterization of the many complex interdependencies within the material/process/structure space. This approach and scale of effort is expected to significantly advance world-record efficiencies. More importantly, the combinatorial approach to process windowing and characterization would dramatically reduce time-to-commercialization. A more fundamental understanding of the device and process-dependencies resulting from Intermolecular's HPC work flow will permit procurement/development of more cost-efficient production tooling, facilitate rapid debugging of pilot lines and drive faster ramps to very-large-scale production.

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☞Click here to return to Table of Contents

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<< PREVIOUS PAGE | NEXT PAGE >>

Click here to return to Table of Contents

Mike Moore
Vice President, SVTC Solar

In the consumer-based society in which we live, the expectation is always that we will receive more value in the products we buy every year. As engineers and businesspeople in the solar industry, it's our job to continue to meet this expectation. Many of us have migrated from the semiconductor industry where we are very familiar with the continued scaling predicted in Moore's Law. The expectation of continuous improvement is also very active in the solar industry, with the unrelenting drive to grid parity and beyond.

In this issue of Future Photovoltaics, you will find three examples of how innovation is happening and has happened in the crystalline silicon (cSi) space.

Researchers from imec report on a potential solution to reduce the silicon content, thus reducing the highest individual cost component in manufacturing cSi-based solar cells. While achieving efficiencies above 18 percent with an iPERC cell on 130 micron thick wafers, they also address the major challenges with wafers this thin of wafer bowing and carrier recombination.

Chandra P. Kattak from GT Solar reviews the progress that has been made in the last 35 years in the manufacturing of silicon wafers for solar cells. Since the silicon requirements for solar cells and integrated circuits are different, the evolution has taken very different paths. Dr. Khattak leads us through the progression for the basic Bridgman process to where we are today with high-volume multi-crystalline manufacturing processes based on evolutionary changes from this early starting point.

The third article is a summary of the outcome of the 2nd Workshop on Metallization of Crystalline Silicon Solar Cells. At this conference, almost 200 of the industry's top engineers in metalization met to discuss future trends. As you will see in this summary, there are still many opportunities, including new pastes, multiple-pass screen-printing, and various plating techniques to optimize the metalization schemes to increase efficiencies. Results of a survey are also included, the general consensus of which is that screen-printing will be the major form of metalization for the next decade.

Future Photovoltaics
SILICON WAFER PHOTOVOLTAICS

Click here to return to Table of Contents

GT Solar (NASDAQ: SOLR), headquartered in Merrimack, N.H., is a leading global provider of PV manufacturing equipment, process technology and services for the solar industry. The company's products and services allow its customers to optimize their PV manufacturing environments to achieve lower cost of ownership.

Polysilicon production services – Our polysilicon business offers CVD reactors and related equipment engineering service such as trichlorosilane (TCS) and silane engineering services to existing polysilicon producers and new market entrants. Our CVD reactors utilize the nonproprietary Siemens process, a widely used and proven polysilicon production process that has been in existence for nearly 50 years.

Multi-crystalline ingot growth furnaces – The primary focus of our photovoltaic business includess the manufacture and sales of DSS crystallization furnaces and ancillary equipment required in the operation of DSS crystallization furnaces to cast multicrystalline silicon ingots. We have established a leading position in this market with over 1,300 systems installed. We also provide turnkey integration services to new PV market entrants looking to establish high-volume, integrated manufacturng environments for the production of wafers, cells and modules.

Services – We have been doing business in China since 2002 and are continuing to expand our base of operations to better serve the growing number of our China-based customers. In September 2009, we opened our Shanghai production facility to provide spare parts inventory, a demo and training center, and other customer service capabilities fo our Asia-based customers.

Innovations in Thin-Wafer Silicon Solar Cells Boost Efficiency Beyond 18%

Els Parton, Jef Poortmans
imec

Abstract

The photovoltaic market is dominated by solar cells based on bulk crystalline silicon with a market share of more than 90 percent. Research focuses on keeping the costs down while improving the efficiency. This is just what the Belgian research institute imec has done: making thinner (thus cheaper) wafer-based solar cells with efficiencies above 18 percent.

The unifying theme of the solar community is cutting down costs while maintaining or increasing the conversion efficiency of solar cells.

When analyzing the cost of present silicon solar cells, about 50 percent of the cost is related to the silicon used as a substrate. If you thereby take into account the (temporary) lack of polysilicon feedstock, it looks like a wise decision to look for new concepts using less silicon. In the case of wafer-based silicon solar cells, research roadmaps predict wafers as thin as 40 µm.

Recently, some major steps toward this ultimate thin wafer-based solar cell were taken. Researchers developed industry-applicable processes to make adjustments on the front and back side of the solar cell, enabling a cell that is 130 µm thick (as compared with conventional 220 µm thick cells) and that exhibits over 18-20 percent efficiency (as compared with 16-17 percent for today's wafer-based solar cells).

Wafer Bowing

It's a nice idea to use thinner wafers, but putting it into practice is a bit more difficult. The first obstacle one encounters is wafer bowing. This is mainly caused by phenomena at the solar cell back side. In standard solar cell processing, aluminum is applied to the complete back surface to serve as metal contact. The alloying process and the thermal mismatch between the silicon substrate and aluminum cause an extended stress field, which is translated into bowing in cases where thinner wafers are used. Obviously, the bowing creates several problems in wafer handling and module manufacturing.

Carrier Recombination

Another problem with thinner wafers is the carrier recombination at the back side of the solar cell. The region at the back side that is highly doped with aluminum (called "aluminum back surface field," or BSF) provides only moderate surface passivation. For very thin cells, the back-side recombination phenomenon gains in importance and causes losses both in terms of short-circuit current density and open-circuit voltage.

Solution: Local Instead of Full Aluminum BSF

The answer to both problems mentioned above is the use of local aluminum BSF contacts. Imec developed industry-applicable techniques to achieve this. In contrast to standard solar cell processing, the aluminum is not deposited directly onto the back of the silicon substrate. Instead, a SiO_2/SiN dielectric layer is deposited using a low-temperature deposition technique and is subsequently laser-perforated. On top of this, aluminum is screen-printed and fired to form local BSF contacts through the perforations.

The use of local aluminum BSF has many advantages:

- The bowing problem is completely eliminated because the stress induced by aluminum-alloying is only local.

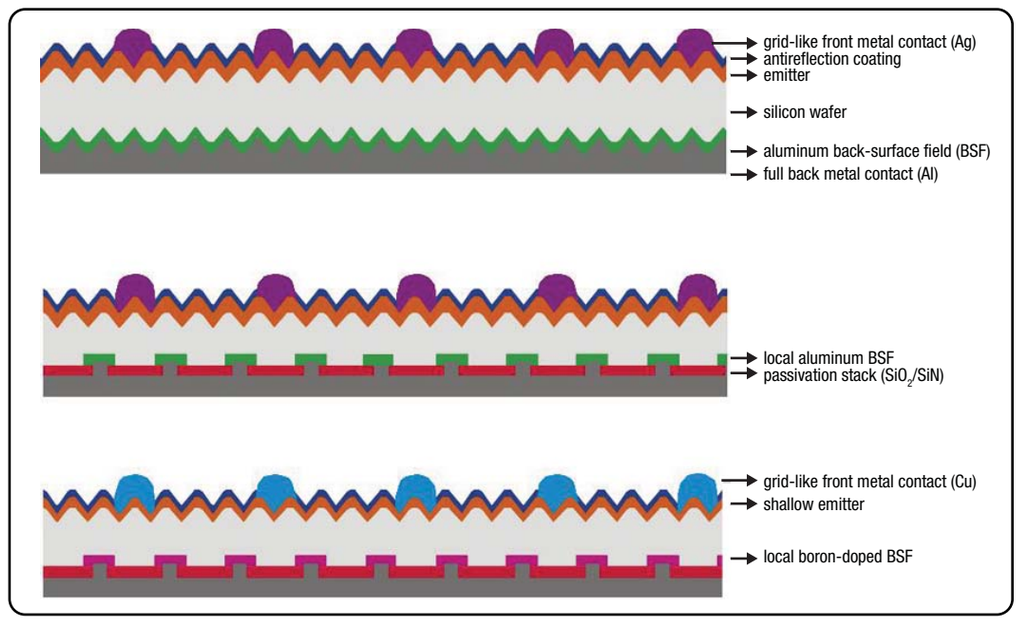

Figure 1 – Cross section of solar cell concepts showing a standard solar cell (top), and the innovations realized by imec to boost the efficiency above 18% with thinner wafers. All processes used are industry-applicable.

<< PREVIOUS PAGE | NEXT PAGE >>

Even for wafers as thin as 80 µm, no bowing is observed.

- A large part of the silicon is isolated from the aluminum, which reduces the carrier recombination at the back side. As a consequence, the short-circuit current and open-circuit voltage are increased again.
- The back-side structure of the solar cell when using these processes is more reflective at infrared wavelengths beyond 1000nm than the standard cell with full aluminum BSF. This is because of the polishing as well as the reduction of infrared-free carrier absorption due to the area reduction of highly doped regions at the back side. This improves light confinement and thus conversion efficiency.

The solar cell concept described here is also referred to as iPERC and is being licensed to solar cell manufacturers.

A crucial aspect of the iPERC concept is the need to decouple the surface treatments for the front and back side. To achieve an excellent back-side surface passivation, the surface must be flat, whereas the front needs to be textured. For this reason, plasma texturing processes were developed to enable this surface decoupling. The processes are applicable on any type of wafer of any thickness.

Shallow Emitter

To increase solar cell efficiency, the optimization of the emitter is crucial. The emitter design can be improved by lowering the surface concentration of dopants near the surface. Simulations show that the highest cell efficiencies are achieved with emitters with a surface concentration around 10^{19} at/cm^2 and a junction depth around 1 µm. The increased efficiency of solar cells with a shallow emitter is related to a better blue response.

Imec researchers developed an industry-applicable process to make a shallow emitter. The process is based on an industrial diffusion process using $POCl_3$. A drive-in step is added to move the dopants deeper into the silicon, thus lowering the surface concentration. Next, the highly doped top layer is removed by chemical etching.

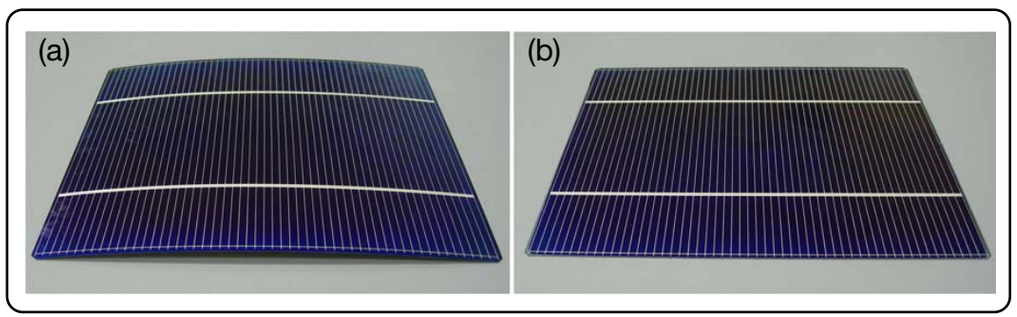

Figure 2 – With thinner wafers, the wafers start to bow if the standard solar cell structure is used. When shifting to local aluminum BSF instead of full aluminum BSF, this problem is resolved. Wafers as thin as 80 µm become possible without bowing. (a) 156 cm^2 130 µm-thick silicon solar cell with full Al BSF; (b): 156 cm^2 130 µm-thick silicon solar cell with local aluminum BSF.

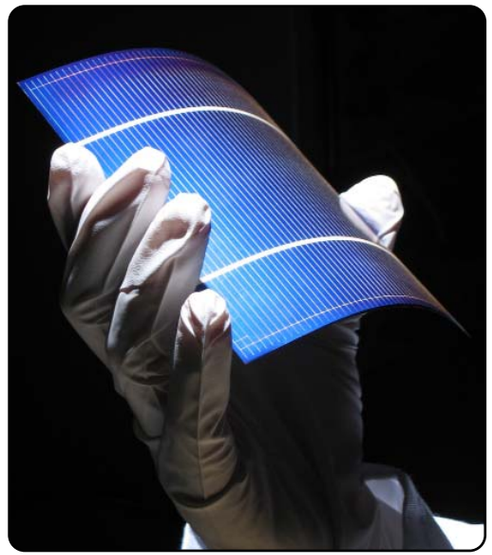

Figure 3 – Large-Area Solar Cell on a Very Thin Wafer (80 µm)

Advanced Front Metalization Stack

When using the above-mentioned emitter design with lower surface dopant concentration, an adapted front metalization scheme is required.

A two-step metalization plating process was developed. This process is based on the idea of applying first a thin metal layer and subsequently applying a thick highly conductive metal layer. The thin seed layer will be optimized to contact the lowly doped emitter. The second, thick metal layer needs to be highly conductive, so it can consist of either silver or copper.

The imec researchers chose copper as the front contact material mainly because of price considerations. Although the cost

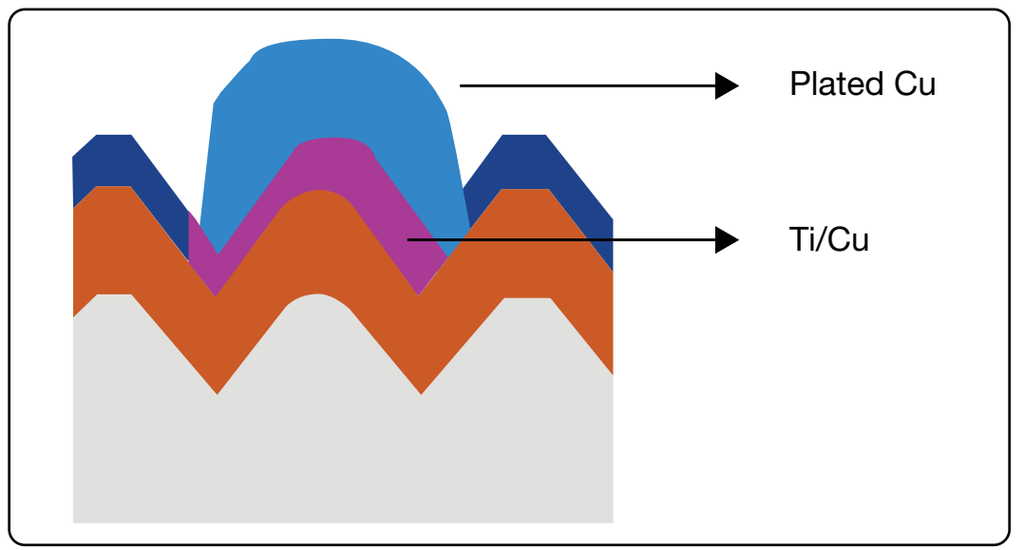

Figure 4 – Scheme of the Advanced Metalization Stack Showing Cu-Plated Contacts

<< PREVIOUS PAGE | NEXT PAGE >>

of both silver and copper has increased over the years, copper is relatively cheap compared with silver.

Not many solar cell manufacturers have, however, applied copper, because of contamination issues. Based on its expertise in CMOS processing and the use of copper in chip interconnections, imec developed a barrier layer for use in solar cells, preventing copper diffusion into the silicon. The latter would otherwise decrease the solar cell performance.

Taking all this into consideration, the two-step metalization process uses a thin Ti/Cu contact layer and a thick highly conductive copper layer. The Ti/Cu layer has several functions: It acts as a barrier layer to prevent copper diffusion into the silicon; it serves as a seed layer to enable electroplating; and it is the contact layer for the lowly doped emitter.

Plating Instead of Printing

For the advanced metalization stack mentioned above, a plating technique was used. Today, printing techniques are mostly used to make the front contacts. The most widely used technique is screen printing, but also used are alternative printing techniques such as inkjet-printing and aerosol jetting. The main concern here is to achieve a good aspect ratio of the contacts (minimizing the shadowing losses) while maintaining a high throughput capability.

The advantage of using a plating technique is that it enables making more narrow contacts as compared with printed contacts. It is a well-known technique from the CMOS industry, and allows for an efficient deposition of a layer of pure metal. Smaller line widths with increased aspect ratios can be achieved, decreasing the shadowing losses and thus increasing the solar cell efficiency. Also, plating is very well suited for thin substrates as no substantial mechanical force is used during the process.

Above 18% Conversion Efficiency

To conclude, an iPERC solar cell was developed with additional features, namely a shallow emitter and advanced front metalization using copper plating. This resulted in a conversion efficiency of 18.4 percent for large-area cells (125 cm^2). Imec continues to look for improvements for wafer-based solar cells, eventually targeting cells that are only 40 µm thick and exhibit efficiencies above 20 percent. ■

About the Authors

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Jef Poortmans – *See bio on page 8.*

☞Click here to return to Table of Contents

Lessons From the 2nd Workshop on Metallization of Crystalline Silicon Solar Cells

Guy Beaucarne,[1] Jaap Hoornstra,[2] Gunnar Schubert[3]
[1]Dow Corning [2]ECN Solar Energy [3]Sunways AG

Abstract

About 190 metalization experts gathered in Constance, Germany in April for the 2nd Workshop on Metallization of Crystalline Silicon Solar Cells. Presentations and discussions clearly showed that screen-printing is not running out of steam because of various innovations in processes and pastes. Interest in the seed-and-plate approach has somewhat decreased. Cu plating has gained in importance but is facing several hurdles before it can be industrially implemented.

Introduction

Metalization is one of the key process steps to fabricate solar cells with high performance in a cost-effective way. More than 85 percent of photovoltaic solar cell manufacturing uses thick film screen print metalization to produce solar cells, but a lot of research is also carried out on alternative metalization schemes or variations to screen-printing. The success of metalization technology development is crucial for the evolution of solar cell technology toward lower production costs and higher efficiencies.

Recognizing that existing photovoltaic events did not provide an ideal setting for experts to discuss these topics in detail, we decided to organize a dedicated and focused workshop on the topic of metalization of crystalline Si solar cells. The number of participants in this workshop is limited and much time is reserved for panel discussions, informal exchanges and networking.

The 1st Metallization Workshop, held in Utrecht, The Netherlands, in 2008, turned out to be a great success. The second edition was held in Constance, Germany on April 14 and 15, 2010. Around 190 scientists and engineers from solar energy institutes, universities and companies all over the world gathered in the Konzil, a historical building facing the Lake of Constance, to share and discuss the latest developments in solar cell metalization. This report aims to summarize the major lessons learned from the workshop. More information (including presented slides) is available on the website www.secondmetal.eu.

<< PREVIOUS PAGE | NEXT PAGE >>

Screen-printing Still Reigns Supreme

Front-side metalization is commonly achieved by screen-printing a Ag containing paste in a grid pattern on the silicon nitride-coated wafer, and then applying a short thermal anneal, during which the paste etches through the nitride to make contact with the top region in the Si wafer and Ag particles are sintered. The exact mechanism of contact formation was touched upon in several contributions. The process of formation of Ag crystallites and simultaneously of a glass layer on top of those, which was originally described by Gunnar Schubert,[1] seems supported by several contributions, although some in the metalization community questioned the importance of the crystallites in the electrical contact.

It was recognized that much progress has been made at the level of paste development to enable low contact resistance on high sheet resistance emitter, enabling substantial efficiency gain. Further development in that direction and enhanced understanding of the processes will lead to pastes with even higher performance,[2] but it was stated that at present, no paste can contact emitters with surface concentration below 10^{20} cm^{-3}.

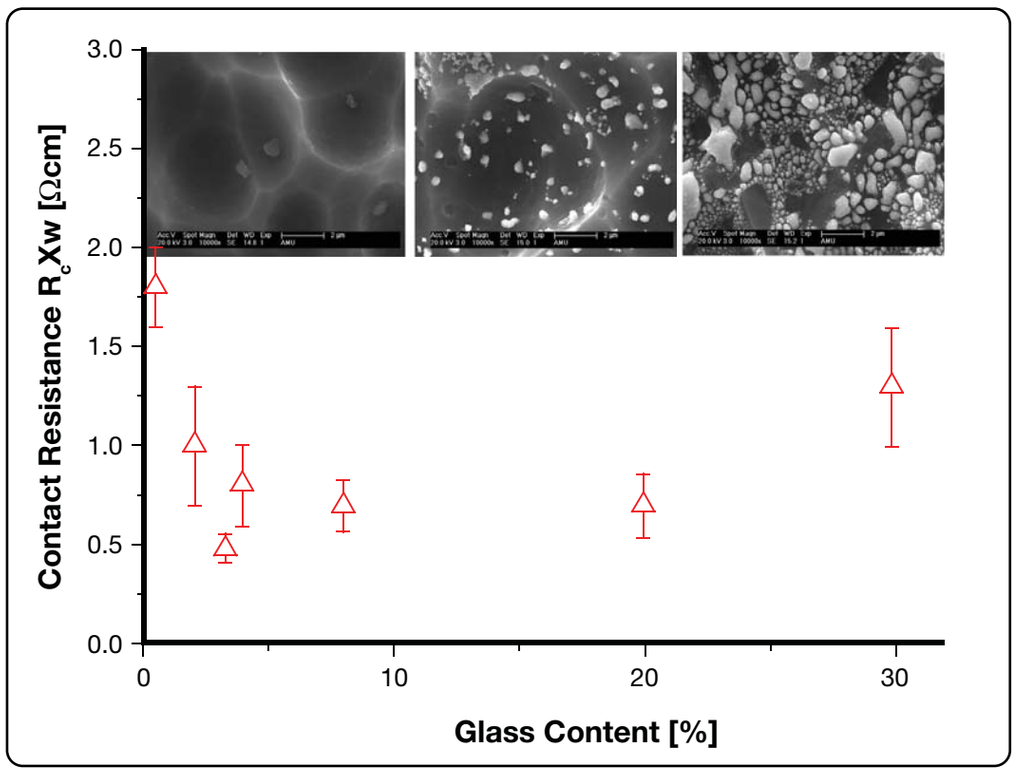

Figure 1 – Contact Resistance Measurements as a Function of Glass Content[2]
Reproduced with permission from the presentation at the workshop of Matthias Hörteis, Fraunhofer ISE

The effect of the peak temperature dwell time on the contact formation, and in particular, the thickness of the glass layer causing high contact resistance, was discussed.[3] The results suggested that improvement in performance might be obtained by innovation in annealing processes. That could be achieved by adapting belt furnaces or by switching to alternative techniques, such as, e.g., induction firing.[4]

The issue of Ag diffusion into sensitive regions of the device was pointed out,[3,5] and clearly represents a danger for shallow emitters. To avoid this problem, a deeper and lowly doped emitter is desired. It is, however, impossible to create by traditional phosphorus diffusion a deep and lowly doped emitter that at the same time displays a high surface concentration necessary for contacting by screen-printing. The advent of new emitter formation methods relying on techniques originally developed for microelectronics, such as epitaxy, was presented as a possible solution.[6]

An often-mentioned drawback of screen-printing is the large line width that leads to high shading losses. Several innovations are being introduced that aim to solve that problem. One solution is to print narrow (but relatively thin) lines twice on top of each other, to achieve narrow (60-100 µm) and sufficiently thick lines. Tests on very large batches demonstrated the feasibility of this approach.[7,8] Another approach with substantially less process complexity could be single printing of narrow lines with large aspect ratio using stencils instead of screens, as indicated by promising results presented by Jaap Hoornstra from ECN.[9] A material-based solution is to use a hot-melt material that solidifies quickly upon printing, also enabling high aspect ratio lines with a single screen-print.[10] Another innovative printing technique that was presented is the off-contact laser transfer printing technique that could become an alternative to screen-printing if sufficiently high aspect ratios are achieved.[11]

In general, thick film printing of a Ag front grid was presented as a versatile technique with a large scope for further improvement both at process and paste level. Its adaptability was also evidenced by successful adaptation for back contact cells with via metalization.[12] Interestingly, the need for lead-free pastes did not seem a primary concern among cell manufacturers, who demand equivalent performance from lead-free alternatives. Bithmuth-based products are, however, in development, and a paste manufacturer felt confident that the performance gap with Pb-containing pastes would be closed in the coming years.[13]

Seed and Plate

The strong progress in Ag screen-printing seems to have decreased interest in the "seed and plate" approach for the front grid. This is a hybrid approach where a very narrow line is first printed by a fine-line printing method (often an off-contact method such as aerosol printing or inkjet printing), fired through silicon nitride, and then thickened by plating, most often Ag light-induced plating (LIP). The introduc-

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tion of this technique in production, which seemed imminent at the time of the 1st Metallization Workshop, has been slower than anticipated. Nevertheless, outstanding cell results presented at the 2nd workshop reminded the audience of its strong industrial potential, such as an 18.7 percent cell on 239 cm^2 Cz wafers obtained by combining inkjet printing and LIP.[3] This approach also was shown to work well for alternative cell structures, featuring, e.g., alternative front passivation stacks AlO3/SiN stacks and shallow B-emitters on n-type wafers.[14]

The emergent fine-line printing techniques were shown to impose very different requirements on inks in terms of viscosity and particle size compared to screen-printing pastes,[15] but also to enable the printing of alternative metals with conductivity close to bulk if the appropriate solution and nanoparticle-based precursors are used.[16]

Cu Plating Metalization Schemes

Several long-term solutions for front grid metalization are based on Cu plating. Indeed, one can potentially obtain higher performance, through the ability to contact high-efficiency emitters with low surface doping and without glass interlayer, and lower cost through the replacement of Ag by Cu.

A first step toward such long-term Cu-based metalization schemes is to apply the seed-and-plate approach. First a thin-printed Ag line is fired through nitride, but the line is thickened with Ni and Cu plating instead of Ag LIP. In such a structure, diffusion of Cu into the cell and resulting harmful contamination is a concern, but a detailed study of cell degradation showed that plating conditions could be found where Cu diffusion is avoided completely.[17]

Ni is often used as first layer in a Cu metalization scheme. It creates contacts with very low resistance upon annealing through the formation of Ni silicide, even on emitters with low surface concentration. Moreover, it enables self-aligned process schemes, either through selective silicidation or by auto-catalytic plating onto Si. Finally, a sufficiently thick nickel layer is also an effective barrier against diffusion of Cu. Several contributions identified the challenges with Ni, such as the danger of shunting through the emitter[18] and problematic adherence of Ni barrier layers.[19]

A contribution from imec shared the experience learned from a similar switch to Cu that took place in integrated circuit processing in the past. Some learning can be directly transferred, e.g., in the fields of contamination control, diffusion barriers and adherence.[20]

Rear Side

There were fewer presentations on rear-side metalization, although the topic is also of crucial importance for cell performance. For example, the thickness, doping concentration and uniformity of the traditional Al-BSF/Al contact has an important impact on cell efficiency.[21] It was noted that higher temperatures lead to a thicker and more highly doped BSF, leading to better Voc, but that this benefit could only be exploited if the front surface metalization is adapted for higher temperatures.[9]

Detailed studies of local Al BSF formations were presented, which are formed in advanced cell structures with dielectric passivation and local contacts. These talks confirmed the creation of pits and trenches upon Al alloying in narrow openings described by Guy Beaucarne in the 1st Metallization Workshop.[22] The contributions indicated that Al availability and size of the opening of the dielectric is critical for the depth of the alloyed contact.[23] It was also shown with detailed cross-sectional studies that Si diffuses in Al far away from local contact (up to 20 µm away from the opening), and the link was established between this observation and the relatively thin BSF formation in the locally alloyed region.[24]

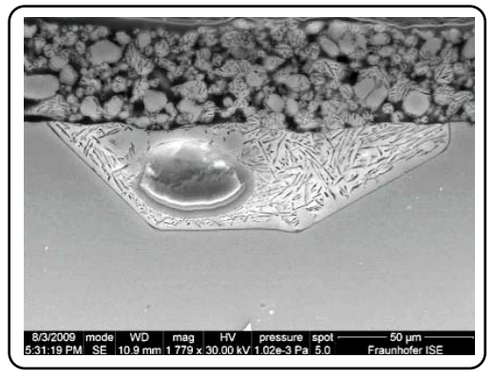

Figure 2 – Cross section SEM picture of a locally alloyed Si-Al contact. Particles with lamellas indicate Al-Si eutectic formation and therefore evidence of Si diffusion. *Reproduced with permission from the presentation at the workshop of F. Grasso and L. Gautero, Fraunhofer ISE.*

Series resistance in the rear structure of dielectric passivated cells is an important issue. It was shown by simulation that resistive losses are likely to be lower in PERC structure (with blanket Al coverage) than in structures with Al fingers at the rear.[21] An optimal structure for cells with rear nitride passivation and metallic grid might involve the use of a firing-through AgAl paste. This was shown to work well on devices with B-BSF,[25] but will be a challenge for cells relying on local Al-BSF.

To obtain the blanket Al deposition for PERC type cells, the traditional technique consisting of screen-printing a thick Al layer can be used. However, for reasons of process control and future cost reduction, high-throughput PVD (physical vapor deposition) is an attractive alternative. An important step toward an industrial solution for Al PVD was demonstrated at the workshop in reports on promising results with prototype in-line vacuum thermal evaporation.[26,27]

Link Between Cell Metalization and Module

New cell metalization can pose challenges for module assembly. Conversely, issues with module assembly might have important implications for the design of the cell metalization. To address this, a special session on the relationship between cell metalization and module fabrication was organized, with only invited speakers.

The first step in module manufacturing is the interconnection of cells by soldering a tin alloy-coated Cu ribbon onto the cell busbars. This process is delicate and can lead to several problems, such as cell breakage, insufficient adhesion and damage to the metalization.[28] Cell designs should minimize the amount of solder joints and display flat busbar surfaces. The stress induced by solder joint cooling combines with stress created by metalization. The resulting stress in the device is also determined by the proper-

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ties of the interconnection material, the applied thermal treatment and cell geometry, and is directly related to yield.[29]

Electrochemical reactions during interconnection and operation were discussed and shown to have a possible impact on metalization if not well controlled. It was also indicated that present paste-based metals are brittle and that cracks propagate from wafer into the metal.[30]

Finally, a module concept was presented for back-contact MWT cells, where the metalization design of the cells is adapted to the module concept.[31] During this talk, a statement was made that is probably more general than for back-contact modules alone: Cell structures and processes, including metalization, should be developed together with the module concept as one system.

The Participants' View on the Future of Metalization

At the end of the workshop, the participants were asked to give their views on the development of metalization in a questionnaire. The results (Figure 3) showed that screen-printing is expected to remain dominant in the next 10 years, but that emerging concepts will gain significant share within five years.

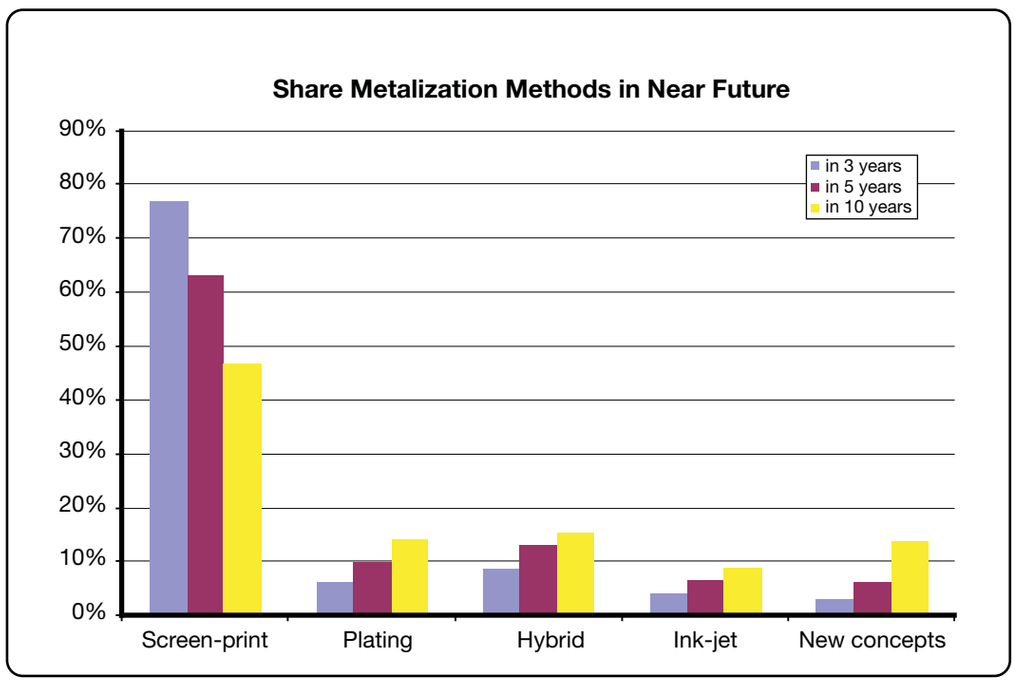

Figure 3 – Anticipated Share of the Different Metalization Techniques in the Coming Years.

Conclusion

The 2nd Workshop on Metallization of Crystalline Silicon Solar Cells provided excellent insights in the status and development of metalization technology. Although screen-printing has been around for a long time, it is efficient, quick and reliable, and its performance is being stretched by some innovations, making it hard for alternative techniques to emerge. The hybrid Ag seed-and-plate approach is the only technique that could be introduced in the short term, but has lost some of its appeal because of improvements in traditional screen-printing. Metalization schemes based on Cu plating appear to be the ultimate solution in terms of line width, cell performance and material costs, but several hurdles need to be overcome before it can be widely adopted.

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<< PREVIOUS PAGE | NEXT PAGE >>

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Jaap Hoornstra *joined ECN Solar Energy in 1995 and is mostly involved in metalization. Among others, he participated in the European project DOLMET and led EC2C. Jaap is also operational manager of SunLab, an ECN daughter company commercializing Corescan and Sherescan instruments.*

Gunnar Schubert *obtained his M.Sc. in physics in 2002 at the University of Konstanz. In 2006, he received his Ph.D. in the area of thick film metalization of crystalline silicon solar cells at the photovoltaics department of the University of Konstanz. Since 2006, Gunnar has been working in the R&D department of Sunways AG. He is presently head of R&D Solar Cells at Sunways.*

☞Click here to return to Table of Contents

PRINT this article E-MAIL this article

<< PREVIOUS PAGE | NEXT PAGE >>

Development of Directional Solidification Systems for Silicon

Chandra P. Khattak
GT Solar Inc.

Abstract

In 1975 when photovoltaics (PV) was contemplated as an alternate renewable energy source for terrestrial applications, silicon ingot technology was identified as a major area to pursue, and it was expected that with innovations, overall costs could be reduced. A historical description of events leading up to the current state of the directional solidification systems (DSS) furnaces for multi-crystalline silicon ingot production and making PV approach grid parity are discussed.

Introduction

Directional solidification is one of the most commonly used approaches to prepare high-technology materials with controlled size, shape and structure so it can be further processed into devices/applications. Historically, the Bridgman process is used during initial development stage and, depending on the material, variations of the process are developed for that material of interest that allow optimization and commercialization. For example, in the metals industry, directional solidification was favored over traditional casting so oriented grains were formed in the structure. In the case of high-performance turbine blades, near-net-shapes were produced to reduce costs. The next step was adding a pig tail to achieve grain selection, resulting in single crystal turbine blades with significant improved properties. Similarly, in the non-metals area, specific processes were developed for various oxides, fluorides, etc. Some of the variants of the Bridgman process are Stockbarger, Stepanov, inverted Stepanov, top-seeded growth (TSG), heat exchanger method (HEM), vertical gradient freeze (VGF), horizontal Bridgman (HB), etc.

Silicon is one of the most important materials of modern times. This material was initially processed about 60 years ago and has had a history of development very different from most other materials. In spite of producing silicon in a very pure, mono-crystalline, defect-free form, it is amazing that further improvements are still being made in the semiconductor industry and improved devices are being manufactured.

Silicon has had two lives in the high-technology applications and the paths chosen for these two applications have been very different. During the 1950s the discovery of the transistor led to silicon development for the semiconductor industry. While silicon was a mature material in the 1970s, as the backbone of the semiconductor industry, it could not meet the requirements of terrestrial PV applications. This was in spite of the fact that silicon solar cells were used for space exploration. Therefore, silicon had to go back to the drawing board to the Bridgman process and travel a new path for terrestrial PV applications, which has been very different than the beaten path for semiconductor applications. The history of the semiconductor path is well known; this paper discusses the PV path for silicon processing and how it affected not only the ingot growth but the entire sequence up to the production of solar modules.

Starting Point

The traditional Bridgman process involved lowering the temperature of a molten charge in a furnace to achieve solidification. The crucible was round with the bottom section tapered to a point. After melting the entire charge in the crucible, it was lowered and solidification was initiated from the bottom and progressed toward the top. The tip at the bottom of the crucible favored limited grains to be nucleated resulting in large grain formation in the resultant ingot. Sometimes, single crystals were formed. It was soon recognized that vibrations in the charge could be reduced if the hot zone instead of the crucible was moved; this was named modified Bridgman. VGF involved keeping the hot zone and the crucible stationary

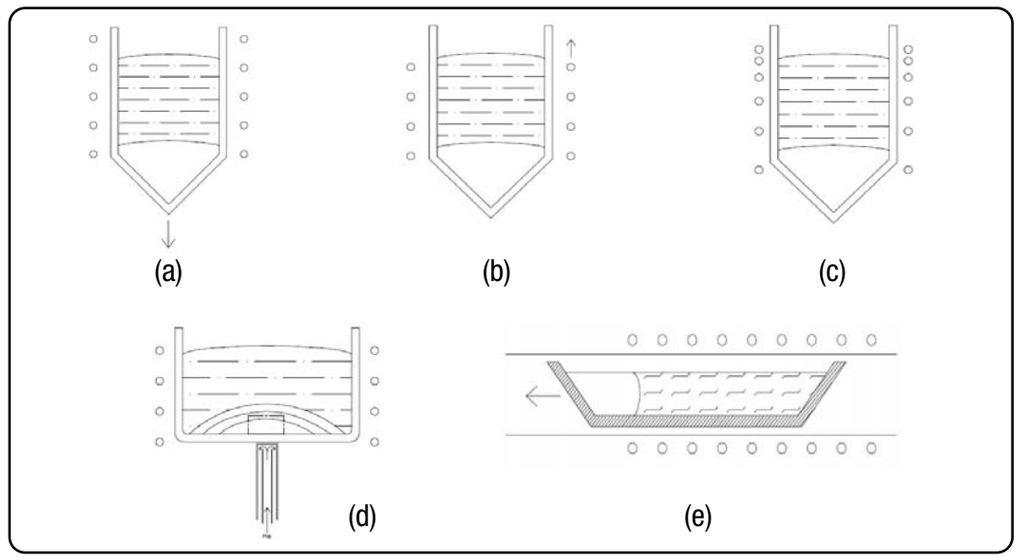

Figure 1 – Schematic Representation of Variations of the Bridgman Process showing:
(a) Vertical Bridgman (VB), (b) Modified Vertical Bridgman (MVB), (c) Vertical Gradient Freeze (VGF), (d) Heat Exchanger Method (HEM), and (e) Horizontal Bridgman (HB)

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and building a temperature gradient in the hot zone. Other variations were seeded growth – here an oriented seed crystal was placed at the bottom of the charge and parameters were adjusted that growth initiated off the melted-back seed crystal so mono-crystalline growth could be achieved. This led to active cooling of the seed crystal to ensure it was not melted out and that the growth was controlled. Processes, such as HEM, were developed to grow large, high-quality crystals of difficult materials. A different approach was the HB, where, instead of the vertical gradient/growth, a horizontal configuration was used (see Figure 1).

All such variations involved melting and directional solidification of the charge be carried out in a crucible. This means that the reaction between the crucible and the melt as well as the crucible and solid are important considerations. Crystal pulling techniques, such as Czochralski (Cz), TSG, Stockbarger, Stepanov, etc., were developed where solid was pulled out of the melt so it never contacted the crucible; hence, crucible and the solid reactions were not important. These techniques were also directional solidification processes but quite different from the Bridgman process.

In the early 1950s the Cz process was adapted for silicon ingot growth because the reactions between the solid and crucible could not be managed in the Bridgman process.

First Path for Silicon

Metallurgical grade (MG) silicon was produced as an alloying agent in the metals industry. This material was fragile; hence, it could not be used for structural applications. In the 1950s materials research at Bell Laboratories required high-purity silicon that could be processed into semiconductor devices. As was tradition, silicon was directionally solidified using the Bridgman process. The choice of crucible material was rather limited because molten silicon is very reactive and impurities in the crucible could contaminate the silicon. Silica (SiO_2) was available in high-purity form and the reaction product ended up as oxygen contamination in silicon. Silicon grown in silica crucibles resulted in cracked ingots. This cracking was attributed to differential thermal expansion between silicon and silica. At high temperatures when silicon solidified it bonded to the crucible. During cool-down, after directional solidification, silicon contracted much more than the crucible, resulting in high stresses. Below 650°C, silicon underwent a ductile-to-brittle transition resulting in cracking of the ingot and the crucible.

Hino and Stauss[1] were able to solidify a crack-free 50-g silicon ingot by using a paper-thin silica crucible. Under these conditions the crucible cracked due to weakening because of crystalline phase formation during growth. This led to relieving the stress between the crucible and the ingot and the ingot was left intact. The reliability of a thin crucible for growth of large ingots was questioned; hence, alternative approaches were pursued.

In the early 1950s the Cz process was adapted for silicon ingot growth because the reactions between the solid and crucible could not be managed in the Bridgman process. Since that time, the emphasis has been in producing more and more improved devices. This has yielded production of silicon feedstock up to 13 9s (99.99999999999 percent) purity, up to 450 mm diameter, defect-free, mono-crystalline ingots with controlled carbon and oxygen specifications. Compared to silicon, no other material has gained such levels of purity, defect-free structure, large-size and commercially used for state-of-the-art devices.

Second Path for Silicon

In the 1970s there was recognition that an alternate renewable energy source was necessary for worldwide use. One of the areas selected was PV. This selection was natural because it had been used for space explorations. Detailed analysis revealed that it was a very expensive choice for terrestrial applications. Costs had to come down by orders of magnitude. Silicon was identified as a material of choice because of the maturity of the semiconductor industry and widespread commercialization. Further analysis showed that the semiconductor industry had focused on very high performance and this had resulted in making silicon highly pure, defect-free and reliable. Moreover, silicon wafers constituted about 1 percent of the device cost so reducing the cost of silicon was never a high priority. In comparison, for terrestrial PV, silicon was almost 50 percent of the total costs. Therefore, reliability and performance of solar cells could be compromised in favor of cost reductions.

In 1975 it was not possible to envision a clear path, starting with the Cz process, to develop low-cost silicon production for terrestrial applications. Once again, the starting point for the new path was retraced to near the Bridgman process. Since past data with the Bridgman process was not encouraging, different groups worked on different approaches. Heliotronics[2] in Germany and Solarex[3] in United States favored casting approaches in which silicon was melted in one crucible and poured into molds for directional solidification. The molds were maintained below the melting point of silicon so the material in contact with the crucible was chilled and, therefore, did not bond strongly to the crucible. Usually the bottom of the mold was cooled, so directional solidification progressed from the bottom of the mold to the top. However, growth also progressed from the side-walls. This resulted in lack of uniformity, consistency and degradation in performance of solar cells.

An alternative approach was to adapt the HEM[4] for silicon. This technique was in production for high-quality sapphire crystals at Crystal Systems in the United States. Growth of 25 cm diameter silicon (which was the production size for sapphire in 1975) compared to the 7.6 cm diameter for silicon by the Cz process appeared very appealing. It was apparent that if HEM was going to work for silicon, a new crucible was necessary that allows crack-free silicon ingot production. Looking beyond this cracking issue, the crucible should: not contaminate the silicon; be readily available; allow scalability

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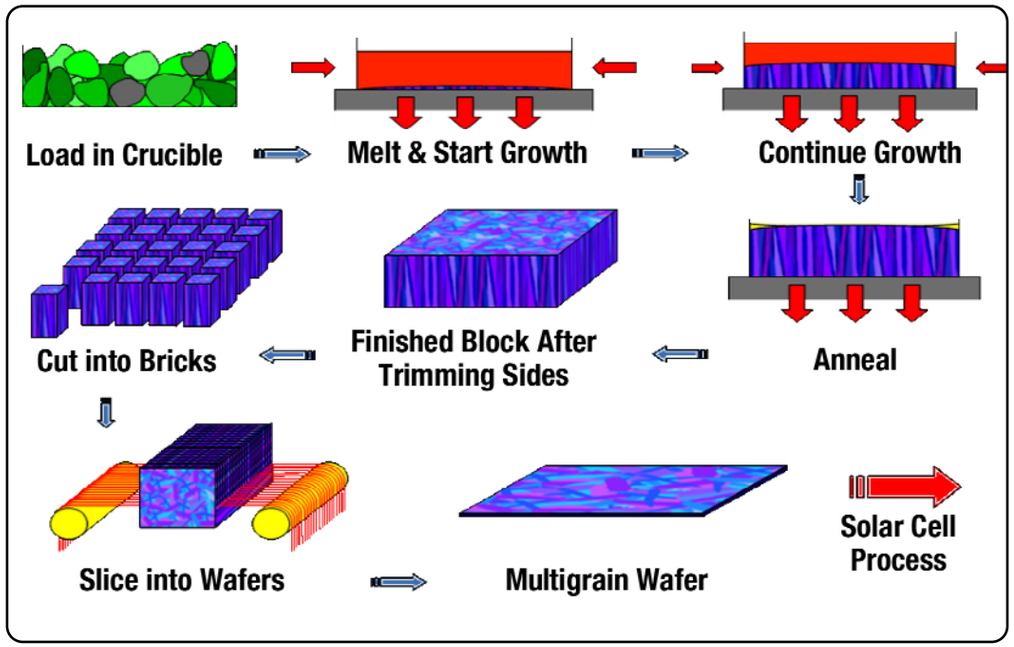

Figure 2 – Process Steps Involved in Converting Silicon Feedstock Into Multi-Crystalline Wafers for Solar Cell Applications

to large sizes; be low cost. Among the candidates, silica was the choice material, as it was abundant, available in high purity and large size, and readily available for large-scale production. Therefore, once the cracking problem was resolved it would be smooth sailing toward making PV a reality for terrestrial applications.

Many types of processes to produce silica crucibles were attempted. Various coatings and encapsulants were tried but the ingot cracking problem was tough to beat. Finally, a slip cast silica crucible was glazed by a flame treatment on the inside surfaces of the crucible.[5] This crucible produced crack-free silicon ingots. This was the first report of a large crack-free silicon ingot produced by directional solidification.[6] The glazed layer bonded to the silicon ingot after directional solidification and, during cool-down, separated from the rest of the crucible. This minimized the stress on the ingot and prevented it from cracking. The glazed layer was very thin (<1 mm thick). Once an appropriate crucible was developed, a path to meet the goal could be seen but many innovative approaches had to be incorporated to bring the technology to its present status. At all times, the emphasis was to reduce costs in manufacturing and to produce a consistent and uniform product without compromising the quality.

Approaching the Goal

As mentioned earlier, silica crucible imparts oxygen to the silicon. Therefore, processing was carried out under vacuum instead of under an argon blanket. This was expected to reduce argon costs. However, reactions in the hot zone under vacuum had to be understood for this operation.[7] Grooving of the crucible wall near the liquid surface had to be minimized also.

Once a suitable crucible was developed, a natural extension was to form a square ingot because square solar cells yielded higher area coverage in modules compared to the traditional round variety. Therefore, module costs were reduced on a $/watt basis due to additional power output. General consensus, in the late 1970s, was to plan in terms of using 100 mm square solar cells. This dictated that approximately 11 mm square ingots be produced and to get higher throughput multiple crucibles used in the furnace. The suggestion to grow 22 cm or 33 cm square ingots and section them into four or nine square bars of 100 mm size was considered ridiculous. Similarly, section-

Figure 3 – A typical DSS furnace set up for production of multi-crystalline silicon ingots. This system is bottom loading and components are set up in two levels for better utilization of space.

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ing with a diamond band saw was unthinkable. Currently, the PV industry is growing 84 cm square ingots and sectioning them into bars routinely.[8]

The size of the HEM furnace parts was quickly scaling up with larger ingot sizes and there were no commercial furnaces for purifying the hot zone parts prior to use. By semiconductor standards using these parts without halogen treatment for purification was out of question. An innovative approach was attempted in that the hot zone assembled using unpurified parts be subjected to a "bake-out." During this step the furnace was taken well above the operation temperatures for ingot growth under vacuum so that volatile impurities were boiled off and residual impurities were reacted to form compounds such as carbides. Under ingot growth conditions the hot zone parts were subjected to lower temperatures than in the "bake-out"; hence, contamination was minimized.

The glazed crucible had run its course because preparing the crucible was labor intensive and the reliability under non-standard conditions was not satisfactory. This was becoming a bigger problem as ingot size increased. Therefore, instead of glazing the inside surfaces of the crucible, a coating was applied that prevented direct contact between the silicon ingot and the silica crucible. The silicon-nitride-based coating[9] was unstable under vacuum; hence, growth under an argon blanket was optimized such that the oxygen contamination in the silicon was minimized. Emphasis was placed on producing large grains with columnar, coherent, nearly vertical-oriented grain boundaries growing side by side, tailored to produce high-efficiency solar cells.

Once high-quality, multi-crystalline silicon product – specifically tailored for PV application – was characterized, it was important to set up large-scale production of consistent and uniform silicon ingots without the necessity of skilled production labor. Therefore, a fully automated HEM furnace was built where the requirements of production labor was limited to loading/unloading of the furnace. Several decades of experience and know-how was imbedded into the furnaces and control system to achieve this goal.[10,11] There was continuous effort to update the system as more data was gathered and analyzed. The process flow for production of multi-crystalline silicon wafers is shown in Figure 2.

When the ingot size of 69 cm square, 240 kg was realized, it was essential to undertake a major redesign effort to retain the advantages of the HEM design and make improvements in other areas to produce next-generation furnaces that are current DSS.[12] It was confirmed that the quality of the silicon was not compromised and that the new furnace was user-friendly, had further scale-up capability and addressed most of customers' needs. It is bottom loading and, instead of the crucible moving down in the heat zone, the insulation is raised without moving the crucible (see Figure 3). The cycle time for processing has been reduced for the DSS furnaces and significant cost reductions have been achieved overall.

It has been important to further reduce the silicon ingot production costs. An innovative approach with DSS furnaces was to grow 84 cm, 450 kg silicon ingots instead of 69 cm, 270 kg ingots using most of the hardware for the smaller ingots.[8] Replacing the heat zone of the 69 cm ingot DSS furnace can upgrade the furnace to produce the larger 84 cm ingots and thereby get significant increased throughput at reduced costs.

Conclusions

Even though the semiconductor industry was mature and operating successfully, it could not be readily applied to making PV an alternate energy source in 1975. A back-to-basics approach combined with continuous improvements had to be undertaken in the silicon ingot growth area to achieve the current state of the industry. DSS systems have emerged as the most prevalent technology that has made significant inroads in approaching the near-grid-parity levels for PV.

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About the Author

Dr. Chandra P. Khattak – *chief technologist at GT Solar, has been actively involved in photovoltaics since 1977. He is recognized for his numerous technical contributions in directional solidification, crucible development and feedstock areas that led to commercialization of silicon ingot production technologies. Dr. Khattak adapted the heat exchanger method for growth of silicon ingots from concept to commercialization, which was licensed to GT in 1997. He joined GT Solar in 2006.*

☞Click here to return to Table of Contents

PRINT this article E-MAIL this article

<< PREVIOUS PAGE | NEXT PAGE >>

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Torsten Brammer
Chief Scientist, Sunfilm AG

The main commercial technologies in photovoltaics are based on wafers made of mono- and multicrystalline silicon, thin films made of CdTe, thin films made of CIGS and thin films made of silicon. The produced volume from all thin film plants in 2009 was around 1.6 GW with a share of around 0.6 GW for thin film silicon (for reference: the total installed power including all technologies in 2009 was around 7 GW*). Within the thin film silicon technology sector, the produced volume is split among more than 10 companies, with United Solar Ovonic, Sharp, Kaneka and Mitsubishi Heavy Industries leading the pack. The key advantages of thin film silicon are the high availability of inexpensive and environmentally friendly raw materials, and with that, a low price volatility of the essential raw materials. Further, thin film silicon production lines are based on a relatively simple production process that allows a high fab utilization and a high production yield. Finally, the produced energy per installed nominal power is inherently very high. The key challenges are the improvement in efficiency and the cost reduction for the silicon deposition tools.

In this first issue of Future Photovoltaics, Luc Feitknecht gives a comprehensive overview of the key development steps for thin film silicon technology starting in the 1970s with the first thin film silicon layers and devices. The path to highly efficient devices, including the implementation of tandem and triple junctions, is described. This includes the consequences of the Staebler-Wronski effect, which is sketched in a very descriptive way. The paper also covers the latest developments and development needs for cost-efficient deposition of the silicon layers.

*All market data taken from ACCELIOS Solar – TFPV Market Update 01/2010 (www.accelios-solar.com)

The Advantages of Amorphous Silicon Solar Cells

Luc Feitknecht
University of Applied Sciences of Technology Buchs NTB

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Abstract

Are high efficiency and high deposition rate the keys to the success of thin film silicon solar cells? The early days of thin film silicon are sketched to understand the present situation of this promising technology. Thin films have seen a second boom phase in the last three years, but over the last 15 years, it has rather lost market share. Conversion efficiency of today's thin film silicon modules are on the edge of 10 percent, and enormous cost-saving potential exists compared to wafer-based solar cells.

A Look Back to the Early Days: History

It was in the year 1973 when in Dundee, Scotland, Spear and LeComber discovered interesting electronic properties of silicon layers, which have been fabricated onto foreign substrates by using the glow discharge deposition method. Further important steps were the possibility of doping such films by mixing phosphine or diborane with silane gas for the fabrication of these non-crystalline semiconductors. In 1976, good news came from the RCA labs in Princeton, where Carlson and Wronski reported on an amorphous silicon solar cell of 2.4 percent conversion efficiency.[1]

A climax for amorphous silicon solar technology is reached in a 1993 publication by J. Bauer et al. of Siemens Solar in Munich, Germany announcing a pilot-line module with a 10.7 percent initial conversion efficiency of 1 ft^2 in size.[2] The worldwide market share of amorphous silicon solar modules makes up about 30 percent. But by the year 2002, the situation has completely changed, and the PV module manufacturer BP Solar announces it will abandon two leading thin film PV manufacturing projects.

A Look Into the Device: Technology

Today amorphous-silicon-based solar modules have a market share of below 10 percent of the world PV market. Over 90 percent of solar modules are based on crystalline silicon (wafer-based) technology. Such a device is commonly fabricated on a 300-500 µm thick p-type doped silicon wafer. A single solar cell has an open-

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circuit voltage of a minimum of 0.5 volts and a short-circuit current density of a maximum of 30 mA/cm^2. Maximum conversion efficiency in the lab is 24.75 percent, and in production, 14-20 percent.

Basic Difference Between Wafer Devices and Thin Film Devices

A classical p-n diode has a very thin depletion zone between the p-type and n-type silicon. The key parameters of the diode are carrier lifetime and mobility. Decent crystalline wafers in the integrated chip industry also have ideal properties for solar technology applications.

A thin film silicon diode does not have comparable material properties when fabricated in a p-n configuration. An elegant way out of this situation is the use of an intrinsic (undoped) silicon layer. In the order of the deposition sequence p-i-n, layers are deposited on a transparent contact layer onto a glass substrate. An electric field spans over the intrinsic absorber layer. Typical amorphous solar cells have a thickness of 0.3 µm. This configuration has been the basis of thin film silicon devices for nearly 40 years.

One single thin film solar cell has an open-circuit voltage of 0.8 volts and a short-circuit current density of a maximum of 15 mA/cm^2 for amorphous silicon absorber material and 0.5 volts on up to 27 mA/cm^2 for microcrystalline silicon absorber material; lab records of stacked devices exceed 15 percent of conversion efficiency. Industrial thin film silicon modules have conversion efficiencies around 6 percent, and stacked cell modules range from 7.5 to 9.2 percent stabilized conversion efficiency.

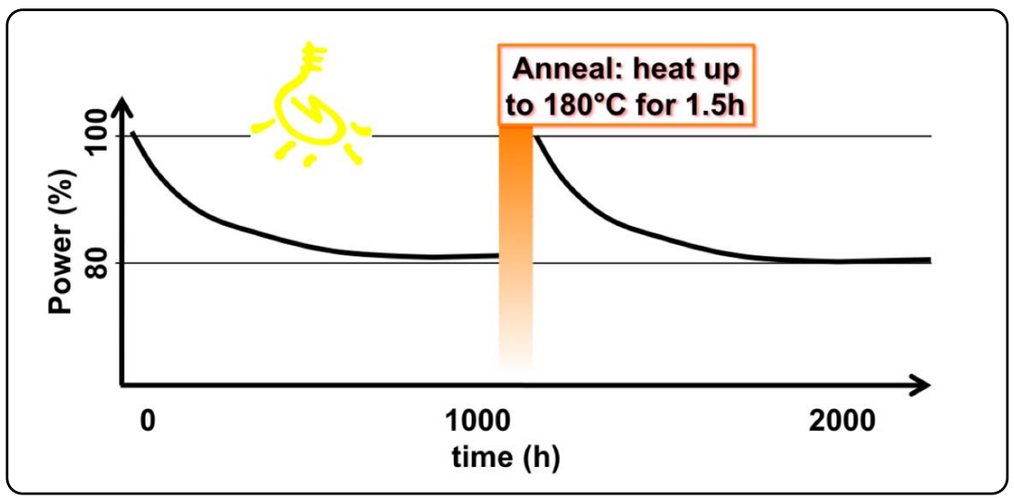

Figure 1 – The metastable behavior of amorphous silicon (the Staebler-Wronski effect): Light-induced degradation reduces the output power of a solar cell under continuous illumination in the lab; under a thermal annealing, the initial values are reached again.

Challenges for Thin Film Silicon Photovoltaics

There is no doubt there is still potential to reduce cost in the manufacturing process of thin film modules: Material consumption is a factor of 1000 lower compared to wafer-based devices; the use of foreign substrates (glass, steel foil or plastics) as a carrier material opens the way for very low-cost photovoltaics.

Up to the year 2002, every factory had to order individual pieces of equipment or even build its own equipment and put it into operation individually. With the advent of "turnkey" equipment suppliers such as Oerlikon Solar, Applied Materials, ULVAC, Anwell, etc., the second wave of thin film silicon industrialization just recently started, and this is an indicator for a certain market maturity.

Two approaches seem evident to shorten the necessary time to fabricate the silicon device: first, the increase of the deposition rate, and second, the introduction of a massively parallel coating process. Chronar was one of the pioneering first-generation companies chosen to coat 48 glass plates at once in the same vacuum deposition chamber.[3] Oerlikon Solar (formerly Unaxis Balzers) chose a batch process, where a glow discharge process runs on 20 identical vacuum chambers and the deposition rate is increased by choosing 40 MHz instead of

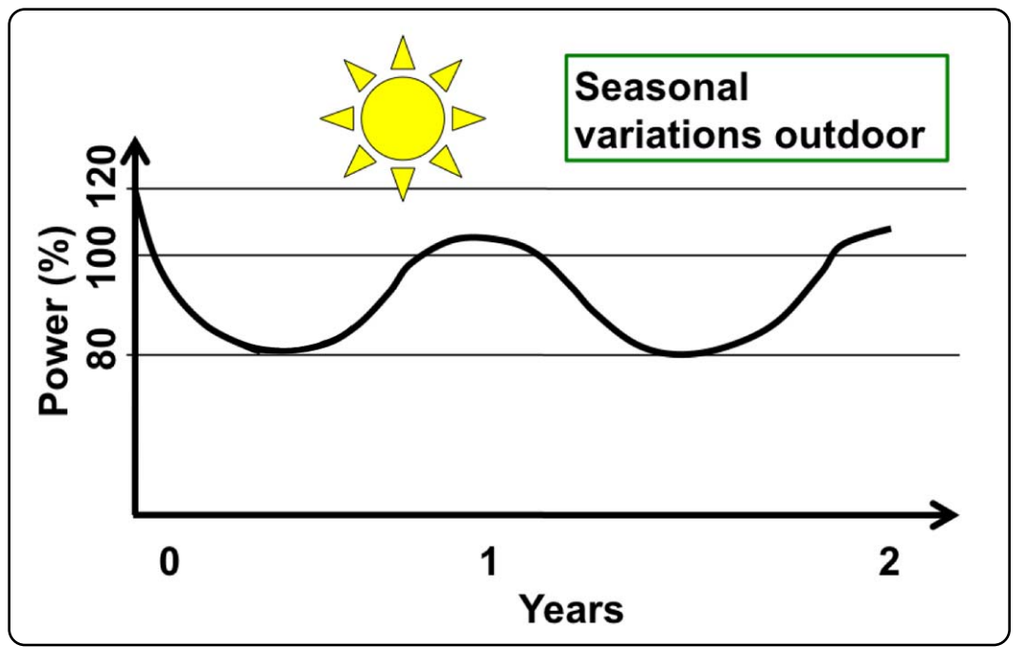

Figure 2 – Amorphous silicon solar cells, under outdoor conditions, have a cyclic power output over several years. In summer, the temperature helps anneal the light-induced degradation effect of the cool sunny season.

<< PREVIOUS PAGE | NEXT PAGE >>

13.56 MHz as the plasma excitation frequency.[4] Applied Materials chose the standard deposition frequency, but used the generation 8.5 size of glass substrates (5.7 m^2), which was already well known from the active-matrix TFT display industry.[5] This is a remarkable step in productivity compared to most suppliers working on 1.4 m^2 or even smaller substrate sizes. A third method toward achieving high productivity is the introduction of roll-to-roll coating processes using flexible substrates such as steel foil or plastics onto which the solar cell material is continuously deposited – similar to a web-coated food wrapping paper.

A major drawback of amorphous-based solar cells is often seen in the Staebler-Wronski effect (StWE), which is a light-induced reduction of electric power out of the amorphous silicon module. A typical power vs. time curve shows reduced power for cool seasons, but this decrease recovers to a certain extent in hot seasons. Amorphous silicon modules are in reality well-suited for hot climatic regions because of a more pronounced recovery of StWE under hot outdoor temperatures. In addition, the material property of amorphous silicon brings a better temperature coefficient than wafer-based solar material – all solar cells tested under standard test conditions (e.g., 1000 W/m^2, AM1.5 spectrum and module temperature of 25°C) perform less well if operated at higher temperatures, but amorphous silicon suffers less (-0.25 percent/°C) than wafer-based silicon (-0.5 percent/°C).

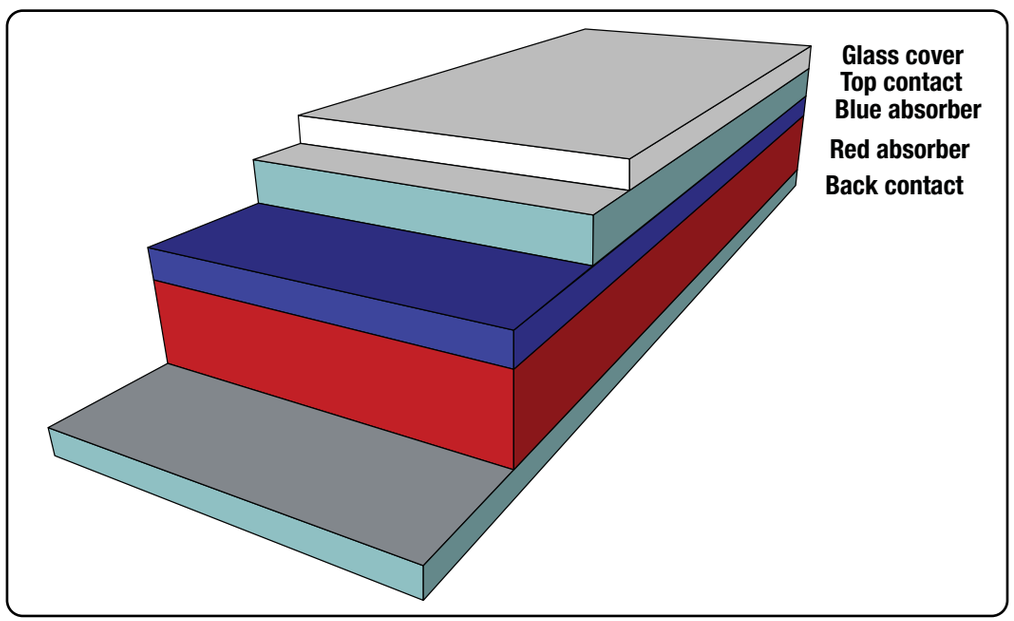

Figure 3 – Sketch of a Stacked Solar Cell (e.g., aSi/aSi or Micromorph Tandem) Where a First Blue-Absorber Sits on Top of a Red-Absorber

An elegant way to overcome low-conversion efficiency and the drawbacks of the Staebler-Wronski effect is the introduction of stacked cells. The key to the success of this concept is that StWE is proportional to the absorber thickness of the top solar cell. By maintaining the thickness of the full stack identical to the one single-junction device, the top cell has a reduced film thickness yet the same field between the p-type and the n-type films, and the device suffers less from the StWE. Early single-junction devices suffered by up to 50 percent of light-induced degradation, whereas today aSi/aSi tandem stacks can reach values as low as 15 percent.

Unisolar is well-experienced in a three-junction stack – aSi/aSi-Ge/aSi-Ge – where the addition of the element germanium helps change optical absorption properties, and hence a first blue-absorber followed by a green-absorber and finally a red-absorber are stacked to build a triple-junction solar cell.[6] Micromorph solar cells consist of two distinct silicon absorbers, where the crystallinity (or the degree of periodicity in the silicon atom network) also changes the absorption properties of the cell: The amorphous top cell is a strong blue-light absorber and the transmitted red light is "recycled" by absorption in the microcrystalline silicon bottom cell.[7]

Conversion efficiency improvements of thin film silicon devices today focus mainly on increasing the device current. A reduced reflection prior to the absorber layer, reduced absorption losses of inactive layers and an enhanced optical path within the absorber layer yield better photo-currents. The insertion of an intermediate reflector between the top cell and the bottom cell increases the top current at the cost of the bottom current – this loss in bottom current has to be recovered by thicker absorber layers or enhanced back-reflecting material behind the cell stack.[8] Further efficiency potential may be gained by addressing the voltage of the stacked cell by adding, e.g., traces of germanium.

By looking at the whole manufacturing process, i.e., from the raw materials gas and glass down to the module mounting system and the connection to form PV-systems producing electricity, there must be similar optimization potential for other industrial goods, such as the semiconductor industry or information technology. Similar learning curves as in Moore's Law in the semiconductor industry are observed in photovoltaics. System prices are reduced by 20 percent by a doubling of worldwide shipments.

In summary, thin film silicon photovoltaics has a considerable track record. The improvement of conversion efficiency is an important issue that is about to cross the two-digit border – at what manufacturing cost this border has to be crossed is an open question. The second important issue is not only silicon deposition rate but also manufacturing cost. Key ingredients to reduce the costs of thin film PV manufacturing are lean production and a market-driven R&D roadmap. Already today, there are net advantages of thin film silicon over wafer-based photovoltaics such as the temperature coefficient and the cost-saving potential.

<< PREVIOUS PAGE | NEXT PAGE >>

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☞Click here to return to Table of Contents

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CONCENTRATED PHOTOVOLTAICS

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Brad Hines
Vice President of Engineering, Idealab

After years of fits and starts, the concentrating photovoltaic (CPV) industry is abuzz with excitement, with the recent announcement by Amonix of its $129 million Series B and Solaria's $45 million funding.

The story of CPV has been one of perpetual promise, always just slightly over the horizon. Concentration was first proposed as a solution to the high cost of photovoltaics decades ago, but there has always been a chicken-and-egg problem. CPV works best with purpose-built solar cells, but CPV module volumes could not amortize the costs of volume manufacturing lines for these cells. In the 1990s, both Amonix and Sunpower developed purpose-built silicon concentrator cells, but volumes remained low, and CPV was not able to climb the experience curve. Meanwhile, numerous CPV companies came and went, while Sunpower exited CPV altogether.

Meanwhile, the space industry developed very-high-efficiency cells for spacecraft, where cost is secondary to mass as a product requirement. These exotic triple-junction cells are well matched to CPV, which can leverage their high efficiency while keeping costs in line with conventional technologies.

Spectrolab led the charge in terrestrial triple-junction cells, followed by Emcore, by Azur Space in Europe and then by a wave of startups and new entrants, including Cyrium in Canada and a number of Asian LED manufacturers. But these cell suppliers, and prospective investors, also had the chicken-and-egg problem – should they take the risk to ramp to volume with no clear volume customer identified?

Now, with Amonix and Solaria funded, and with companies like Soliant Energy and Skyline Solar targeting penetration of other market segments, the "chicken" is coming to roost. Somebody is going to be making a lot of CPV product, and they're going to need a lot of solar cells.

CPV cell efficiencies are now exceeding 40 percent, and are expected to go to 50 percent or more within a decade, with little increase in cost. This extra efficiency means extra power production from the same hardware, which means higher margins flowing directly to the bottom line of CPV cell manufacturers and module makers. This, coupled with rapidly dropping costs as CPV moves up the experience curve, bodes well for this technology in the next few years.

Quantum Dots: Higher CPV Efficiencies, Same Production Cost

Bruno Riel
Cyrium Technologies

Abstract

The solar cells that were developed for the space industry have found their way into the terrestrial photovoltaic market. Cyrium Technologies has combined these cells with a novel technology, quantum dots, to optimize their performance for terrestrial generation of power. These quantum dot-enhanced cells (QDEC) have been introduced at the focal point of concentrator photovoltaic systems, an industry that is poised to revolutionize clean tech.

Introduction

Research and development projects have improved photovoltaic (PV) cell efficiencies progressively. The familiar graph by National Renewable Energy Laboratory (NREL) found on Wikipedia[1] traces the progress back to the mid-1970s. This article will focus on an industrial process involving the introduction of quantum dots in triple junction concentrator photovoltaic (CPV) cells as a means of further increasing cell efficiencies. Figure 1 shows a typical efficiency wafer map for a 4-inch QDEC wafer manufactured with quantum dots in Cyrium's mass production process.

Before discussing quantum dots and their impact on the photovoltaic industry, we should begin with a question . . .

What Is CPV?

In flat panel PV, solar cells, commonly crystalline silicon, are mounted at a fixed incline to maximize exposure to the sun. These silicon-based PV materials, which represent approximately 85 percent of industrial production, have conversion efficiencies of 10 to 20 percent. In contrast, concentrator PV (CPV) systems do not expose the solar cells directly to the sun. They use optics to "concentrate" the light onto solar cells of reduced size. This presents two benefits: the conversion efficiency increases logarithmically as light intensity increases, and importantly, less solar cell material is needed.

By reducing the amount of solar cell material needed, CPV shifts some of the costs of the energy-producing systems from the semiconductor industry to older highly commoditized industries (metal, plastic, glass). With the solar cells now representing a smaller fraction of the system cost, they can be replaced with the very high conversion efficiency solar cells developed for the satellite industry. These triple-junction solar cells use a combination of semiconductor materials to reach approximately twice the conversion efficiency of industrially produced silicon-based PV materials.

CPV systems, by exposing solar cells to sunlight through optical systems, are only sensitive to direct sunlight. The light that falls on a bright sunny day represents approximately 1,000 W/m^2, of which ~850 W/m^2 is not reflected off surrounding and atmospheric materials, and is therefore termed direct normal incidence (DNI). CPV systems therefore incorporate tracking systems to keep the optical system

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			40.4	40.6	40.7	40.8	40.9	40.9	41.0	41.0			
		40.8	40.7	40.7	40.7	40.2	40.9	40.9	40.9	40.9	40.9		
	40.8	40.9	41.0	40.9	40.3	40.4	40.5	40.6	40.6	40.9	40.8	40.6	
	41.0	41.3	40.9	40.9	40.6	40.8	40.8	40.7	40.6	40.9	40.8	40.8	
40.8	41.1	40.9	40.8	40.8	40.8	40.5	40.3	40.5	40.6	40.5	41.0	40.9	40.8
40.8	41.1	41.0	40.9	40.7	40.6	40.3	40.4	40.1	40.4	40.3	40.6	40.7	41.0
40.9	41.1	40.6	40.7	40.6	40.3	40.6	40.3	40.2	40.5	40.6	40.8	40.7	40.6
41.0	41.2	40.9	40.8	40.1	39.8	40.4	40.5	40.3	40.5	40.3	40.8	40.6	40.0
41.2	40.9	40.9	40.8	40.4	39.7	40.2	40.3	40.6	40.7	40.3	40.8	40.6	40.8
41.1	41.1	40.9	40.5	40.5	39.7	40.5	40.6	40.5	40.3	40.4	40.4	40.6	40.1
	40.7	40.8	40.7	40.0	39.0	40.0	40.5	40.2	40.4	40.8	40.6	40.8	
	40.8	40.1	40.7	40.6	40.1	40.1	40.4	40.6	40.7	40.5	40.6	40.6	
		39.4	40.4	40.5	40.5	40.6	40.7	40.7	39.9	39.1	40.4		
			40.9	40.7	40.0	39.9	40.6	40.7	38.2	38.2			
				39.2	38.4	39.3	40.2	40.5	40.0				

Figure 1 – Quantum-dot enhanced cell efficiency (%) map. Four-inch wafer of InGaP/InGaAs(QD)/Ge triple-junction 5.5 x 5.5 mm cells.[2]

<< PREVIOUS PAGE | NEXT PAGE >>

aligned directly onto the sun. Even though this represents additional costs, because the solar cell represents a significantly reduced fraction of the system cost relative to flat panel PV, and because the system itself is produced in commoditized industries, CPV systems are manufactured at a competitive ¢/kWh (levelized cost of energy, as discussed in the final section of this article).

Challenge: Middle Cell Limitation

Solar cells convert light by exciting electrons across the band gap (Eg) of a semiconductor, creating electron-hole pairs. The p-n junction then drives these electrons and holes in opposing directions, producing a potential difference approximately equal to the band gap.

Triple-junction cells, because they share the available light over three sub-cells, have reduced currents relative to single-junction cells. The sub-cells, because they are stacked and therefore connected in a series circuit, see their voltages add up yet are limited in current by the sub-cell producing the lowest current. The addition of the three voltages more than compensates for the reduced current, so that the output power of triple-junction cells is greater than that of single-junction cells. This is how CPV cells reach their higher conversion efficiencies.

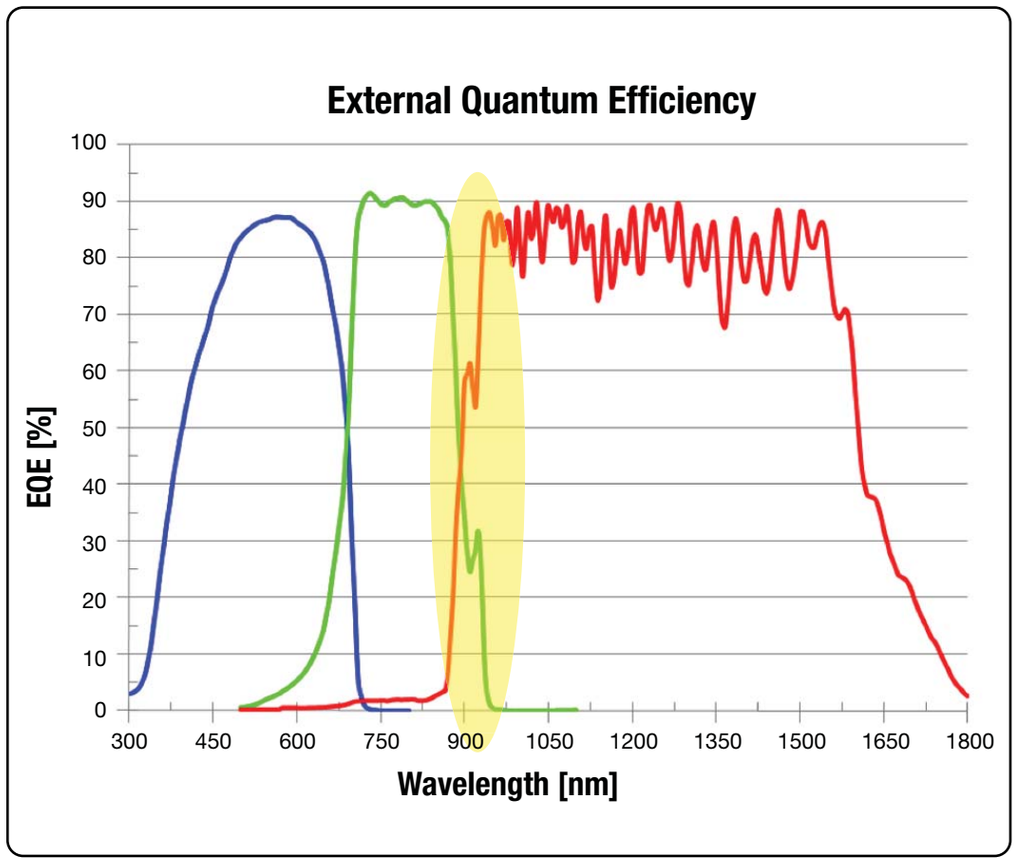

Figure 2 – External quantum efficiency of the three sub-cells in the QDEC product showing the middle cell (in green) "stealing" current (highlighted) from the bottom cell (in red).[2]

The thickness of each sub-cell must be adjusted based on its absorption efficiency and the amount of light available in the spectral range it covers. Standard triple-junction solar cells comprise three cells: a top cell of (Al)GaInP (Eg ≈ 1.9 eV); a middle cell of GaAs (Eg ≈ 1.4 eV); and a bottom cell of Ge (Eg ≈ 0.7 eV). Because the Ge layer (the substrate) is much thicker than the other two cells (more than 100 µm vs. a few µm), and because it covers a much greater spectral range, the current produced by the Ge cell far exceeds that produced by the GaInP and GaAs cells. Even in the standard design, the GaInP, which is adjusted to match the current of the GaAs cell, still has some "wiggle room"; making it thicker would increase its current, but the GaAs cell is effectively maxed out.

Solution: Quantum Dots

If a semiconductor heterostructure consists of a region of lower band gap material bordered on either side by higher band gap material, the electron and holes mentioned in the previous section will be confined within the region of lower energy. The smaller the region of lower energy, the higher the energy levels of the electrons and holes are pushed up (imagine squeezing a balloon horizontally in your hand, making it expand upward vertically). By adjusting the size of the region of lower energy, it is therefore possible to design the energetic properties of the material; in other words, it is possible to tailor-design the band gap of the composite material. Such confined structures produced in one, two or three directions of the same structure are referred to as quantum wells, quantum wires and quantum dots, respectively.

Nature provides a mechanism that leads to the spontaneous formation, or self-assembly, of ensembles of quantum dots. The self-assembly of quantum dots occurs due to the relaxation of strain energy in epitaxial systems in which the deposited material has a lattice parameter that is significantly larger than that of the underlying material. InAs has a lattice parameter that is 7.2 percent larger than GaAs. Quantum dots therefore form in the growth of InAs on GaAs, creating a structure that is somewhat reminiscent of the appearance of water droplets on a flat surface.

Similarly to how the thickness of a sub-cell can be adjusted to optimize the current it produces, through band gap engineering it is possible to adjust the current produced by reducing or expanding the range of light that is absorbed by a sub-cell: wider range → more light → more current and vice versa. Quantum dots, by strongly confining the energy levels of the electrons and holes, offer the solar cell designer the greatest control in band gap engineering.

<< PREVIOUS PAGE | NEXT PAGE >>

Quantum Dot Benefits to Triple-Junction Cell Performance

By introducing InAs-based quantum dots in the GaAs sub-cell, and by engineering these quantum dots to have an effective band gap that is slightly lower than that of GaAs, Cyrium's technology has made it possible to extend the band edge of the middle cell to longer wavelengths, thereby stealing current from the Ge bottom cell. This is illustrated in Figure 2, where we can see that the absorption of the GaAs sub-cell in QDEC devices is extended from roughly 890nm to 940nm, and where we can also see a proportional drop in the light absorption of the Ge bottom sub-cell.

The Ge cell therefore has its current reduced, but still has enough current to avoid limiting the triple-junction current. The GaAs cell has its current increased, by an amount proportional to the extra area under the green curve in Figure 2, say 15 percent (more quantum dots → greater percentage), and due to its absorption properties, the GaInP top cell can be increased in thickness to match the increased current of the GaAs middle cell. As a result, the current of the triple-junction cell is increased by 15 percent, and the voltage contribution of the GaAs middle cell is reduced minimally, proportionally to the reduction in band gap of the middle cell over the voltage of the triple junction, roughly 50 mV in 3.0 V, about 0.17 percent. This leads to an increase in triple-junction conversion efficiency of about 13 percent (1.15 x 0.98).

	Reference Model	Model 1	Model 2	Model 3	Model 4
System selling price per watt	$5	$5	$4.53	$5	$4.80
1 MW plant selling price	$5,000,000	$5,000,000	$4,525,000	$5,000,000	$4,800,000
Efficiency of cells at 25C	38%	42%	42%	42%	42%
Watts per cell at operating T	15.6	17.2	17.2	17.2	17.2
Number of units required	64103	57998	57998	57998	57998
Average selling unit price [1]	$78	$86	$78	$86	$83
Cell cost to system co.	$10	$10	$10	$17	$13
Total cell cost to system co.	$641,026	$579,976	$579,976	$960,927	$724,969
Unit cost (assuming 20% margin) [2]	$62	$62	$62	$62	$62
Unit cost (everything except cell)	$52	$52	$52	$52	$52
Total cost (everything except cells)	$3,358,974	$3,039,072	$3,039,072	$3,039,072	$3,039,072
Total cost for the plant	$4,000,000	$3,619,048	$3,619,048	$3,999,999	$3,764,042
Margin for the system co.	20%	28%	20%	20%	22%

[1] Cell, bypass diode, carrier, primary & secondary optics

[2] Hardware, heat sink and average amortized BOS

Assuming no secondary cost reduction in production/installation due to efficiency increase - LCOE models suggest there would be.

Figure 3 – Cost model for HCPV system deployment accounting for increase in cell efficiency. Model 1: All benefits to system manufacturer. Model 2: All benefits to end user (e.g., utility). Model 3: All benefits to cell manufacturer. Model 4: Shared benefits.

The leading cost metric used by the energy industry is the levelized cost of energy (LCOE), commonly expressed in ¢/kWh, which is the average cost of energy produced over a plant's lifetime.

Business Impact of Quantum Dot-Enhanced Cells

The cell design change involved in introducing quantum dots in the GaAs cell is done entirely in the epitaxial process; no changes need be made to the industrial production process either downstream (wafer fab, assembly) or upstream (substrate processing) of the epitaxy. No change in equipment, no additional steps in processing and no additional steps in inspection need be introduced. In other words, the extra conversion efficiency, the extra watts produced, are obtained at nominally the same processing cost.

The leading cost metric used by the energy industry is the levelized cost of energy (LCOE), commonly expressed in ¢/kWh, which is the average cost of energy produced over a plant's lifetime, calculated in terms of the present day value of energy. In addition to the amount of energy produced, LCOE models consider the following: initial capital investment, operating costs, depreciation, component life, value of system at end of useful life, annual system degradation, as well as financial considerations such as cost of capital (investment and operational), inflation rate and price of energy at distribution point.

For a given plant power production, a gain in conversion efficiency produces second-order cost reductions in production and deployment, such as reduced cost for real estate (X percent more power from the cells means roughly X percent less real estate needed); reduced deployment costs (proportionally fewer systems to transport and install); proportional reduced financing costs, etc.

Table 1 presents a model of the impact of an increase in conversion efficiency on profit margins. A 10 percent relative increase in efficiency is assumed, but no second-order cost reductions are assumed in production or deployment. Models 2, 3, and 4 partition the margin benefits among

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the supply chain and end user, and model 1 attributes all benefits to the systems producer, who obtains in this case a relative margin increase of 40 percent.

Ultimately, the business impact of quantum dot technology in the CPV industry is due to a cell redesign that does not involve any increase in process cost. Cyrium's epitaxial quantum dot technology leads to gains in efficiency in energy generation and reductions in costs across multiple contributions to LCOE.

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About the Author

Bruno Riel – *In 2004, Dr. Riel left his position as a research officer at the National Research Council Canada to join Cyrium Technologies as director of Advanced Materials. He helped design the quantum dot material, as well as Cyrium's III-V on Ge nucleation process, and grew the first prototypes of quantum dot-enhanced GaAs solar cells. Dr. Riel is a strong proponent of the Theory of Constraints – Lean Six Sigma in the fabless manufacturing model, and is now Cyrium's director of Quality Assurance and Reliability.*

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MANUFACTURING EQUIPMENT & MATERIALS

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Bryan Ekus
Managing Director, International PV Equipment Association

In today's photovoltaic industry, the challenges are in many ways the same as any global manufacturing sector – to improve efficiency and quality, reduce costs and optimize the manufacturing supply chain. The IPVEA (International Photovoltaic Equipment Association) continually strives to help its members in particular, and the industry in general, to achieve these goals with a series of initiatives. Key to these initiatives is our partnership with publications, such as Future Photovoltaics, that investigate the latest ways in which research and development can help move forward on commercial goals.

The research in the following paper looks in particular at the cost-per-watt reduction. Among many other elements, cost-per-watt reduction is key for commercial success, and this is being achieved through reduced material cost and higher cell efficiencies. In order to achieve these higher efficiencies, effective passivation of the rear surface of industrial solar cells is required.

While thermally grown silicon oxides provide an excellent level of surface passivation on low-doped p-type surfaces, dry thermal oxidation processes require relatively high temperatures and long process times. To decrease both oxidation temperature and process time, the dry oxidation process can be replaced by a wet oxidation.

Researchers from RASIRC and the Fraunhofer Institute for Solar Energy Systems (ISE) report on using wet oxides grown from purified steam to provide a high level of surface passivation. This is at least comparable to wet oxides grown by the standard pyrolytic steam process, where the water vapor is generated from high-purity gases. In this manner, conversion efficiencies above 20 percent can be achieved.

Click here to return to Table of Contents

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Generating Energy for PV-Specific Standards

For the global photovoltaic (PV) power industry to prosper, it must become more competitive with the cost of traditional electric power. That means reducing the cost per kilowatt-hour (kWh) associated with solar-generated power to a level that yields grid parity between solar power and traditional electricity.

Among the factors that weigh on the PV industry's ability to achieve grid parity are standards that add to the total cost per kWh. Following standards is a preferred practice as specifications ensure quality in components, processes, manufacturing and end-product performance.

However, in some cases, PV standards may be stricter than what is necessary to ensure the safe, efficient generation of power. By their nature, tighter specs are more costly. As PV energy producers and market suppliers work toward reducing costs, they need to examine existing standards and determine if less stringent specifications can yield acceptable results while saving money.

Swagelok is addressing one such area of PV manufacturing that defines specifications for stainless steel components used in the production of solar cells. The new Swagelok Photovoltaic Process Specification (SC-06) is the photovoltaic industry's first specification for processing stainless steel fluid system components. It's based on our work in the industry, and continues Swagelok's leadership in process-specific cleaning, which began in the 1980s with ultrahigh-purity components.

With Swagelok SC-06, you can now specify fluid system components with cleanliness and purity levels that closely match the true process requirements for solar cell production. Products processed with SC-06 bridge the gap between ultrahigh-purity standards and the more limited requirements of general industry products. Applied to gas handling components in your system, this specification is designed to help lower overall cost of system ownership. All with the peace of mind that comes with the quality and reliability of Swagelok® products. Using SC-06, our customers take one step closer to grid parity.

To learn more about Swagelok SC-06 and applicable products, visit: www.swagelok.com/solar

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<< PREVIOUS PAGE | NEXT PAGE >>

Comparison of PV Efficiency Using Different Types of Steam for Wet Thermal Oxidation

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[1]RASIRC [2]Fraunhofer Institute for Solar Energy Systems (ISE)

Abstract

Effective passivation of the rear surface of industrial solar cells is required to improve the conversion efficiency. Thermally grown silicon oxides provide an excellent level of surface passivation on low-doped *p*-type surfaces. However, dry thermal oxidation processes require relatively high temperatures (~1000°C) and, due to the low growth rate, long process times. To decrease both oxidation temperature and process time, the dry oxidation process can be replaced by a wet oxidation. The most common way to introduce high-purity water vapor into the oxidation tube is pyrolytic generation from high-purity gases (H_2 and O_2). Recent technology has enabled the direct purification of steam – a simple cost-effective option for the supply of water vapor. The passivation quality of dry and wet oxides, the latter grown from pyrolytic-generated water vapor and purified steam, was compared. The passivation quality for the wet oxides grown from purified steam was found to be comparable to those oxides grown from pyrolytic-generated steam. On laser-fired contact (LFC) solar cells, conversion efficiencies well above 20 percent could be reached independent of the oxide that was applied for the rear-side passivation.

Introduction

Cost-per-watt reduction is the key for commercial success of photovoltaics. This is being achieved through reduced material cost and higher cell efficiencies. Cost reduction occurs through a combination of multicrystalline silicon, thinner wafers and higher levels of automation. Cell performance is improved via new structures like PERC-type[1,2] solar cell structure, where a passivated rear side becomes crucial. However, an industrially feasible rear surface passivation layer is still needed.

Using silicon nitride, excellent surface recombination velocities have been achieved on *p*-type surfaces.[3] However, the relatively high density of fixed positive charges within this layer creates a shuntlike behavior when integrated as the rear-side passivation of PERC-type solar cells.[4]

The highest conversion efficiencies so far have been realized for cells with a rear surface passivated by a thermal SiO_2.[5] The introduction of thermal oxidation into industrial production processes therefore is investigated.[6-8] However, the high temperatures (~1050°C) that are needed for dry thermal oxidation are not compatible with the solar cell production process. Above all, multicrystalline silicon substrates demand low temperatures for oxide growth to avoid minority carrier lifetime degradation.[9] By replacing dry oxidation with wet oxidation, process temperatures can be lowered from ~1050°C to below 900°C.

A major drawback to rear oxide passivation has been the time and temperature required to grow a passivated layer. Dry oxide passivation has been considered the premier technique for growing high-quality oxide. The time to grow a 100nm film is 84 minutes at 1050°C. Cost reductions can be achieved by replacing monocrystalline silicon with multicrystalline. However, at high temperature, the multicrystalline wafers can degrade. If a lower temperature such as 850°C is used, time to grow an oxide is 22 hours. This is not practical for production purposes.

By moving to wet thermal oxidation, process time can be reduced to 58 minutes at 850°C. If only a 10nm film is needed, a wet oxide film can be grown in less than five minutes. While it is well known that wet thermal oxidation is significantly faster than dry oxidation, films grown in dry oxidation are assumed to have better electrical performance. The most common way to introduce high-purity water vapor into the oxidation tube is the pyrolytic generation from high-purity gases (H_2 and O_2). This technique was developed for semiconductor processing where processing cost and safety are secondary to film performance. With respect to solar cell processing, the ability to eliminate the costs associated with hydrogen and oxygen combustion and the related safety issues opens the opportunity to evaluate other methods for steam generation. A new technology that generates ultrapure steam by purifying steam generated from deionized water was tested. RASIRC Steamer was installed on a Tempress furnace for testing purposes. The Steamer uses deionized water as its steam source,

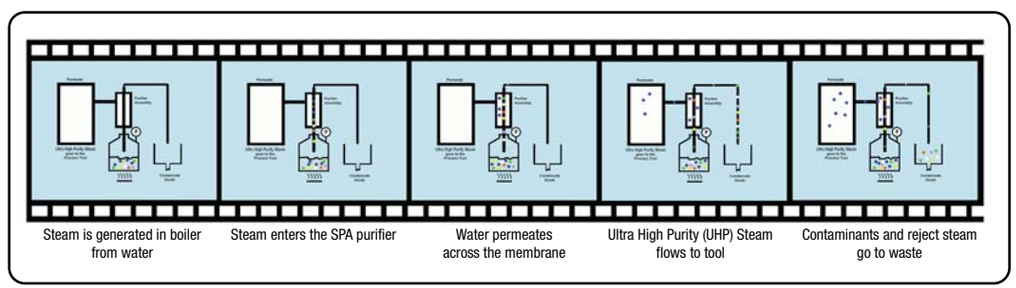

Figure 1 – Direct Steam Generation, Purification and Delivery Process

<< PREVIOUS PAGE | NEXT PAGE >>

thus eliminating all dependence on hydrogen and oxygen gases. The Steamer creates ultra-high-purity steam using controlled delivery systems and proprietary steam purification technology.

The Steamer uses a non-porous hydrophilic membrane that selectively allows water vapor to pass. All other molecules are greatly restricted, so contaminants in water such as dissolved gases, ions, TOCs, particles and metals can be removed in the steam phase. The need for a carrier gas is eliminated and the steam is delivered at a constant positive pressure. This enables delivery of 100 percent pure water vapor, ensuring maximum theoretical oxide growth rate is achieved. Figure 1 illustrates the basic steam purification and delivery process.

Figure 2 shows a comparison of oxidation times for dry and wet processes. The growth rate between different steam delivery technologies is also shown with the steamer being the fastest and water bubblers being the slowest for wet oxidation. Based on these potential advantages in cost, safety and throughput, a comparison of the passivation quality of dry and wet oxides – the latter grown from pyrolytic generated water vapor and purified steam – is presented.[10]

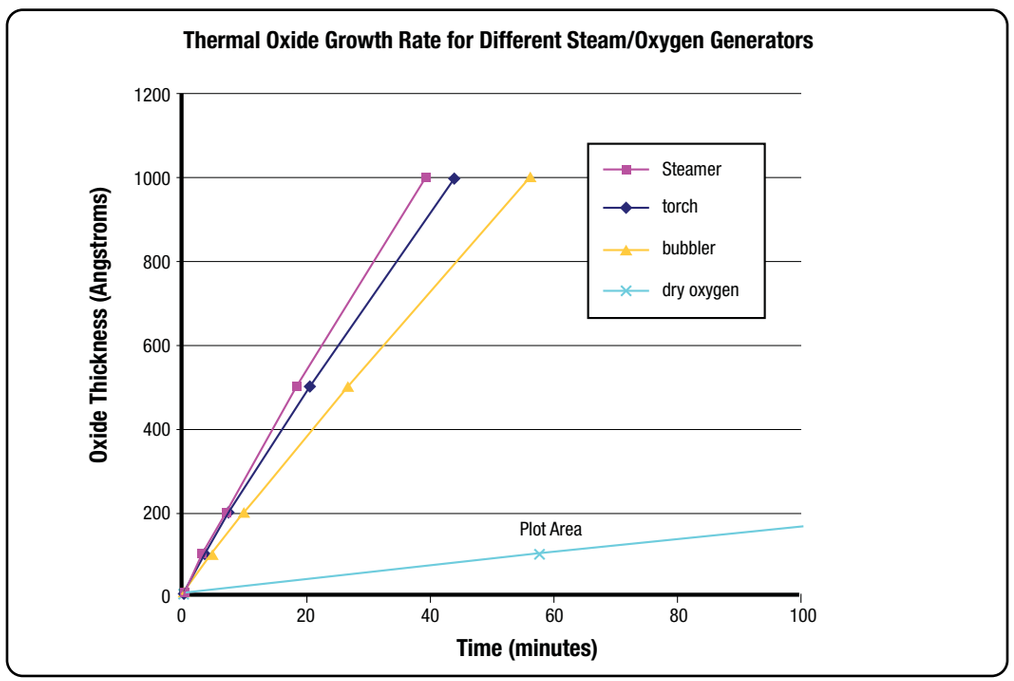

Figure 2 – Typical Oxide Growth Rate for Wet Oxidation With a Steamer, Torch or Bubbler vs. Dry Oxidation at 900°C

Lifetime Investigation

Experimental

Dry and wet silicon oxide layers have been grown on 250 µm thick 1 Ω cm *p*-type FZ silicon wafers. Wet oxides were grown at 850°C under H_2O ambient (80nm: 60 min, 200nm: 150 min). The water vapor for the wet oxidation was introduced into the tube in two different ways:

- purified ultrapure steam (RASIRC® Steamer)
- pyrolytic generation from ultrapure gases $H_2$and O_2

The steam generator and the torch for the pyrolytic generation of water vapor were not installed in the same tube; thus, wet oxidations were performed at different furnaces. Dry oxidations were grown at 1050°C under ambient oxygen (80nm: 40 min, 200nm: 150 min) in the same tube as the wet oxidation using purified steam. After oxide growth, all samples received a forming gas anneal (FGA) at 425°C for 25 min. The QSSPC method (lifetime tester WCT 120) is used to measure the injection-dependent effective lifetime τ eff [11].

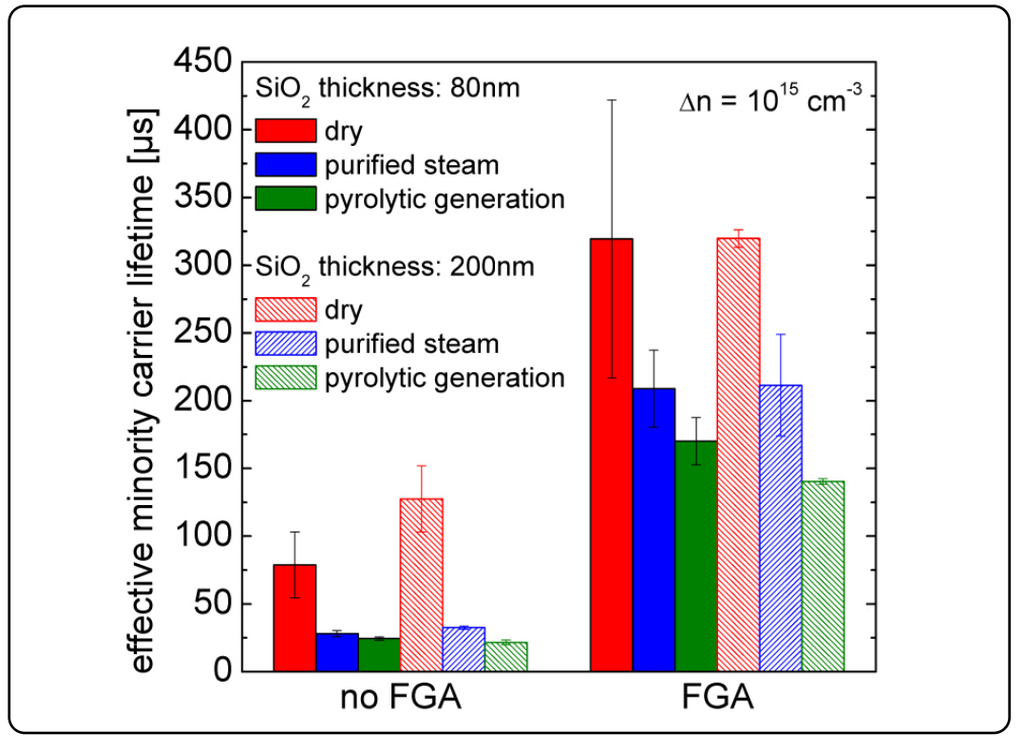

Figure 3 – Comparison of the surface passivation quality of dry and wet thermal oxides. The wet oxides were grown from purified steam as well as from pyrolytic generation of water vapor.

Results

The measured lifetimes (at an injection level of Δn = 1015 cm^{-3}) of the samples passivated by the different oxides are shown in Figure 3. As expected, after the post-oxidation anneal in a forming gas atmosphere, the measured lifetime of all samples increased significantly. With a measured lifetime of ~300 µs, the dry thermal oxide shows the highest passivation quality. Nevertheless, the wet oxides show a sufficient level of surface passivation in the range of ~150 to ~200 µs. The wet oxides grown from purified steam provided a higher level of surface passivation relative to pyrolytic steam generation. However, different oxidation tubes of different furnaces have been applied for the wet oxidations, leading to an uncertainty of the direct process comparison. The injection level dependence of the oxidized samples is shown in Figure 4. The samples passivated by the wet oxide grown from pyrolytic-generated water vapor show a more pronounced injection-level dependence compared to the other oxides after FGA. For the operation at the solar cell rear side under one-sun illumination (i.e., low-level injection), such a behavior might alter the efficiency potential. The rear side of the high-efficiency solar cell is covered by aluminum and thus at the device level, the rear side oxides receive an anneal process,[12] which considerably enhances the passivation quality compared to the anneal in forming gas. Therefore all oxides are expected to perform a sufficient level of rear-side passivation for the applied LFC solar cell structure.

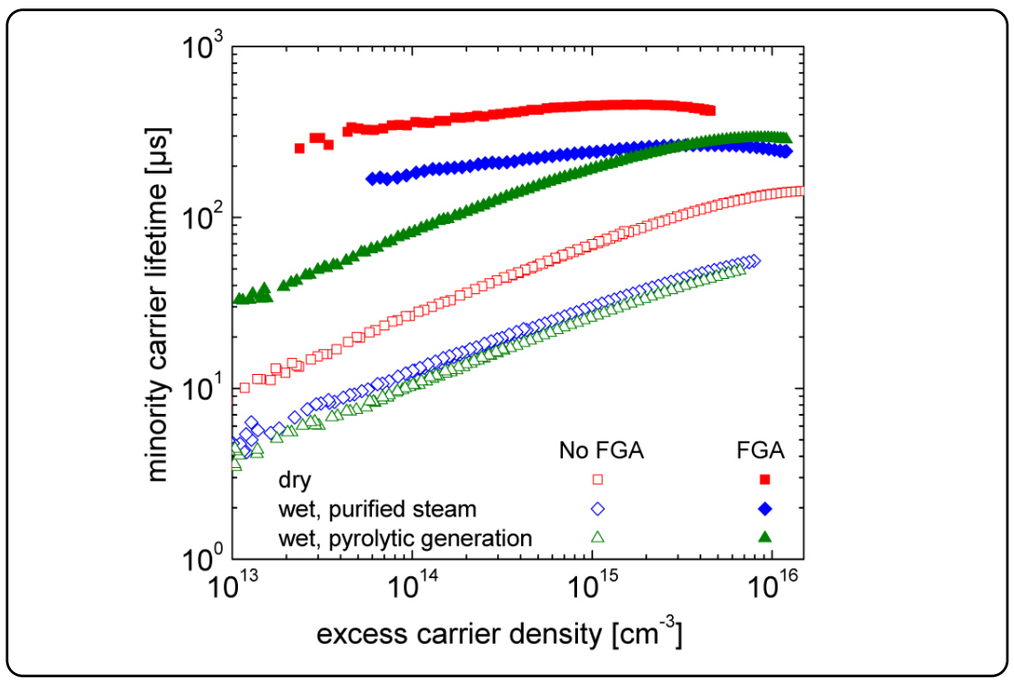

Figure 4 – Injection-dependent lifetime of dry and wet ~100nm thick thermal oxides. The wet oxides were grown from purified steam as well as from pyrolytic generation of water vapor.

Solar Cells

Experimental

In order to investigate the rear-surface passivation quality of the different dry and wet oxides, LFC solar cells were fabricated on <100> 1 Ω cm, FZ, *p*-type c-Si wafers with a thickness of 250 µm. These cells (area = 4 cm^2) feature a front surface with inverted pyramids and evaporated Ti/Pd/Ag front contacts that are thickened by light-induced plating.[13] The rear surface is passivated by the respective ~100nm thick thermally grown silicon oxides that have been presented in section 2. This oxide also acts as the diffusion mask for the front-side phosphorus diffusion. The rear-side metallization is realized by a 2 µm thick aluminum layer that is contacted by the laser-fired contacts (LFC) process that leads to the formation of a local Al-BSF underneath the contacts.

$POCl_3$ diffusion occurred at 810°C, resulting in a sheet resistance of ~110

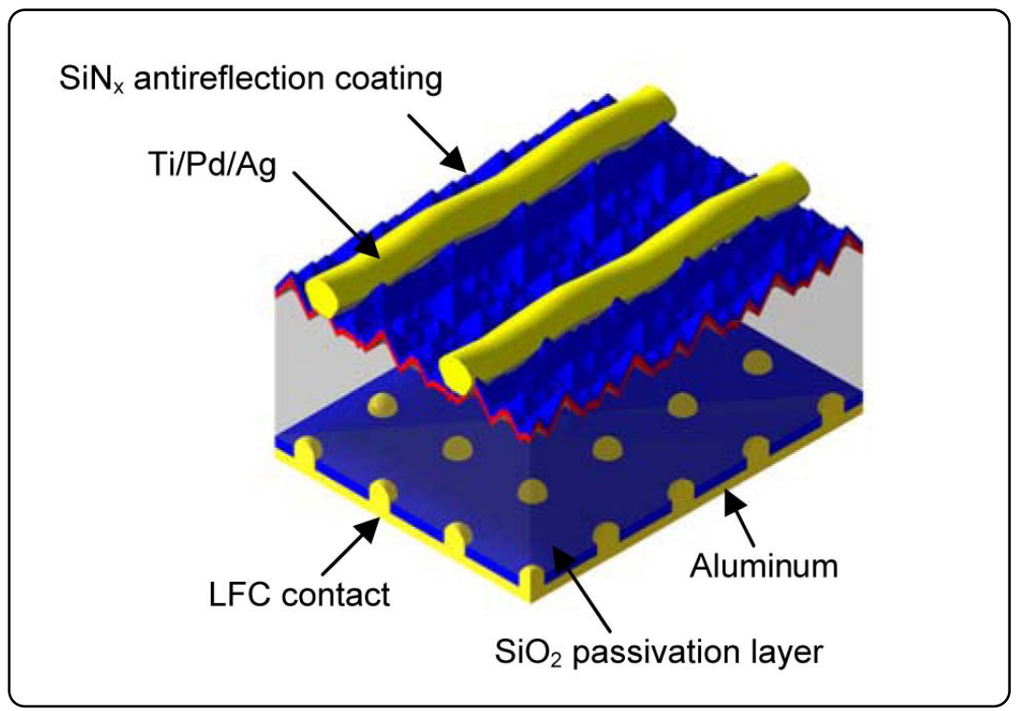

Figure 5 – Applied LFC Solar Cell Structure

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Ω/sq. This front-side phosphorus emitter is passivated by a 70nm thick SiNx ($n \approx 2$). To ensure the electrical contact and to remove the damage introduced by the X-rays during the e-gun evaporation processes, the samples achieved an annealing step at 425°C in forming ambient gas. The structure of the applied LFC solar cell is shown in Figure 5.

Results

The one-sun parameters of the LFC solar cells featuring the rear-side passivation by the different dry and wet thermal oxides are summarized in Table 1. It can be seen that the open-circuit voltage of the solar cells (the most sensitive one-sun parameter with respect to the surface passivation) with the different oxides for the rear-side passivation is comparable. With an average of 650.6 mV and a maximum of 652.4 mV, the highest Voc could be reached with the rear side passivated by the dry SiO_2. However, also for the wet oxides, average open-circuit voltages of 648.4 mV and 649.3 mV for the oxides grown by purified steam and pyrolytic generation of water vapor, respectively, have been reached. Also the short-circuit current density of 39.8 to 39.9 mA/cm² is comparable for all cells. Thus, a high conversion efficiency (>20 percent) could be obtained for all cells.

For cells passivated by the wet oxide grown from purified steam, an average series resistance of ~0.8 Ω cm² was determined. For the other cells, a considerably lower series resistance of ~0.5 Ω cm² could be measured.

The higher series resistance is due to the fact that purified steam is 100 percent water vapor. The pyrolytic steam is 90 percent water vapor and 10 percent oxygen. This reduces the maximum growth rate by 7 percent.[14] This was reported as a thickness of 110nm for the wet oxide grown from purified steam and a thickness of 100nm for the dry oxide films and the pyrolytic steam. The LFC process for purified steam cells was inferior to the cells with the optimum oxide thickness of ~100nm, as can be seen by the micrographs of the LFCs in Figure 6. For the 110nm thick SiO_2, the contact region in the middle of the contact is only connected to the rear-side metal by narrow metal bridges. The LFC process was optimized for the 100nm. The faster growth rate of purified steam is an advantage over pyrolytic steam for throughput purposes, but requires that recipes be modified for optimum LFC performance. Even without optimization of the LFC process, wet oxides grown from purified steam are well suited for the application of rear-side passivation of high-efficiency LFC solar cells.

Conclusions

Wet oxides grown from purified steam have been shown to provide a high level of surface passivation that is at least comparable to wet oxides grown by the standard pyrolytic steam process, where the water vapor is generated from high-purity gases (H_2, O_2). The rear side of solar cells have been passivated by a wet oxide grown from purified steam at a temperature of 850°C. As a reference, a standard wet oxide was grown at the same temperature as well as a dry oxide grown at 1050°C. For all cells,

	V_{oc} [mV]	J_{sc} [mA/cm²]	*FF* [%]	η [%]
dry oxidation (1050°C)				
Average (28 cells)	650.6 ± 1.3	39.8 ± 0.3	80.1 ± 0.7	20.7 ± 0.2
Best	652.4	39.9	80.5	21.0
wet oxidation, purified steam (850°C)				
Average (28 cells)	648.4 ± 3.4	39.9 ± 0.5	78.1 ± 1.0	20.2 ± 0.3
Best	650.7	40.1	79.1	20.6
Wet oxidation, pyrolytic generation (850°C)				
Average (28 cells)	649.3 ± 1.8	39.8 ± 0.2	79.5 ± 1.5	20.5 ± 0.4
Best	651.7	39.9	80.5	20.9

Table 1 – One-sun parameters of LFC solar cells with different rear-surface passivations: (i) dry SiO_2; (ii) wet SiO_2 (purified steam); (iii) wet SiO_2 (pyrolytic generation of water vapor)

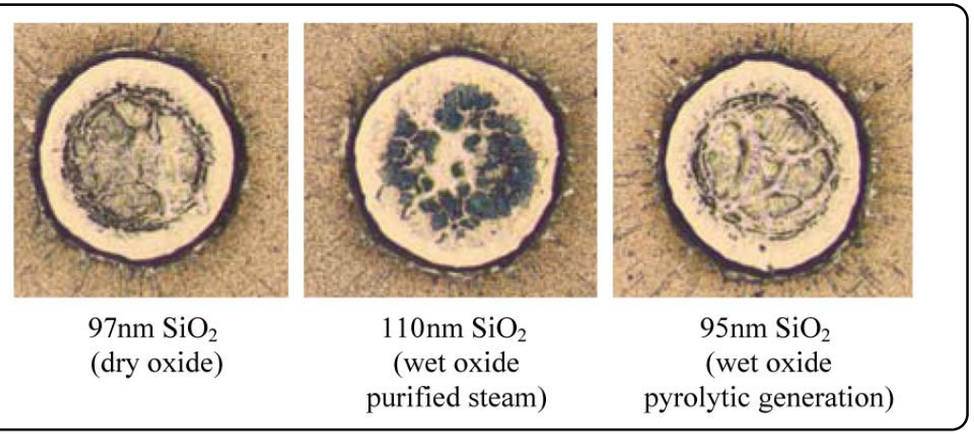

Figure 6 – Micrographs of the rear-side LFCs. Due to the increased thickness of the wet oxide grown by purified steam (exceeding the optimum thickness of ~100nm), the LFC of these cells did not work properly.

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conversion efficiencies above 20 percent could be achieved. The average open-circuit voltages for the different rear-side passivation layers lie in a very close range of 648.4 mV for the wet oxide grown from purified steam to 650.6 mV for the dry oxidation.

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About the Authors

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☞Click here to return to Table of Contents

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MANUFACTURING, SYSTEMS & SOFTWARE

Click here to return to Table of Contents PRINT this article E-MAIL this article

Steve Roberts
Automation Engineer, Heliovolt Corporation

Overheard at a technical conference: "The nice thing about standards is … that there are so many to choose from." With both semiconductor processes and electronics assembly under one roof, PV manufacturers have an interesting challenge in deciding which standards, material handling systems and software to use. Whether it's GEM/SECS or OPC, conveyors or robots, MES or SCADA, PCs or PLCs, the decisions are primarily influenced by an individual's past experience, product price, supplier reputation and referrals from other manufacturers. Of course, some competition between suppliers is necessary to drive innovation and keep cost low. However, since PV manufacturers don't talk publicly about their supplier and product selections, we are likely developing too many overlapping solutions to the same problems.

In this first issue of Future Photovoltaics, it is my privilege to introduce two articles that describe opportunities and strategies that will lead to more functional and economical systems and automation for PV manufacturing.

In "PV Manufacturing System Standards at the Crossroads: A Future Retrospective," Alan Weber reviews the "good, bad and ugly" history of the development of various automation standards for semiconductor manufacturing. He proposes that PV manufacturers have a unique opportunity to leverage the benefits and avoid the pitfalls from this past experience as they adopt standards for their factories.

In "Accelerating the Movement to Grid Parity in Photovoltaic Manufacturing," Alan Levine recommends the cost of ownership (COO) model, discrete-event simulation, factory physics and other standards used in semiconductor and flat panel display (FPD) manufacturing for PV. Although PV factories with typical single-product lines seem less complex today, the PV industry will likely evolve to multi-product lines with many of the same requirements as these similar industries.

While it is probably too early for competitive PV manufacturers to collaborate directly on manufacturing systems today, eventually we will realize that we are protecting many of the same secrets and begin to consolidate the duplicate components into more functional and reliable systems. Future Photovoltaics is one forum in which we can begin this discovery.

We look forward to your opinions on these topics and suggestions for future articles.

PV Manufacturing System Standards at the Crossroads: A Future Retrospective

Alan Weber
Alan Weber and Associates

With apologies to Robert Frost, I believe the PV industry stands at an interesting juncture, especially with respect to its approach for developing manufacturing information and control system standards. The industry has a rare opportunity to learn from recent history in the semiconductor industry, and to apply these lessons directly. However, this does *not* necessarily mean following in those same footsteps …

The evolutionary path for industry standards is certainly well trodden and the most familiar, but one can't help but wonder what lies beyond our current view of the potential pathways forward. Moreover, longtime participants of the standards development community who have seen the evolution of semiconductor factory information systems and standards know what is at stake, and realize this is far more than just an intellectual exercise.

The purpose of this article is to acknowledge the progress that has already been made in this relatively young industry, and highlight the issues – technical and business – that should be considered before launching the next major round of effort.

What the PV-EIS TF Has Done Right

Rather than just adopting an existing standard from a similar but distinctly different industry, or picking what may have seemed like an acceptable though proprietary solution at the time, the European Photovoltaic Equipment Interface Specification Task Force (PV-EIS TF) first settled on a prioritized set of requirements. This may seem obvious to some, but many person-eons of software development have been wasted by ignoring this first step.

Next the task force divided itself into two groups, and did a principled and reasonably quantitative analysis of the two major solution alternatives in the context of the requirements, and made their decision based on the results of that process. While it might not have been the first choice for all concerned, the decision to adopt the SEMI Generic Equipment Model (GEM) suite of standards was reached with consensus, and in the words of the ballot authors, "an agreement on one model was considered a groundbreaking and positive outcome of the task force for all involved." Quite an accomplishment.

Having agreed on this key starting point, the group then tailored it only slightly (exclusions/additions) to better suit the PV requirements *without* adding any significant development work. Examples include limiting it to the HSMS protocols (i.e., Ethernet only); specifying SEMI E10 for Overall Equipment Effectiveness (OEE) reporting; adding requirements for specific data values and events; limiting the number of formats for IDs and time stamps; associating equipment/process data with the production context information so they can be correlated later on; and finally provisions for electronic delivery of data dictionaries, testability and other items that leverage almost two decades of GEM experience in the semiconductor industry.

However, this is just the beginning of a long journey. What else should be considered before drawing the next set of block diagrams?

Technical Issues to Consider Next

Although the PV industry is still relatively new, with the recent drop in prices for the end products, there is significant competitive pressure all along the supply chain. In this environment, it is important to decide what role standards should play in accelerating productivity improvements during this growth phase without restricting innovation. This very issue has faced the semiconductor industry at numerous times over the roller-coaster ride of the last 25 years, and this experience provides a number of lessons that can now be applied.

First of all, standards should be viewed like any other complex technology product family, so the entire technology adoption cycle should be planned for. Doing the technical development is less than half of the overall picture. From the point of view of a standard's customers, this includes awareness, interest, experimentation, validation and finally adoption. The activities of a standards group must be tailored to address the careabouts in each phase, so they might include promotion, education, validation prototype development, more promotion, pilot site joint development, migration planning and so on.

This last topic (migration planning) deserves special mention, as the lack of such a plan has delayed or doomed many ambitious standards efforts. This includes understanding what the current "state of the practice" is for the domain of a new standard, and an understanding of how the current stakeholders will be affected. In the words of Mike Leitner (SEMI Standards Communications Committee co-chair circa 1990), "God was only able to create the world in six days because he didn't have an installed base." We definitely live in an evolutionary world.

Another key lesson has to do with system performance. Believing that the adoption process will be much quicker *this* time (despite the lessons of history), we spend a lot of time worrying about whether the computing and communications platforms will support the complexity of a new standard. But this is effectively shooting behind the (system technology) duck. If instead we take the perspective that solutions will be available at the time of actual production that are 10x

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faster and 10x cheaper than today's approaches, the performance problems will mostly take care of themselves. In this case, Moore's Law works to our advantage.

Other key questions that deserve deeper exposition include: What do we now wish we had done with the benefit of 20/20 hindsight? What would we have done differently? And just as important, what would we *not* have undertaken?

A trap familiar to many of us is the temptation to over-engineer. Jack Ghiselli has pointed out many times that "standards are an agreed-upon *arbitrary* technical solution to a business problem" and that the effort needed to raise standards' quality from good to excellent is not worth the investment, even if a team had a clear idea of what that would mean.

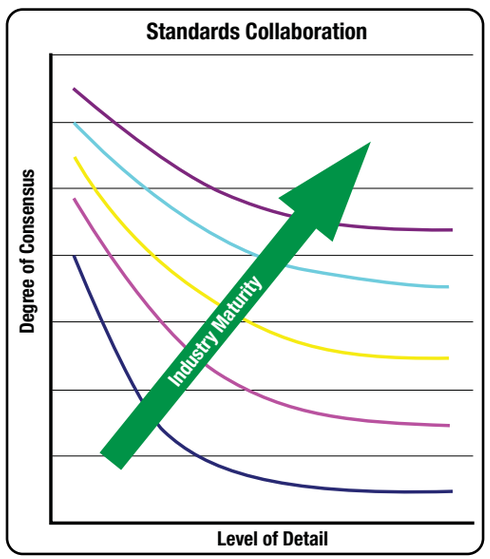

Figure 1 – Industry Maturity and the Consensus Process

Examples fresh in mind include many of the security aspects of the "new" Equipment Data Acquisition (EDA) suite, in particular, the E132 Authentication and Authorization services.

Another example with which I have direct experience is the Recipe and Parameter Management (RaP) standard. While technically very sound and thoroughly tested by three distinct rounds of prototyping and reference implementation development over a six-year period, and promotion across the globe, it still suffers from lack of adoption. What are the reasons for this? Probably a mixture, but at their core, too much complexity for too small a market.

Still another lesson has to do with dependence on other industries. While we have been rightly admonished for inventing a lot of our own standards without seriously looking at what was happening in other industries, the alternative has risks as well. A prime example of this was the decision to use the SECS message on the emerging GM-MAP protocols (who else will admit to remembering this?). When GM-MAP was first introduced and heavily touted, few suppliers of industrial control systems were willing to stand up and voice their objections to this direction, despite the lack of evidence that its complexity was achievable at a reasonable cost. So SEMI Standards participants expended the effort to develop a binding for the SECS-II message set over the GM-MAP network layers. All this technical and administrative effort was lost when the MAP effort collapsed under its own weight …

So the corollary that results is this: When adopting well-proven standards from other (or ideally, multiple) industries, resist the temptation to add too many layers of industry-specific requirements. Picking on EDA again, to some extent, this has already happened; despite the use of ubiquitous Web technologies (XML, XSD, WSDL, etc.), there is still significant complex domain-specific information to deal with, and this has slowed implementation considerably (that, and an ill-timed downturn).

Technology issues are just part of the story. It's also important to look at what business issues have gotten in the way.

The Business of Standards

The biggest problem we consistently face is the cyclical nature of the industry. Moreover, the period of the business cycles is considerably shorter than a full generation of standards. Confounding this problem is the fact that the human resources required are special – people who possess a combination of domain-specific technical skills and industry business sense … precisely the kind that are least available to do standards work during a downturn.

It is also a mistake to try to go too fast – it takes time to build consensus, and if the scope is too large or the level of detail required too great to accomplish in a reasonable time frame, the result will be something that is so abstract it will be useless. This lowering of results and subsequent expectations is an understandable outcome of the "least common denominator" effect, which dominates participant behavior if the overall manufacturing process is in a state of flux and the related supply chains haven't stabilized. As the industry matures, it becomes easier to achieve consensus on a meaningful level of technical detail, which is graphically shown in Figure 1.

On this topic, it is almost impossible to predict this early in the industry's life cycle who the eventual market leaders will be, so nobody is really in a position to define de facto standards. A related topic is M&A activity – just when you think you've got the competitive landscape mapped and balanced, some company will leave the fairway and purchase another company, upsetting the family system. This can be especially disruptive to a food chain if portions of a standard are only supported by a small number of companies.

Another lesson to learn is avoiding linking standards to a major substrate size change or some other industry sea change. The example from the mid-'90s that comes to mind is

OBEM and the 300 mm transition; OBEM wasn't quite ready when the bulk of GEM300 standards were passed, and since this required a complete re-engineering of the embedded equipment control systems, it missed an important development window for the equipment suppliers. Many of the ideas did find their way into the E120/E125 metadata standards for the next generation of data collection, but it was disappointing for the suppliers that had committed major software development efforts to the emerging standard.

Another trap to avoid is believing the myth of "plug and play" at the major application level. It's a well-observed phenomenon that leading companies want to stay that way by keeping as much of the market as possible, and all the customer pressure in the world can't convince them

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to provide a portion of a solution that's not commercially viable on a stand-alone basis. This was one of the principal lessons learned from the SEMATECH CIM Framework program. Although a number of suppliers adopted the basic architecture for their MES products families, the ability to achieve a "best of breed" mix of application modules was never realized. From an architecture and performance standpoint, in this era (late '90s), it was not realistic to expect multiple suppliers to share a common set of infrastructure technologies (read: CORBA was not universally adopted). Moreover, there was not really enough market to go around, so every supplier pursued every opportunity. Today it is technically feasible for major applications to interact effectively, but they still must agree to a lot of detail at the interface points. The only exceptions that come to mind are the well-defined applications with high value, like scheduling and real-time dispatching.

Finally, there is a great need for significant and representative end-user participation, not only through the standards organizations, but perhaps also through pre-competitive consortiums and other collaboration mechanisms. This approach somewhat levels the influence across the stakeholder community, and provides stable funding and continuity over the time frame required to develop ambitious standards.

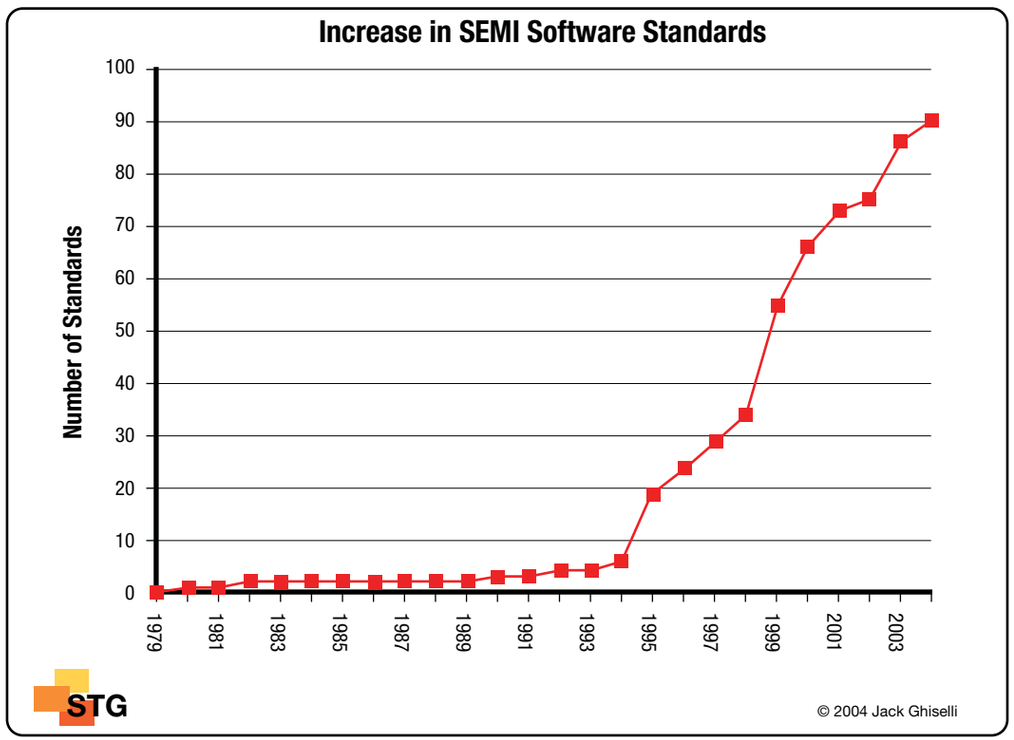

Figure 2 – Standards Development Rate Over Time

What Next?

The answer to this question from a standards development standpoint is not so evident, as the next steps should be guided by a few cycles of learning and accumulated production volume. However, from a deployment and usage standpoint, the following is clear.

Use these standards to collect abundant equipment and process data, even if the applications for it are not apparent at the outset. In particular, make sure enough context information (lot name, substrate ID, recipe name, recipe step number, time stamps, etc.) is included to allow the raw equipment data to be correlated with the production activity at the time. Bandwidth and storage are essentially free, compared to the cost of trying to reconstruct history through the excavation of shallow databases with broken crumb trails.

Implement the OEE models so the equipment suppliers have a baseline performance metric on which to build continuous improvement programs for throughput, reliability and maintainability. Even before the nominal process flow stabilizes the industry, it is not too early to begin characterizing equipment behavior at a fairly granular level. This is especially important as prices drop and the cost pressures increase.

It is probably too early to add much more detail to the interface after the machine-to-machine interface definition is complete. The current shortage of significant end-user participation means there will be few new actual requirements brought to the table. Supplier motivations for continued participation will either be to look for competitive advantage by standardizing some unique feature they have that others have difficulty producing (offensive behavior), or to avoid being locked out (defensive). Finally, with the degree of innovation now seen in the various process flow alternatives, it is possible that some technical discontinuity could change the fundamental factory architecture, reinforcing the idea that the standards development community should stay focused at/near the equipment level. A historical look at the cumulative number of standards created over time for the semiconductor industry (Figure 2) reinforces this point. ■

About the Author

Alan Weber *is the president of Alan Weber and Associates, Inc., a consulting company specializing in semiconductor advanced process control, e-diagnostics and other related manufacturing systems technologies. He was previously the VP/GM of KLA-Tencor's Control Solutions division. Prior to that, Alan spent eight years at SEMATECH and 16 years at TI. He holds a B.S. and an M.S. in electrical engineering from Rice University.*

☞Click here to return to Table of Contents

PRINT this article E-MAIL this article

<< PREVIOUS PAGE | NEXT PAGE >>

Accelerating the Movement to Grid Parity in Photovoltaic Manufacturing

Alan Levine
Wright Williams & Kelly, Inc.

First the good news: The PV industry is maturing. Fortunately for us, our cousins have broken a lot of useful ground. The IC industry has provided insights about how to grow, handle and process silicon. The display industry has provided us information about how to handle and process large, delicate substrates.

Background

While many see the IC industry as closest to the solar industry, it actually mimics the display industry more. Display processes are shorter and more linear than IC processes, with limited re-entrant flows. The processing is high volume, high speed and much less defect sensitive than ICs. There is much less differentiation among products and the capital costs for a facility are similar in magnitude. Perhaps most importantly, there is a clear economic hurdle from an established technology that must be overcome in order to capture significant market share.

In the display world, flat panel displays (FPD) had to overcome the incumbent cathode ray tube (CRT). The ability to lower manufacturing costs enabled FPD prices to drop sufficiently and opened the door to several niche applications. Getting there was no easy task. It involved smart choices on cost-effective manufacturing while concurrently meeting key performance criteria. After decades of development, FPD found a key niche in laptops. Companies saw positive returns on a large enough scale to warrant major investments into new markets. In virtually every segment of FPD, manufacturing efficiency has been the key in transitioning from a niche supplier to a dominant market share position.

The solar world's version of the CRT is called grid parity. As with the CRT, grid parity is not a single number, but an array of numbers based on several factors. Each time grid parity is achieved for a niche, the solar market grows. Achieve grid parity with the mainstream power generation techniques and the world changes.

When we accelerate the industry on the path toward grid parity, we open new markets, improve profits and create the momentum that allows for greater opportunity. So how do we accelerate ourselves along this path?

Grid parity is not easily achieved. Volume alone will not get us there. The quickest way to achieve grid parity is to use our resources wisely. What does this mean? It means innovation and operations must be tied to value. The tools that connect technology to value are known as operational models. Operational models mimic the operation in software (i.e., a factory, a business, a process), in whole or part, in order to assess whether the path the organization is on (roadmaps, developments, etc.) will achieve the desired results. The concepts are tested in software to determine the payback, allowing smart choices to be made about the next steps for the business. At the core of operational modeling is one simple principle: Every decision, even a decision that appears technical, is a business decision.

Productivity Improvement Methods

The tools that were developed to analyze the IC and FPD industries were, and continue to be, enabling technologies for these industries. The tools, such as cost of ownership (COO), cost and resource modeling, and discrete-event simulation, have resulted in massive improvements in cost and performance. These tools are available to the solar industry, and they work beautifully. The underlying standards developed by Semiconductor Equipment and Materials International (SEMI) ported over to the FPD world seamlessly and they also port over to the solar world. The methods that allow information to be analyzed are common to semiconductors, displays, magnetic heads, crystal growing, solar cells, solar modules and thin film panels. These are solved problems. Nonetheless, the solar industry has been reluctant to embrace these tools. While our relatives have done graduate work in these areas, the solar PV world is, by and large, still working on Factory Productivity 101.

The power of operational modeling can be seen from the smallest changes, such as a modest change at a specific process step, all the way to looking at multiple factories running multiple products in multiple locations around the world.

Let's start with a few cautionary notes about common methods employed currently. Intuition does not work well when more than a few variables are in play. Most analyses are laden with subtleties. Single-product factories quickly become multi-product factories with embedded development lines. Companies are constantly ramping products up and down. One company might adopt cash flow as the most critical metric; another company might choose IRR. Quick and dirty spreadsheets used for simplified "greenfield" situations have proven woefully inadequate in real-world situations.

Suppliers occasionally offer a cost analysis to prospective clients, but typically show only what helps them the most. Manufacturers are often just as bad. One client told us that every person who did cost analysis in their operation had their own unique way of doing it. The silver lining was the recognition that cost analysis mattered.

Still, cost is only a modest part of the drive to lower cost per watt. Value is an integral part of the equation. Among solar PV suppliers and manufacturers, it is rare to find the ability to analyze cost and value concurrently.

Using a simple concept to illustrate the way forward, let's look at changing a

<< PREVIOUS PAGE | NEXT PAGE >>

material at a specific process step. How does this change the cost? There are several possibilities. The material itself has a cost. The material may impact the tool it is used on in several ways, such as reliability, preventive maintenance or throughput. It may impact other materials or waste disposal. It may impact multiple processes, not merely the one process where the material is used. Some of these impacts, such as a change in tool productivity, can change the Factory Physics®. It may impact yield, the value of the finished unit and even the probability of a failure in the field. One modest change can have a large number of impacts.

In practice, while it is possible to model everything, most decisions require far less rigor.

When a potential change is identified, the next step is to determine the areas of impact. This is key. There is a tendency to limit the analysis to areas where it is easy to gather data while avoiding what might be more challenging or time-consuming areas of data collection/analysis. This is where we find out if management is serious about optimizing the business, since several things become apparent rather quickly. Does management provide adequate time to do a proper analysis? Are the necessary resources, tools and/or experts available to do the analysis? Are data sets readily available that allow the analysis to be performed more efficiently?

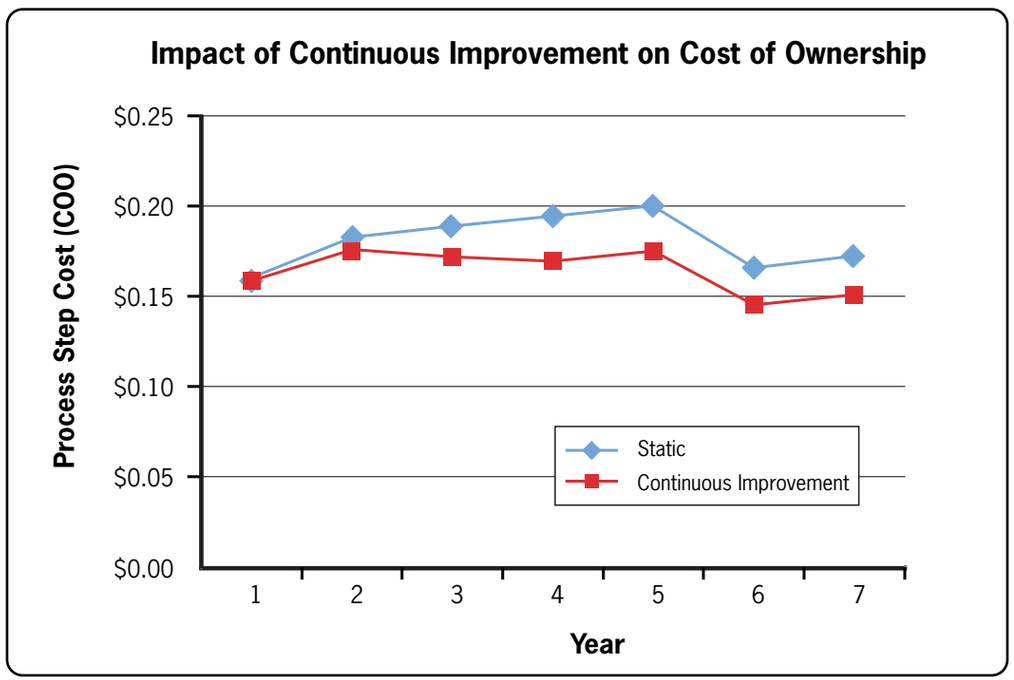

Figure 1 – Continuous Improvement Driven by COO Methodologies

In our experience, technologists and engineers do not spend time calling the finance department to get burdened labor rates; nor should they. In practice, much of the information required to do an analysis is readily available, but a person is unlikely to get the information if it requires them to go to 15 different places to chase it down.

Creating the infrastructure to do analysis work is low in cost and technically straightforward. The major "problem" is rather subtle. The input information cuts across functional lines within the organization, meaning a buy-in must happen across the operation. This broad "buy-in" can create difficulties, even if the technical issues are very modest. In practice, this "buy-in" happens readily when the edict comes from the person at the top of the organizational chart.

The proper use of operational models involves determining the right set of items to consider, not merely what is easiest. This is done by using a list of questions to guide the user in setting up the analysis. In the previous example, one question is, "What other process steps might change based on the original change?"

Once the set of questions has been developed, the next step is to determine the appropriate analysis tool. To analyze a process step, where the issues are essentially self-contained within the step, COO is a very effective tool. To look at sequences that are self-contained, a different form of COO can be used. The COO example in Figure 1 is for a single step. It shows how a sophisticated approach, incorporating continuous improvement, makes a major difference in determining the costs of the operation.

Using the continuous improvement capability in TWO COOL®[1] allows COO to be examined in a realistic manner. In this example, inflation drives labor and material costs up, while improvements in raw throughput, reliability and test times drive costs down. Continuous improvement provides a COO benefit of about 5 percent in year 2 and increases to about 14 percent beginning in year 4.

Once value enters the equation, often in the form of a change in selling price, COO can no longer capture the monetary benefits. At this point, cost and resource modeling takes over. Of note, COO is a subset of cost and resource modeling. Cost and resource modeling looks at the operation as a whole. Often, decisions can be made with subsets of information. If there is a single principle in dealing with models, it is to make them useful, not perfect. By looking at the entire operation, a wide array of potential questions can be answered:

- Will the enterprise make a profit?
- How many people are needed?
- What is the cash flow?
- When to ramp one product down and another up?
- Where to build a new product?
- Should the organization build or outsource?

These decisions can be either tactical or strategic. In either case, modeling provides objectivity, which improves the quality of the decision. The example in Figure 2 shows how product costs change as the factory ramps up some products and ramps down others.

<< PREVIOUS PAGE | NEXT PAGE >>

Projecting total product costs is critical to driving high ROIs. Here, an output from Factory Commander®[1] shows the evolution from a single product factory in the first year to a multi-product factory in subsequent years. The change in total costs reflects the changing costs and volume for each individual product.

There is another element that impacts the relentless drive to improve productivity: factory physics. Factory physics is a broad term used to describe how the operation behaves. In practice, the interactions between complex processes, queues and reliability can have substantial impacts on the productivity of a factory. While there are many aspects to this, the most critical issue typically revolves around optimizing the bottleneck resource. A well-designed operation will usually have the most expensive capital toolset be the bottleneck. The challenge is to ensure the bottleneck is fed with production units 100 percent of the time it is available. Any idle time lost at a bottleneck translates to lost capacity for the entire factory. This is what differentiates a bottleneck process or tool from other processes.

Bottleneck analysis gets complex very quickly. For example, take a situation where two products are run through a non-bottleneck operation. The operation for the first product runs slowly; the operation for the second product runs quickly. If there is a change in the product mix that increases the demand for the first product, the non-bottleneck operation can suddenly become a bottleneck. In practice, there are many items that impact factory physics.

In order to accurately address bottleneck management, a technique called discrete-event simulation is employed. This technique allows companies to see the interactive effects of a very wide array of factors. Often, the challenge in managing a bottleneck resource is driven by an understanding of the variability in reliability of prior steps.

Even when resource availability is highly predictable, it can be a challenge to optimize the factory. For example, preventative maintenance (PM) is highly predictable. Optimizing PMs, especially between linked systems, can be difficult. One step may require a cleaning every 1,000 units, another may require a recalibration every four hours, and a third may need a conditioning process with every 100 µm of deposition.

However challenging the PM schedules are, addressing the variability in reliability is the tougher task. This is not just reliability at the bottleneck, but reliability at upstream process steps that impact the bottleneck. Further complicating the situation is the availability of the resources needed to fix down tools – both people and parts. People have a big impact on downtime characteristics. Cross-training of maintenance staff can be a powerful way to improve bottleneck productivity. Another powerful method is to determine an optimal set of dispatch rules for each tool group. However, the rules are rarely

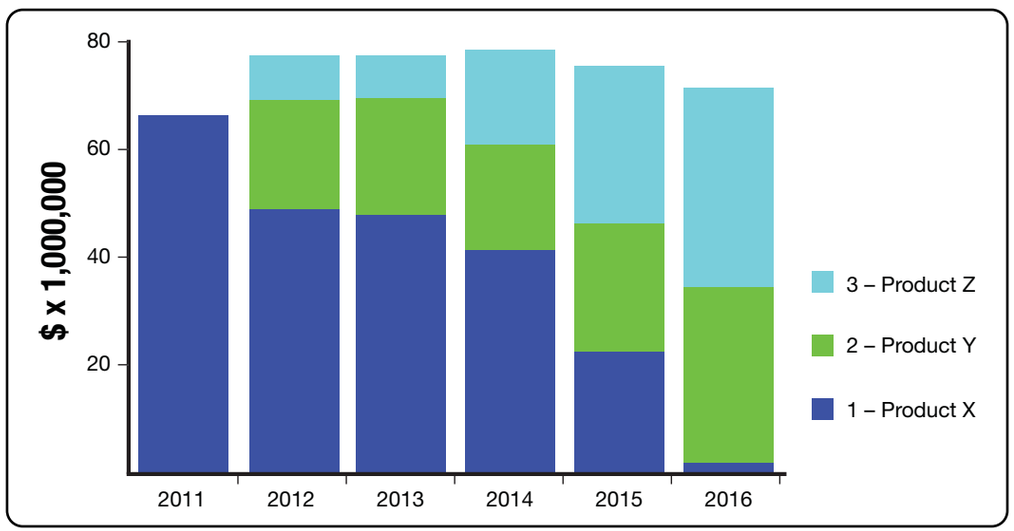

Figure 2 – Total Annual Cost, by Product, in a Multi-Product Factory

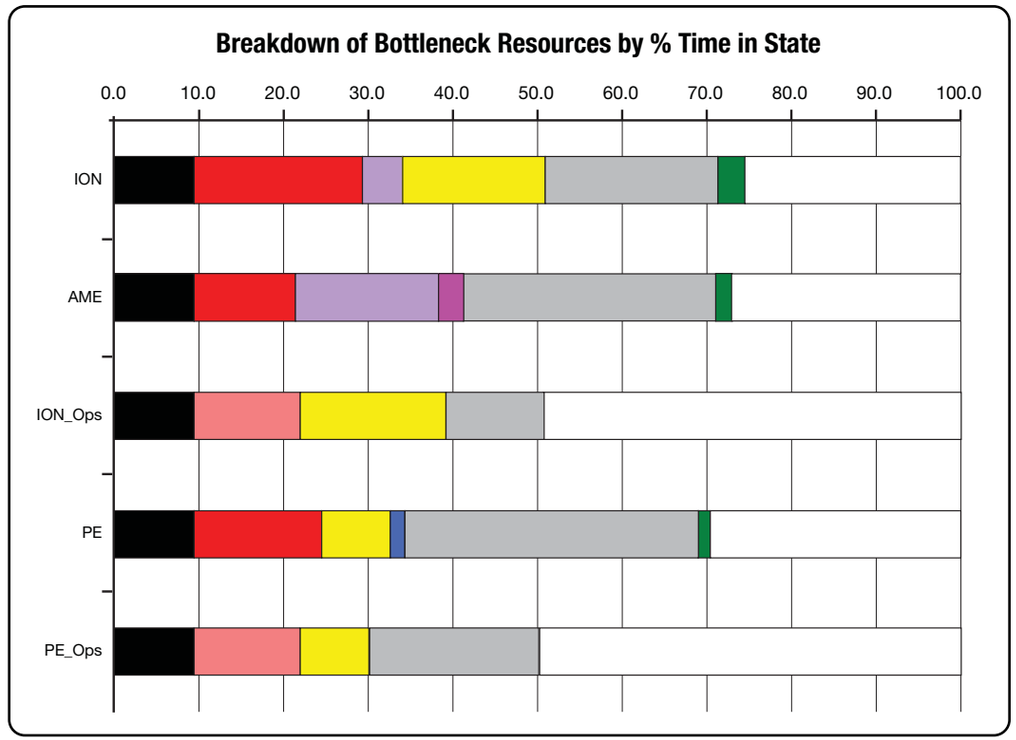

Figure 3 – Operational States of Bottleneck Resources

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intuitive and the number of variations can be quasi-infinite. Discrete-event simulation is the best way to look at a large variety of rule combinations in a very short time frame. Things like intelligent cross-training and an optimal set of dispatch rules can achieve capacity increases of 10-20 percent, even in seemingly well-run operations (see Figure 3).

Factory Explorer®[1] and its discrete-event simulation engine create a detailed understanding of the constraints on the factory. In Figure 3, five resource sets are analyzed for potential bottleneck situations, three tools sets (ION, AME and PE) and two operator sets (ION_Ops and PE_Ops). The colors represent the percent of time a resource is in a given state (i.e., PM, unscheduled downtime, setup time, processing, etc.). Analyzing bottlenecks is necessary to determine the highest payback when allocating resources.

Summary

Technologists try to optimize things like surface reflectivity, uptime and uniformity; but in reality, it comes down to optimizing money. If technical decisions are not tied to money, almost certainly resources aren't being employed wisely. The challenge for companies in the PV industry is to form a bridge between technology, operations and business. The methods for doing this have been pioneered by related industries. The solutions are out there. Invest in them and your business will have a sustainable competitive advantage.

Reference

1. TWO COOL®, Factory Commander®, and Factory Explorer® are commercial software packages from Wright Williams & Kelly, Inc. ■

About the Author

Alan Levine *has spent 30 years working in high-technology manufacturing, with an emphasis on manufacturing productivity. He has been with Wright Williams & Kelly, Inc. since 1995 and focuses on helping clients increase the value they receive from their complex operations. Previously, Alan held positions with Fairchild Semiconductor, KLA Instruments and Ultratech Stepper. He holds a degree in chemical engineering from Cornell.*

☞Click here to return to Table of Contents

PRINT this article E-MAIL this article

METROLOGY, TEST & FAILURE ANALYSIS

Click here to return to Table of Contents PRINT this article E-MAIL this article

Dean Levi
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As the global PV industry expands beyond $40 billion per year in revenues, the race is on to squeeze out every last dollar, euro or yuan from the production process. A major factor in success for PV manufacturers going forward is maximizing production yield through statistical process control and statistical quality control. This presents significant challenges and opportunities in in-line metrology. Unlike the semiconductor industry, there is a lack of well-established metrologies for in-line process control in PV manufacturing.

The development of advanced in-line metrology will facilitate higher manufacturing yields, faster production line ramp-up, lower production cost and higher module efficiencies for a wide range of PV technologies and manufacturers. Advanced statistical process and quality control are keys for the global PV industry to reach the level of manufacturing sophistication required to achieve terawatt production levels.

Alain C. Diebold of the College of Nanoscale Science and Engineering at the University at Albany discusses two promising optical techniques for characterization and metrology of thin film CIGS PV. Ellipsometry is well established for in-line metrology in the silicon semiconductor industry, and promising for monitoring and control of layer thickness and material properties in CIGS PV. Photoluminescence and time-resolved photoluminescence are useful means of characterizing carrier transport in CIGS thin films. Careful measurement and analysis of TRPL can provide a measure of minority carrier lifetime and has been shown to correlate with CIGS device efficiency.

We carry on the theme of minority carrier lifetime (MCL) in our second article, where Tanaya Mankad of Sinton Instruments provides an insightful discussion of the application of MCL measurement for quality control in wafer silicon PV manufacturing. She describes the basic physics of the measurement, why it is useful and what some of the complications and pitfalls are in the process. Measurement of MCL is well established in the wafer silicon PV field, and she provides an overview of the most commonly used techniques as well as a discussion of where in the production process MCL measurement is useful.

Optical Characterization and Metrology of CIGS Photovoltaic Films Using Ellipsometry and Photoluminescence

Alain C. Diebold
College of Nanoscale Science and Engineering

Abstract

The silicon semiconductor community is familiar with the use of ellipsometry and photoluminescence for characterization and metrology. Single-crystal semiconductor films provide "well behaved" samples that are well suited to these methods. Extending these methods to silicon and other inorganic-based photovoltaic (PV) materials (CIGS, CdTe) requires development of new optical models and great care during data interpretation. Ellipsometry is well suited to process control applications and determination of the complex refractive index, while photoluminescence evaluates quality of CIGS through measurement of the lifetime of the electron-hole pairs produced by light absorption. This article reviews the application of these methods to Cu(InGa)Se_2 (CIGS) PV materials and structures. Clearly, many other measurements are done to ensure high efficiency, uniformity and yield.

Introduction

This article will focus on the measurement of thin polycrystalline CIGS films on glass substrates. Recently, the National Renewable Energy Laboratory (NREL) produced CIGS solar cells with ~20 percent conversion efficiency.[1] The low cost of thin film solar cells such as CIGS has resulted in considerable interest in commercialization of CIGS. The optical properties and thus the efficiency of the solar cells depend on the structure and elemental composition of the individual layers and the integration of the processes used to deposit the films in the "film stack."[2] A generic film stack for a CIGS solar cell is shown in Figure 1. A 0.3 to 1 µm molybdenum film is deposited directly on the glass substrate and acts as a back electrical contact. The 1 to 2.5 µm thick CIGS layer is deposited on the molybdenum contact. The CIGS is p type due to intrinsic defects and has a band gap of between ~1 eV to ~1.65 eV depending on the composition.[3,4] The CIGS is capped with a 0.005 to 0.01 µm CdS film. Although the top contact varies, it always has a larger band gap. In some cases it is intrinsic zinc oxide topped with aluminum (n type)-doped ZnO. NREL has shown a film stack with a 0.25 µm thick top contact made from a combination of zinc oxide and indium tin oxide.

Optical measurement of film thickness is a challenge. One is immediately struck by the amount of interfacial roughness.[2] Optical measurement of film thickness requires a robust optical model that includes film roughness. The presence of the molybdenum layer on top of the glass alleviates concerns about the transparent glass substrate. The composition of the CIGS impacts the absorption edge and the optical properties over a large wavelength range.[3,4] Ellipsometry is an excellent means of determining the absorption edge, spectroscopic refractive index (and thus the dielectric function) and the film thickness.

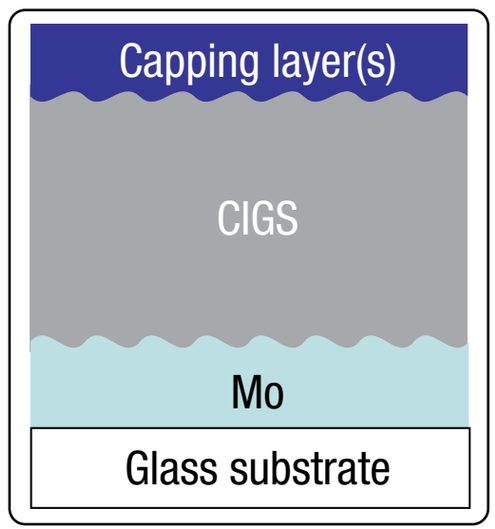

Figure 1 – The CIGS film stack used in solar cells. The molybdenum layer acts as the back contact, and the capping layer can be a combination of a cadmium sulfide (CdS) film topped by indium tin oxide (ITO) or aluminum-doped zinc oxide.

Photoluminescence (PL) is a very useful means of characterizing the recombination of the carrier excited by light absorption. Time-resolved PL (TR-PL) measures the carrier lifetime that has been correlated to CIGS efficiency.[5] NREL has measured a value of several hundred ns for its record ~ 20 percent efficient CIGS solar cell. These researchers point to the influence of many factors in determining the measured value of the lifetime and its relationship to efficiency. The measured lifetime value is influenced by charge separation in the depletion region and measurement conditions (intensity) as well as by the details of data reduction.[5]

Both of these methods are further discussed below. Many other methods are useful in the characterization and metrology of PV materials, including scanning transmission electron microscopy (STEM), capacitance-voltage (CV) profiling, scanning tunneling luminescence spectroscopy (STL) and cathodoluminescence (CL) spectrum imaging.[5] Careful materials characterization allows evaluation of theoretical models of PV behavior. For example, scanning transmission electron microscopy (STEM) has been used to characterize the copper content at the grain boundaries of $CuInSe_2$.[6] Theoretical calculations had predicted Cu vacancies at the (112) grain boundary, which would then be hole barriers. STEM data showed

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that not all (112) grain boundaries have Cu vacancies. Theoretical studies of the observed grain boundary structure show that these grain boundaries are not hole barriers. The point is that theory and experiment work together to further understand the nanoscopic structure and behavior of PV materials.

CIGS Ellipsometry

Ellipsometry is well suited to characterization of optical properties as well as measurement of film thickness across the glass substrate. In ellipsometry, one measures the change in the polarization of light after reflection from (or transmission through) a sample surface. The polarization of light in a specular reflection measurement such as ellipsometry is analyzed in terms of the polarization direction. Light polarized in the plane of incidence is p polarized, and light polarized perpendicular to the plane of incidence is s polarized. Ellipsometry relies on the fact that p and s polarized light reflects differently. In an ellipsometer, the light can be prepared along any angle between s and p polarizations and then the change in this angle measured after reflection. Spectroscopic ellipsometry measures this change in polarization over a large range of wavelengths. Commercially available spectroscopic ellipsometers are capable of mapping film thickness and optical properties across an entire glass panel.

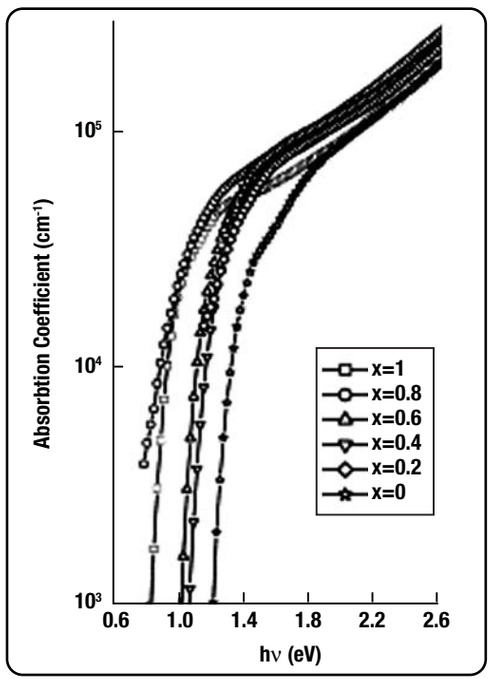

Figure 2 – The absorption coefficient change with the composition of CIGS films. The absorption coefficient of $CuIn_xGa_{1-x}Se_2$ (x = 1, 0.8, 0.6, 0.4, 0.2 and 0) was obtained from ellipsometry data. *(Figure 2 was first published in Ref. 4 and is used with permission.)*

Ellipsometric measurement of film thickness requires knowledge of the complex refractive index (dielectric function) of $Cu(InGa)Se_2$. The complex refractive index is a function of the copper, indium, gallium and selenium content. For example, the absorption coefficient for $CuIn_{0.8}Ga_{0.2}Se_2$ changes with small variations in the copper content is illustrated in Figure 2. Variable angle spectroscopic ellipsometry allows mapping of both thickness and optical properties. The complex refractive index of CIGS is shown in Figure 3, and a laboratory system is shown in Figure 4.

CIGS Photoluminescence

PL and TR-PL are useful means of characterizing carrier transport in CIGS.[7-9] Careful analysis of TR-PL provides a measure of carrier lifetime. As mentioned above, carrier lifetime has been correlated to solar cell efficiency. One recent study points to the differences in PL decay time and intensity between CIGS thin film stacks found in solar cells [ZnO/CdS/CIGS].[8] Both room-temperature and low-temperature (few K) PL have proven useful in characterizing CIGS and CIGS solar cells.[8] As with all measurements, great care must be used in the measurement and interpretation of the data. In order to further discuss this, we first describe PL and TR-PL.

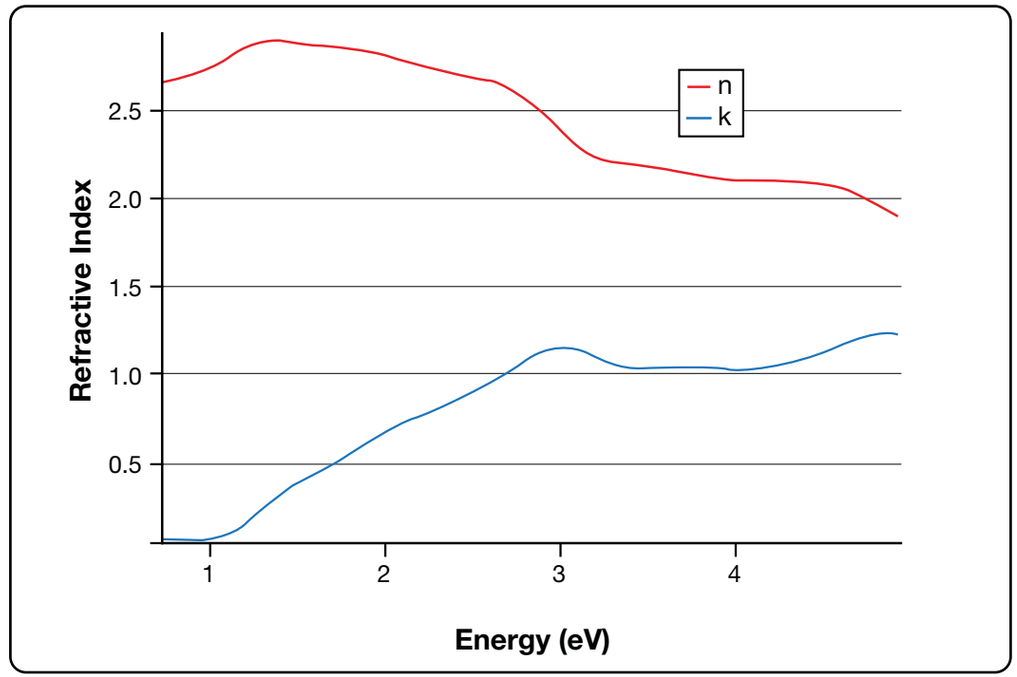

Figure 3 – The complex refractive index (n and k) of a polycrystalline thin film CIGS sample grown at NREL with a Ga/(In+Ga) atio of 0.2. *(Figure courtesy of Dean Levi of the National Renewable Energy Laboratory)*

In photoluminescence, a laser excites electron-hole pairs in the semiconductor sample. The wavelength of the laser must be such that the energy of the photons is more than the band gap of the semiconductor so that light absorption causes the promotion of an electron from the valence to the conduction band. CIGS has a compositional-dependent band gap between ~1 and 1.65 eV. Thus, laser wavelengths between 630nm (~2 eV) and 650nm (~1.9 eV), which are well above the band gap, have been used to obtain photoluminescent data.[7-9] Photoluminescence is the light emitted when the electrons and holes recombine. Time-resolved PL allows one to determine how long the electron-hole pair lasts. The fewer the recombination mechanisms, the longer the carrier lasts. One

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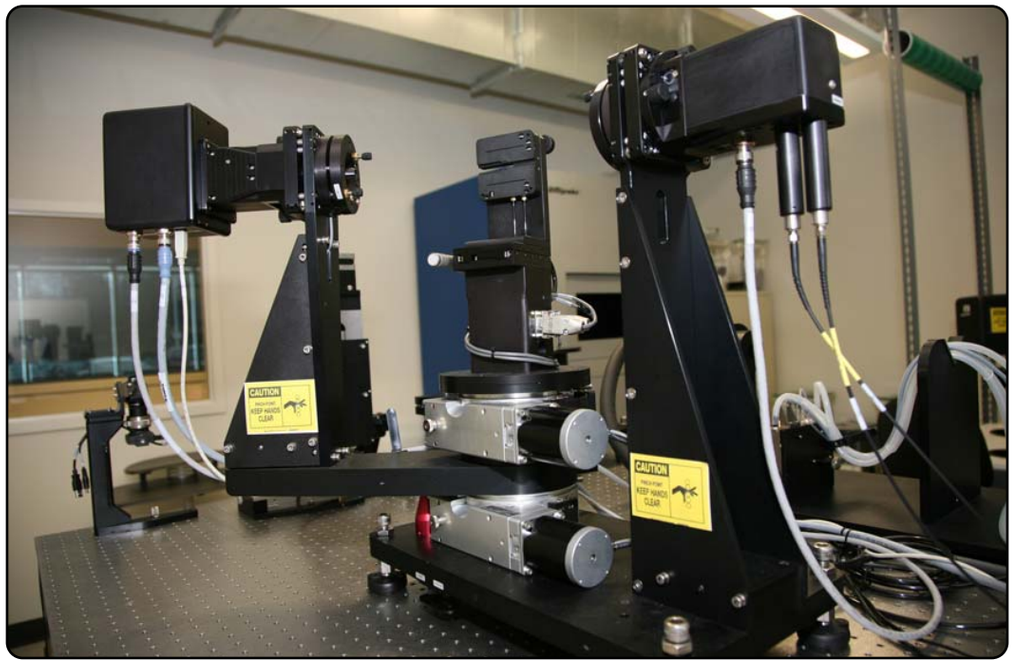

Figure 4 – A dual-rotating compensator ellipsometer in the author's laboratory at the College of Nanoscale Science and Engineering (the RC2™ is manufactured by the J.A. Woollam Company). The modular nature of this and similar ellipsometers makes it highly suited to automated measurement of thickness and optical property uniformity across films on glass substrate used for solar cells.

particularly important mechanism for recombination is defect-induced recombination. Thus, PL lifetime is a measure of the quality of the PL material or solar cell stack. Recently, a method known as Time-Correlated Single-Photon Counting has proven very useful for the measurement of photoluminescent decay curves. Recombination lifetimes of several hundred nanoseconds have been measured using the TCSPC method of measuring TR-PL. A schematic representation of a TR-PL is shown in Figure 5.

As mentioned above, great care must be used in PL and TR-PL measurements. For example, intensity of the laser has a strong impact on the PL signal. The intensity of the PL signal of CIGS films can be a function of the intensity of the exciting laser. The dependence can change after the surface of the CIGS is altered by chemical treatment.[9] One study reported that CIGS film PL is a linear function of laser intensity, while the solar cell stack shows a super linear dependence.[8]

New Opportunities

Collins et al. has shown the advantages of using ellipsometry for in-situ process control for CdTe PV materials deposition.[10] The grain size of CdTe and CdS films is a function of temperature, and the nucleation and growth behavior of CdTe and CdS can be monitored during depositions, and the grain size is a function of substrate temperature. Collins developed a database of the dielectric functions of these materials and was able to study interdiffusion at the CdS/CdTe and CdTe/CdS heterojunctions.[10] Collins has also applied this approach to CIGS.

Real-time process monitoring and development of a PL system capable of manufacturing process control are two distinct opportunities for metrology that deserve consideration.

Conclusions

Ellipsometry and photoluminescence are powerful methods for characterizing PV materials and controlling PV manufacturing processes. Ellipsometry systems for laboratory and glass substrate measurements are commercially available. Photoluminescence and time-resolved photoluminescence systems are laboratory systems assembled from a variety of the available lasers, spectrometers and detectors.

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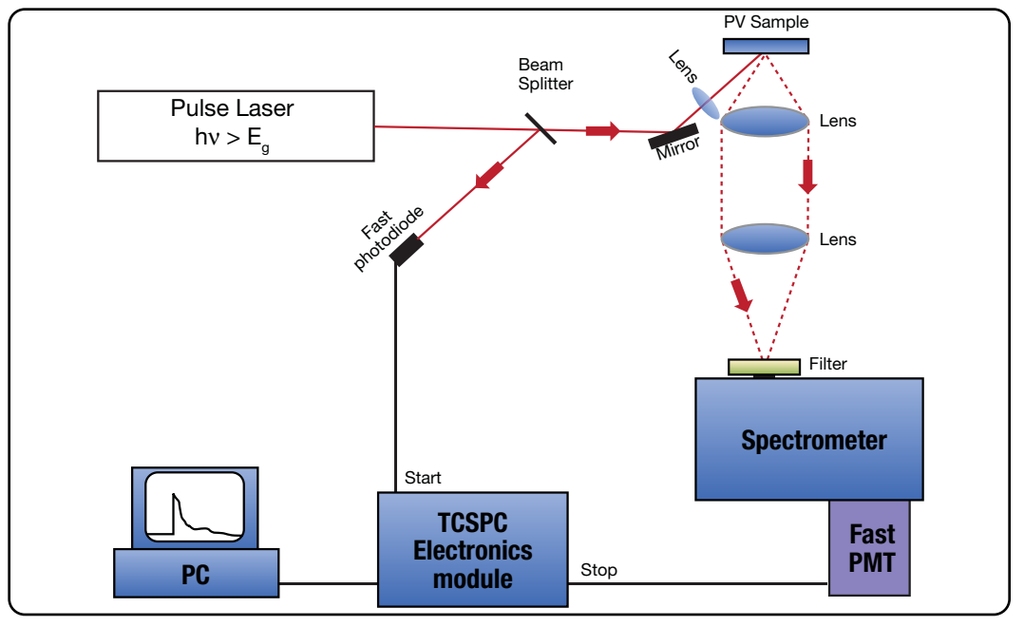

Figure 5 – A schematic representation of a time-resolved photoluminescence system. The time-dependent PL signal intensity is measured after each pulse from the chopped laser beam.
(Figure courtesy of Dean Levi, NREL)

<< PREVIOUS PAGE | NEXT PAGE >>

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See bio on page 6.

☞Click here to return to Table of Contents

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Understanding the Fundamentals of Minority Carrier Lifetime

Tanaya Mankad
Sinton Instruments

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Introduction

The theory of minority carrier lifetime is quite simple: As light hits a solar cell, the absorbed energy excites carriers. If all goes well, every one of these carriers are swept out to the emitter by the built-in field at the device junction, and the solar cell produces current. This is what we expect in perfect cells, but what does "all goes well" mean when we are making every possible compromise to bring down the price per watt of a solar cell? Pure silicon can boast lifetimes of several milliseconds, but between defects introduced during solidification, doping and the thermal abuse of various fabrication steps, those

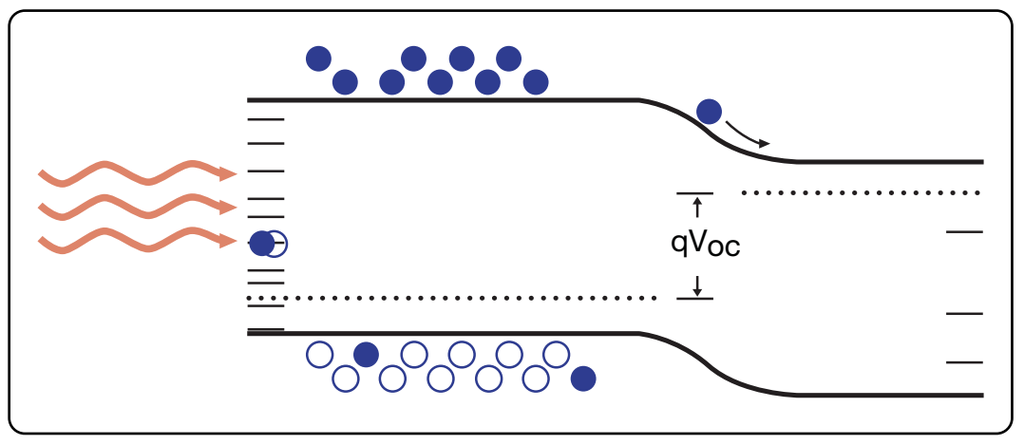

Figure 1 – A p-n junction shown in energy bands. Photogeneration excites electrons to the conduction band, from where they are collected as current. The open-circuit voltage increases as the logarithm of lifetime.

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lifetimes are often measured between 1-50 µs. A thorough understanding of the electronic properties of raw materials, as well as solar cells at various other stages of fabrication, can make the difference between the hairy edge of viability and huge bang-for-the-buck. In an industry where the variability in starting materials and processes is high, the measurement of minority carrier lifetime is a tool that can provide traceability and predictability; in short, the past and future of a sample.

Why Lifetime Is Useful

Generally speaking, minority carriers must have at least a long enough lifetime to diffuse from where they are created out to the device junction, and ultimately to the device terminals. For example, in a typical p-type multicrystalline 200 µm wafer with an electron diffusion coefficient of 27 cm/s, a lifetime of only 1.6 µs would enable a photogenerated electron to cross the entire wafer thickness before it likely recombined with a hole, and was lost forever to the current-collection process. Once we exceed the minimum carrier lifetime for current collection, we start to see a gain in device voltage, as excess photogenerated carriers hang out longer and in greater numbers, increasing the V_{OC} (Figure 1). This description of the elemental physical process should give minority carrier lifetime some cachet, so now we can assign responsibility for measuring (and optimizing) it.

What Happens to Lifetime

Silicon wafers are still the lifeblood for the majority of the photovoltaic industry, and within the scope of this article we will focus on silicon. Table 1 describes a typical silicon process flow.

Coaxing an accurate lifetime from bare wafers can be tricky. The above-mentioned 1.6 µs is about the best we can measure, if surface states gobble up minority carriers as soon as they reach them. Although one-to-one correlations of measured lifetime to actual bulk lifetime have been shown, the best place to get bulk properties is naturally in bulk material, provided that minority carriers can be generated and probed far from the surface. After slicing, and until wafer surfaces are passivated, the measurement of lifetime gets interesting. Some wafers will have incorrigibly poor lifetimes, and are destined for the waste bin. Some seemingly bad wafers, however, can be reformed, through processing steps that passivate various defects responsible for low-lifetime raw material. In this case, the distribution of "acceptable" samples from the bare-wafer stage will expand and skew toward longer lifetimes.

We have established that minority carrier lifetime is not a constant throughout the manufacturing process, but what is often more surprising is that it isn't even a constant for all injection levels: Just the act of adding minority carriers changes the behavior of those carriers. Lifetime is not just a number, but in fact a whole set of numbers, corresponding to different injection levels (Figure 2). Add to this the fact that the "state" of impurities (such as Fe:B or B:O), the photogeneration wavelengths and the detection method all affect the measured lifetime, and it is hardly a surprise that lifetime evolves between fabrication steps.

Luckily, many of these processes and effects are well-understood, and injection dependence turns out to be an asset to the attentive manufacturer. From a sim-

Process Step	Lifetime Indicates:
Brick or ingot	Crystalline quality and contamination level
Wafer	Wafer quality and saw damage
Phosphorus diffusion	Dopant diffusion and front-end process optimization
Nitride	Nitride deposition quality and prediction of solar cell efficiency

Table 1 – Typical Silicon Process Flow

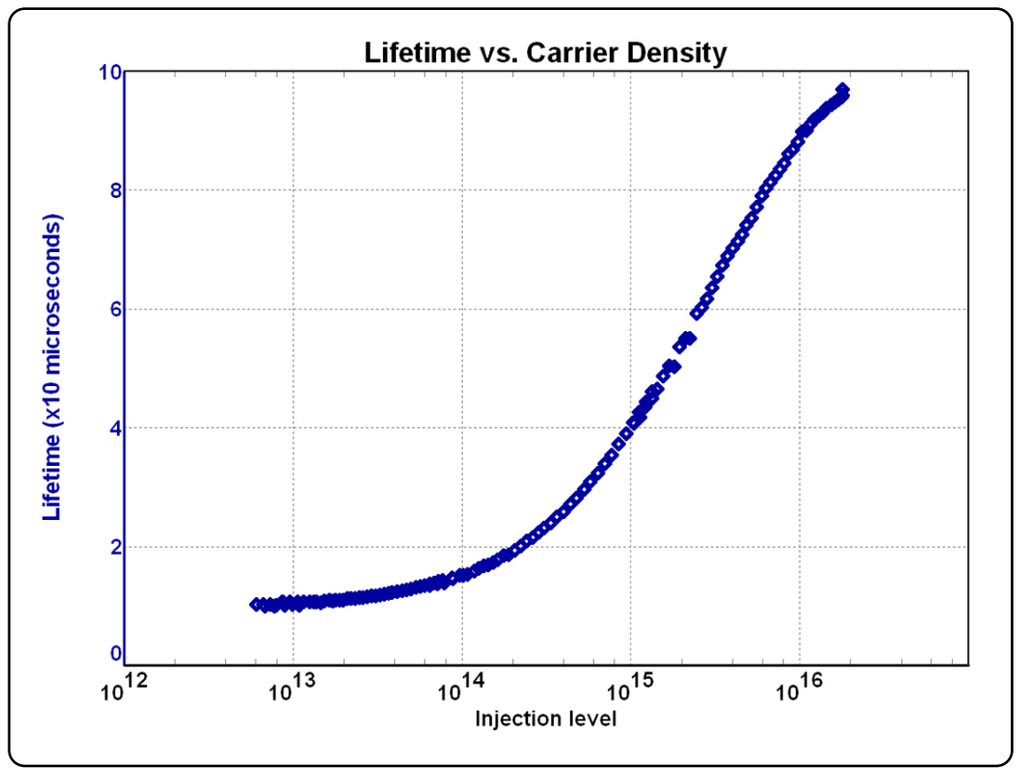

Figure 2 – One Example of a Highly Carrier-Density-Dependent Lifetime Sample

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ple lifetime vs. carrier density curve, we can glean information about many of the recombination sinks in a solar cell if we take a careful look at the underlying equations for lifetime analysis.

Applications of Lifetime Measurement

Although lifetime is often thought of as a single number, it is actually an effective value consisting of many components:

$$\frac{1}{\tau_{meas}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Other}} ,$$

in which the terms for bulk, Auger, and Shockley-Read-Hall are simply the minority carrier recombination due to the associated recombination sink. "Other" sinks such as junction recombination can be added to the sum as follows:

$$\frac{1}{\tau_{meas}(\Delta n)} - \frac{1}{\tau_{Auger}(\Delta n)} = \frac{1}{\tau_{bulk}(\Delta n)} + \frac{J0e,front + J0e,back}{qn_i^2 w(N_A + \Delta n)}$$

The Auger contribution to the recombination is a known function of carrier density, and can easily be subtracted from the effective lifetime at each known value of Δn. For samples with a junction, that leaves a relationship of the form $y = ax + b$, where the slope a is described by J_{0e} (also called the emitter saturation current density), the intercept b is bulk recombination and measured lifetime is a linear function of carrier density with those two fit parameters.

Rewriting the same equation for surface recombination, taking the surface recombination velocity to be

$$S_{eff} \approx \frac{J0e\,(N_A + \Delta n)}{qn_i^2} ,$$

we get the relation

$$\frac{1}{\tau_{meas}(\Delta n)} = \frac{1}{\tau_{bulk}(\Delta n)} + \frac{S_{front} + S_{back}}{w} .$$

As long as the surface recombination velocity is not too high, the two unknowns in this equation (bulk lifetime and Seff) can be solved using two or more samples of different widths. Already the use of lifetime measurement has given us more than one process control parameter, which can be stored, tracked and used for continuous improvement.

At very low injection levels, some lifetime measurement techniques can highlight a precipitous drop in what appears to be carrier recombination, making lifetime seem unbelievably high. This interesting phenomenon is an artifact and not an actual recombination sink, but if interpreted properly, can offer real physical (and nondestructive) insight into an otherwise immeasurable quantity: trap density. Solar-grade silicon often contains crystalline defects and impurities with energy levels near the band edge, which trap photogenerated carriers. These carriers effectively remain quarantined until the traps release them, which can occur with a much longer time constant than the recombination lifetime. Since the carriers never reach the conduction band, they never contribute to terminal current. Many of these trap centers are exactly the defects that are hydrogen-passivated during the cell fabrication process, but not all are. When the trap density is very high, it is likely due to defects in the crystal itself, and the passivation step will be wasted on such samples. Again, lifetime analysis forms the basis for predictive information.

We've shown that lifetime in semiconductors is more complex than, for example, the lifetime (half-life) of an isotope. Yet, it is completely tractable, and extremely powerful. But once we've decided that we want to measure it, whether for statistical process control or for research and analysis, there are more questions to answer. Foremost, which method to use? How do the intrinsic limitations and artifacts of the measurement methods affect the measurement itself, and how close to the real physical parameter can you get, or need to get? And at the end of the measurement, what does lifetime really mean, assuming that we've measured after a process step that adds its own complexities to the device as a whole?

These questions can make lifetime a bit of a black sheep in the family of process control parameters. While optical measurements of solar material nominally yield the same results between machines, electrical characterization can be trickier, and it is important to know and understand the assumptions made by any given technique. There are currently three essential approaches to probing minority carrier lifetime: conductivity measurement, measurement of a secondary optical process, and diffusion length measurement. The first two are used extensively for characterizing both silicon ingots and wafers at all process stages. The commercial manifestations of conductivity-measurement methods include RF-eddy-current, µPCD (microwave photoconductance decay) and MDP (microwave-detected photoconductance). All three methods rely on an optical excitation pulse to generate carriers, and a contactless conductivity-sensing mechanism to probe the decay of those carriers. The opto-electrical techniques include PL (photoluminescence) and ILM/CDI (infrared lifetime mapping or carrier density imaging); these measurements are suited to and have evolved with high-resolution detector arrays, and therefore almost always offer 2D images of lifetime without the need for a scanning sensor. PL relies on an excitation source to promote electrons to the conduction band, and detects the light from radiative recombination; ILM/CDI map the free-carrier absorption or emission of infrared radiation. Diffusion length measurements, such as SPV and EBIC/LBIC, also quantify the ability of a material to transport carriers to current-collecting terminals. If the diffusion coefficient is known, the lifetime can be calculated, but as these measurements are not in widespread use for direct lifetime measurement, we will not discuss them further.

Most of the commonly used techniques use one of two analysis methods, or sometimes a combination of both. The simplest regime is transient analysis, governed by the relation

$$\tau_{eff} = \frac{\Delta n(t)}{\frac{dn}{dt}} .$$

Calculation of transient lifetime requires only an abruptly terminating excitation pulse and the ability to quantify both the instantaneous carrier density and its decay constant. A density-dependent lifetime curve can obviously be extracted from this method by calculating lifetime at multiple Δn points on the dn/dt decay. The second method uses slowly

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varying excitation, and requires knowledge of the photogeneration rate G. The governing equation, from the general solution to the continuity equation, is

$$\tau_{eff}\ (\Delta n) = \frac{\Delta n(t)}{G(t) - {}^{d\Delta n}/_{dt}},$$

which also lends itself to a carrier-dependent analysis. If we do not vary the excitation source at all, we are in a steady-state condition. When we vary it with a time constant much slower than the expected lifetime, it is commonly known as "quasi-steady-state."

It may have seem that the above three equations are too simple to encompass the broad range of measurement techniques and lifetime dependencies described previously. This is partially true; it is the calibration of a raw measurement (for example in volts, or in light intensity) to an accurate value of Δn that gives each technique physical validity. Table 2 offers a comparison of techniques.

Conclusion

The choice-of-a-lifetime metrology system depends in the end on the needs of the user. Some considerations may be the application or process stage, in-line or off-line measurement, data storage availability and of course cost. High-resolution images are extremely valuable for development, but may not be necessary or feasible for in-line applications. There may be instances where a true bulk lifetime is more valuable at one fabrication stage than another, where a relative decay time may be used productively. Lifetime metrology can look inward, to the material, or outward, to the process. In either case, the insights are certainly worth your time.

	PL	CDI/ILM	RF (eddy current)	µPCD	MDP
Mode	QSS or Steady-state	QSS or Steady-state	QSS or Transient	Transient*	Transient**
Quantity measured	Radiative recombination	Free-carrier absorption/emission	Conductivity change caused by excited minority carriers	Reflected microwave intensity	Reflected microwave intensity
Resolution	• Single-shot high-res map • Pixels may be at different injection levels	• Single-shot high-res map • Pixels may be at different injection levels	Scanning capability, low-res	Scanning capability, medium-res	Scanned array of sensors
Calibration	As radiative recombination intensity is a function of the product of doping and carrier density, a conductance sensor is often used to calibrate the result	The free-carrier absorption by minority carriers is calibrated against wafers of known dopant density	A mobility model is used to convert conductance to carrier density, and generation models to calculate generation where needed	*The transient analysis is not often presented in terms of carrier density. Instead, a direct decay time of microwave reflection is calculated, which correlates with minority carrier lifetime under low-injection conditions	**Similar to µPCD, except the transient pump pulse is longer, allowing more physical measurements at high injection
Trap correction	Lifetime data available even below the intrinsic carrier density; PL is not subject to trapping artifacts	Trap density may be calculated from the artifact	Trap density may be calculated from the artifact	No trap correction available	Trap density may be calculated

Table 2 – Comparison of Techniques

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Tanaya Mankad *has been the senior engineer at Sinton Instruments, Inc. since 2001, where her responsibilities include industrial algorithm development for lifetime analysis. She has previously worked in next-gen photolithography and IC process-control metrology. Tanaya earned her MS in electrical engineering from the University of California, Santa Barbara, and her undergraduate degree in EE and physics from Princeton University.*

☞Click here to return to Table of Contents

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<< PREVIOUS PAGE | NEXT PAGE >>

Click here to return to Table of Contents

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The compilation of PV modules and inverters to an optimal performing system is a challenging engineering task. Looking at the module market, everywhere you'll find the "standard panel." They have different specifications in mechanical sizing, requirements for fixing (frames, clamps for glass-glass modules) and electrical properties (open circuit voltage, short-cut current, MPP voltage and current ranges depending on the applied cell technology). The specific values cover a wide variation area. And inverters also have broad input parameters for input voltage and MPP voltage.

The system design to bring the various parameters together in order to reach a high-performance ratio is a science of its own. The number of modules in parallel and series, the number of independent strings with separated MPP tracker, the ratio of PV generator power vs. inverter peak power are the screws that can be turned. When in surplus, one must consider different operation strategies (e.g., feed-in tariffs in several countries in Europe, tax credits in the U.S., etc.), and the design even becomes region-dependent.

The market in the U.S. differs from, e.g., the one in Europe. Different traditions in roofing (clay/concrete tiles vs. shingles) and other subsidy structures (feed-in tariff vs. tax credits) require different strategies in the system design as well. The following article describes the situation for installation in the U.S.

Pairing Inverters and Panels by Application: Part 1

Pallab Chatterjee
Silicon Map

The U.S. marketplace for solar configurations has resulted in different pairing and selection criteria for inverters and panels based on their use in commercial or residential applications. These selections hold true even when connected to the same grid. This discrepancy has to do with regional, state and local regulation, inspections and anticipated use models, the basis of which are not well defined in facts, but in profit margin.

The recent popularity in the growth of "retail" solar installation companies has brought about some interesting pairings of product offerings on the market. There are currently two main bins of installers – small local companies of typically 10 people or fewer, and larger regional-based companies with over 40 people with multiple local divisions. The smaller firms address both residential and commercial projects with the same design-and-install teams. The larger firms have separate groups for residential and commercial projects, and they typically include architectural support for the commercial projects. These larger firms tend to have different teams handle installation on the two project types.

A key component to the solar installation process is the financing options available for the end user (customer) to be able to purchase the systems. The current state of the industry has this financial aspect heavily tied to the technology selection for projects. The larger firms tend to have the financial basis to support either their own financing vehicles to customers or work with major financial institutions to arrange financing for customers. As a result, the technology selection (inverters, panels, switches, etc.) is not directly tied to the financial structure of the project. Most smaller firms have some sort of "factory financing" option available where the panel and inverter manufacturers/distributors provide access to customer end financing for projects.

This relationship between financing sources and the technology selection has led to an interesting trend in installations. The designs and material selection are often based on the minimization of cost by the supplier and the terms of the financing rather than best technical fit. As there are a variety of specifications for like panels (e.g., 190W residential panels range from 12.5 to 17 percent efficiency, and have 5- to 25-year warranties, and varying ambient operating temperature ranges) that are often not taken into account in selection on a project. Rather,

<< PREVIOUS PAGE | NEXT PAGE >>

based on the installation configuration software from the inverter manufacturers (such as Sunny Design by SMA Solar Technology, or the Fronius Configuration Tool), the gross panel wattage and layout are selected. The actual panel selection is then based on the financial opportunity for the financing of the project, and secondarily the technical review of the wattage and net power delivered to the system and life cycle.

Right now, the average life cycle of a solar company (large or small) is under five years; as a result, the extent of the warranty period is a moot point, as the likelihood of the installer being around when the parts start to show wear is minimal. (Note: There are several solar installers that achieve sufficient size to be either self-sustaining or a publicly traded entity, which will most likely be here in 20-plus years).

There are two classes of panels – those targeted toward commercial customers and those targeted toward residential. The main differences are in size (commercial panels tend to be slightly physically larger) and in the look/profile of the panels. The residential panels tend to be "darker"-colored trim in lower-profile panes and mounts to minimize projection from the roof. The panel efficiency does not come into play to differentiate the two applications due to the inverter selection process. As an example, a typical residential inverter would be spec'd at 3000W max output. Although it states that it has over 95.5 percent efficiency, it recommends a max PV source power of 3750W. This means the actual efficiency is at 80 percent, and that the additional efficiency of the panels (the 5 percent swing from 12-17 percent) does not produce any net results to the system, other than an "overvoltage stress" to the capacitors and bridge in the inverter. For this reason, lower-efficiency panels are generally chosen, to reduce stress on the inverter and increase profitability for the project.

The inverter selection drives much of the pairing decisions. There are two main types of systems used for point of use applications – grid-tied and grid-interactive. Figure 1 shows a typical grid-tied system. These systems provide power back into the power panel, and any excess power gets sent to the grid and utilizes the "net metering" application on the modern power meters. The excess power is what causes the meter to "spin backward," resulting in energy credits against use. Figure 2 shows a typical grid-interactive system. These systems also have a battery backup loop that provides power to the panel when the power grid is not operational.

There are fewer suppliers of grid-interactive inverters than there are grid-tied inverters, which results in less pricing variation on those products. The grid-interactive inverters are a more expensive product, and as the solution requires the additional cost of the batteries, this type of system becomes a more expensive solution/installation. The result of the selection of the higher-end installation typically results in the selection of higher-efficiency panels with a longer-duration warranty. In this marketplace, it is typical to see Outback Grid Interactive inverters and Sharp high-wattage panels designed for Off-Grid applications.

The grid-tied systems are where the tight coupling comes into play for panels and inverters. Some of the suppliers (e.g., SunPower) have both panels and inverters in their product line. Their installation network is through an exclusive network of dealers and installers that are essentially bound to a single-vendor solution for both commercial and residential applications. Provided you are in a community where the inverters from that supplier meet the permit requirements and are approved for installation by the local inspectors, then the single-vendor solution is viable. The single-vendor solu-

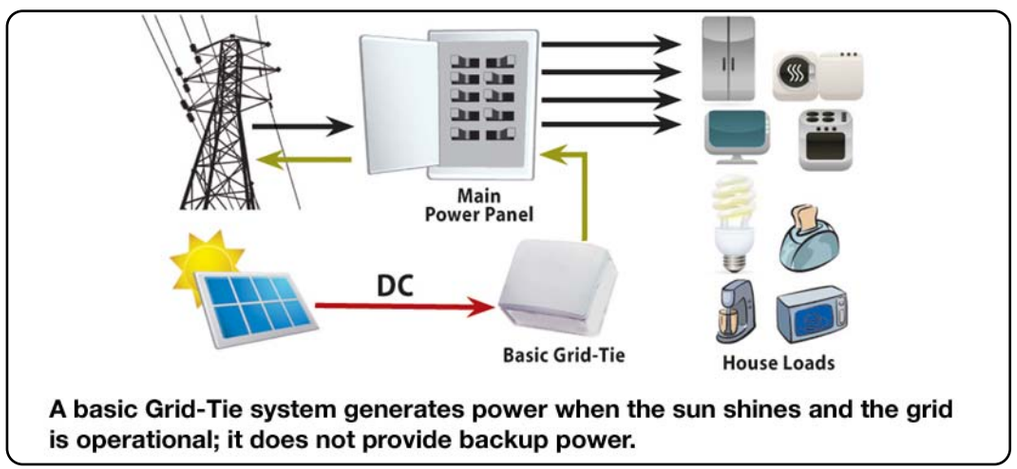

Figure 1 – Typical Grid-Tied System *Courtesy of Outback Power Systems*

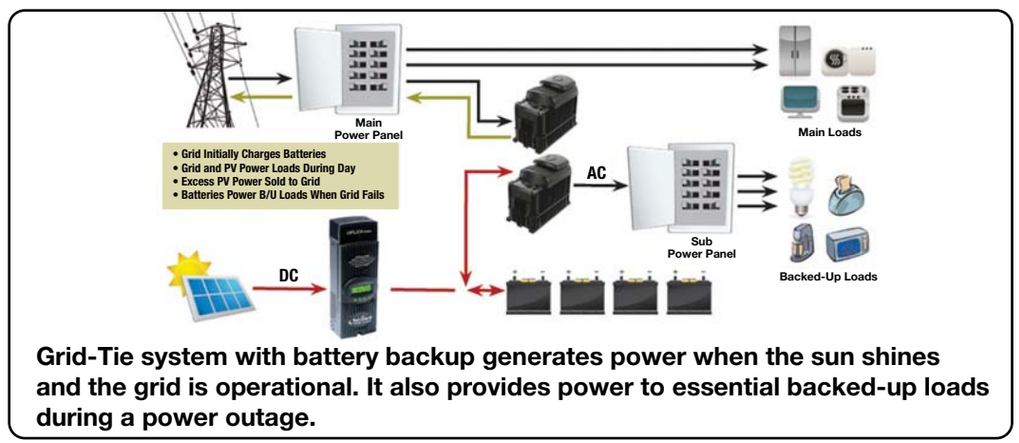

Figure 2 – Typical Grid-Interactive System *Courtesy of Outback Power Systems*

<< PREVIOUS PAGE | NEXT PAGE >>

tions are also tied to financial arrangements that target maximized panel use (and thus profit margin) for the inverter configurations (e.g., 3800W of panels for a 3300W inverter).

More than likely, local inspection regulations do not support all of the inverter manufacturers in business today for a given locality. As a result, the installers are focusing on two or three major brands such as Fronius, SMA and Outback. These inverter providers have a range of products for both residential (lower-power) and commercial (higher-power) systems. The chief difference is the loading configuration of the systems with panels. In commercial environments, it is typical to see a 5500W output inverter with 5520W-5640W of panels connected. A similar residential application might show 5750W on the same device. The "overvoltage stress" on the inverter in the residential application will tend to show degradation in performance sooner than the commercial application. These independent inverters work well with most third-party panels, and the pairing has to do with the profitability obtainable through the distribution chain. Most of the installers using SMA small-configuration "Sunny Boy"-type inverters have leaned toward the lower-efficiency, more readily available and lower-cost panels to increase margin and the installation costs. The applications using the larger configurations of the SMA products, as well as the Fronius and Outback products, tend toward the 25-year product life panels in the 14 percent-plus efficiency area. This has a higher material cost, but a lower installation cost, and typically results in a long-term high business opportunity based on the size of the units installed and total net profitability from being able to leverage the pricing from multiple distributors and suppliers.

The pairing of the inverters and panels has to be tested and qualified for the installers to ensure that the full assembly chain (panels, mounts, wiring, shut-off switches, inverters and power panel connection) all works together. In this mode, there is a preferred list of parts and suppliers on an approved vendor list (AVL) that can be created for different applications (residential, commercial, grid-tied, grid interactive, etc.). Installation time frame and product availability is not as much of an issue for the mixed vendor solution as it is for the single-vendor solution. There tends to be a much stronger case for pricing stability in an installation project with the use of third-party inverters that have been tested with third-party panels vs. single-supplier solutions. ■

About the Author

Pallab Chatterjee *has been an independent circuit and systems designer since 1985. He has specialized in high-reliability, consumer- and sensor-based systems with over 400 projects completed to date. Pallab is a senior member of the IEEE and vice chair of the IEEE SFBA Nanotechnology Council. He also writes for several trade publications and serves on several conference organizing committees including the International Solar Energy Technology Conference (ISETC.org).*

☞Click here to return to Table of Contents

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<< PREVIOUS PAGE

ADVERTISERS INDEX

Click here to return to Table of Contents