MOC6 FPGA Board User Guide

Contents

1 Introduction

The MOC6 FPGA board are designed specifically for use with MSS PMOD modules and can host up to three dual-PMOD connector modules simultaneously. It is built on a six-layer PCB featuring two internal ground planes and two dedicated 3.3V power planes. This gives it the lowest achievable supply noise and best isolation between the analog and digital domains. Overall the board emphasizes ease of use and robust functionality.

Power can be supplied either through a USB-B connector and/or an external 5–15V source. No jumpers are required for power selection, and both inputs may remain connected without conflict. The power path is fully reverse-protected, eliminating concerns about accidental miswiring. The onboard 3.3V linear regulator provides an additional 800mA specifically to ensure all six PMOD ports can be powered simultaneously.

At its core is a Spartan-7 FPGA with 80 DSP slices, making it well-suited for interfacing with MSS modules. The devices also provide ample configurable logic to implement a 32-bit MicroBlaze soft processor.

For development, the board includes a USB-to-JTAG bridge for seamless integration with Vivado, as well as a high-speed USB-UART interface capable of up to 6Mbps for efficient data transfer to and from a PC, including Python-based processing or generation workflows. An external JTAG header is also available for advanced users.

Additional features include four jumper switches that double as configurable I2C and SPI inputs, and a four-LED debug bank for monitoring clocks and data buses. All I/O ports meet the PMOD electrical and mechanical standards. There is no need to worry about improper configuration damaging any hardware.

2 Features

Xilinx XC7S25 Spartan-7 FPGA

- 23,360 logic cells four 6-input LUTs and 8 flip-flops
- 1,620 Kbits of fast block RAM
- 80 DSP slices
- Internal clock speeds exceeding 450MHz
- Programmable over JTAG and Quad-SPI Flash

Memory

- 16MB Quad-SPI Flash
- Automatic Boot from flash with JTAG override anytime

Power

- Powered from USB or any 5V-15V external power source
- Three TI switching regulators for the digital rails using DCS technology
- Ultra-low noise (0.6uV RMS) MSS LDO for the PMOD 3.3V supply

USB

- USB-JTAG Programming circuitry
- USB-UART Bridge 6mbps

Switches, Push-buttons, and LEDs

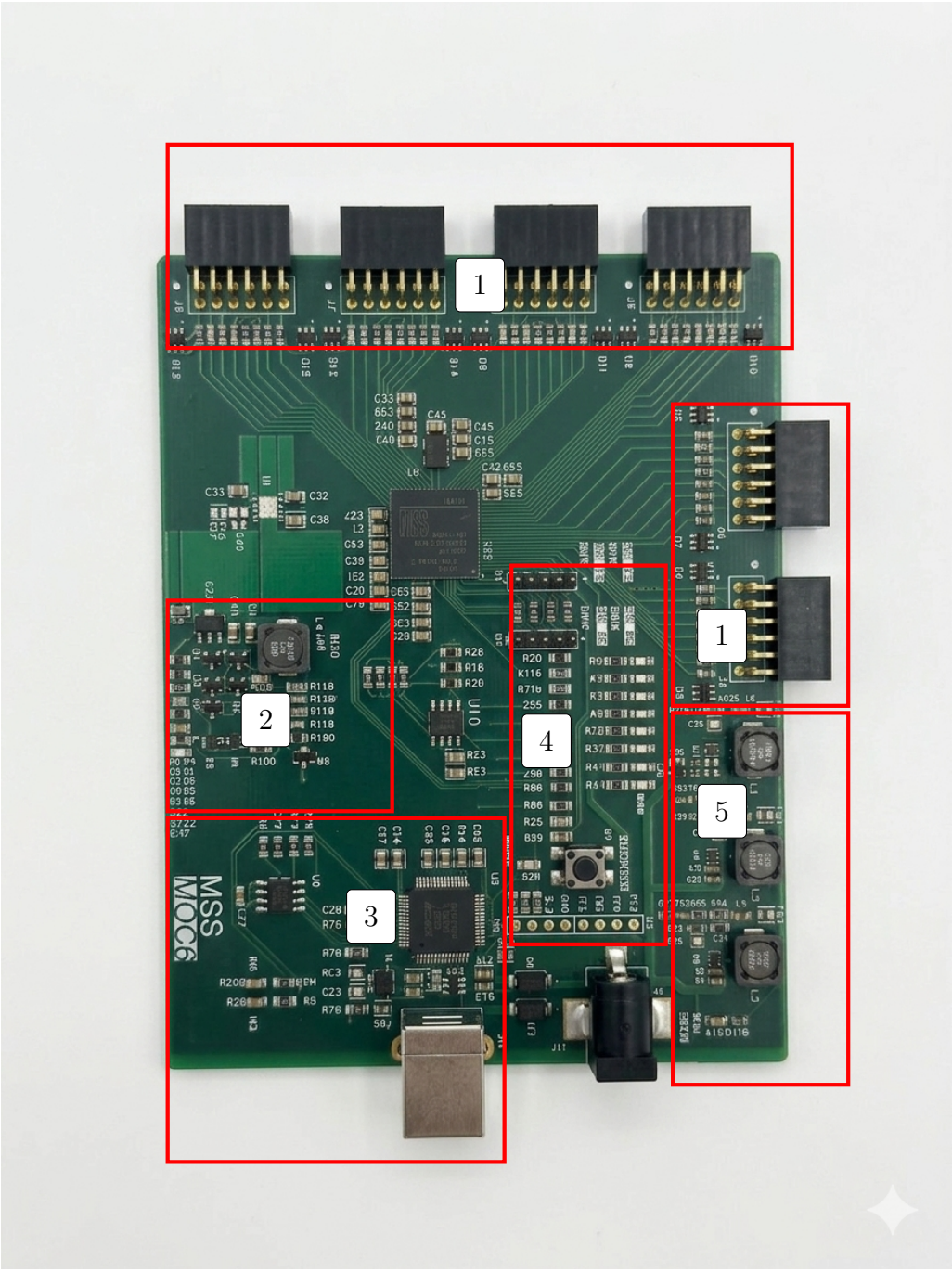
- 4 jumper switches double as SPI or I2C inputs with pullups
- 1 Reset Button
- 8 user programmable LEDs
- 2 TX RX UART LED
- 1 DONE LED

Expansion Connectors

- 6 (12) lead PMOD ports overcurrent protected
- 54 total FPGA I/O inlucding UART TX and RX

3 MOC6 Board

Below is the topside and botomside view of the MOC6 FPGA board. All ports, jumpers, and LEDs are labeled with the pin indentifier on the actual FPGA. This makes the names exactly the same as the identifiers that appear in the Vivado XDC constraints file. There is no need to cross reference a separate document to connect devices to the board.



Reference	Callout		Notes
1	PMOD ports		
2	3.3V MSS LDO	0.6uV/rt Hz	1Hz,1MHz -100dB PSRR
3	USB-JTAG USB-UART		
4	SPI/Switch/LED/Program/JTAG I/O		
5	Digital Power		

4 Software Support

MOC6 is fully compatible with Vivado ® Design Suite versions 2020.0 and newer. Once connected to the computer with a USB-B cable open the hardware manager within vivado and use the auto connect feature. To program the device select the XC7S25 model and the proper *.bit file in the project sub-directories. To program the QSPI a *.bin file will need to be generated during the implementation phase. To configure this go to hardware manager and select add configuration memory device. Scroll through the list and select the device below. MX25L3233FM2I-08Q Once that is done program the device and press the PROGRAM button on the MOC6 board.

The QSPI is non volatile and will be the default program on power up or when the PROGRAM button is pressed. It is sometimes useful to compare two different designs by first programming the QSPI with one design and then programming the FPGA with a *.bit file. Once the *.bit file is loaded the device will run and immediately upon pressing the PROGRAM button the *.bin file will run instead.

5 Power

The figure below outlines the power scheme used in the MOC6 FPGA board. The main difference between this scheme and schemes used in other FPGA boards is the ultra-low noise LDO that powers the PMOD ports is specifically designed to work with and achieve the best performance out of MSS modules. The LDO achieves on overall output noise of 0.6uV RMS from 10Hz to 100kHz. There is no ripple normally present in other digital power supplies. Other than that it's use is seamless to the user and it has plug and play interoperability with any PMOD module.

Additionally the overall power scheme of the MOC6 is versitile and robust. Both USB and power can be plugged in at the same time without any need to select jumpers. Also should you need to use external power such as a battery or other supply the DC input is protected against reverse biasing up to 20V. If for some reason the PMOD power is shorted the linear regulator will go into current limit and the power to the FPGA will be unchanged. No damage will occur.

Precautions should be taken when debugging new designs connected to the MOC6, especially when excessive power consumption or a potential supply short is possible. Although the MOC6 supports an external supply up to 15V, it is recommended to use either a regulated 5V external supply or USB power during initial bring-up. A short on the PMOD power rail at higher voltages can place unnecessary stress on the onboard LDO and may lead to damage or unstable behavior.

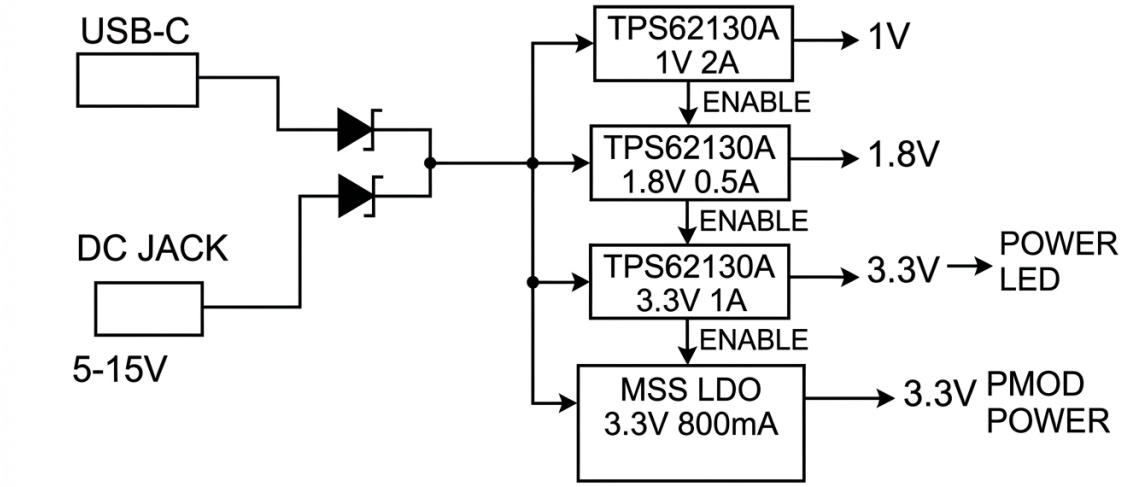


Figure 1: MOC6 Power Structure

6 Oscillator

The MOC6 board uses a SIT8008AC-33-33E-100.000000 100MHz oscillator connected to pin M9 of the Spartan-7 FPGA. With only 1.8ps RMS cycle-to-cycle jitter—about six times better than typical crystal-based sources—it provides a noticeably cleaner clock for ADC and DAC applications, improving achievable SFDR and SNR. This low-jitter input can feed the FPGA's MMCMs or PLLs to generate a wide range of internal clock frequencies and phase relationships. For full details on clocking rules and capabilities, see AMD's 7 Series FPGAs Clocking Resources User Guide.

Within the device, the Clock Wizard IP is the simplest way to configure these resources. You specify the clocks you need, and the Wizard handles VCO limits, divider choices, jitter optimization, and buffer insertion, selecting either an MMCM or PLL automatically. It's the most reliable way to build clock networks without manually instantiating primitives.

The MMCM is the more flexible of the two clocking blocks, supporting wide-range synthesis, fractional divides, fine phase shifting, duty-cycle correction, and jitter filtering—ideal when you need multiple unrelated clocks or tight timing for ADC/DAC interfaces. The PLL is simpler and lower-power, suited for straightforward frequency multiplication or division when advanced phase control isn't required.

Spartan-7 devices group these resources into Clock Management Tiles, each containing one MMCM and one PLL, enabling multiple independent clock domains. In practice, designers use MMCMs for precision and versatility, PLLs for efficient basic synthesis, and the Clock Wizard to make the whole process painless.

7 USB UART Bridge

The MOC6 uses an FTDI FT2232HL USB-UART bridge to let a PC communicate with the FPGA through a standard Windows COM port. FTDI's free VCP drivers convert USB traffic into UART data, which is exchanged with the FPGA over a simple two-wire TXD/RXD interface connected to pins K15 and L12. Once the drivers are installed, any PC application that can access a COM port can send and receive serial data through this link.

Two onboard LEDs provide immediate activity feedback: LDTX indicates data transmitted from the PC, and LDRX indicates data received. Signal directions follow the DTE convention, with the PC treated as the data terminal.

The FT2232HL also implements the USB-JTAG interface, but the JTAG and UART channels operate completely independently. Using the UART interface does not interfere with programming the FPGA, and vice-versa. Integrating both functions into a single device allows the board to be powered, programmed, and communicated with over one USB connection.

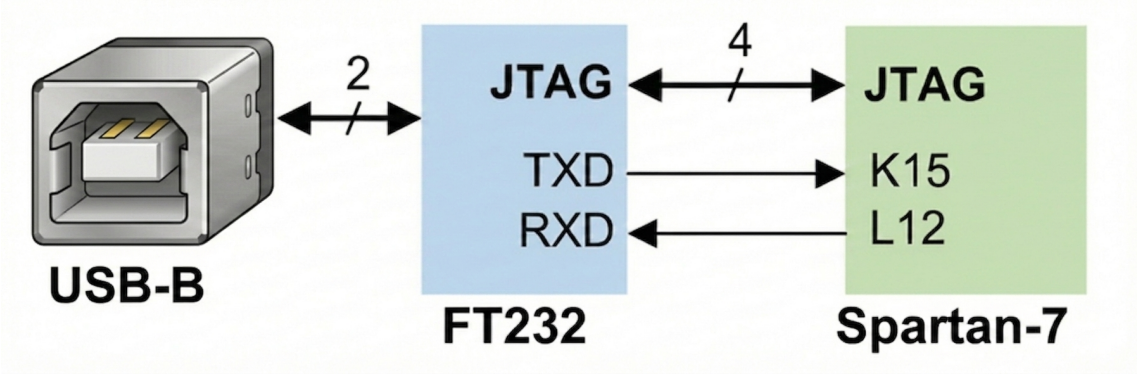


Figure 2: MOC6 JTAG and UART to USB-C structure

8 PMOD Ports

The MOC6 board has six PMOD ports enabling it to use several MSS modules simultaneously. They conform with the PMOD standard pinout and configuration. Each port includes two ground connections and two connections to the low noise 3.3V PMOD supply discussed previoulsy. Each pin is protected with a series 200 ohm resistor. This makes them robust and an excelent choice for new designs where a wrong configuration would normally break a standard FPGA.

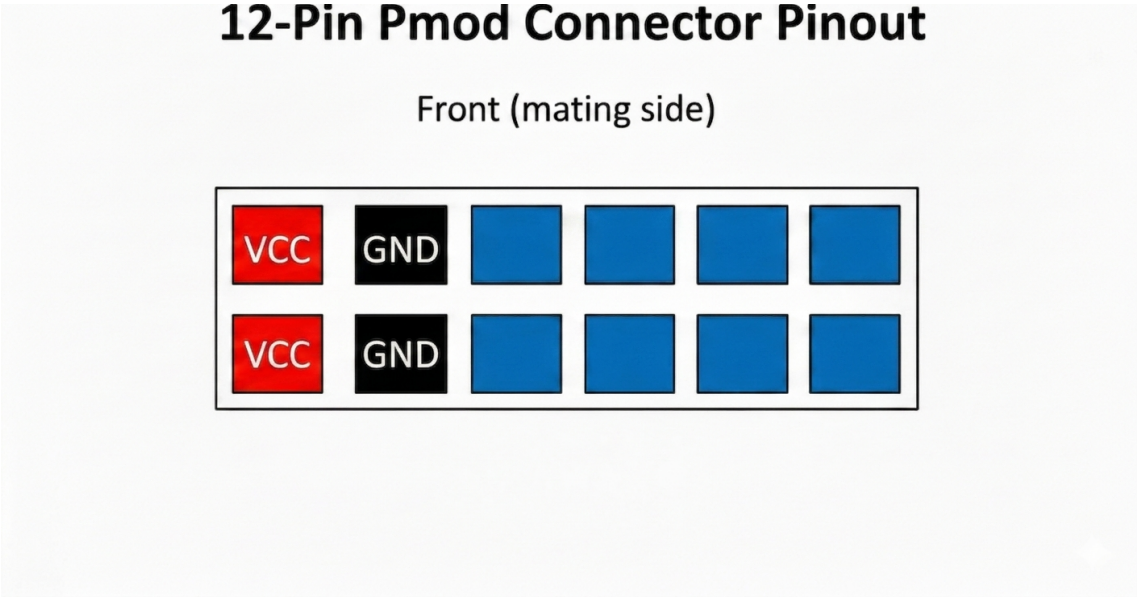


Figure 3: MOC6 PMOD port