PLLXplore 1 Module User Guide

Contents

1 Introduction

The PLLXplore 1 board brings an entire world of PLL experimentation into a single, convenient PMOD module. Built around fully digital PLL concepts, it allows you to implement everything from a basic integer-N PLL to advanced fractional-N architectures with Delta-Sigma frequency synthesis. Start with our introductory HDL example to build a synchronous phase-frequency detector, then expand and customize it however you like—even all the way to an asynchronous time-to-digital-converter-based fractional-N PLL. You're free to design your own control structures, explore new architectures, and push the boundaries of what a digital PLL can do. PLLXplore 1 is great for absolute beginners all the way to experimenting professionals. With PLLXplore 1, your only limit is your imagination.

2 Features

- 1 to 50MHz VCO 1-10 or 4-50 MHz pin selectable
- 1MHz output 4th order Delta Sigma DAC
- 70pS RMS Jitter @ 50MHz
- 3.3V Single Supply from PMOD
- 20KHz ADC loop filter
- Exploratory Bandgap Circuit W/ test signal generator

3 Applications

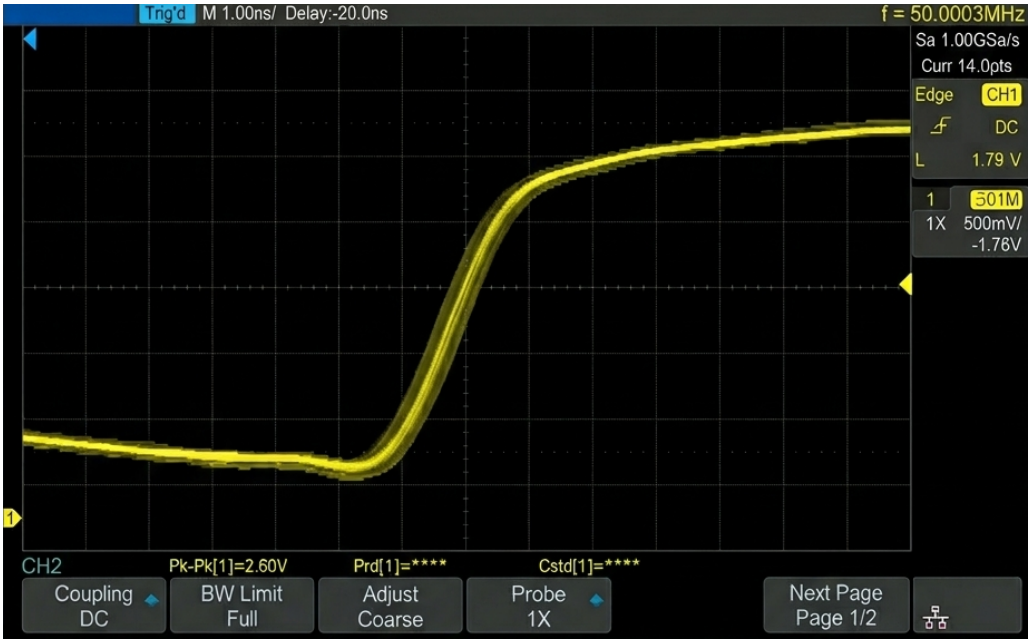
- All digital PLL
- Fractional N PLL/Delta Sigma/MASH
- Up to 1MHz Delta Sigma Signal Generator
- LF MF and HF band HAM frequency synthesizer
- Dither techniques
- PLL control loop development

4 Specifications

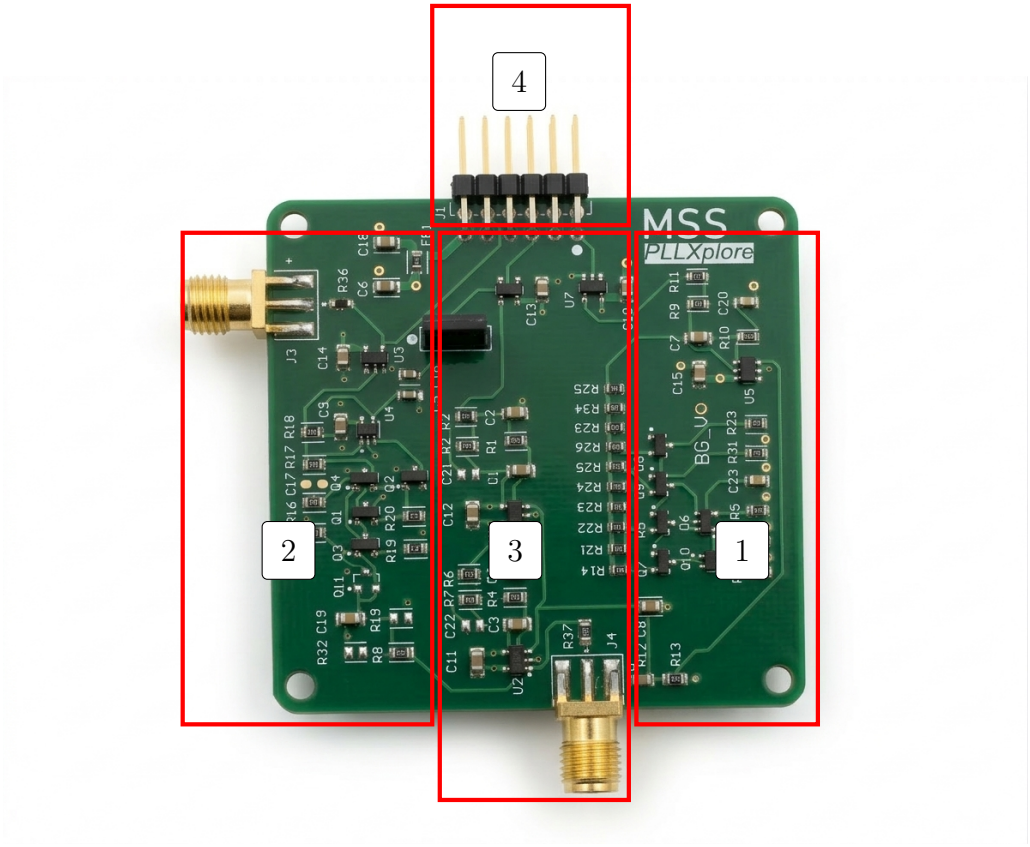
Parameter	Value	Unit
Supply Voltage	3.3	V
Supply Current	25	mA
VCO output	1-50	MHz
DAC SFDR -6dB FS	-55	dB @1MHz
DAC Output Noise	75	uV RMS
DAC/VCO output	3.25	Vpp

5 Performance

Below is the measured performance of the PLLXplore at 50MHz. The scope plot shows 70pS RMS of period jitter.



6 Board



Reference	Callout	Notes
1	Bandgap and test DAC	1.65V
2	VCO and loop filter	1-50MHz
3	DAC filter and driver	1.2MHz BW 3.25Vpp
4	Digital I/O	

7 Software Support

The PLLXplore 1 includes three compressed Vivado project that's already configured for the MOC FPGA boards, and they can be adapted to any PMOD-style FPGA board with only minor edits to the .xdc file.

The first vivado project file is for implementing the PLL function and is called PLLXplore$_PLL.The$

The second vivado project is for the Delta Sigma ADC output. I can be used to generate signals up to 1MHz output with moderate fidelity.

The third vivado project file is for testing the discrete bandgap block that is on the PLLXplore board.

8 Connecting the PMOD module

Connecting the PLLXplore 1 is straightforward because the pins follow the PMOD standard: 0.9-inch spacing with a dual-row 12-pin, 0.1-inch header.

The module must only be inserted into a PMOD port in the correct orientation. A single-pin offset or an upside-down insertion can damage the module, since misalignment can place PMOD supply pins directly onto unprotected I/O pins. The MOC FPGA boards themselves are not at risk, but the modules can be permanently damaged if connected incorrectly. Always power down all boards when connecting or disconnecting modules.

Once aligned properly, the module can be used without concern for I/O configuration. The MOC FPGA boards follow the 200-ohm PMOD output-impedance guideline, which prevents damage from pins that might otherwise be driven incorrectly during development or testing.

The DAC output and the PLL output have separate female SMA outputs to connect to external circuitry. The DAC output has a 50 ohm output impedance. Any current more than 70mA above and below the supply rails will damage the part. The PLL output has a 50 ohm output impedance. reverse driving the output port beyond 70mA is not recommended. Please double check all connections before powering up.