



SigmaXplore 6FD Module User Guide

Contents

1	Introduction	2
2	Features	2
3	Specifications	2
4	Performance	3
5	Board	4
6	Software Support	4
7	Connecting the PMOD module	4
8	Pinout	5

1 Introduction

SigmaXplore 6FD is a fully differential, 6th-order Delta-Sigma CIFB ADC designed to showcase the more advanced concepts in Delta-Sigma conversion. This kit features a completely discrete implementation of a high-order architecture, allowing you to explore the true benefits of multistage Delta-Sigma design in a hands-on, intuitive way. With an oscilloscope, you can examine the system node-by-node and observe the dynamics, stability, and behavior of every internal stage—something rarely accessible in high-performance ADCs. The input accepts a single-ended 0–3.3 V signal and interfaces directly with a standard PMOD FPGA connector for custom digital signal-processing workflows. You can begin with our provided HDL files and expand or refine them as your skills grow. Whether your interests lie in high-performance audio conversion, instrumentation-grade measurement systems, or advanced mixed-signal architectures, SigmaXplore 6FD offers a powerful platform for deep learning and experimentation.

2 Features

ADC

- 6th order CIFB Delta Sigma Converter
- Single bit or four-bit DAC feedback
- Feedforward cancelation
- 3MHz to 10MHz sampling rate
- plugs directly into dual FPGA PMOD connectors
- 92dB SNR, -95dB SFDR
- 3.3V Single Supply from PMOD
- Single ended input
- Fully discrete design

APPLICATIONS

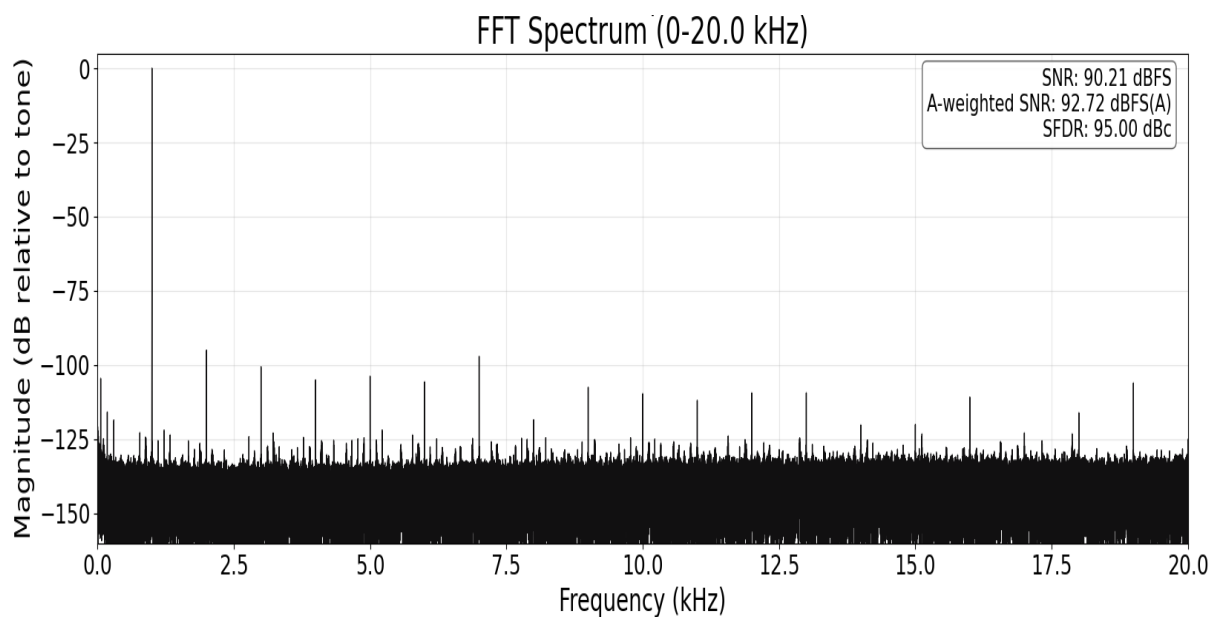
- Delta Sigma practical learning for personal, professional, or an educational lab
- LAB grade signal measurment
- Complete analog input signal chain.

3 Specifications

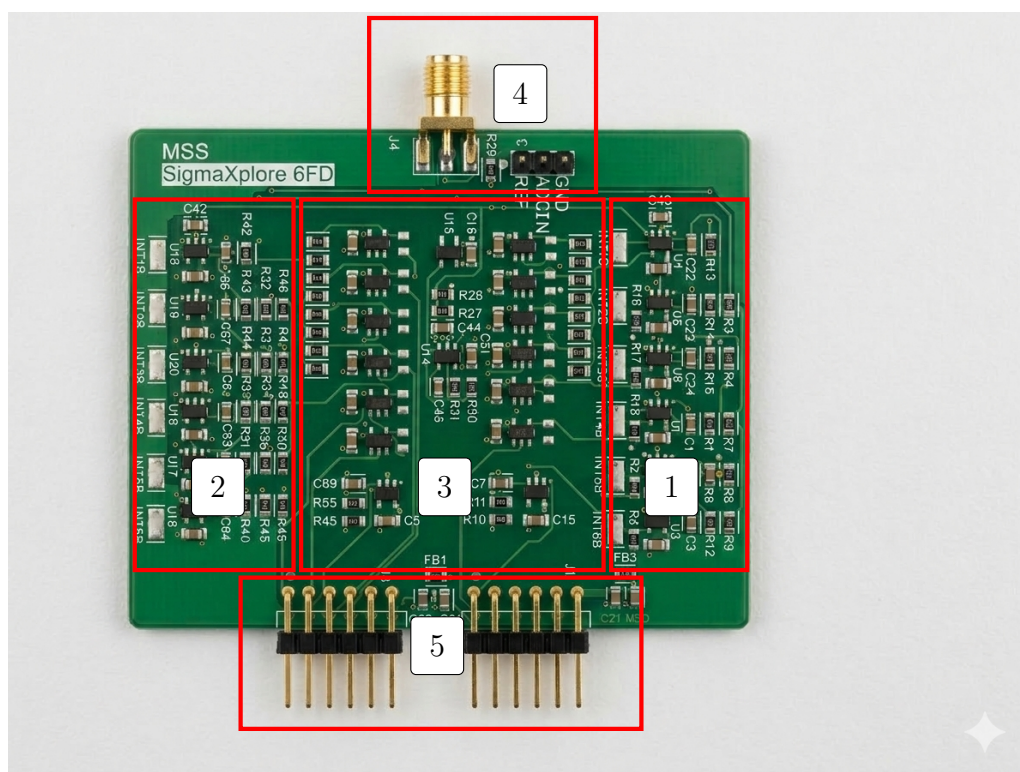
Parameter	Value	Unit
Supply Voltage	3.3	V
Supply Current	90	mA
SNR	-92	dB
V _{in}	3.25	V _{pp}

4 Performance

Below is the measured performance of the SigmaXplore 6FD with the SigmaXplore DAC driving it with a 1kHz -3dB Full Scale (2.3V_{pp}) input. The ADC is configured for 20 bits with an OSR of 128. The 2nd order DAC is configured for 20 bits and is driven by a CORDIC NCO. The ADC resolution and sample rate are determined by the clock frequency, oversampling ratio, and number of integrator stages and can be easily modified through vivado code changes.



5 Board



Reference	Callout	Signal/Part	Notes
1	ADC integrators	(6) stages	
2	ADC integrators	(6) stages	
3	Feedback DAC/ input buffer		
4	Female SMA input	3.25Vpp input	Swing limited by buffer
5	14 Bit I/O and power		FPGA connection

6 Software Support

The SigmaXplore 6FD includes a compressed Vivado project that's already configured for the MOC FPGA boards, and it can be adapted to any PMOD-style FPGA board with only minor edits to the .xdc file.

There are plenty of opportunities to improve upon the baseline performance that comes with the compressed vivado file. This includes linearization math, equalization filtering, feedback patterns, among other things.

7 Connecting the PMOD module

Connecting the SigmaXplore 6FD is straightforward because the pins follow the PMOD standard: 0.9-inch spacing with a dual-row 12-pin, 0.1-inch header.

The module must only be inserted into a PMOD port in the correct orientation. A single-pin offset or an upside-down insertion can damage the module, since misalignment can place PMOD supply pins directly onto unprotected I/O pins. The MOC FPGA boards themselves are not at risk, but the modules can be permanently damaged if connected incorrectly. Always power down all boards when connecting or disconnecting modules.

Once aligned properly, the module can be used without concern for I/O configuration. The MOC FPGA boards follow the 200-ohm PMOD output-impedance guideline, which prevents damage from pins that might otherwise be driven incorrectly during development or testing.

The ADC input can be driven within the 3.3V rails without problems. Driving more than 10mA above and below the rails will result in damage. Please double check all connections before powering up.

8 Pinout

Below is the pinout when facing the inputs of the SigmaXplore 6FD.

N_DS_FB_P	PS_IN_P				
FIR_FB_P0	P_DS_FB_P				
FIR_FB_P2	FIR_FB_P1				
NC	FIR_FB_P3				
GND	GND				
3.3V	3.3V				

N_DS_FB_N	PS_IN_N				
FIR_FB_N0	P_DS_FB_N				
FIR_FB_N2	FIR_FB_N1				
NC	FIR_FB_N3				
GND	GND				
3.3V	3.3V				