DesTest MAX-Switch

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Revision 1

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Introduction

The DesTest MAX-Switch (aka DesTest Switch, aka ‘Switch) project builds upon the DesTestMAX cartridge to provide a complete 64K RAM test solution.

The ‘Switch boots into MAX (or ULTIMAX) mode to perform the initial 4K memory test, then switches to 64K mode to test the full 64K of memory. This arrangement allows the ‘Switch to work in a wide-range of situations.

The 6510 CPU, VIC-II and PLA need to be functional, though the ROMs, CIAs and SID are not required and can be removed if socketed. See the C64 Hardware Considerations section for more details.

A DesTest MAX-Switch cartridge will also work in a Commodore 128. DesTest MAX-Switch will automatically run in ‘64 mode yet requires the ‘128 kernal, a working Z80 and a working MMU. The VDC is not required.

Building a DesTest MAX-Switch Cartridge

Unlike DesTestMAX or DesTestFull, both of which can use standard C64 cartridge PCBs (such as the Versa64Cart), the cartridge for DesTest MAX-Switch contains extra electronics required for automatic switching between 4K (MAX) mode and the regular 64K mode.

Details on how to obtain a MAX-Switch PCB can be found on the factorofmatt.com website.

There you will also find a separate document that will document the required bill of materials and detail how to assemble your cartridge.

Features of your DesTest MAX-Switch Cartridge

Your DesTest MAX-Switch cartridge comes with two simple, but effective hardware features intended to help you diagnose problems with your C64 more easily.

Power LED

Often when attempting to fix a poorly C64, the first thing we do is remove the keyboard. Unfortunately this takes the power-LED with it and it can be difficult to see if the unit is powered-on or not. The Power LED found to the top-left of the DesTest MAX-Switch cartridge takes the place of the missing keyboard-LED and will help prevent accidental cartridge or chip insertion or removal while the power is on.

Reset Button and LED

The reset-LED on the cartridge (next to the reset-button) indicates the state of the reset (/RST) signal. Under normal circumstances, this LED will illuminate for a short time at power-up then extinguish. (It will also illuminate while the RESET button is pressed). If the reset LED doesn't illuminate or if it doesn't then extinguish after a short period of time, then something is most likely wrong with the reset circuit on the C64 or '128.

Running the Diagnostics

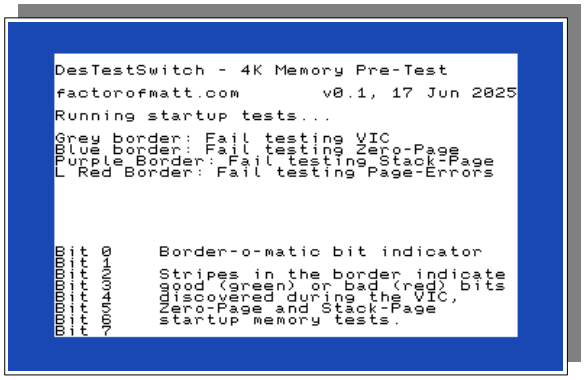
Exactly what you see when you power on your machine with a DesTest MAX-Switch cartridge installed depends on exactly what is wrong with the system. The DesTest MAX-Switch cartridge requires the CPU, VIC-II, PLA, and supporting circuitry to be functional in order to be of any help. An entirely blank screen is a good indication that one of the big-three chips or their support logic is malfunctioning and the cartridge will be of little use.

If you are familiar with how the DesTestMAX cartridge operates, the initial screen display and tests will be familiar. The 'Switch cartridge first tests the initial 4K of memory then, if that memory is found to be working, the cartridge reconfigures itself and proceeds to test the entire 64K.

Like the DesTestMAX cartridge, the ROMs, CIAs and the SID are not required for full DesTestSwitch operation.

4K MAX-mode Startup Tests

When the cartridge first starts it tests the VIC-II, Zero-Page, the Stack Page, the RAM multiplexers and the checksum of its own ROM. The startup screen will be displayed immediately upon cartridge startup and remains only for a few seconds while the startup tests run.



- The VIC-II has 47 registers mapped into the $D000 block of address space. We don't use all the features of the VIC-II during testing, so many of these registers can be considered as general

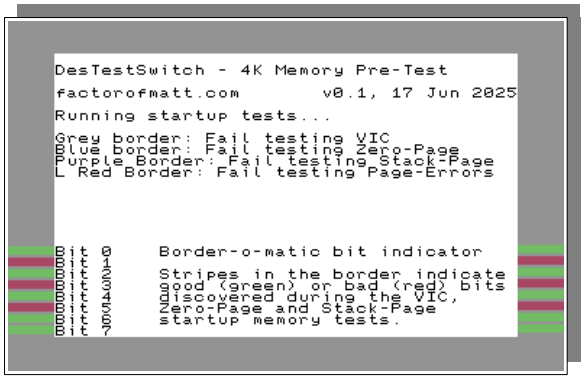
read/write ‘memory’. Testing is performed on these registers to verify that they can be written and read as expected.

- The Zero Page is one of the two 256-byte memory pages treated specially by the 6510. It would be impractical to write a full memory test without using at least some of zero-page, so we test it early here. The test does not use zero-page (or the stack) to do so.
- The Stack Page is the other 256-byte memory page treated specially by the 6510. The stack allows the use of subroutines (JSR/RTS). We test the stack page (without using it or zero-page) so that we have some confidence we can use subroutines for the more comprehensive tests.
- Failures in the C64’s memory address multiplexer circuitry can lead to seemingly random memory corruption known as Page Errors. Since we do use a little of the 64K memory during tests, we test the multiplexers early to avoid possible corruption.
- A 16-bit checksum is calculated for the entire contents of the DesTest MAX-Switch code ($E000-$FFFF). If the checksum is incorrect the EPROM image could be corrupt or could indicate that address decoding logic in the C64 is faulty.

An error detected in any of these first 4 tests will cease testing and the display updated to indicate the failure:

VIC Test Failure

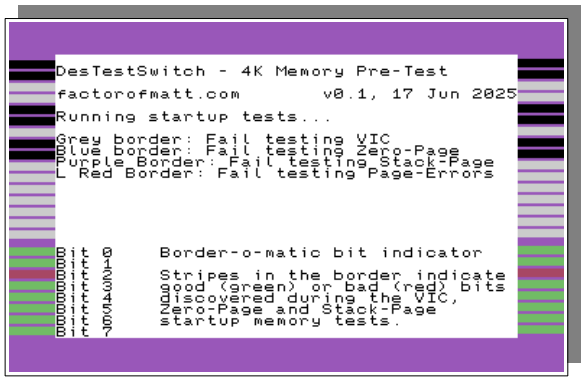
A failure during the VIC test results in a grey border with the failing bits displayed in the bottom part of the screen:



The border-stripes show data bits (D0-D7, top to bottom) that showed inconsistencies while testing the VIC-II registers. Here we see that data bits 1, 3 and 5 were detected as bad. This may be of diagnostic use if another data attached chip in the system is corrupting the bus – or it may simply indicate a marginal VIC-II.

Zero Page or Stack Page Failure

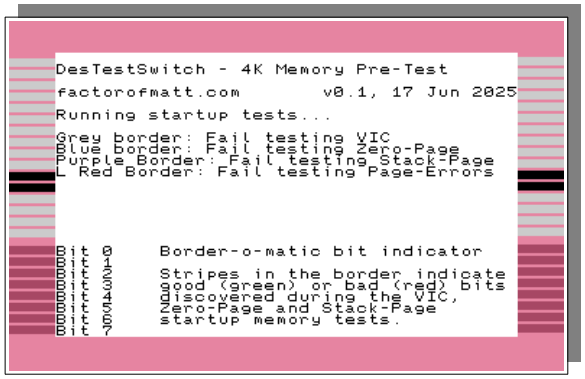
A failure during either of these tests results in a blue (zero-page) or purple (stack page) border plus stripes indicating the fail-address and failed bits:



The border stripes show address bits (A0-A15, top-to-bottom) and data bits (D0-D7, top to bottom). A black address bit is 1, light grey is 0. A green data bit indicates a good bit, red indicates bad. Here we see that data bit 2 was detected as bad and that the most recent memory location found to be bad was $01B3.

Page Error Failure

A failure during the page-error (multiplexer) tests results in a light-red (pink) border plus stripes indicating the fail-address-bits and failed bits:



Page errors occur when some set of addresses gets incorrectly mapped to a different set of addresses. This can happen both inside a memory chip or in the case of a C64 when the address multiplexers fail. Imagine that address-bit 2 is always stuck ‘on’: a read or write at address 0 would actually be a read or write at address 4 (plus 1 maps to 5, 2 to 6 and 3 to 7 and so on every 4 bytes throughout memory). Similar situations exists if a bit is stuck ‘off’ or accidentally tied to another bit entirely.

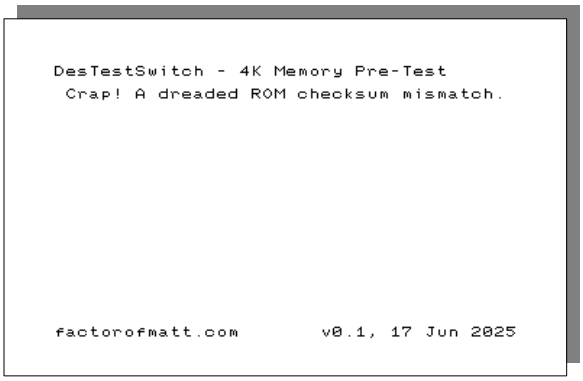
The March-B tests used to detect memory errors are totally capable of detecting page errors, though we choose to explicitly check for them early to avoid accidental memory corruption. While every effort is made during the main set of tests to not actually use memory, a couple of addresses are used and they

are at risk of corruption if the multiplexers are bad. This test hopefully eliminates the possibility of the multiplexers being bad and allows us to use some (previously tested) locations with a measure of confidence.

Unlike other tests, the fail-address-bits indicate which address-bits seem to be faulty (bits 9 and 11 in the above example) rather than a specific address. Such information can be useful (with help from the C64 schematics) to determine which multiplexer is likely faulty.

Code Checksum Failure

A checksum failure is indicated by a white border and a message indicating the checksum error. Under certain circumstances, the text of this screen may be garbled or otherwise unintelligible. See the Limitations section for details.

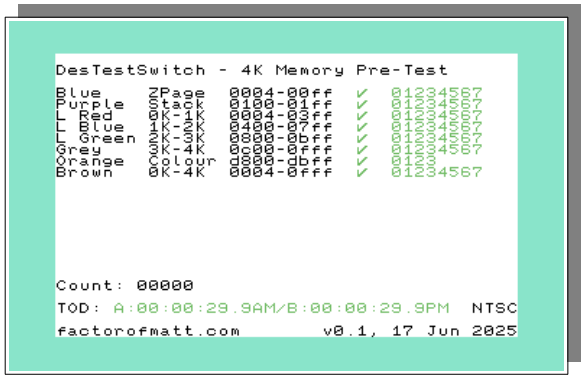


4K MAX-mode Tests

After the startup tests complete, we have enough confidence in the system to go ahead and test the entire 4K of memory. Depending on how much memory is good/present or if the VIC-II can “see” it properly this screen may be garbled. There are 8 tests here:

- Zero Page (blue border): Tested again
- Stack Page (purple border): Tested again
- 0K-1K (light red border) : first 1024 bytes (including the Zero and Stack pages)
- 1K-2K (light blue border) : second 1024 bytes
- 2K-3K (light green border): third 1024 bytes
- 3K-4K (dark grey border): last 1024 bytes. This VIC-II gets the display matrix from this region so there will be activity on the display during this test.
- Colour RAM (orange border): VIC-II colour information is stored in this region
- All RAM (brown border): All 4K is tested at once

It isn't strictly necessary to split the tests up as above, but it allows a little bit of visual flair for some tests and also means we can use a little pre-tested memory for storage of address/bit-error information.



64K Startup Tests

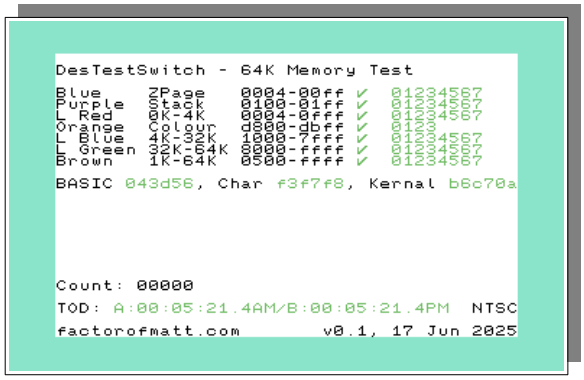
After the switch into 64K mode, the same set of startup tests as MAX mode are run again for good measure and the Page Errors test this time includes all 64K. A failure during the 64K startup tests can be interpreted in the same way as the MAX startup tests as described above. Since the Page Errors tests now tests all 64K it may find multiplexor errors that the 4K tests did not.

64K Main Tests

After the startup tests complete, we have enough confidence in the system to go ahead and test the entire 4K of memory. Depending on how much memory is good/present or if the VIC-II can "see" it properly this screen may be garbled. There are 8 tests here:

- Zero Page (blue border): Tested again
- Stack Page (purple border): Tested again
- 0K-4K (light red border) : first 4096 bytes (including the Zero and Stack pages)
- Colour RAM (orange border): VIC-II colour information is stored in this region
- 4K-32K (light blue): the lower half of the C64 RAM.
- 32K-64K (light green): the upper half of the C64 RAM.
- 1K-64K (brown): the entire C64 RAM.

As with the MAX 4K tests, it isn't strictly necessary to split the tests up as above, but it allows a little bit of visual flair for some tests and also means we can use a little pre-tested memory for storage of address/bit-error information.



At the bottom of the screen is the count of the number of times we've looped through all the tests. Each cycle takes about 5 ½ minutes.

The tests will loop forever if no failures are determined.

Any test failure will halt testing, though tests in the current cycle (except possibly All RAM) are finished first: we might as well collect as much information as we can.

The Zero Page, Stack Page, 0K-1K and All RAM tests do not collect error information (since it would be overwritten by the destructive nature of the tests).

Interference (static) in the Border

As each of the memory tests is running you'll notice that the border flickers slightly (it may look like interference or static). This is entirely intentional and acts to inform you that the tests are still running.

ROM Checksum Display

After each test, the extended (24-bit) checksum of the BASIC, kernal and character ROMs are calculated and displayed. If the checksums match those of known 'good' ROMs, then the checksum is displayed in green. If the checksum is unknown, then it is displayed in RED. Should a bad-checksum seem to change after each test, then that is a good indication that the ROM in question is having electrical issues.

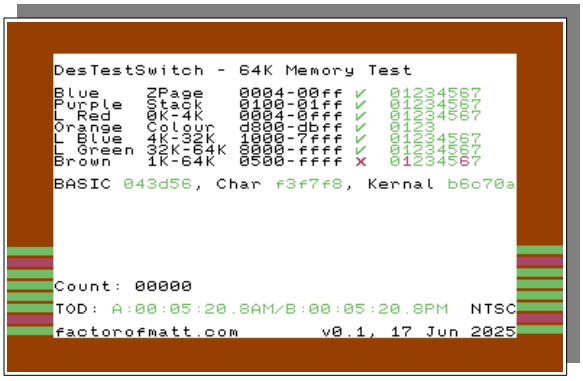
Note: a red checksum doesn't necessarily indicate a bad ROM, just that DesTest MAX-Switch doesn't recognise it. This may be due to the ROM being customized in some way or simply a valid ROM not included in the 'Switch database. The checksums for all common standard ROM revisions are included in the database including the JiffyDOS variants.

CIA Time Of Day Display

The TOD information (derived from the CIAs if they're present) shows how long the tests have been running. Throughout the tests the times displayed should remain consistent between the two CIAs. Should the times not be consistent (ignoring AM/PM) then the times will be displayed in red instead of the usual green. Red times may indicate faulty or missing CIAs.

Error Detected, No information saved

If no error information was collected, the border stripes show data bits (D0-D7 top to bottom) green for good, red for bad.



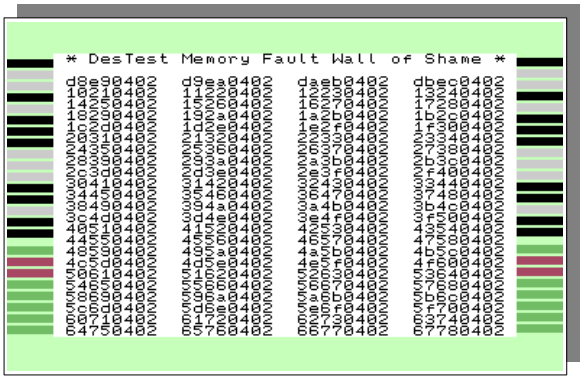
Error Detected, Information saved.

In the event that we were able to collect some address/bit-error information it is displayed on the following screen. Each error record is 8 hex digits wide:

- First 4 digits: The address at which an error was detected
- Next 2 digits: An indication of bits that were written as 0 but were read as 1
- Last 2 digits: An indication of bits that were written 1 but were read as 0

An error record of 04150402 indicates that at address $0415 bit 2 ($04) was mistakenly read as 1 and bit 1 ($02) was mistakenly read as 0. Patterns may emerge both in addresses and bad bits that can indicate the source of problems.

Note: some addresses may appear multiple times since the testing algorithm walks through memory both backwards and forwards a couple of times each.

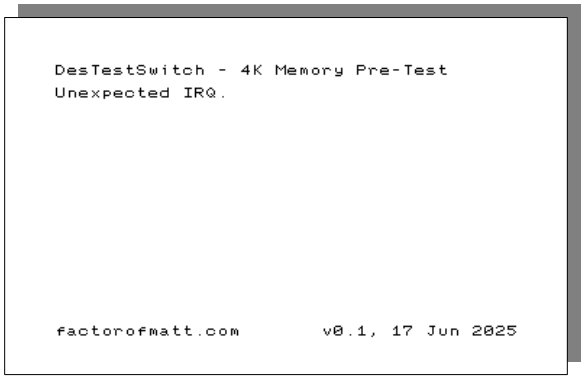


Interrupts

An unwanted interrupt could cause havoc during the middle of a test: interrupts write to the stack which really wouldn't be great if we're testing that memory or if that memory is suspect. During the 4K tests, the IRQ and NMI are handled correctly and will display the screens as shown below. In the 64K tests, no IRQ or NMI handlers exist and, while interrupts are disabled during these tests, an NMI (such as generated when hitting the restore key) may crash the system.

IRQ (4K)

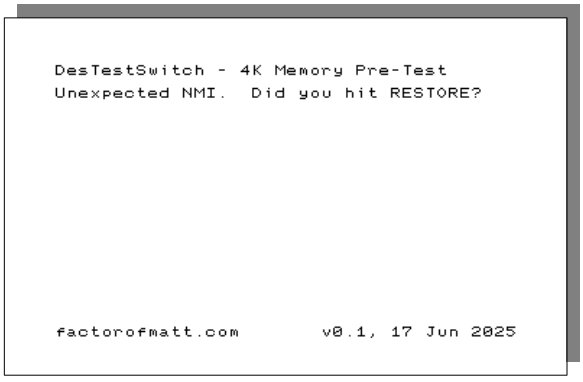
Under normal circumstances no IRQs should occur during normal DesTestMAX operation. The CPU is left free to respond to IRQs and will display the following screen should any occur.



The receipt of an IRQ during the execution of tests could very well indicate something wrong with the interrupt-signal path or a misbehaving interrupt source (VIC-II, CIA etc.).

NMI (4K)

NMIs cannot be disabled. The best we can hope is to ensure that any sources of an NMI are disabled. Unfortunately, the RESTORE key when tapped will always generate an NMI and there's really nothing that can be done about it. If an NMI is received, the following screen is displayed:



If you see this screen and did not hit RESTORE then something (CIA) generated an NMI or something is wrong in the NMI signal path.

If you hit the RESTORE key (possibly in frustration if nothing seems to be happening) and you see this screen, then at least you know the CPU works.

Limitations

DesTest MAX-Switch does assume that the first 4K of memory is mostly healthy. The screen display and the character bitmaps are stored in this RAM. If the first 4K of memory is not healthy, all may not be lost: there's some testing that can continue – but the display may not be readable. Don't despair though, since the border indicators (see below) will still give a strong indication of failing memory-bits.

Memory Errors might not be due to the memory at all. The shared address and data buses in the Commodore 64 are susceptible to accidental hijack by malfunctioning ICs. If a chip writes data to one of these buses when it shouldn't then it can very easily seem like a RAM error when in reality the bus is being corrupted elsewhere. A useful technique can be to remove all non-essential chips in case they are dirtying a bus. The ROMs, CIAs and SID can all be removed (if socketed) and might provide clues if symptoms change after. DesTestMAX is happy to run without those chips. See the C64 Hardware Considerations section for more details.

Border-o-matic bit indicator

This silly name refers to the method used to display address and bit information should the VIC-II otherwise not be trusted to generate a useful text display. This simple technique has been used for other retro computer systems and it seems like a cool way to impart diagnostic information when all else fails.

The border is split into 24 'stripes' each that represents a bit:

- A0-A15 (top to bottom) – Address bits.
  - Black for '1', Grey for '0'.
  - This number represents an address where the memory-test most recently found an error.
  - In cases where no address information can be captured, these 16 stripes are absent.
- D0-D7 (top to bottom) – Data bits.
  - Green for 'good', Red for 'bad'.
  - This value represents a map of RAM data-bits bits where an error was detected. Multiple bits can be flagged as 'bad' and indeed individual bad bits could come from different addresses.

The address shown (if present) will be that of the most-recent error found. This will usually correspond to the lowest faulty memory address of the region being scanned by nature of how the memory is tested. The good/bad bits do not represent any specific byte in memory, rather just an indication of bit-positions that showed an error at some address or other. Different revisions of the C64 use different configurations of physical RAM chips for storage. To map a bit number to a specific chip, See the C64 Hardware Considerations section.

If the border-stripes are shown then testing ceases so the information conveyed may be recorded. A power-cycle or reset is required to re-run the tests.

Testing methodology

The memory testing algorithm used in DesTest MAX-Switch is called March-B. A good description of common memory problems and test methodologies can be found here: <https://redirect.cs.umbc.edu/~reza2/courses/418/Slides/15MemoryTest.pdf>

The March B test performs 4 testing passes over the memory-region-under-test and ultimately verifies that any read or operation performed on a given bit is correct and doesn't affect any other bits in the region. The test is order 17N meaning that each bit under test is written and read a total of 17 times during the test. The test of the entire 64K region available in MAX mode takes about 2 ½ minutes.

Good care has been taken to ensure that no assumptions are made about the validity of memory before it has been tested. Neither Zero Page nor the Stack are used before those two memory regions have been verified since errors in either would cause havoc with the running code.

C64 Hardware Considerations

Commodore released multiple revisions of the C64 motherboard over the years. While these revisions remain mostly compatible with each other, there are a few differences that should be considered when attempting to diagnose a faulty machine.

RAM data bit to IC mapping

DesTest MAX-Switch helpfully indicates which RAM data-bits seem to be misbehaving but does not indicate the specific ICs that need to be replaced or investigated. This is for the simple reason that different revisions of the motherboard have different arrangements of RAM ICs and differing part identification numbers. This table will help you map bit numbers to specific ICs on your motherboard.

Assy# \ Bit	326298	KU14194HB	250407	250425	250441	250466	250469	C128
0	U21	U21	U21	U21	U21	U10	U10	U38
1	U9	U9	U9	U9	U9			U39
2	U22	U22	U22	U22	U22			U40
3	U10	U10	U10	U10	U10			U41
4	U23	U23	U23	U23	U23	U9	U11	U42
5	U11	U11	U11	U11	U11			U43
6	U24	U24	U24	U24	U24			U44
7	U12	U12	U12	U12	U12			U45

Shortboard CIA incompatibility

Elsewhere in this document we've discussed the fact that DesTest MAX-Switch doesn't require the CIAs to be installed in order to operate correctly. Unfortunately that isn't quite true for the most recent version of the C64 motherboard. The Assy 250469 "shortboard" as found in later C64Cs operates a little differently from the other motherboards when it comes to a missing CIA#2 ($DD00-$DDFF).

The PA0 and PA1 signals from CIA#2 control which of the 4 16K blocks of memory the VIC-II will address. The logic is inverted, so to select block 0 ($0000-$3FFF) both bits are set high.

For the first set of C64 motherboards, these two signals float high when the CIA isn't installed. [Though I don't see any specific pull-up resistors, my assumption is that the 74LS258 used to pick the correct 16K block floats its input pins to high internally if not driven to 0, as is the way with most TTL chips].

The shortboard motherboards don't use a 74LS258 to select the VIC-II block, rather it uses the 64-pin super-PLA for that job. For some reason, the PA0 and PA1 signals no longer seems to float to high so the default block for the VIC-II is no longer 0 when CIA#2 is removed. The upshot is that the VIC-II looks at the wrong memory area during the latter stages of DesTest MAX-Switch and the screen is garbled. A 1K to 10K resistor placed between /VA14 and /VA15 (pins 2 and 3) and +5v (pin 20) on the CIA#2 (U2) socket should be enough to overcome this limitation in the short term.