MOS Characterizations

Lab 4

EEE 334
Circuits II

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INTRODUCTION

This labs' main focus is to allow the student to understand the overall basic function of how MOSFET's work. The main points that will be focused on are how the voltage effects alter the overall gain of the MOSFET along with finding the drain current that flows through the transistor. Another focus is on finding the transconductance parameters of the MOSFET. Finding all these things will give a strong foundation to understanding the basic functions of a MOSFET.

Figure 1 was removed due to it only being a photo of myself

Figure 1 Lab Set-Up Selfie Photo

EQUIPMENT and COMPONENTS USED

For this lab the following items were used to conduct the experiments and findings:

- *Digital Multimeter*
- *ADK (Analog Discovery 2)*
- *Large Breadboard*
- *Analog Parts Kit*
- *TI-nspire CX II Calculator*
- *Resistors used: 1x 2.2kΩ*
- *Capacitors used: 1x 1µF*
- *Transistor used: 1x CD4007*

Course of Action

This section covers the processes that need to be done for each part. There will be a detailed description of what needs to be found and accomplished. The completed results mentioned in this section will be found in the results section.

4.1 Determination of Vt and Kn' (W/L) of NMOS

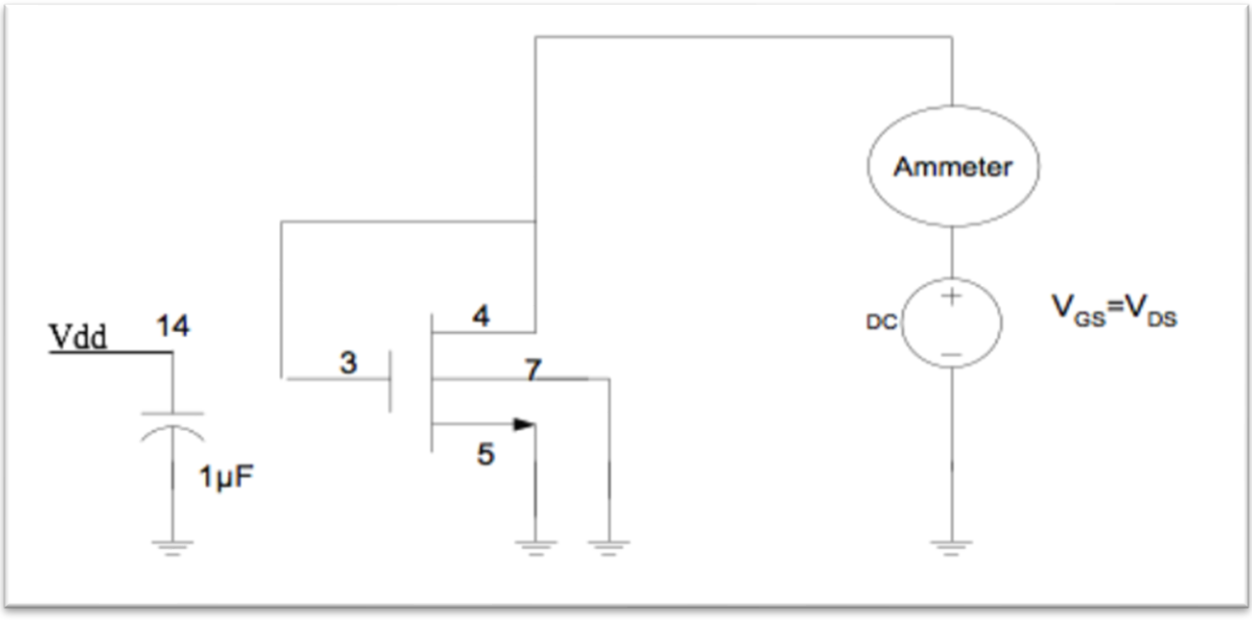

Figure 2 Circuit Diagram for determining Vt and Kn' (W/L) of NMOS

For the first section of the lab, the overall purpose is to determine the transistors threshold voltage along with the $Kn^{'}$ (W/L). This will be accomplished by first building the physical circuit that is depicted in the figure above. Prior to building the circuit the capacitor that is used will be measured and the value will be logged at the beginning of the results section. After that has been completed the ADK will be utilized to sweep the gate voltage from 0V – 5V to record the drain current that results. For the final step of this section the $\sqrt{i_d}$ will be plotted against V_{gs}. With this plot the threshold voltage and transconductance parameters can be found and logged in results.

4.2 Determination of ro and λ of NMOS

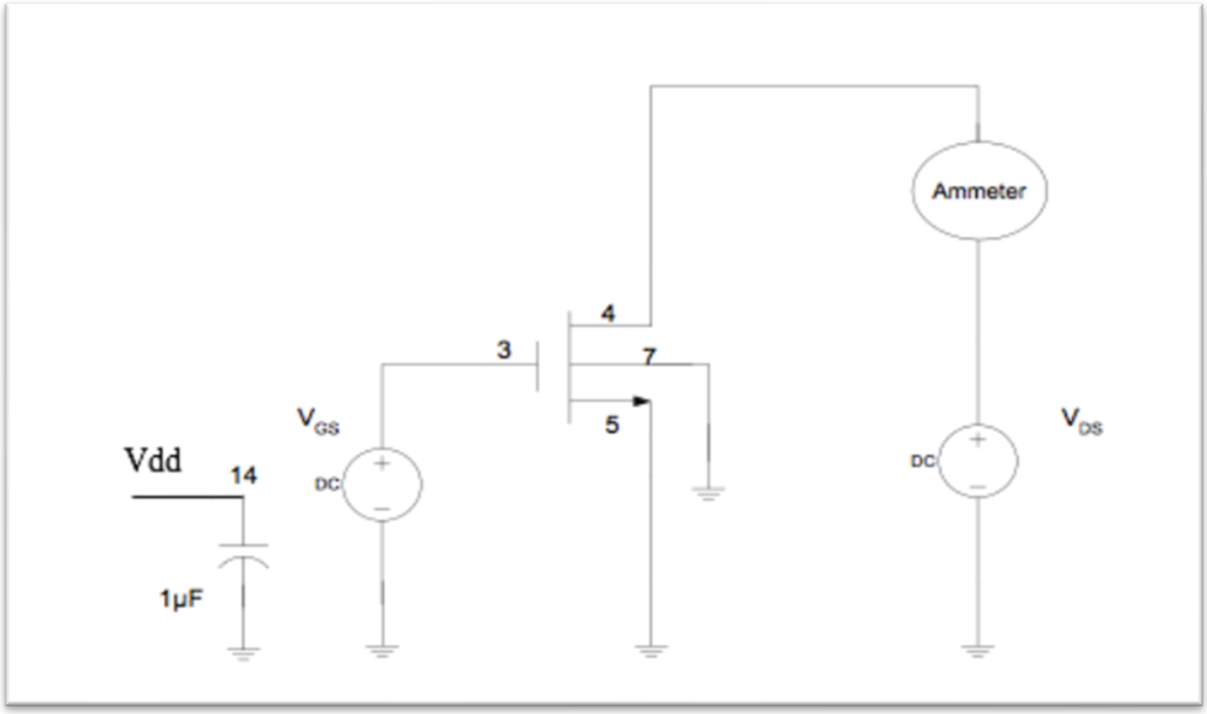

Figure 3 Circuit Diagram for determining of Ro and λ of NMOS

For section 4.2 this will be focusing on trying to find the NMOS values for ro and λ. To accomplish this, first the circuit will be built from the diagram figure displayed above. Due to the capacitor being the same as section 4.1 the value will be the same and stated again at the beginning of the results for this section. Next, the ADK will be used to supply a 3V input to the gate of the transistor. Once this is completed a DC sweep voltage will be applied to the circuit from 0-5V and every 0.5 volts the id will be logged. After the 3V gate experiment is completed a 5V input will be applied to the gate and the experiment will be ran again. Once all the data points have been gathered the id values will be plotted against Vds to be able to find the output resistance for each experiment. Having these plots will then allow for finding the V_A (early voltage) and the λ. After λ is found the average will be taken from the 2 experiments and logged.

4.3 Determination of gm of the NMOS transistor

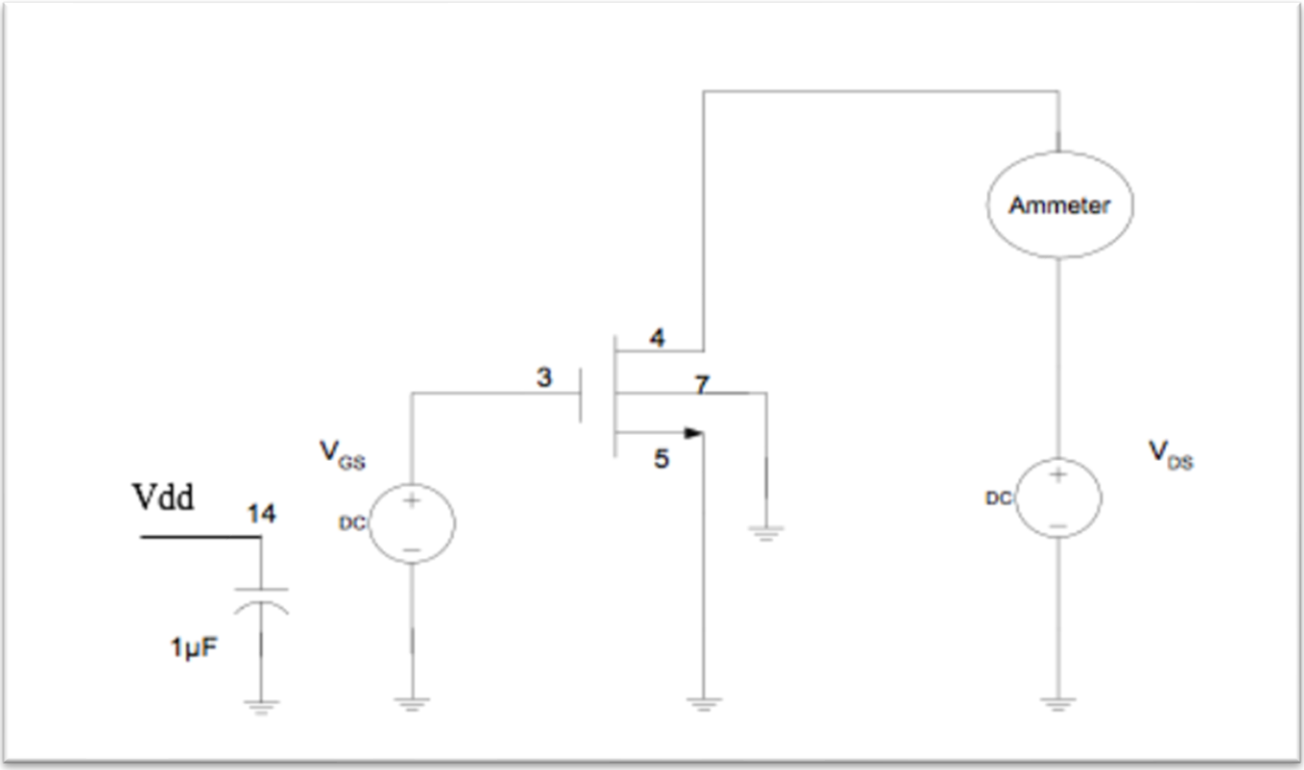

Figure 4 Circuit Diagram for Determination of gm of the NMOS transistor

For section 4.3, the same physical circuit will be used as in the previous section 4.3. For the experiment the drain current will be kept at a constant 5V DC, and the drain current will be measured while the gate voltage is being varied from 2V – 5V in steps of 0.5V. After the drain current values have been logged their results will be plotted against Vgs. From these plotted results the transconductance (gm) can be calculated and the average gm will be calculated and logged.

4.4 Large signal operation: The transfer characteristics

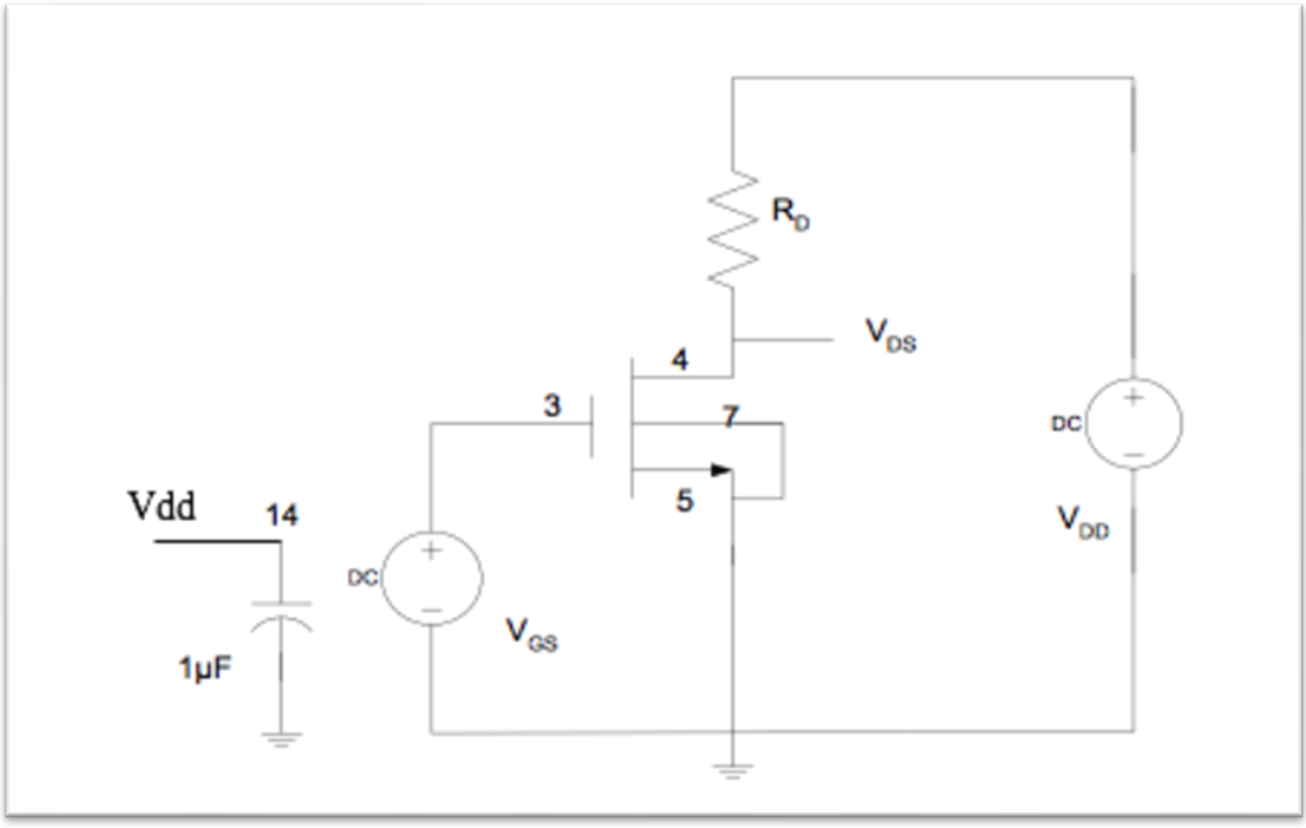

Figure 5 Circuit Diagram for Common Source Amplifier

For the last section 4.4, the circuit will be built to the requirements from the diagram displayed above. Once completed the ADK will be utilized to set the Vdd value to 5V. Similar to previous sections the gate voltage (Vgs) will be varied from 0-5V, and the drain voltage will be logged at 0.5V increments. Once these values are obtained, they will be plotted by drain voltage vs gate voltage. Having this plot then allows for the calculation of the transfer characteristics in the saturation region. Having these calculations for the saturation region, the circuit will now be built in LTSpice simulation software, and a DC sweep will be run for the circuit. Now having these DC sweep values they will be plotted similar to how the physical circuit values were. This will allow to find the transfer curve of the simulated circuit. From this curve, calculations will be run to find the Q point in the saturation region. For the last step, the results will be verified to see how close the physical results were from the LTSpice simulated results.

RESULTS

4.1 Determination of Vt and Kn' (W/L) of NMOS

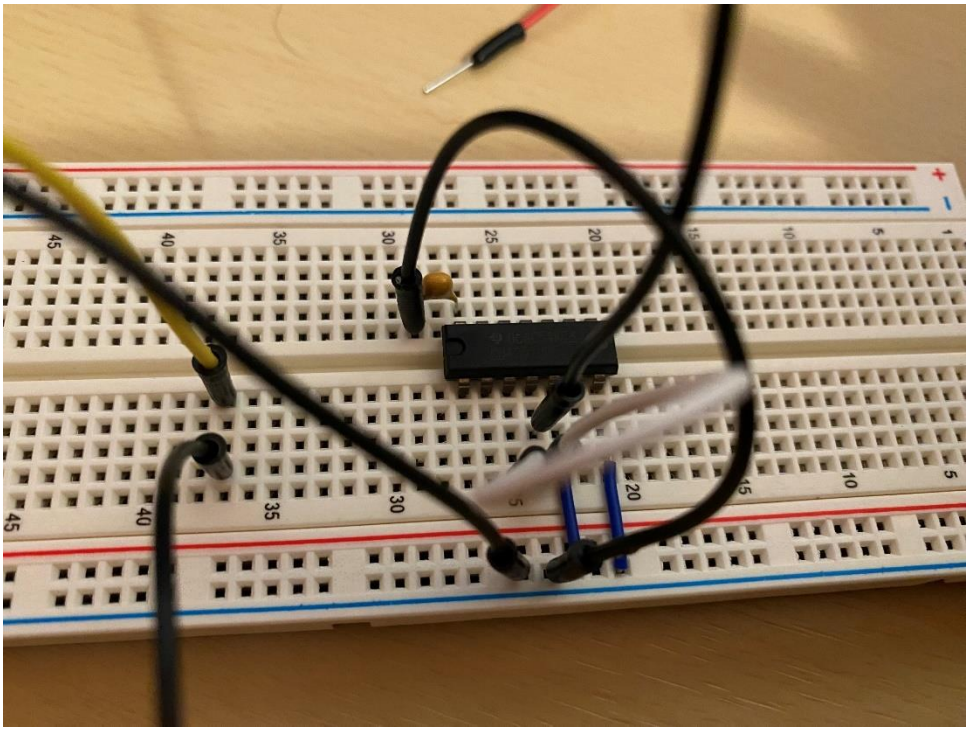

Figure 6 Physical Built Circuit for Determination of Vt and Kn' (W/L) of NMOS

Measured Capacitor used: **C = 0.95µF**

Table 1 Measured Values from Physical Circuit

V_{GS} (V)	i_D (mA)	$\sqrt{i_D}$(mA)
0	0	0
0.5	0	0
1.0	0	0
1.5	0.02	0.141
2.0	0.25	0.5
2.5	0.71	0.843
3.0	1.34	1.158
3.5	2.11	1.453
4.0	2.98	1.726
4.5	3.95	1.987
5.0	5.00	2.236

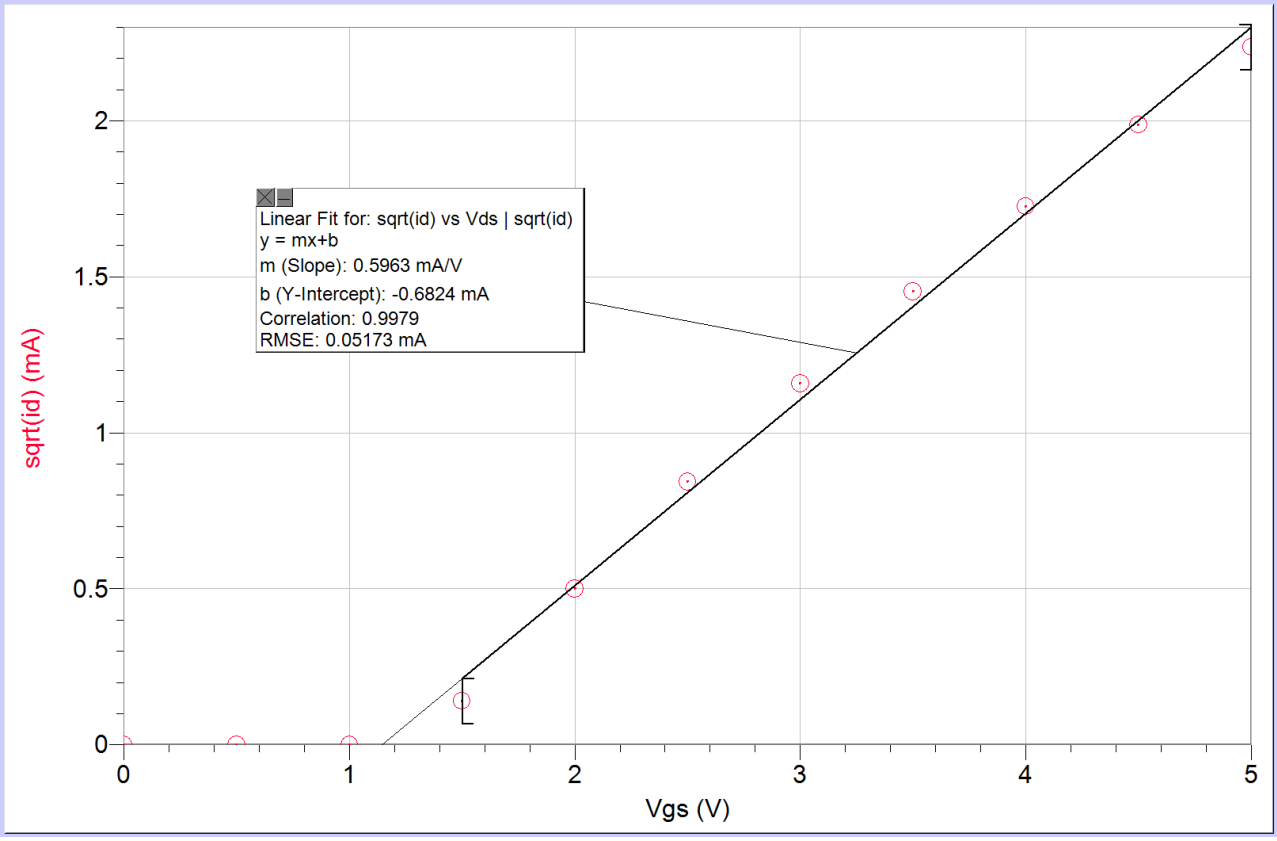

Figure 7 Logger Pro plot of $\sqrt{id}$ vs Vgs

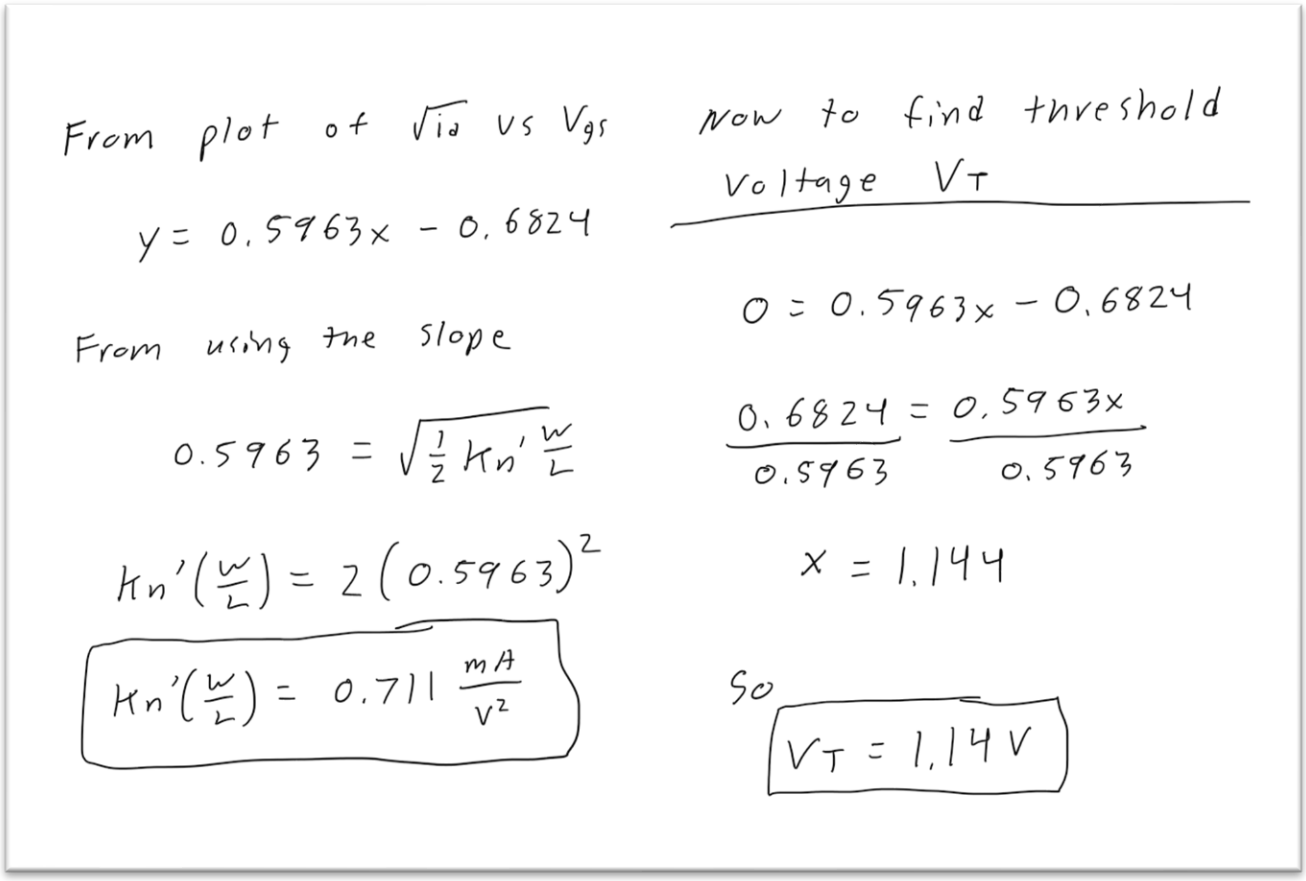

Figure 8 Hand Calculation Results for Section 4.1

4.2 Determination of ro and λ of NMOS

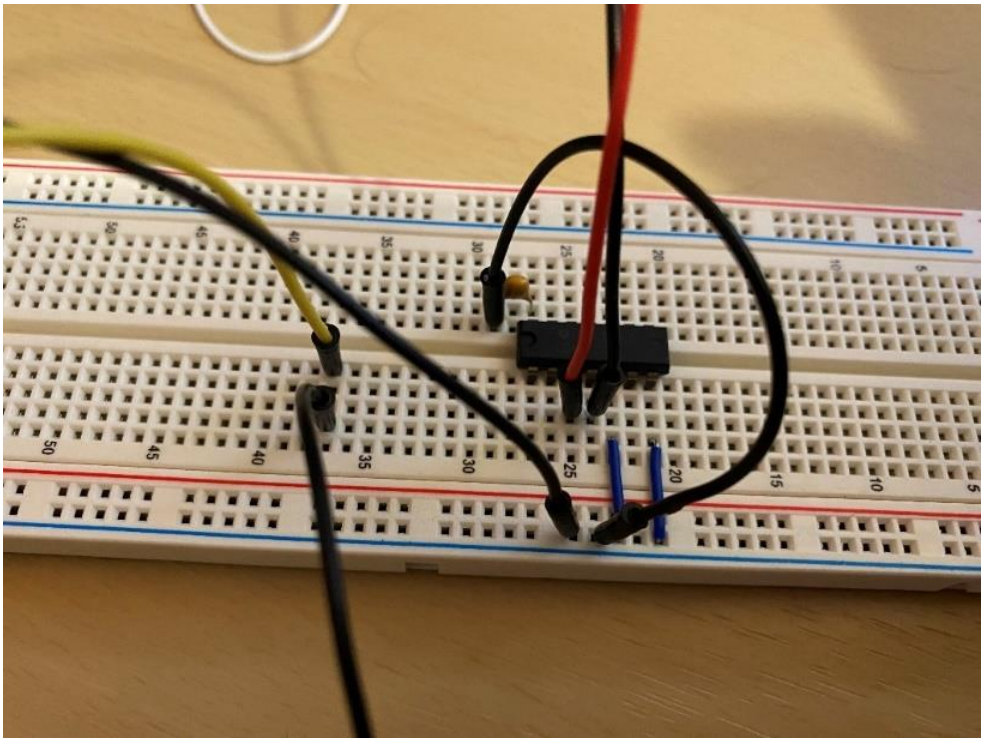

Figure 9 Physical Built Circuit for Determination of ro and λ of NMOS

Measured Capacitor used: **C = 0.95µF**

Table 2 Measured Values for Vgs = 3V

V_{DS}(V)	i_D(mA)
0	0
0.5	0
1.0	1.26
1.5	1.35
2.0	1.37
2.5	1.38
3.0	1.39
3.5	1.40
4.0	1.40
4.5	1.41
5.0	1.41

Table 3 Measured Values for Vgs = 5V

V_{DS}(V)	i_D(mA)
0	0
0.5	1.36
1.0	2.46
1.5	3.68
2.0	4.48
2.5	4.94
3.0	5.13
3.5	5.19
4.0	5.22
4.5	5.25
5.0	5.26

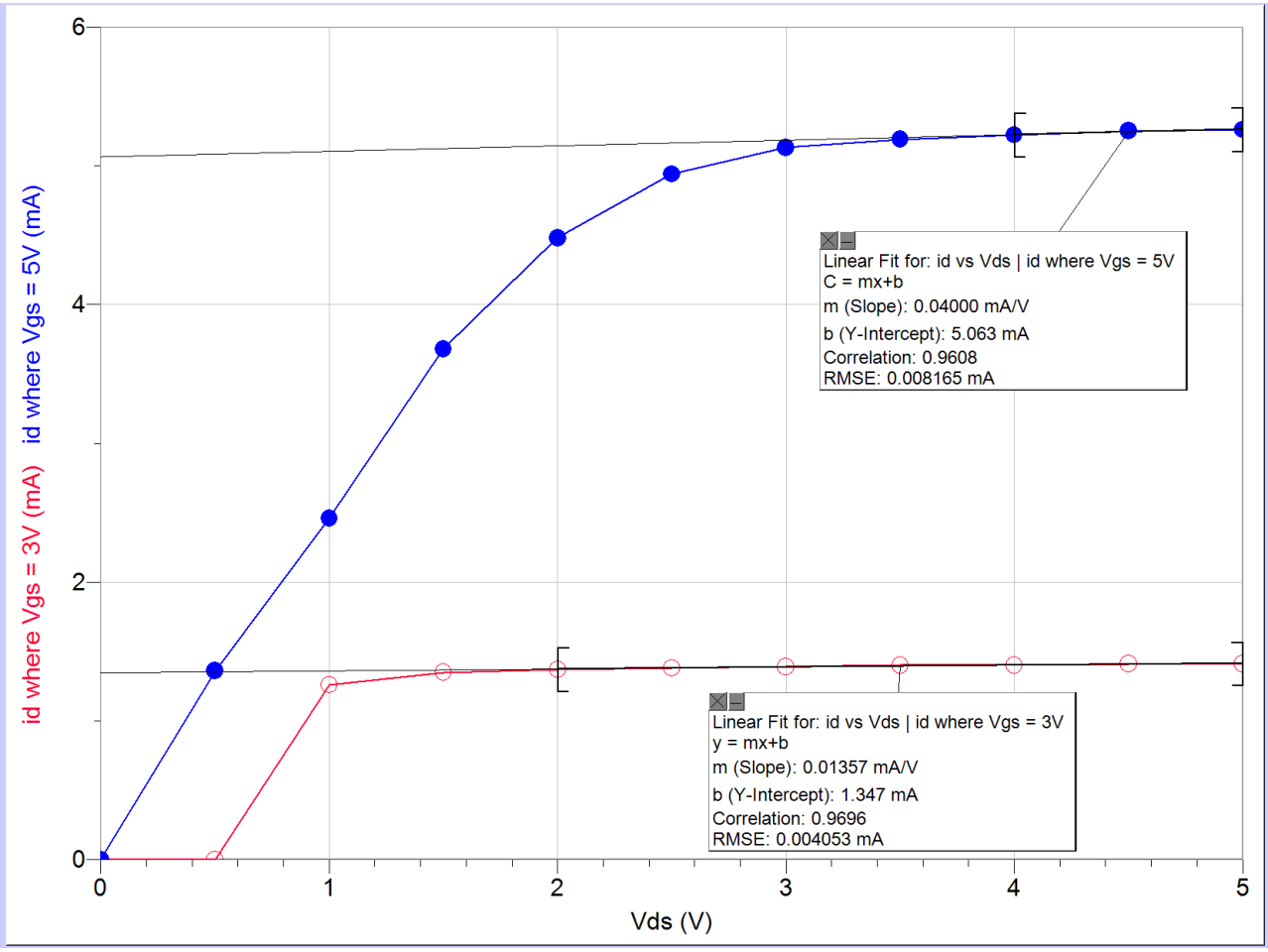

Figure 10 Logger Pro Data Plot for Section 4.2

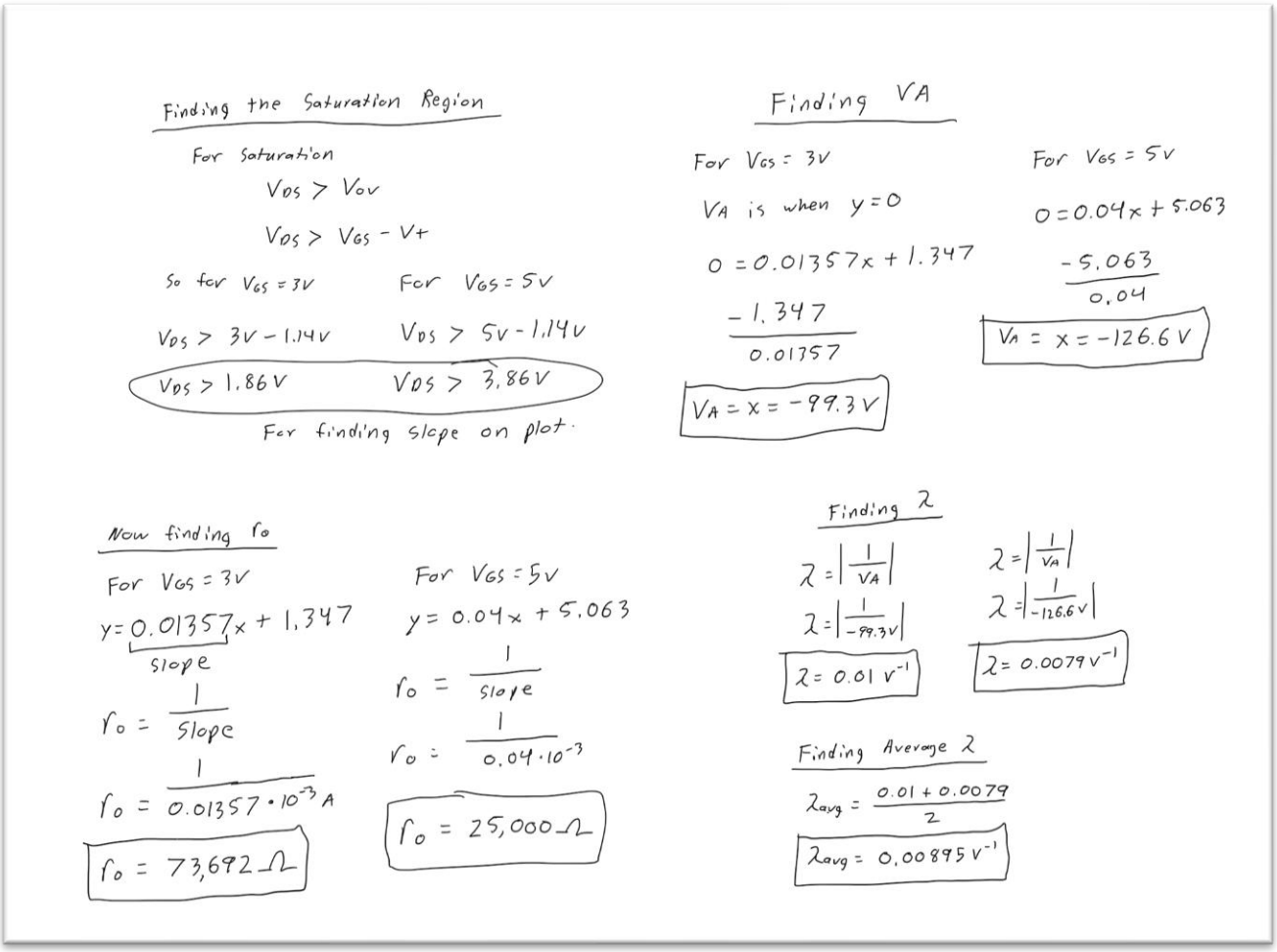

Figure 11 Hand Calculation Results for Section 4.2

4.3 Determination of gm of the NMOS transistor

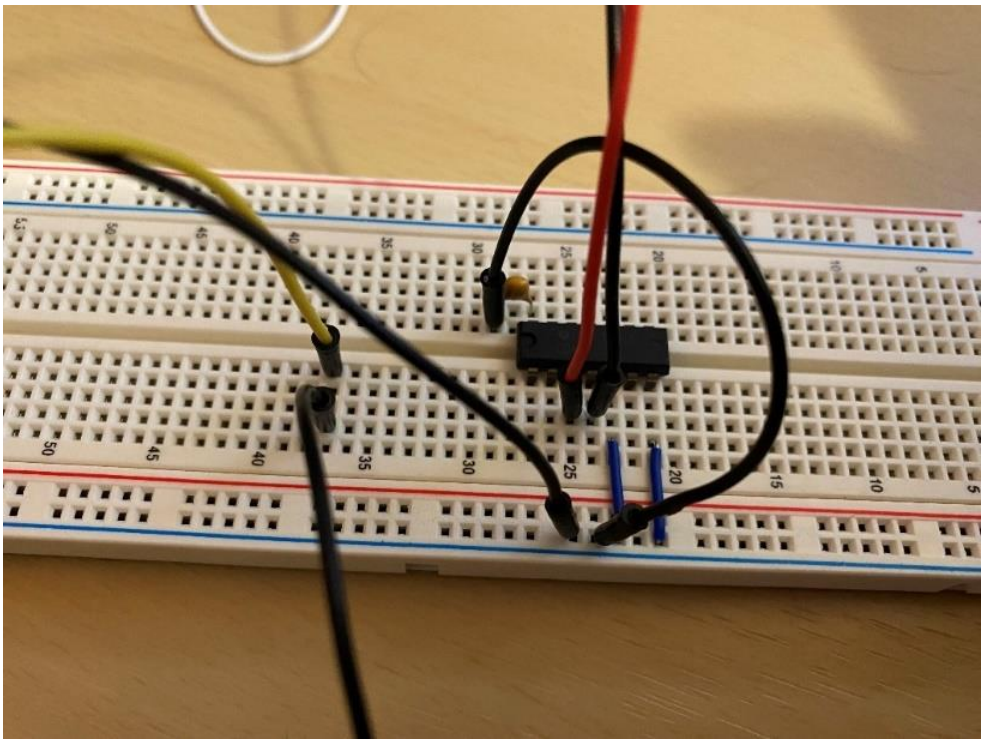

Figure 12 Physical Build for Determination of gm of the NOMS Transistor

Measured Capacitor used: **C = 0.95µF**

Table 4 Measured and Calculated Values for Section 4.3

V_{GS}(V)	i_D(mA)	$gm = \frac{2i_D}{V_{GS} - V_T}$
2.0	0.27	0.6279
2.5	0.74	1.0882
3.0	1.39	1.4946
3.5	2.19	1.8559
4.0	3.10	2.1678
4.5	4.10	2.4405
5.0	5.17	2.6788

Average gm from physical

Total from table values

$\frac{12.3537}{7} = gm_{avg} = 1.7648$

Figure 13 Hand Calculations for Table gm Average

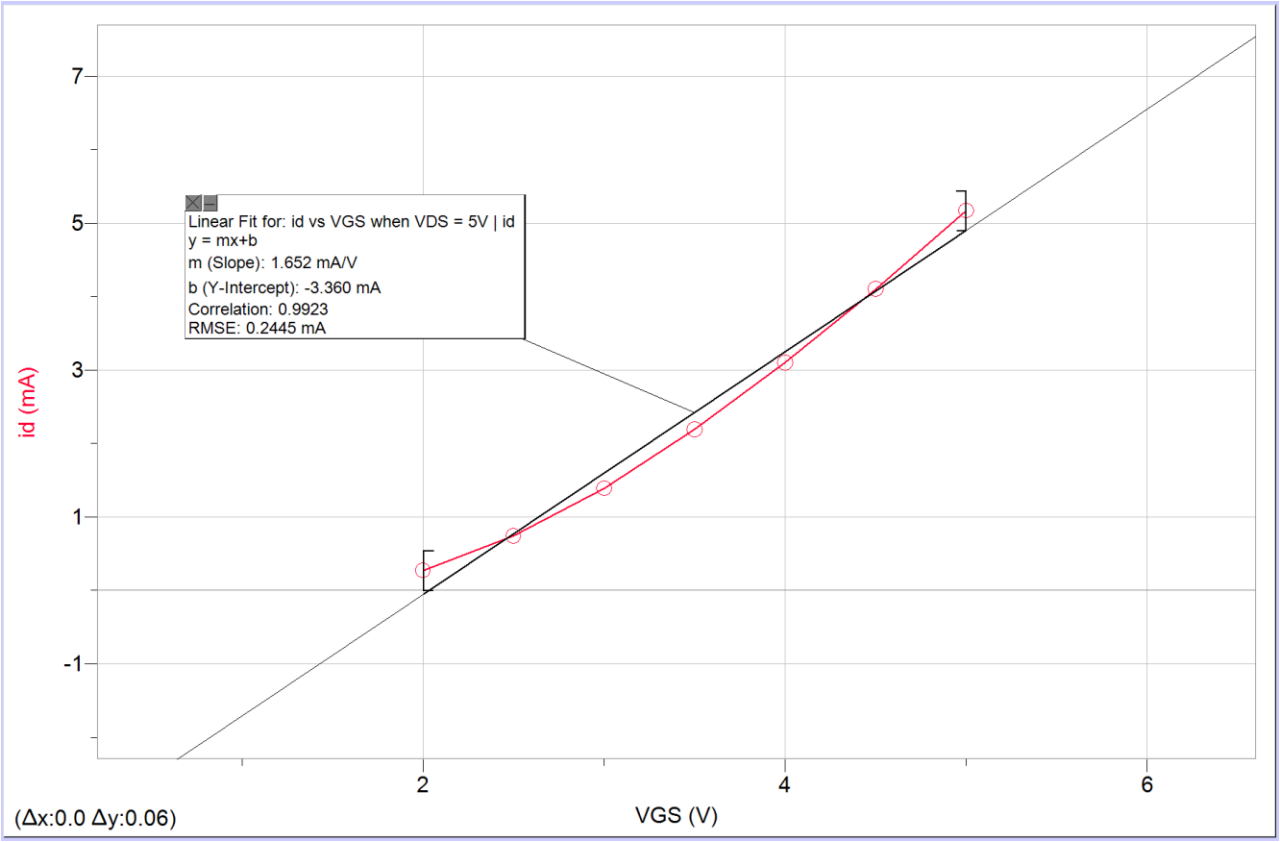

Figure 14 Logger Pro Data Plot for Section 4.3

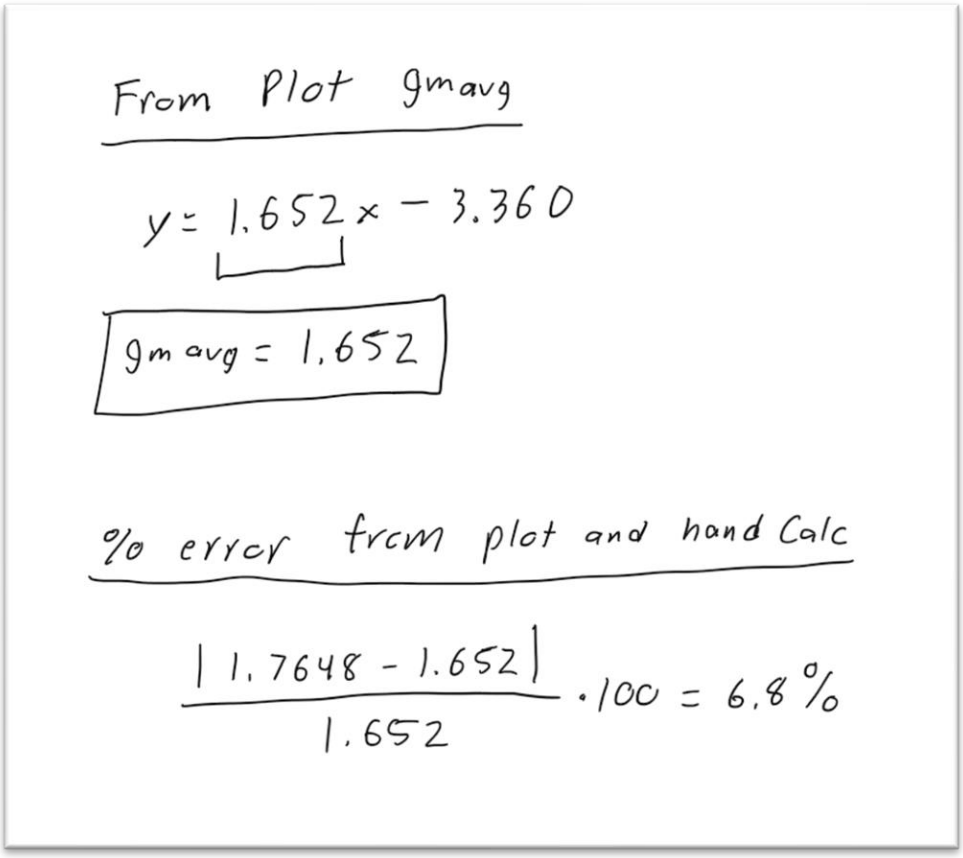

Figure 15 Hand Calculations for Transconducatance (gm) avg and % Error

4.4 Large signal operation: The transfer characteristics

Measured Capacitor used: **C = 0.95µF**
Measured Resistor used: **C = 2182Ω**

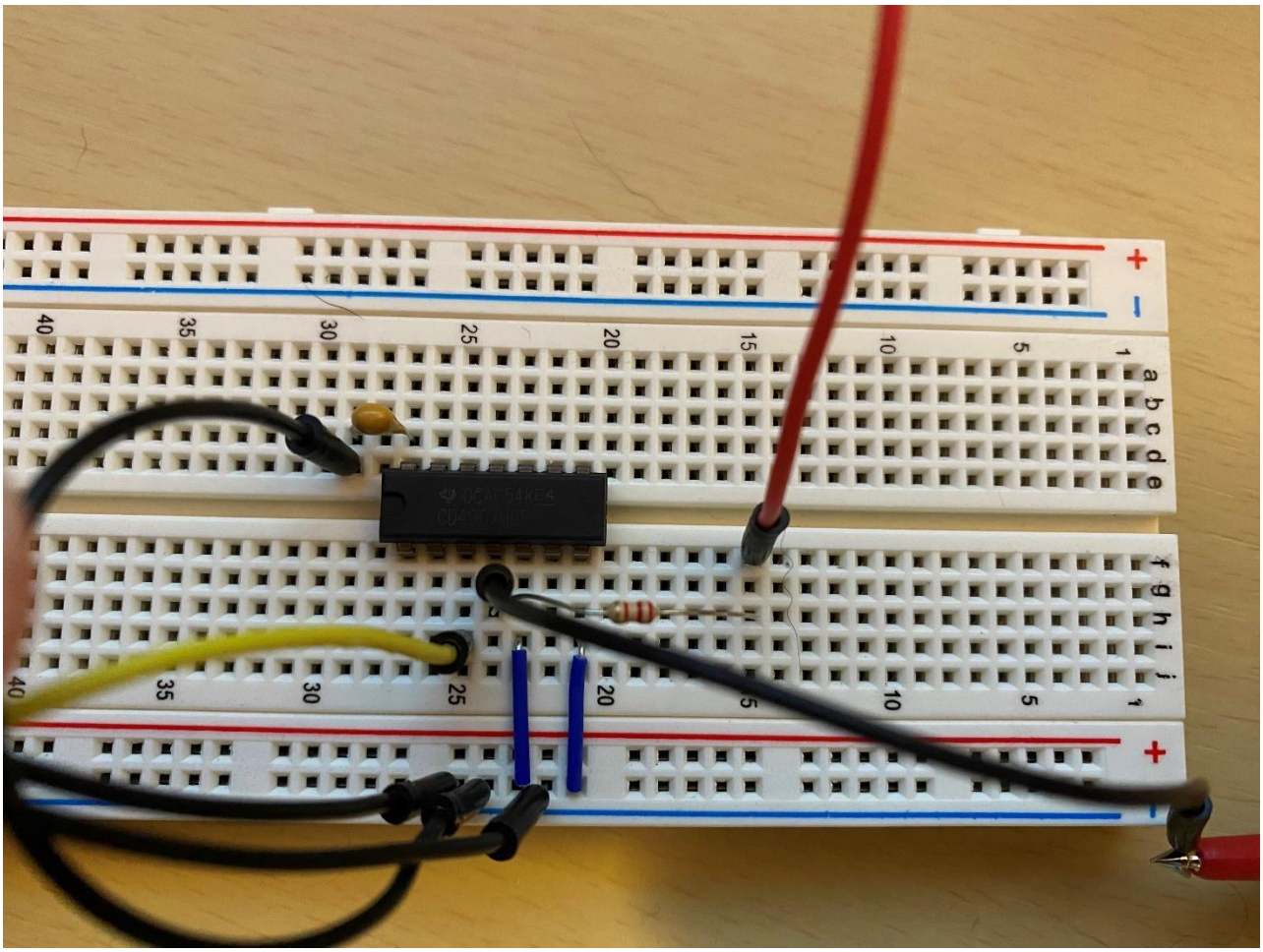

Figure 16 Physical Build for Large Signal Operation

Table 5 Measured Values for Section 4.4

V_{GS}	V_{DS}
0	4.99
0.5	4.99
1.0	4.99
1.5	4.93
2.0	4.39
2.5	3.36
3.0	1.98
3.5	0.93
4.0	0.71
4.5	0.61
5.0	0.55

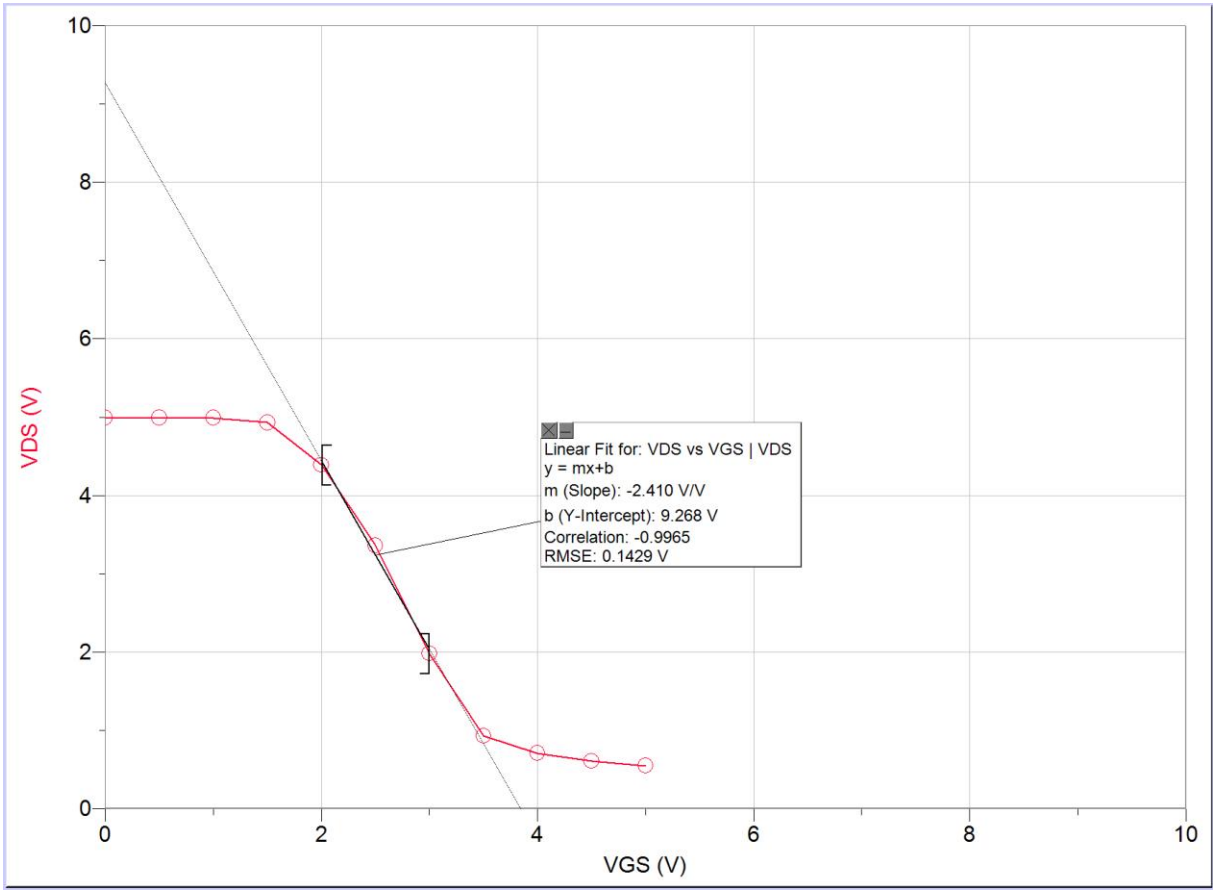

Figure 17 Logger Pro Data Plot for Section 4.4

Slope from Q on plot = -2.410

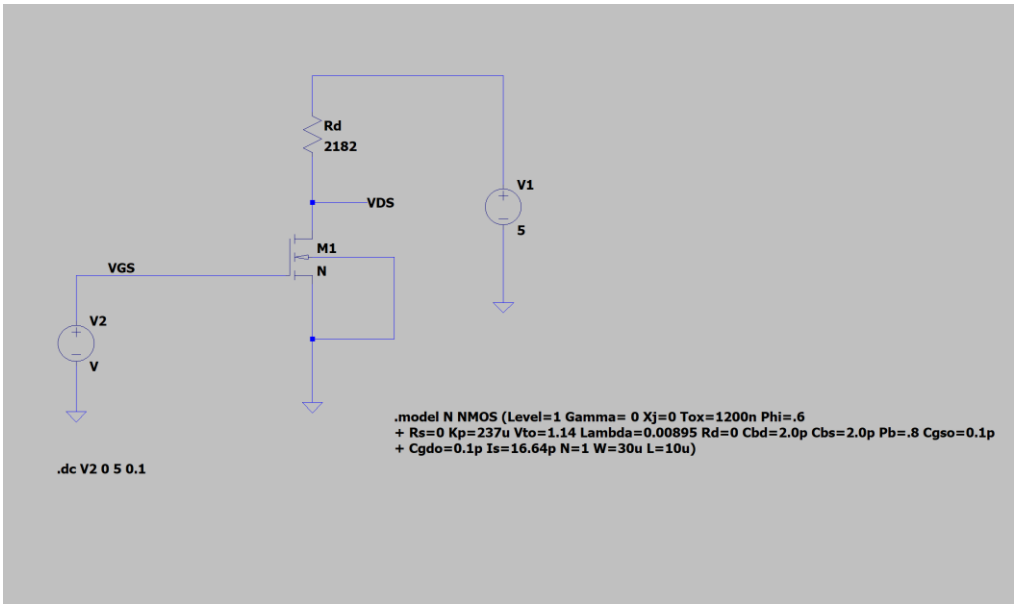

Figure 18 LTSpice Circuit Diagram for Section 4.4

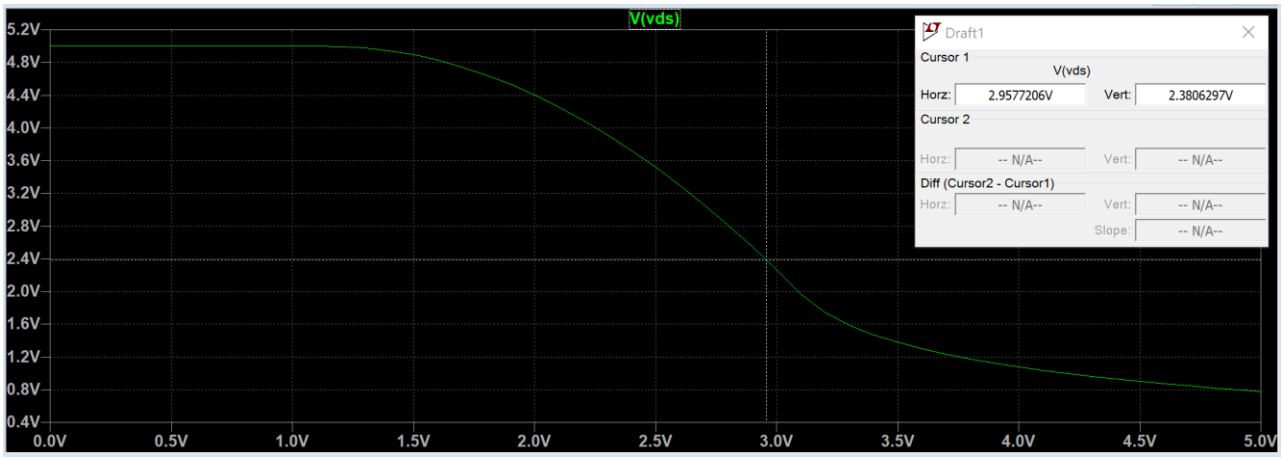

Figure 19 LTSpice DC Transient Analysis for Section 4.4

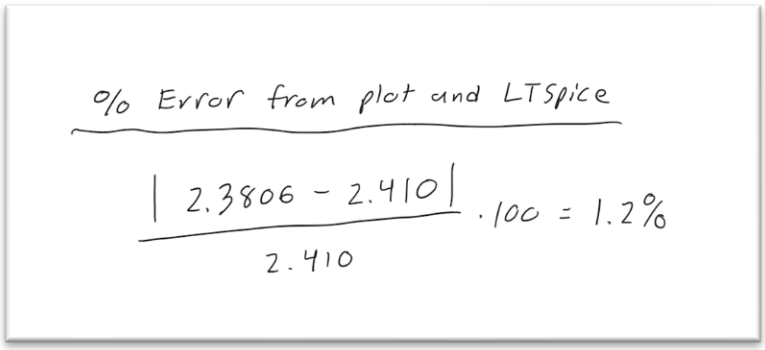

Figure 20 Percent Error Calculations Verifying Section 4.4 Results

CONCLUSION

This lab's main purpose was to allow the student to get a deeper understanding of how a NMOS works along with finding the various values such as Vt, Va, ro, λ, Kn'(W/L), gm, and a few others. It allows for a strong foundation for analyzing the specifications and how transistors work along with practice utilizing various equations.

For the first section 4.1, the focus was finding the kn'(W/L) transconductance of the transistor along with the threshold voltage. This was done by building the circuit and logging the id values from 0-5V. Once the id values were logged, they were converted over to $\sqrt{id}$ values. These values were then plotted vs VGS. A linear fit was applied to the graph omitting the id = 0 values. Running the hand calculations, the kn'(W/L) results came out to be $0.711mA/V^2$ along with the threshold voltage coming out to be 1.14V. These values were important to find, due to them being used in the remaining parts of the lab.

As for the second section 4.2, this focus was shifted finding the values that pertained to ro and λ (channel length modulation). From running the hand calculations for 2 values of VGS of 3V and 5V the ro results were. VGS (3V) ro = 73692Ω and VGS(5V) ro = 25000Ω. Moving into the λ calculations the equation of $\lambda = |\frac{1}{V_A}|$. This means that in order to find λ the early voltage was needed to be found first. From the hand calculations the early voltages came out to be VGS(3V) V_A = -99.3V and VGS(5V) = V_A = -126.6V. Now that these values were obtained the λ could be calculated and came out to be VGS(3V) λ = $0.01V^{-1}$ and VGS(5V) λ = $0.0079V^{-1}$. With a λ average coming out to be λavg = $0.00895V^{-1}$.

In section 4.3, the focus was on finding the value of gm for this transistor. For this experiment the VDS was kept at a constant 5V. Then the VGS was swept from 2-5V, and the drain current was measured and logged at each value. From the results section the gm_{avg} was calculated by adding all the gm values and dividing them by 7. Resulting in gm_{avg} = 1.76. The values were also plotted, and a liner fit was applied to find the slope which also translates to the $gm_{avg.}$ The slope came out to be gm_{avg} = 1.65. Having these two values a percent error was calculated and came out to be 6.8% error this is pretty good for such a small amount of data points taken.

Lastly section 4.4, the focus for this section was to determine the transfer characteristic gain of the MOS amplifier circuit. The resistor value was measured to be 2182Ω. Once the circuit was built the ADK was used to vary the VGS voltage from 0-5V and the drain voltage values were logged. All this data was then plotted and the steepest point in the graph is roughly the Q point that needed to be found. This slope came out to be -2.41. Then the same circuit was simulated in LTSpice making sure the actual measurements taken from previous sections were implemented into the transistor values. Once the circuit was built a DC transient analysis was run and the plot came out to be very similar to the logger pro plot. Where the Q point was roughly at the slope of -2.38. Now that these two values were gathered the percentage error was calculated and came out to be 1.2% which is very close.

This lab overall was much better than previous labs. With this transistor knowledge it will be much easier to understand the characteristics of any transistor and how to find the values besides just relying on the data sheets.

POST LAB QUESTIONS

1. A.

Post Lab Question

1.)

$K_n'\left(\frac{W}{L}\right) = 0.711 \frac{mA}{V^2}$

$V_t = 1.14V$

$i_D = K_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)V_{DS}$

For R_{DS}

$R_{DS} = \frac{V_{DS}}{i_D} = \frac{1}{K_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)}$

So for $V_{GS} = 3V$

$R_{DS} = \frac{1}{(0.711 \frac{mA}{V^2})(3V - 1.14)}$

$R_{DS} = 756.2$

For $V_{GS} = 4V$

$R_{DS} = 491.8$

For $V_{GS} = 5V$

$R_{DS} = 364.4$

Figure 21 Hand Calculations for Post Lab Question 1a

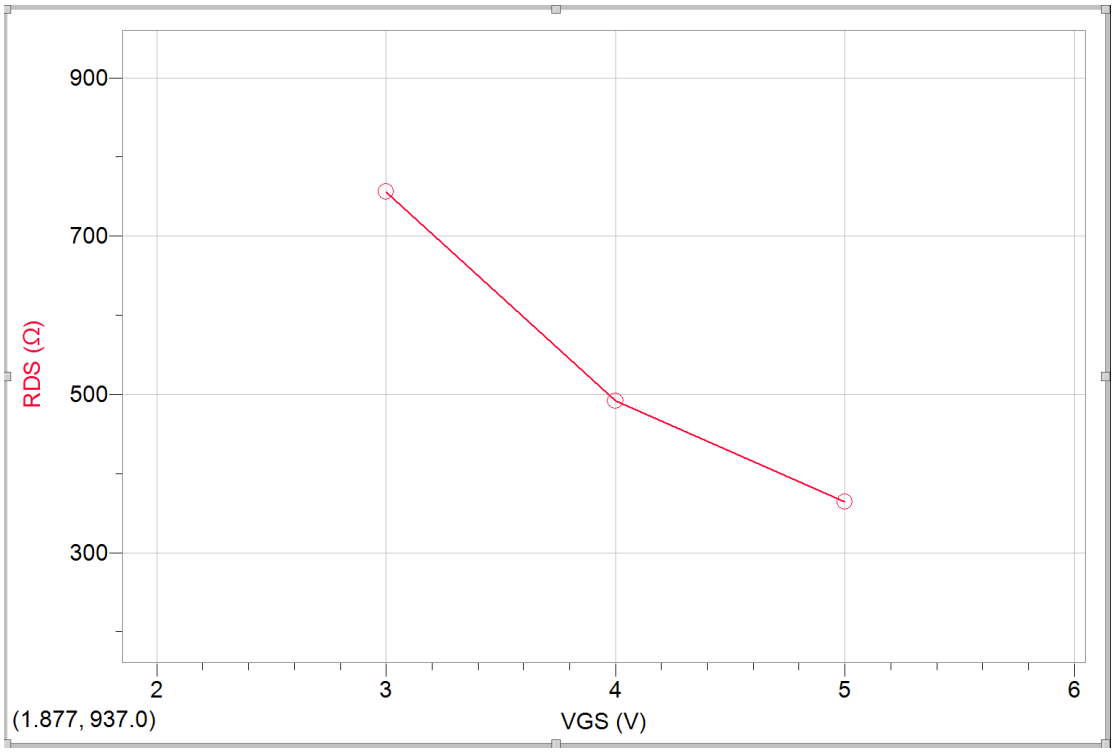

Figure 22 Plot for Post Lab Question 1a

As can be seen from the plot, VGS increases from 3-5V RDS decreases. So, the relationship between them would be inversely proportional.

B. Yes, again referencing the plot above, as VGS is greater than Vt the resistor value decreases proportionally to the increase in VGS. Thus, it can be said that this is in fact a voltage-controlled resistor.

2. Due to this resistance value being much larger than the 2.2k that is in section 4.4 this would result in VGS being very small pretty quickly. From the results from the 1st question Rd is in fact inversely proportional to Vov so the plot would have a very sharp negative slope when compared to the previous lab experiment and would get to 0 pretty quick.

3.

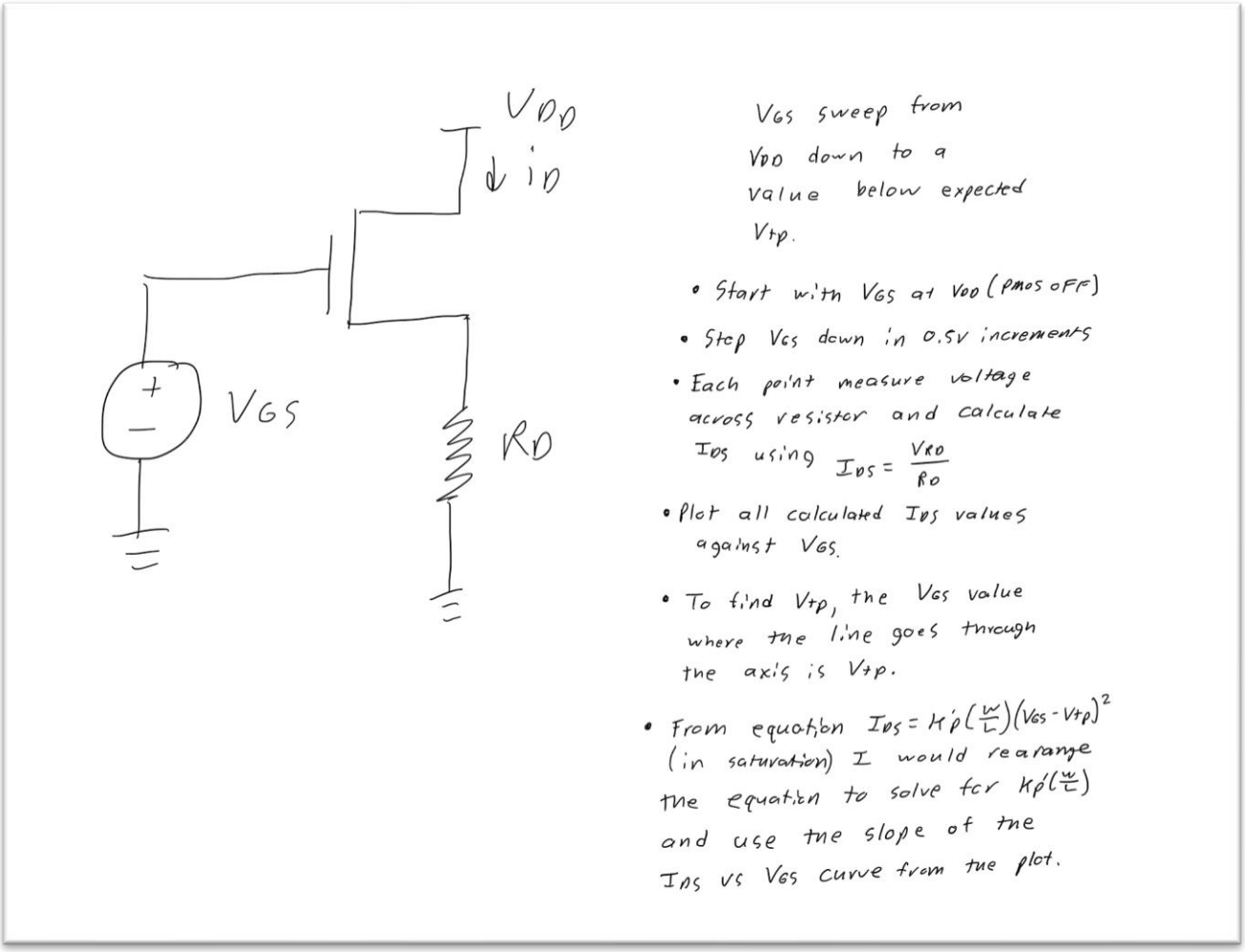

Figure 23 Post Lab Question 3