Single Stage MOS Amplifiers

Lab 5

EEE 334
Circuits II

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Student ID: **************

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INTRODUCTION

This labs' main focus is to allow the student to gain a deeper understanding of NMOS transistors. Similar to the previous lab, the CD4007 transistor along with all the calculated and found specifications, will be utilized for this lab's analysis. This lab will allow the student the ability to see these physical differences from a Common Source, Common Gain, and Common Drain Amplifier. Another focus being on finding the amplifiers frequency, gain, and bandwidth.

Figure 1 was removed due to it only being a photo of myself

Figure 1 Lab Set-Up Selfie Photo

EQUIPMENT and COMPONENTS USED

For this lab the following items were used to conduct the experiments and findings:

- *Digital Multimeter*
- *ADK (Analog Discovery 2)*
- *Large Breadboard*
- *Analog Parts Kit*
- *TI-nspire CX II Calculator*
- *Resistors used: 1x 68kΩ, 1x 2.2kΩ, 1x 200kΩ, 1x 1.5kΩ*
- *Capacitors used: 2x 1µF, 2x 4.7 µF*
- *Transistor used: 1x CD4007*

Course of Action

This section covers the processes that need to be done for each part. There will be a detailed description of what needs to be found and accomplished. The completed results mentioned in this section will be found in the results section.

5.1 DC biasing of an NMOS transistor

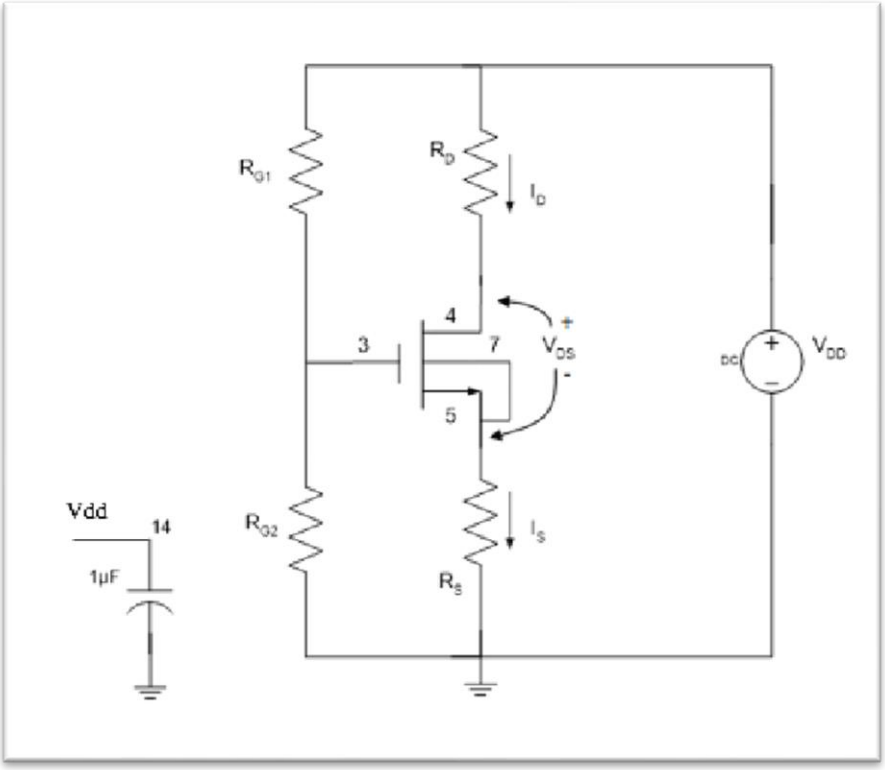


Figure 2 Circuit Diagram for DC Biasing of an NMOS transistor

For the first section of the lab, the circuit diagram in figure 2 will be used to build the physical representation. Previous to the full assembly of the circuit, each resistance value will be measured to verify the accuracy is in with tolerance. These values will be logged at the beginning of the results section. Once completed the handheld multimeter will be used to read and record the values of Vrd and Vrs in the circuit. Having these measured values, the Id and Is can then be calculated from handheld calculations. Now having all these values, the circuit will be built and simulated in LTSpice software to verify the results against the physical readings with the focus being on finding the operating point. Lastly, each of these compared results will be checked with a percentage error calculation.

5.2 Common-Source (CS) Amplifier

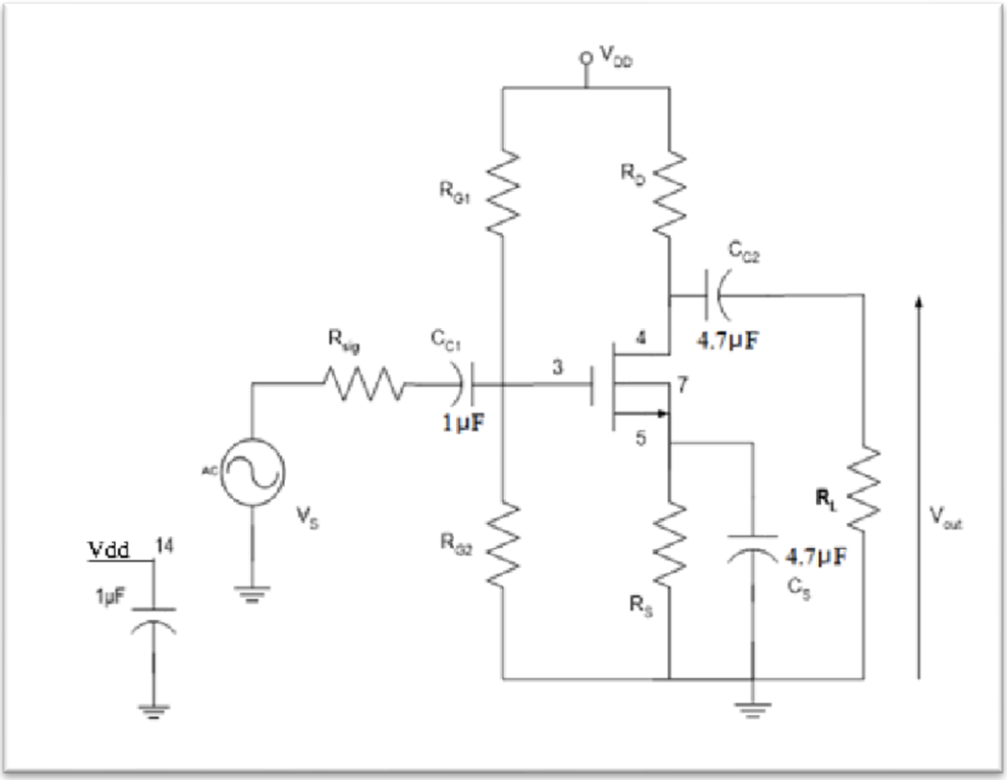


Figure 3 Circuit Diagram for Common-Source (CS) Amplifier

For section 5.2 this will be focusing on building a stronger understanding of a Common-Source Amplifier. The first step would be measuring the capacitor values that will be used in the circuit to verify their values. Once the circuit is built, the ADK will be connected and induce a 100m Vpp with 10kHz signal along with the 5V Vdd. The ADK oscilloscope will then be used to determine the waveforms received from Vs and Vo along with determining the phase shift between the two signals. These waveforms will be then used to measure the Vrms values, and those values will be used to calculate the gain. Once that is complete, the circuit will be built in LTSpice along with importing the values for the transistor from the previous lab. Once the circuit is simulated correctly a transient analysis will be performed on the circuit to determine the Vs and Vo signals. For the last part of the simulation an AC analysis will be performed to determine the frequency response for Vo/Vs. From this analysis the following values will be found utilizing the cursors on the graph, max gain, Fh, Fl, and the bandwidth for the circuit. A percentage error calculation will be preformed to analyze the physical circuits values against the simulated circuits values.

5.3 Common-Gate (CG) Amplifier

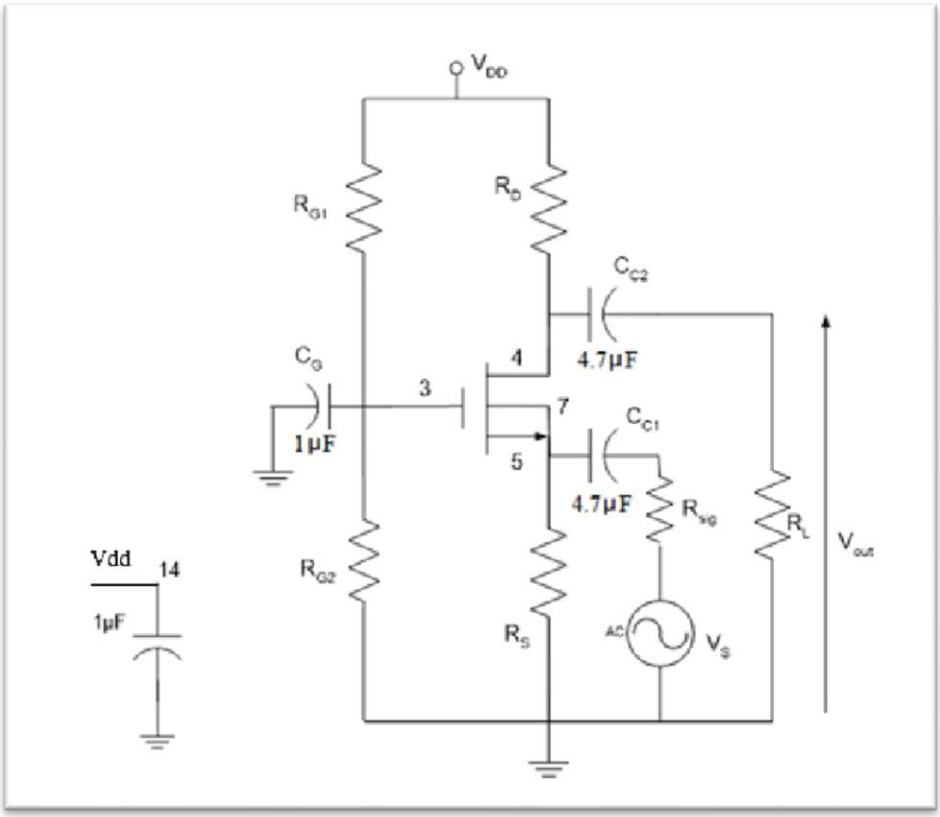


Figure 4 Circuit Diagram for Common-Gate (CG) Amplifier

For section 5.3 this will be focusing on building a stronger understanding of a Common-Gate Amplifier. The measured component values will be the same but in different positions from the previous circuit. Once the circuit is built the ADK will be connected and induce a 100m Vpp with 10kHz signal along with the 5V Vdd. The ADK oscilloscope will then be used to determine the waveforms received from Vs and Vo along with determining the phase shift between the two signals. These waveforms will be then used to measure the Vrms values, and those values will be used to calculate the gain. Once that is complete the circuit will be built in LTSpice along with importing the values for the transistor from the previous lab. Once the circuit is simulated correctly a transient analysis will be performed on the circuit to determine the Vs and Vo signals. For the last part of the simulation an AC analysis will be performed to determine the frequency response for Vo/Vs. From this analysis the following values will be found utilizing the cursors on the graph, max gain, Fh, Fl, and the bandwidth for the circuit. A percentage error calculation will be performed to analyze the physical circuits values against the simulated circuits values.

4.4 Common-Drain (CD) Amplifier

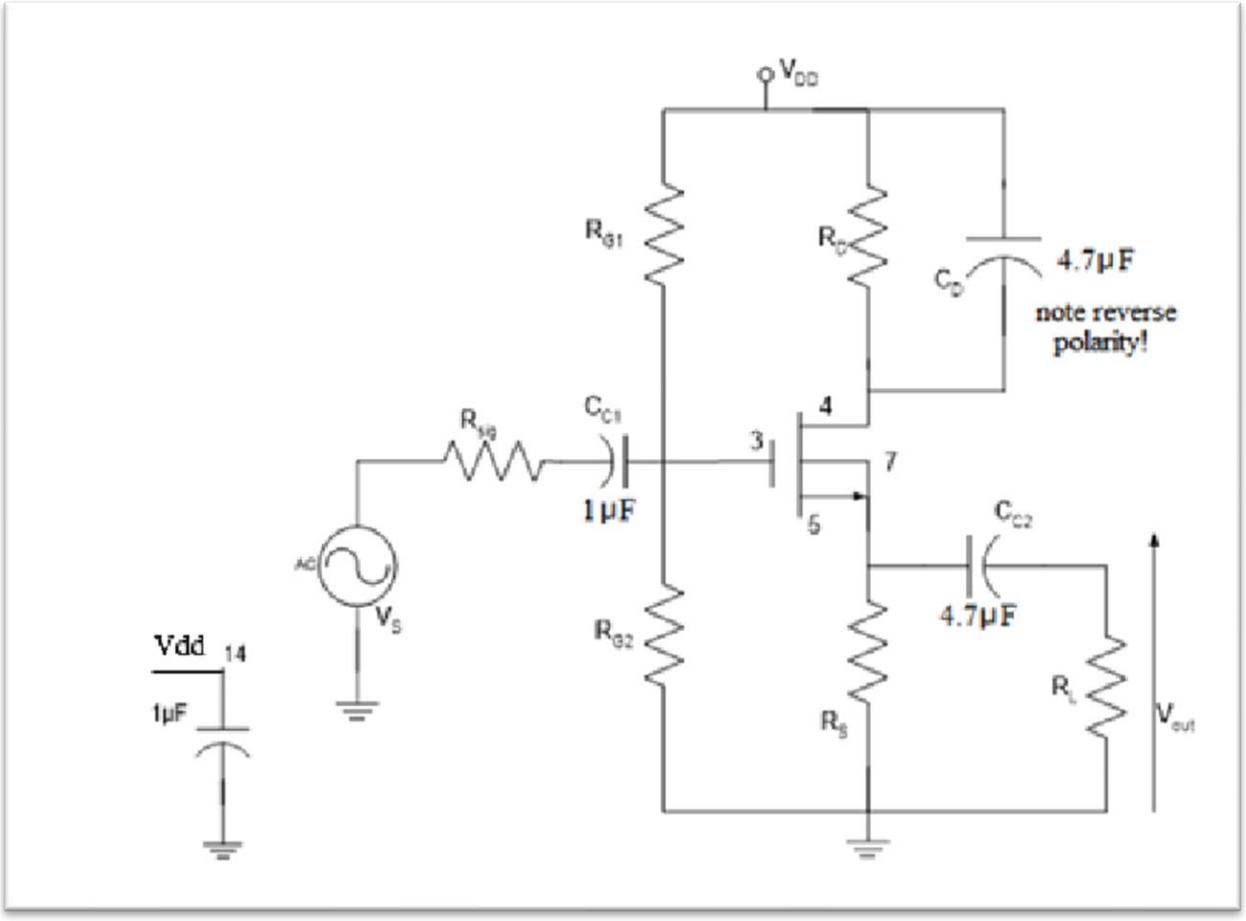


Figure 5 Circuit Diagram for Common-Drain (CD) Amplifier

For section 5.4 this will be focusing on building a stronger understanding of a Common-Drain Amplifier. The measured component values will be the same but in different positions from the previous circuit. Once the circuit is built the ADK will be connected and induce a 0.4 Vpp with 10kHz signal along with the 5V Vdd. The ADK oscilloscope will then be used to determine the waveforms received from Vs and Vo along with determining the phase shift between the two signals. These waveforms will be then used to measure the Vrms values, and those values will be used to calculate the gain. Once that is complete the circuit will be built in LTSpice along with importing the values for the transistor from the previous lab. Once the circuit is simulated correctly a transient analysis will be performed on the circuit to determine the Vs and Vo signals. For the last part of the simulation an AC analysis will be performed to determine the frequency response for Vo/Vs. From this analysis the following values will be found utilizing the cursors on the graph, max gain, Fh, Fl, and the bandwidth for the circuit. A percentage error calculation will be performed to analyze the physical circuits values against the simulated circuits values.

RESULTS

5.1 DC biasing of an NMOS transistor

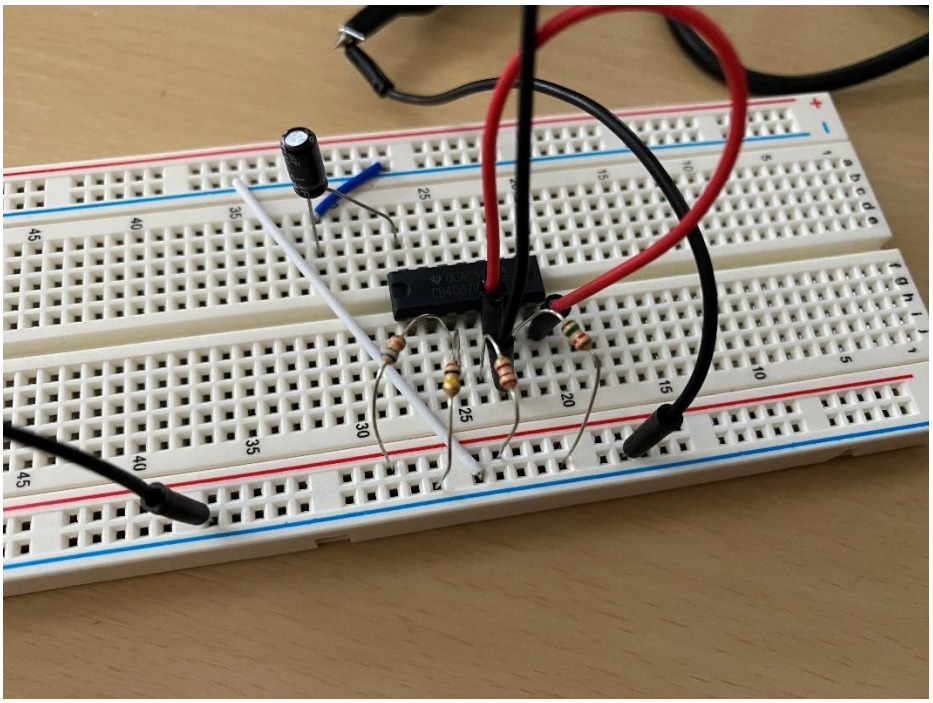


Figure 6 Physical Built Circuit for DC Biasing Circuit

Verified Component Measured Values:
R_{G1}= 67.4kΩ
R_{G2}= 195.9kΩ
R_D= 2174Ω
R_S= 1482Ω
V_{dd} Capacitor = 1.05µF

Measured voltages:
Vds =2.12V
VRD = 1.7V
VRS= 1.16V

****From the Vds above the circuit is biased correctly.**

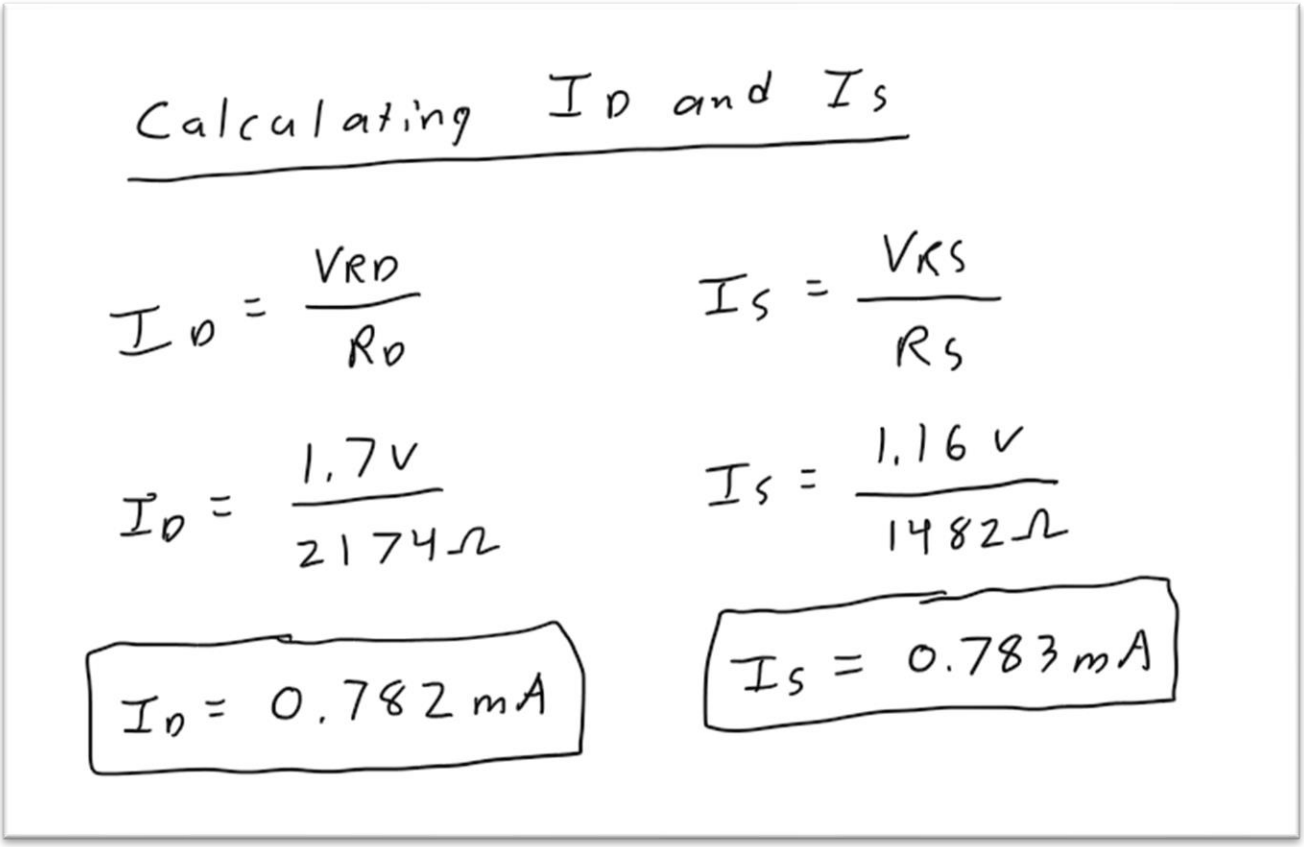


Figure 7 Hand Calculations for DC Biasing Circuit

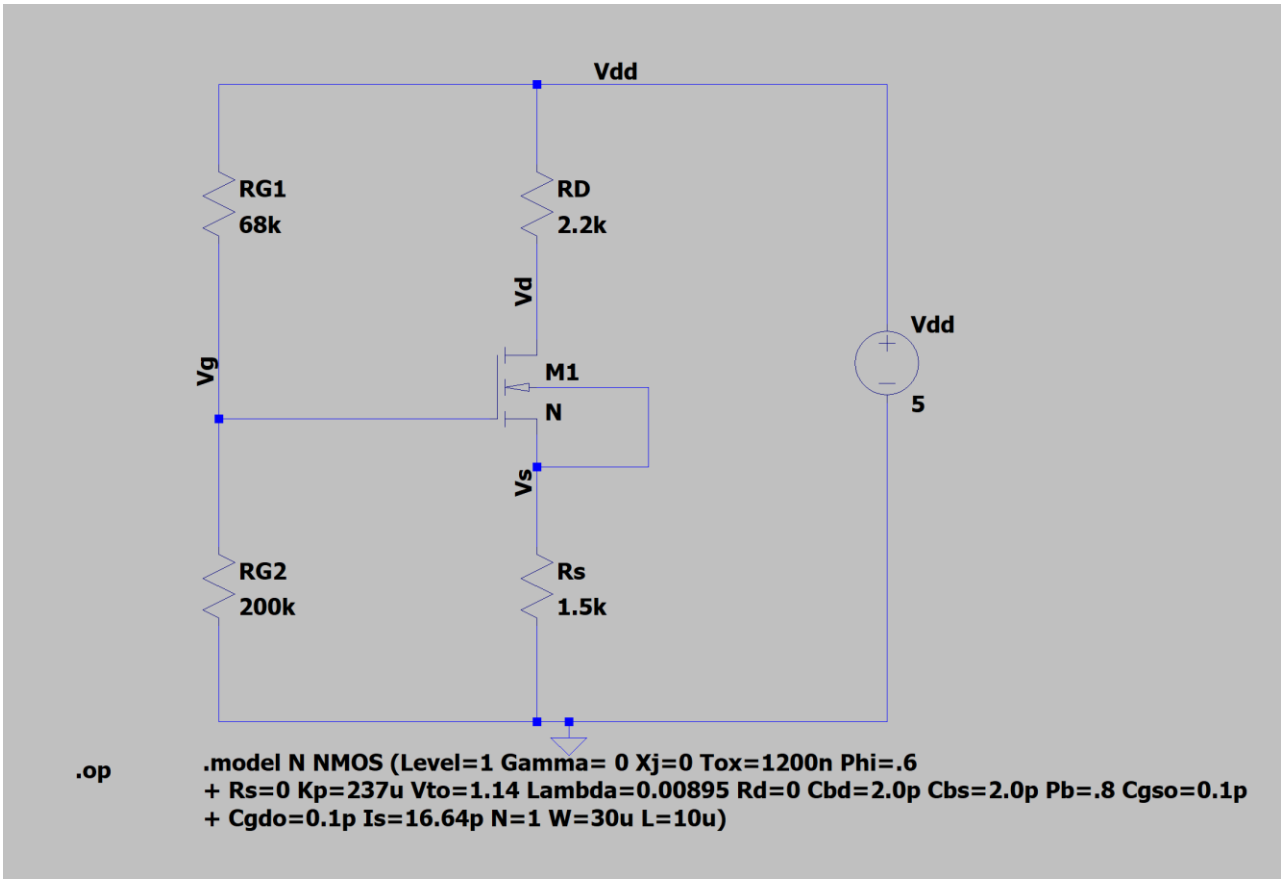


Figure 8 LTSpice Circuit for DC Biasing Circuit

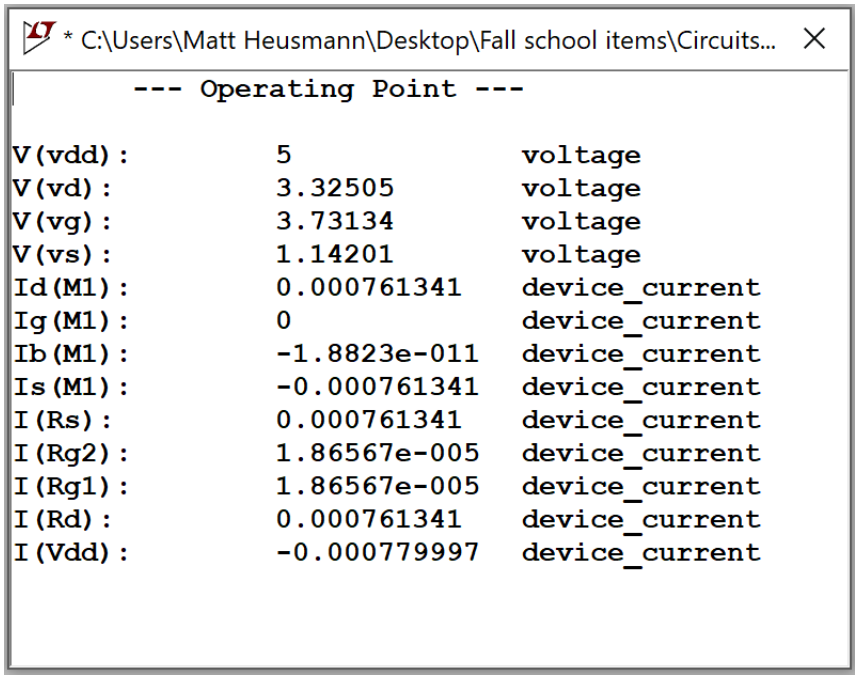


Figure 9 LTSpice Results for DC Biasing Point

$$Percent\ Error = \frac{|Measured - Actual|}{Measured} * 100$$

Table 1 Precent Error Calculations for DC Biasing Circuit

	Measured	**Simulated LTSpice**	**Percent Error**
$\mathbf{V_{DS}}$	2.12V	2.18V	2.75%
$\mathbf{V_{RD}}$	1.7V	1.68V	1.2%
$\mathbf{V_{RS}}$	1.16V	1.14V	1.7%
$\mathbf{i_D}$	0.782mA	0.761mA	2.76%
$\mathbf{i_S}$	0.783mA	0.761mA	2.9%

5.2 Common-Source (CS) Amplifier

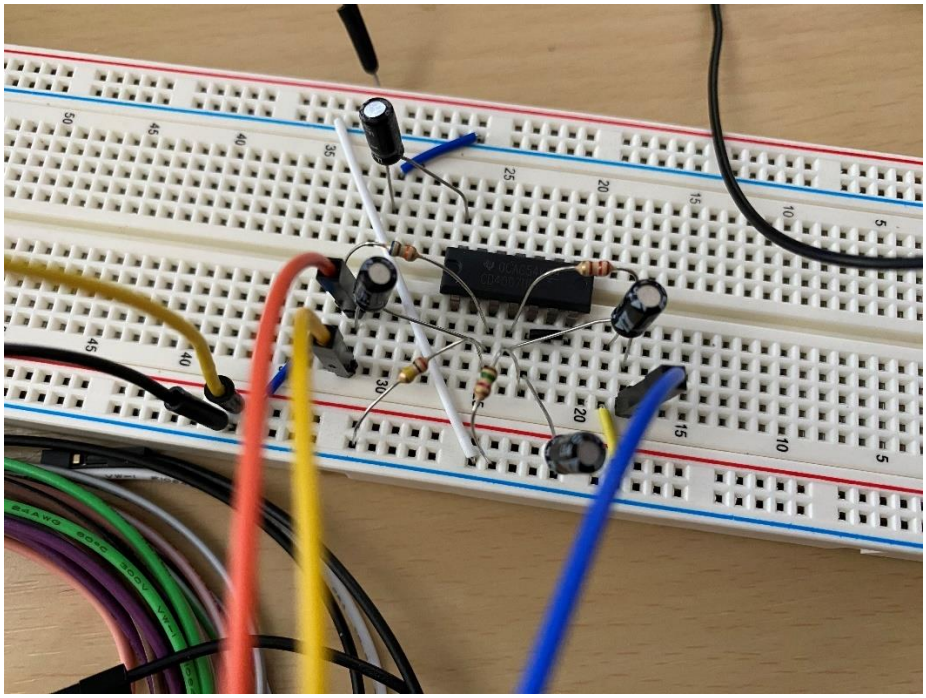


Figure 10 Physical Built Circuit for Common-Source (CS) Amplifier

Verified Component Measured Values:
R_{G1}= 67.4kΩ
R_{G2}= 195.9kΩ
R_D= 2174Ω
R_S= 1482Ω
V_{dd} Capacitor = 1.05µF
C_{C1} = 1.1µF
C_{C2} = 4.6 µF
C_S = 4.8 µF

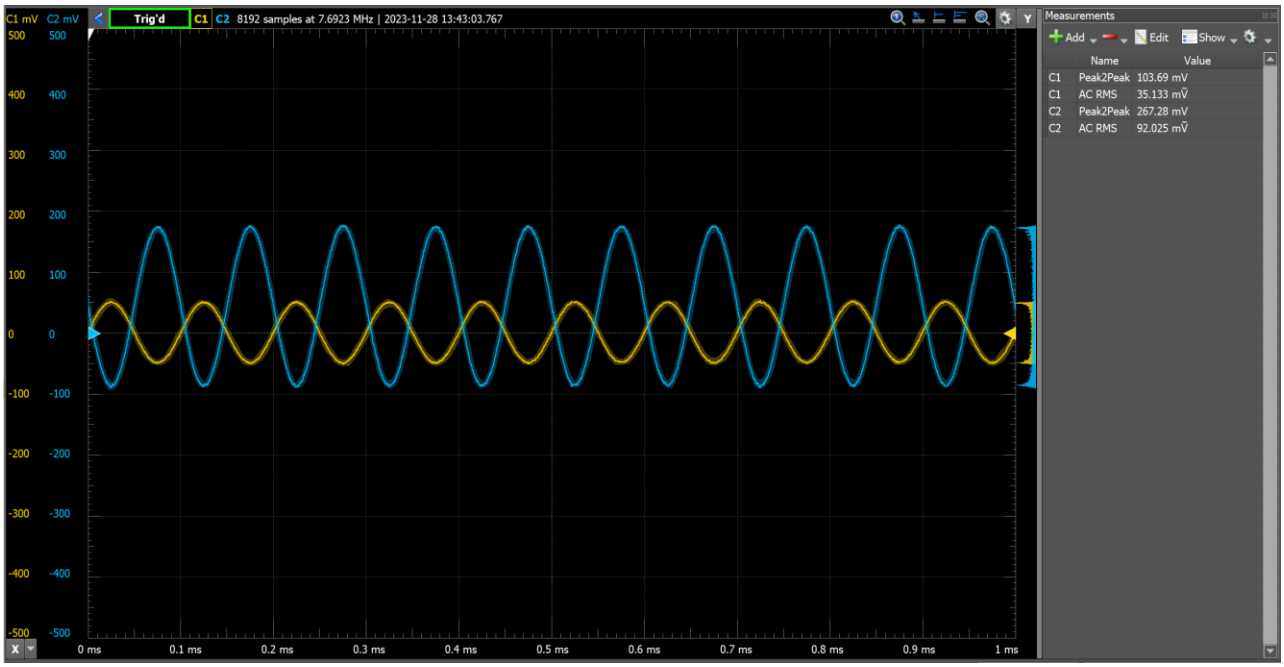


Figure 11 Waveforms of Common-Source Amplifier Vs (yellow) Vo (Blue)

Measured Values:
Vspp = 103.69mV
Vopp = 267.28mV
Vsrms = 35.133mV
Vorms = 92.025mV

****It can be seen from waveforms that the phase shift is -180 degrees.**

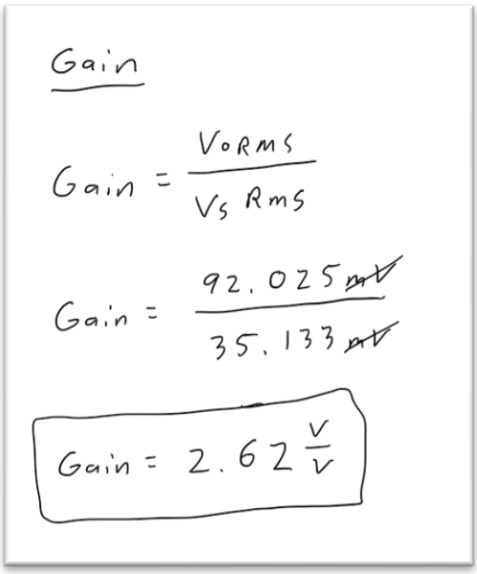


Figure 12 Hand Calculated Gain for Waveform Results

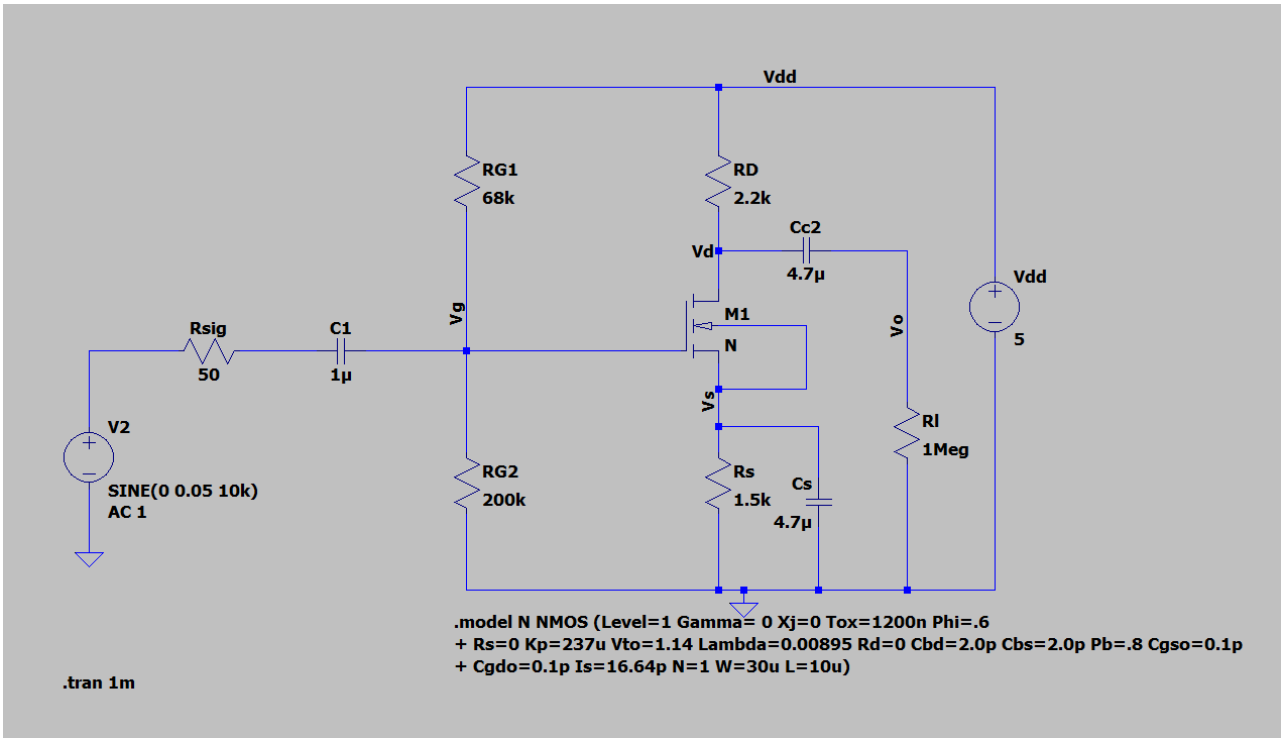


Figure 13 LTSpice Circuit Diagram for Common Source Amplifier

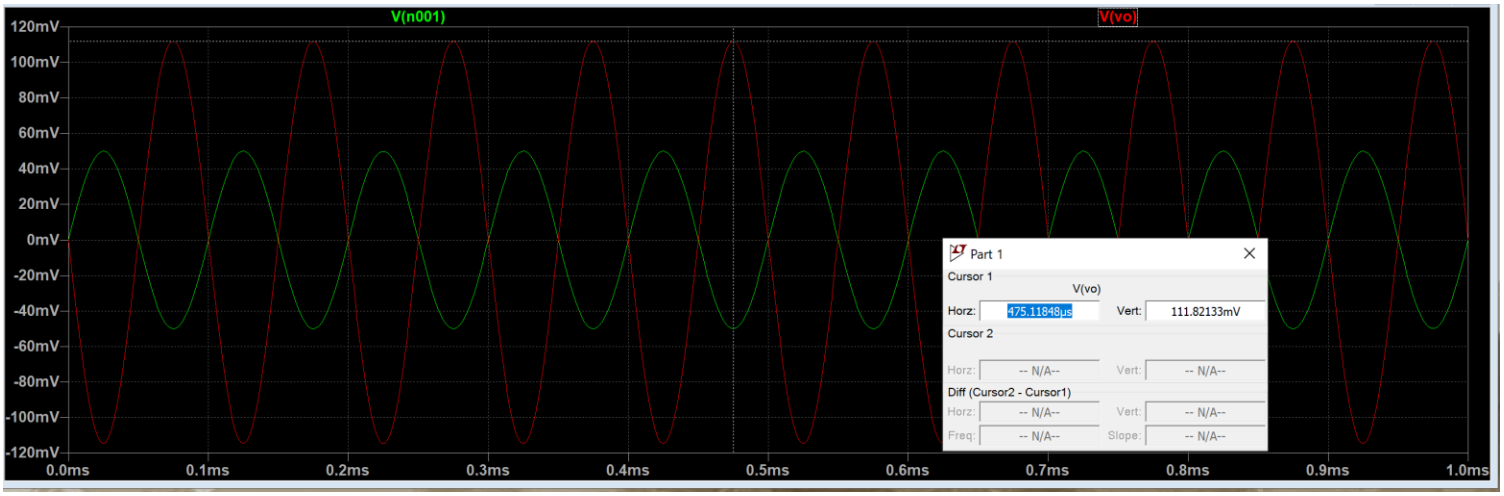


Figure 14 LTSpice Transient Analysis for Common Source Amplifier

LTSpice Transient Analysis Results
Vspp = 100mV
Vopp = 223.64mV

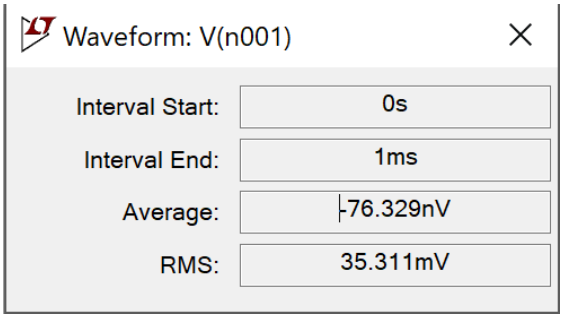


Figure 16 LTSpice Vsrms Common Source Amplifier

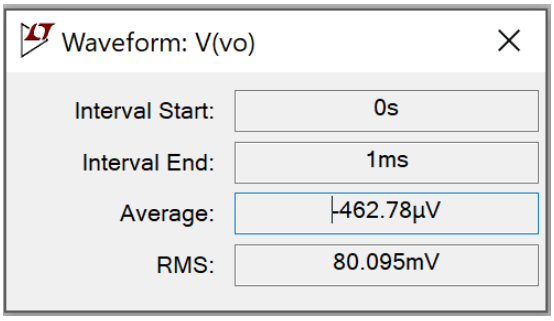


Figure 15 LTSpice Vorms Common Source Amplifier

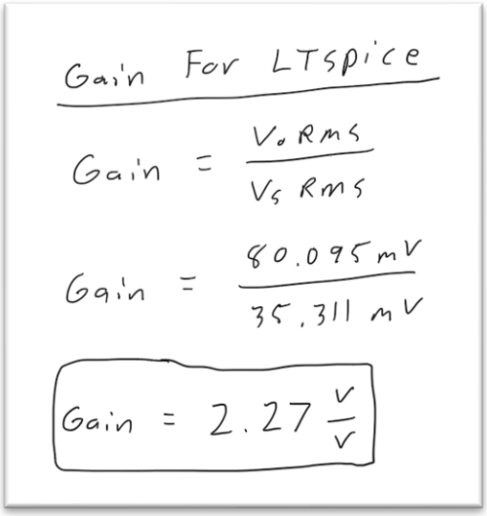


Figure 17 Hand Calculations for LTSpice Gain

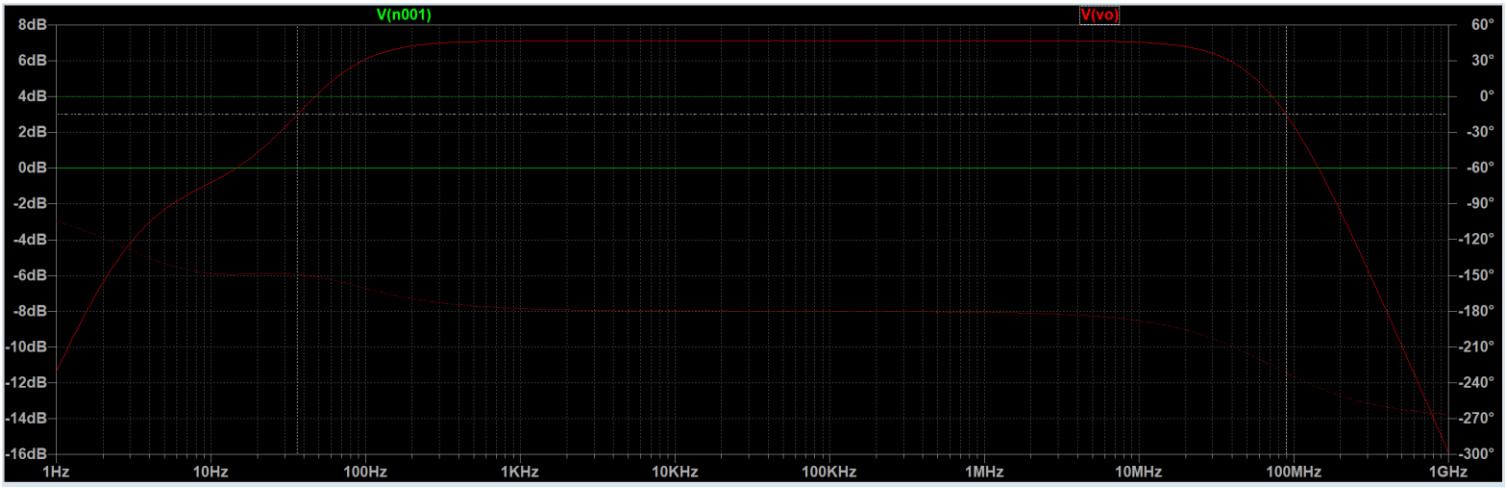


Figure 18 LTSpice AC Analysis for Common Source Amplifier

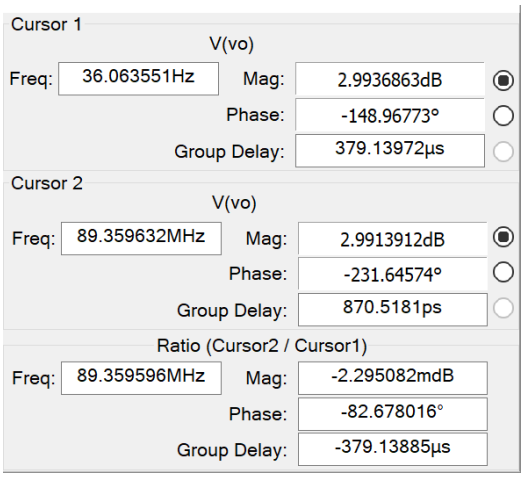


Figure 20 Frequency Response Results for Common Source Amp

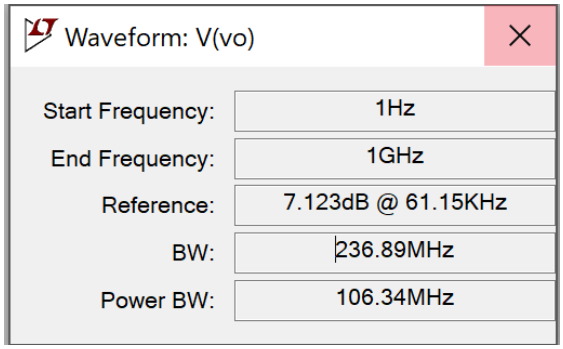


Figure 19 Frequency Response Results for Common Source Amp

AC Analysis Frequency Response Results
Maximum gain = 7.123 dB
fL = 36.064 Hz
fH = 89.359 MHz
BW = 89.359 MHz

Table 2 Precent Error Calculations for Common Source Amplifier

	Measured	Simulated LTSpice	Percent Error
Vs PP	103.69 mV	100 mV	3.6%
Vo PP	267.28 mV	223.64 mV	19.5%
Vs RMS	35.133 mV	35.311 mV	0.5%
Vo RMS	92.025 mV	80.095 mV	14.9%
Gain	2.62(V/V)	2.27(V/V)	15.4%

5.3 Common-Gate (CG) Amplifier

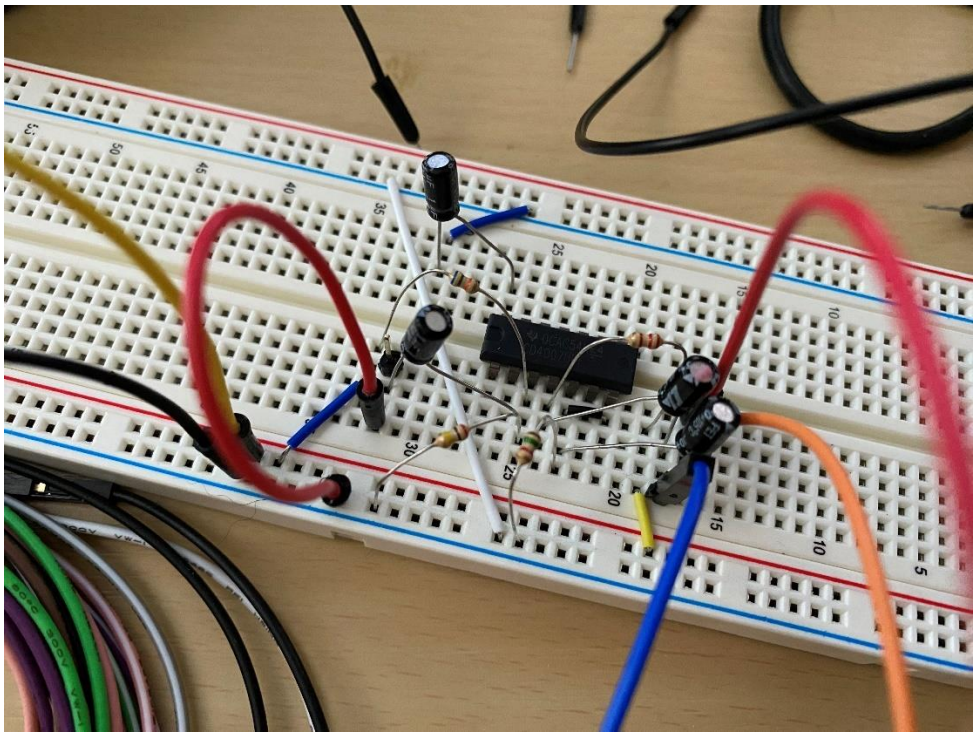


Figure 21 Physical Build for Common-Gate (CG) Amplifier

Verified Component Measured Values:
R_{G1}= 67.4kΩ
R_{G2}= 195.9kΩ
R_D= 2174Ω
R_S= 1482Ω
V_{dd} Capacitor = 1.05µF
C_{C1} = 4.8µF
C_{C2} = 4.6 µF
C_G = 1.1 µF

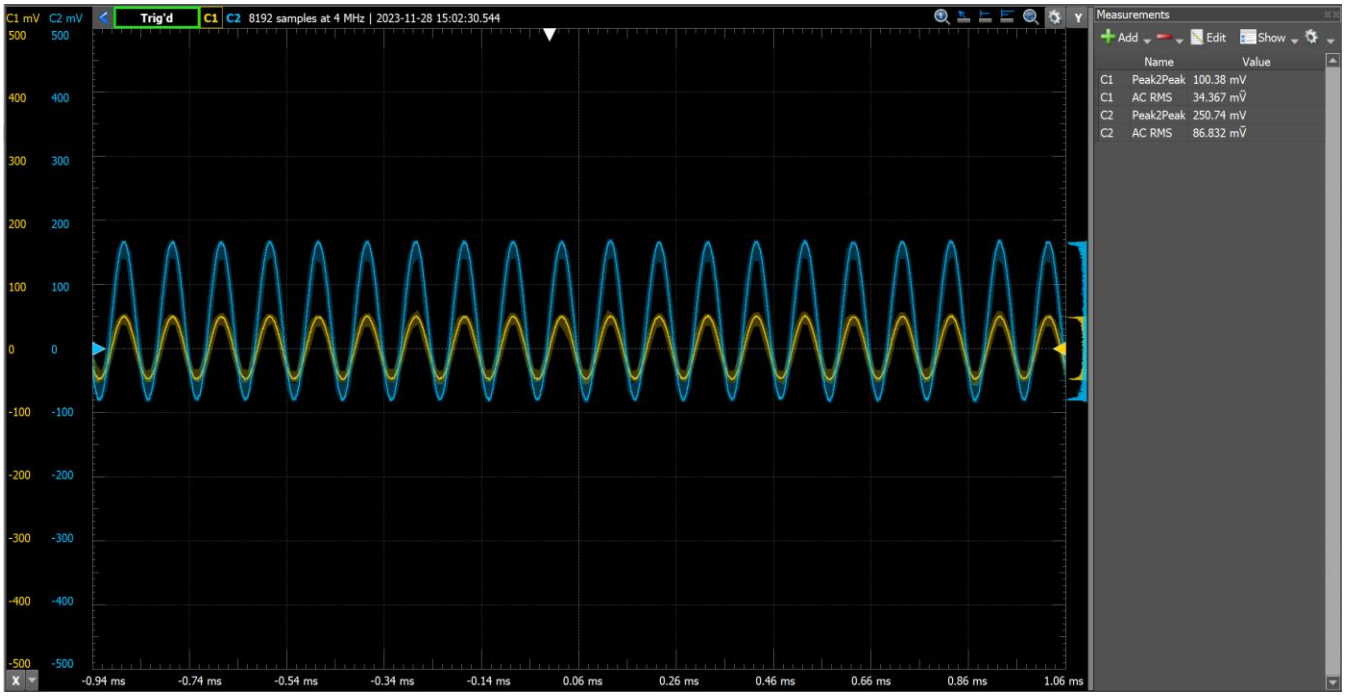


Figure 22 Waveforms of Common-Gate Amplifier Vs (yellow) Vo (Blue)

Measured Values:
Vspp = 100.38mV
Vopp = 250.74mV
Vsrms = 34.367mV
Vorms = 86.832mV

****It can be seen from waveforms that the phase shift is 0 degrees, they are in phase.**

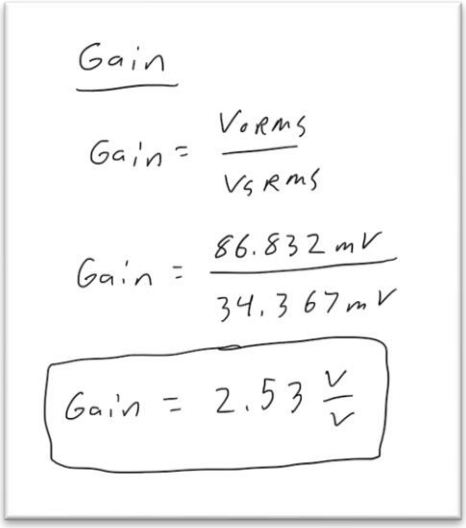


Figure 23 Hand Calculated Gain for Waveform Results

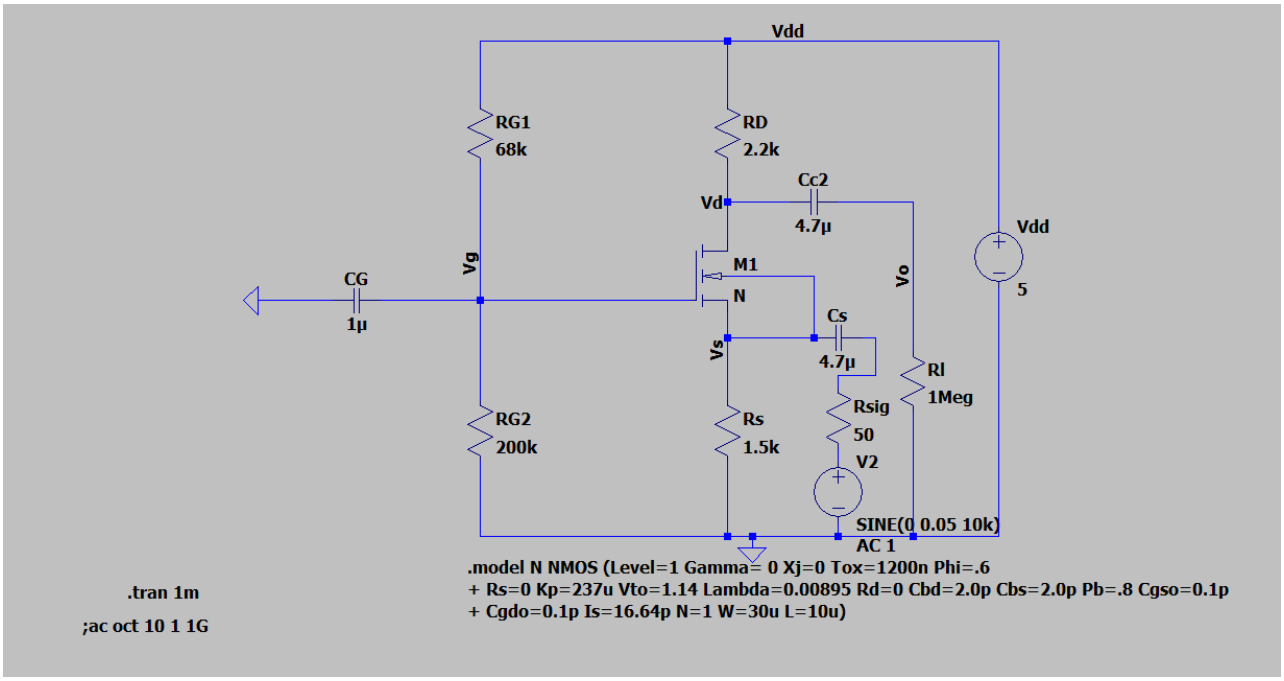


Figure 24 LTSpice Circuit Diagram for Common Gate Amplifier

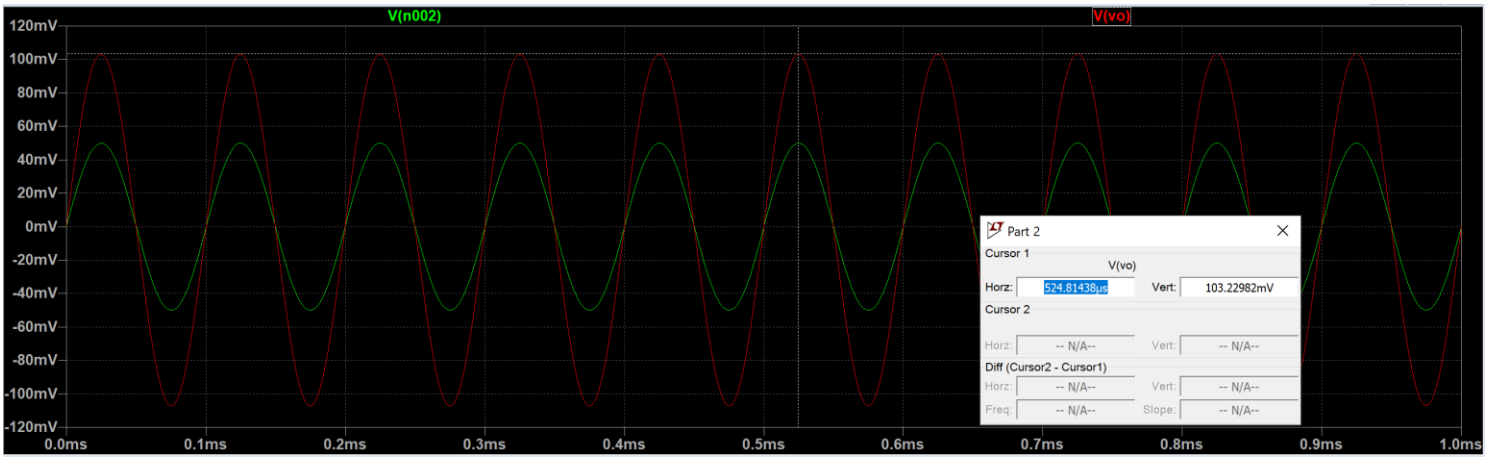


Figure 25 LTSpice Transient Analysis for Common Gate Amplifier

LTSpice Transient Analysis Results
Vspp = 100mV
Vopp = 206.46mV

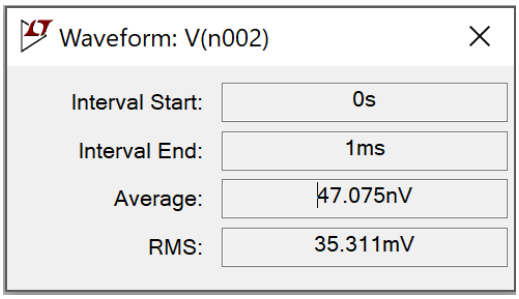


Figure 27 LTSpice Vsrms Common Gate Amplifier

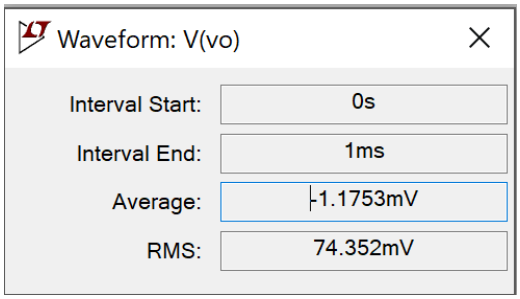


Figure 26 LTSpice Vorms Common Gate Amplifier

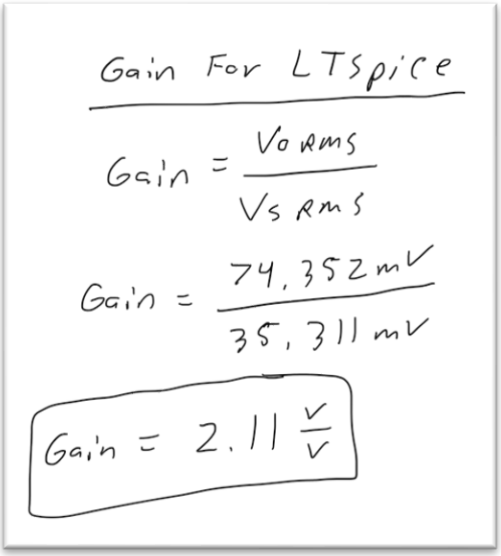


Figure 28 Hand Calculations for LTSpice Gain

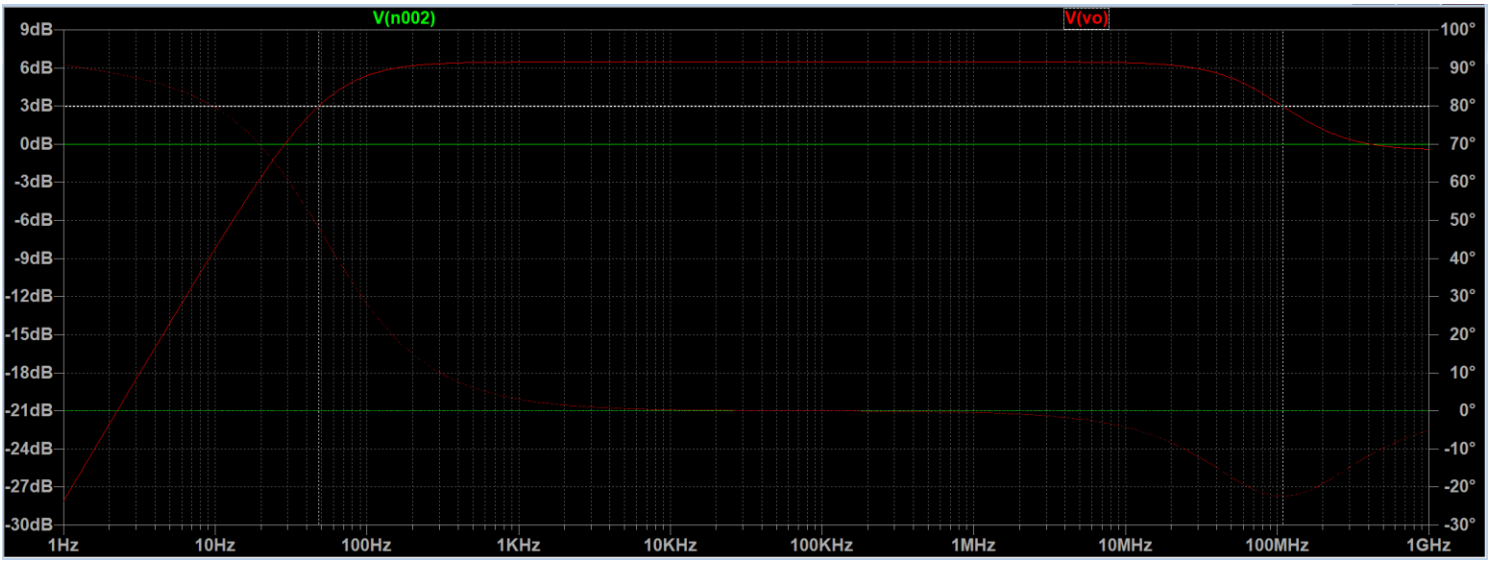


Figure 29 LTSpice AC Analysis for Common Gate Amplifier

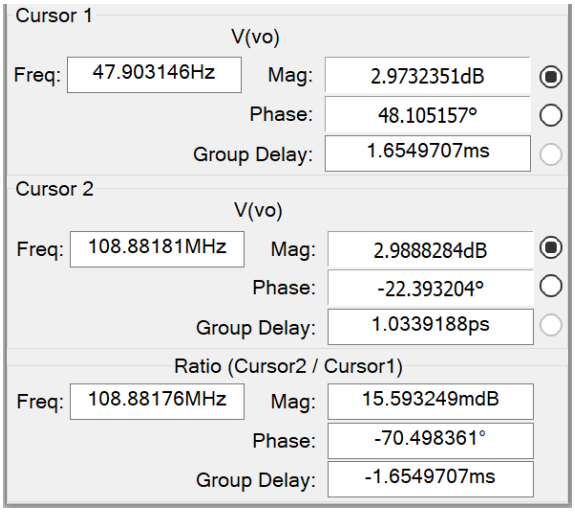


Figure 31 Frequency Response Results for Common Gate Amp

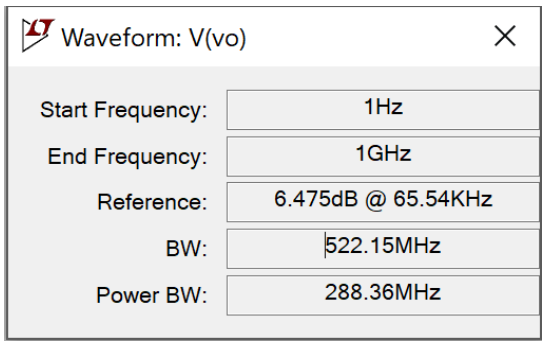


Figure 30 Frequency Response Results for Common Gate Amp

AC Analysis Frequency Response Results
Maximum gain = 6.475 dB
fL = 47.90 Hz
fH = 108.88 MHz
BW = 108.88 MHz

Table 3 Precent Error Calculations for Common Gate Amplifier

	Measured	Simulated LTSpice	Percent Error
Vs PP	100.38 mV	100 mV	0.38%
Vo PP	250.74 mV	206.46 mV	21.4%
Vs RMS	34.367 mV	35.311 mV	2.7%
Vo RMS	86.832 mV	74.352 mV	16.8%
Gain	2.53 (V/V)	2.11 (V/V)	19.9%

5.4 Common-Drain (CD) Amplifier

Verified Component Measured Values:
R_{G1}= 67.4kΩ
R_{G2}= 195.9kΩ
R_D= 2174Ω
R_S= 1482Ω
V_{dd} Capacitor = 1.05µF
C_{C2} = 4.8µF
C_D = 4.6 µF
C_{C1} = 1.1 µF

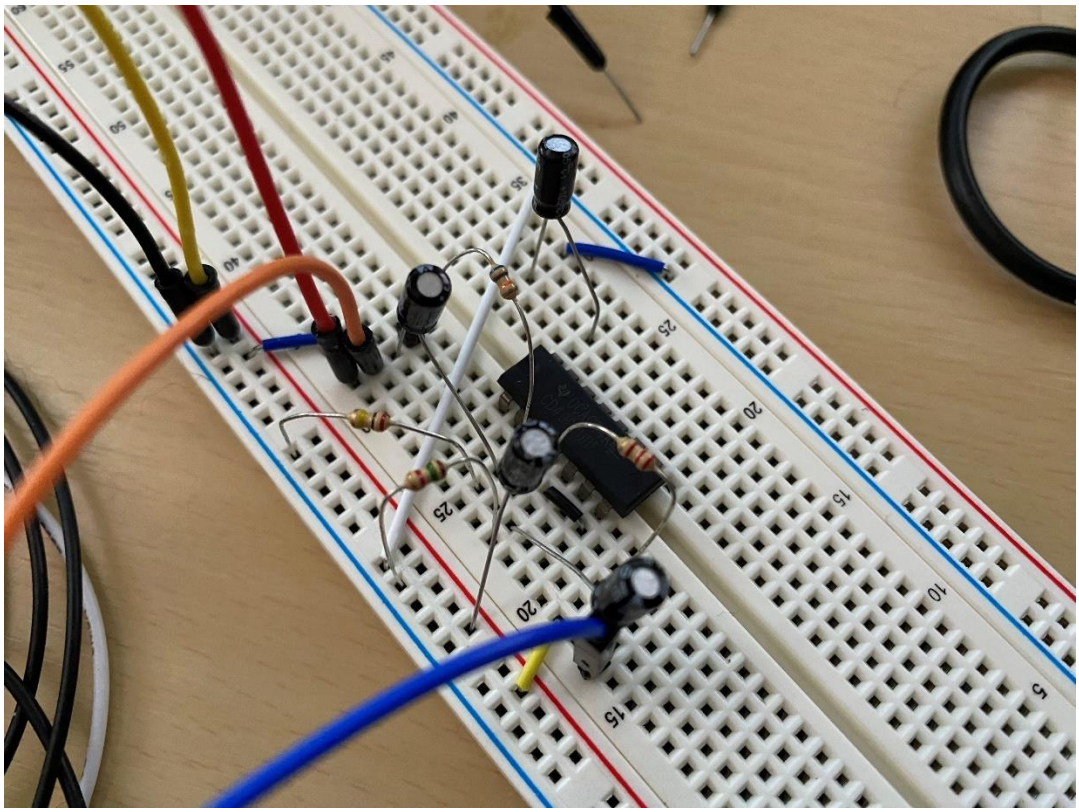


Figure 32 Physical Build for Common-Drain (CD) Amplifier

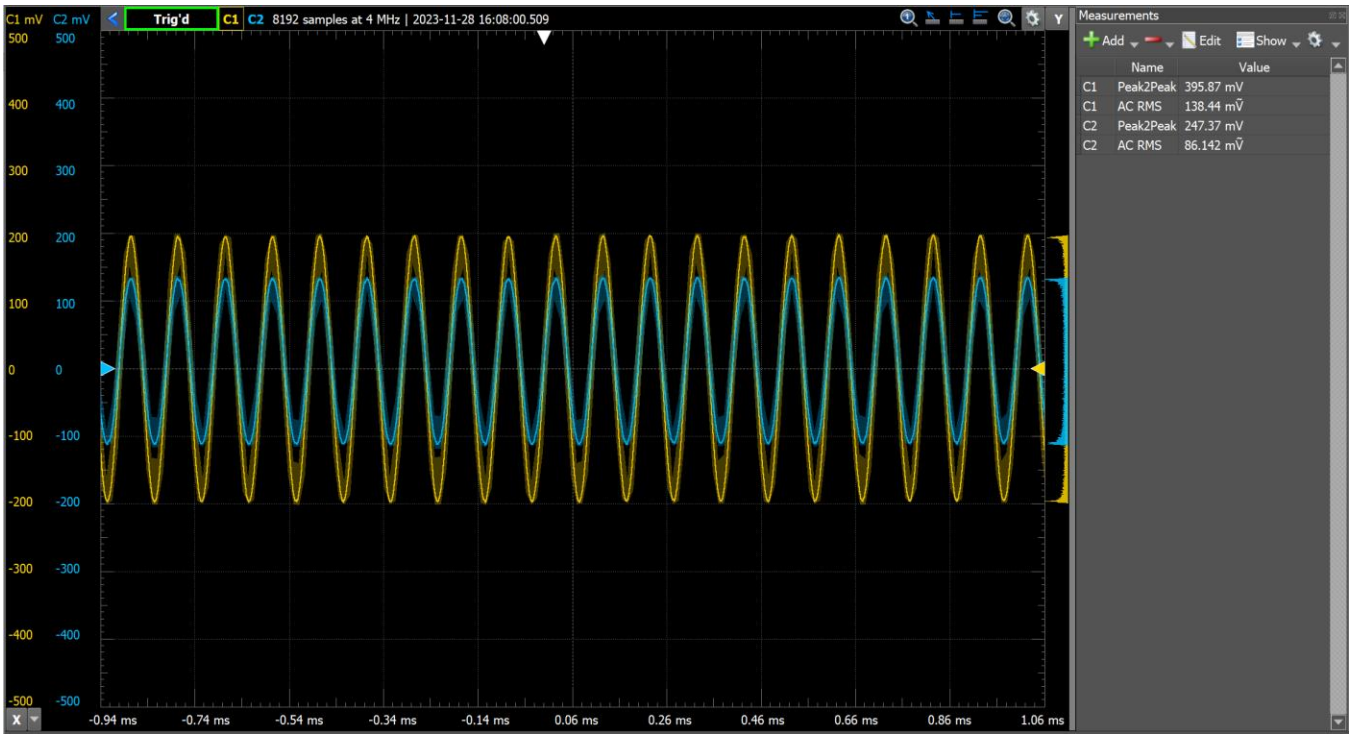


Figure 33 Waveforms of Common-Drain Amplifier Vs (yellow) Vo (Blue)

Measured Values:
Vspp = 395.87mV
Vopp = 247.37mV
Vsrms = 138.44mV
Vorms = 86.142mV

****It can be seen from waveforms that the phase shift is 0 degrees, they are in phase.**

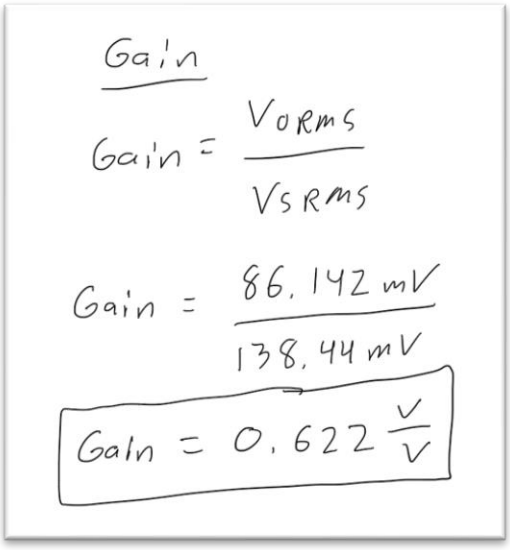


Figure 34 Hand Calculated Gain for Waveform Results

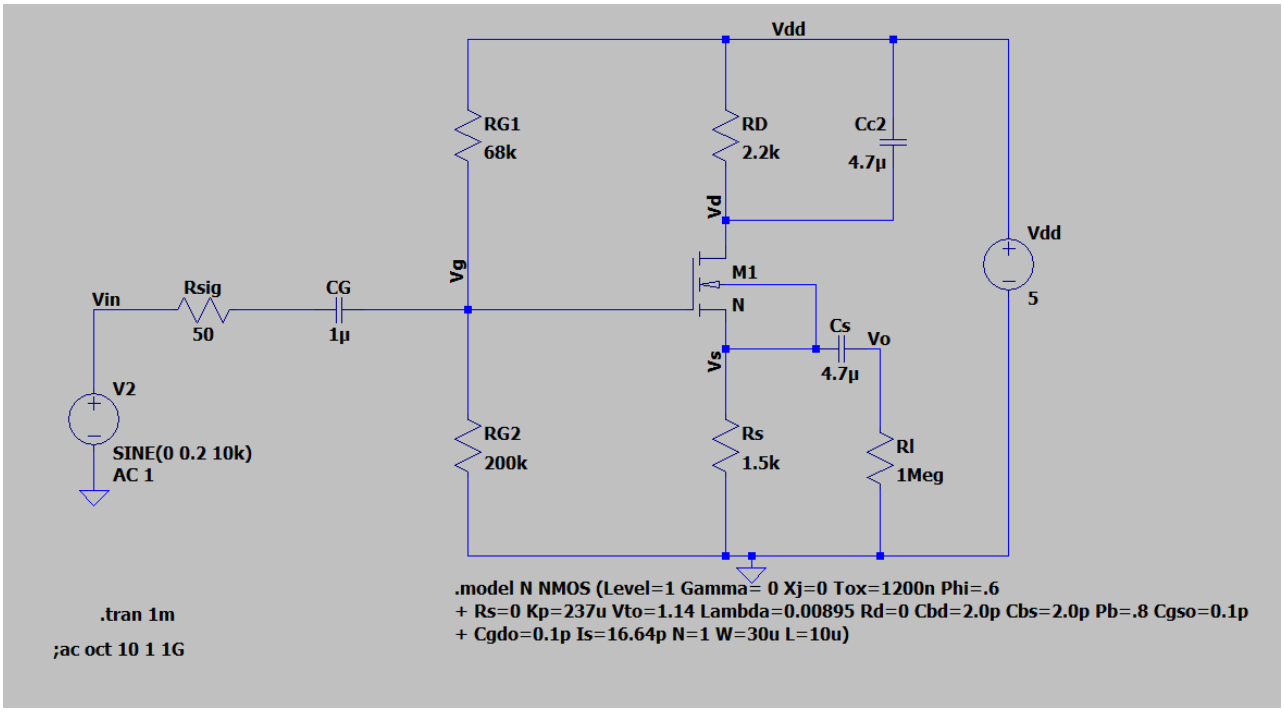


Figure 35 LTSpice Circuit Diagram for Common Drain Amplifier

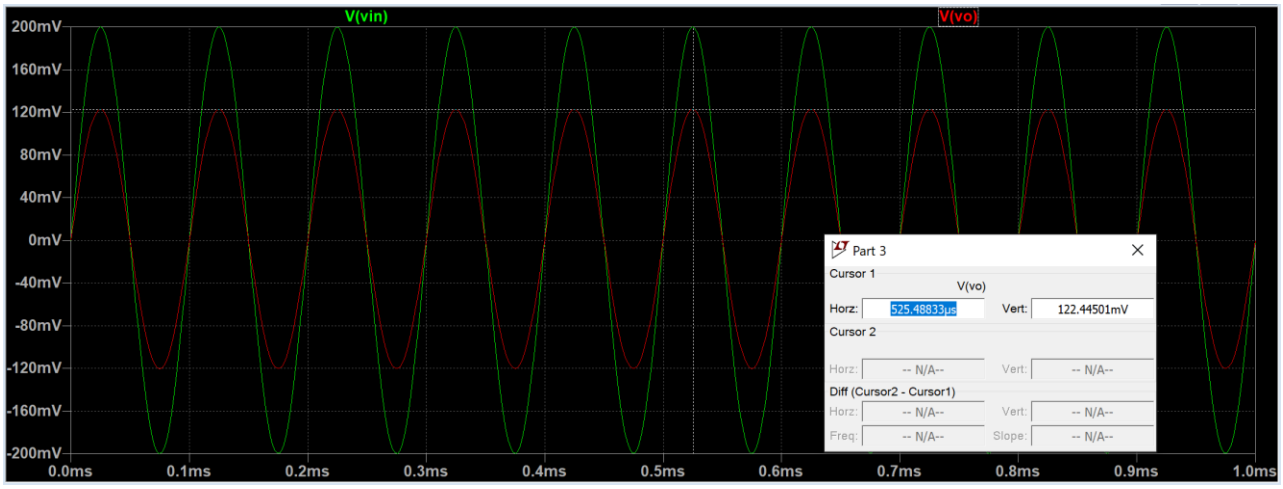


Figure 36 LTSpice Transient Analysis for Common Drain Amplifier

LTSpice Transient Analysis Results
Vspp = 400mV
Vopp = 244.89mV

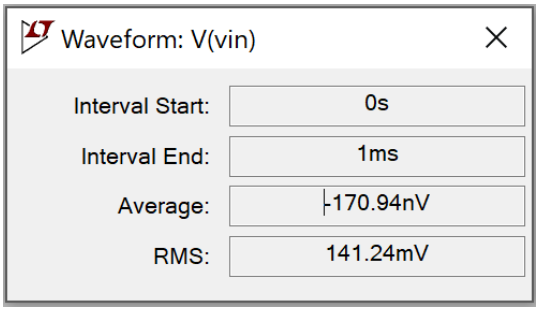


Figure 38 LTSpice Vsrms Common Drain Amplifier

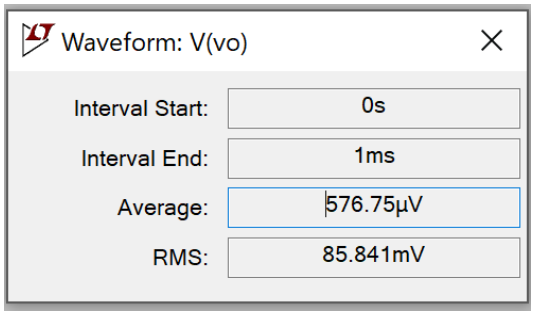


Figure 37 LTSpice Vorms Common Drain Amplifier

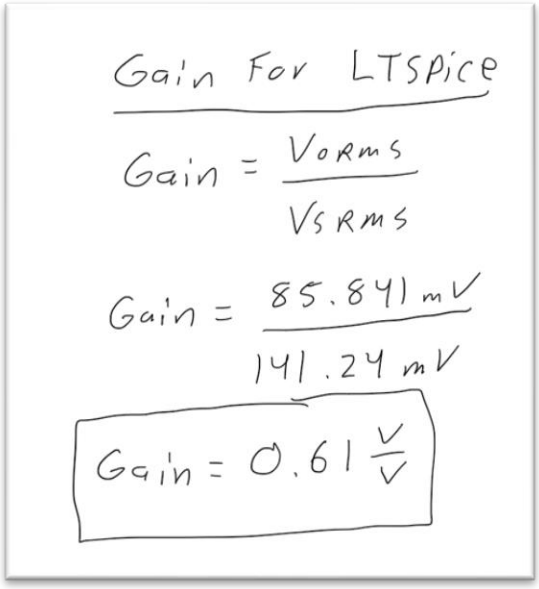
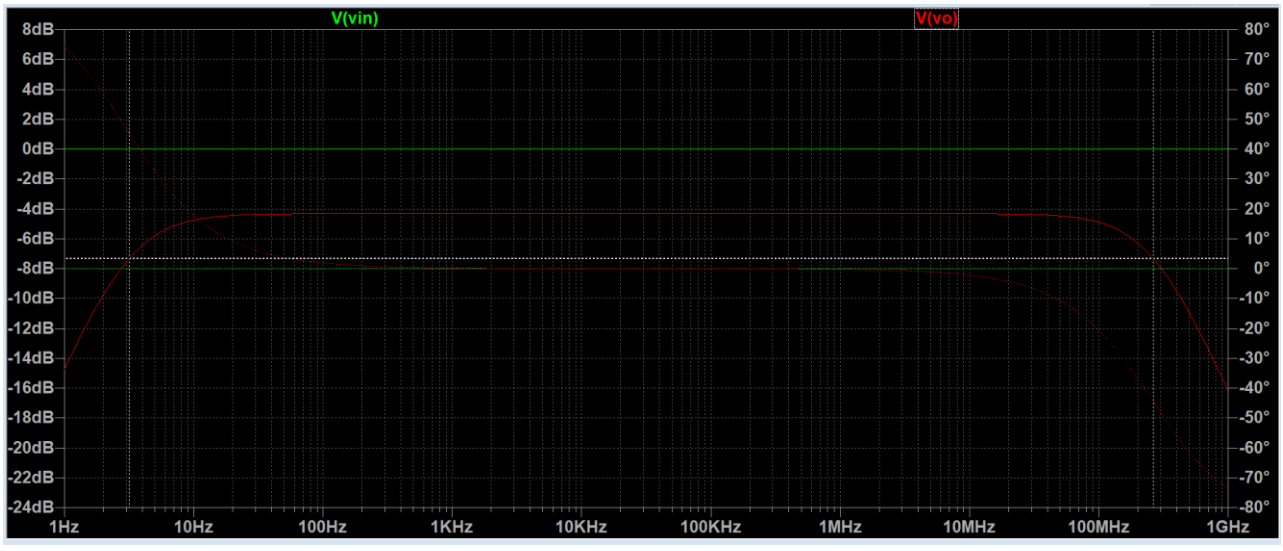


Figure 39 Hand Calculations for LTSpice Gain



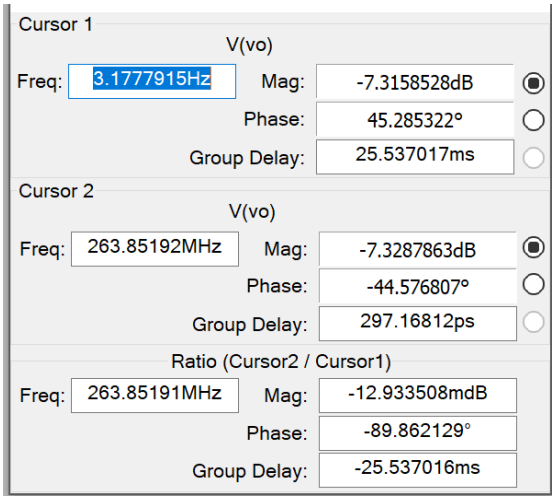


Figure 41 Frequency Response Results for Common Drain Amp

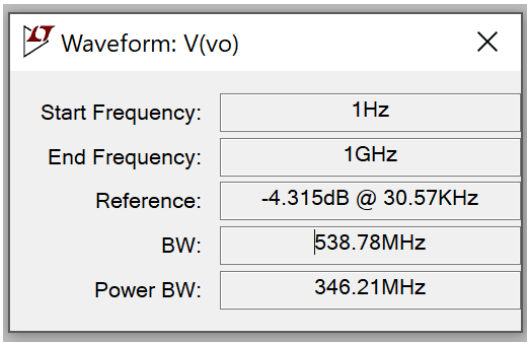


Figure 40 Frequency Response Results for Common Drain Amp

AC Analysis Frequency Response Results
Maximum gain = -4.315 dB
fL = 3.178 Hz
fH = 263.85 MHz
BW = 263.85 MHz

Table 4 Precent Error Calculations for Common Drain Amplifier

	Measured	Simulated LTSpice	Percent Error
Vs PP	395.87 mV	400 mV	1.0%
Vo PP	247.37 mV	244.89 mV	1.0%
Vs RMS	138.44 mV	141.24 mV	1.9%
Vo RMS	86.142 mV	85.84 mV	0.4%
Gain	0.622 (V/V)	0.61 (V/V)	1.9%

CONCLUSION

This lab's main purpose was to allow the student to get a deeper understanding of how NMOS transistors are used when utilizing Common-Source, Common-Gate, and Common Drain circuits.

For the first section 5.1, this sections' main focus was on analyzing the DC biasing of an NMOS transistor. After the circuit was built a reading of 2.12V was taken for Vds which was within tolerance to determine if the circuit was built correctly. Now having the values of Vrd = 1.7V and Vrs = 1.16V, hand calculations were completed to determine the Id and Is of the bias circuit. Those results came out to be Id = 0.782mA and Is = 0.783mA. Having the hand calculations completed the circuit was built in LTSpice to determine the simulated values the circuit should have. At the end of this section percentage error calculations were run to compare the physical circuit and simulated. With all the error percents coming out to be below 3% it is safe to assume that everything was done correctly.

As for the second section 5.2, the lab now starts to analyze each individual circuit. This section was focused on the common-source amplifier. After the circuit was built the ADK was utilized to view the input and output waveforms. From this analysis it was determined that the common source amplifier has a 180-degree phase change from its input to output. Also, from the figures taken of the waveforms the signals should overlap perfectly over each other but inverse due to the phase change. However, this was not the case in the waveforms. The circuit was rebuilt over three times and all the measurements were taken multiple times. It seems that it was in fact built correctly but just something weird was happening with an offset. Having the waveform measurements, the hand calculation was taken to determine the gain. Similarly, to the first, the circuit was simulated, and a transient analysis and AC analysis were performed to find the required values. Once all this was completed percentage error calculations were done and this is where large discrepancies appeared. There were some percentage errors up around 19%. Since the circuit was in fact correct, some of the errors could be due to the offset but it seems most of this error has come from the data input from the previous lab. When finding the parameters some of the values were rounded off and inputted into the transistor parameters. This rounding can be the reason for the large percentage errors occurring in the results section. Even with some large errors it can still be seen that the circuit was in fact analyzed correctly.

As for the second section 5.3, this section was focused on the common-gate amplifier. After the circuit was built, the ADK was utilized to view the input and output waveforms. From this analysis it was determined that the common gate amplifier does not have a phase change like the previous circuit. Having the waveform measurements, the hand calculations were calculated to determine the gain. Similarly, to the first and second circuit it was simulated, and a transient analysis and AC analysis were performed to find the required values. Once again, a fairly large percentage errors up around 19% were present but not for all values. Some were very close to the measured values from the ADK. Since the circuit was in fact correct the errors are best explained by the previous section's explanation. Along with also mentioning that when taking a screen shot of the ADK measurements those values are always fluctuating so when taking a still snapshot it could have been a farther off value then what the average could be. Even with some large errors it can still be seen that the circuit was in fact analyzed

correctly.

Lastly section 5.4, This section was focused on the common-drain amplifier. After the circuit was built, the ADK was utilized to view the input and output waveforms. From this analysis it was determined that the common drain amplifier does not have a phase and is similar to section 5.3. Having the waveform measurements, the hand calculations were calculated to determine the gain. Similarly, to all the previous sections the circuit was simulated, and a transient analysis and AC analysis were performed to find the required values. To a nice surprise these sections readings were almost spot on from the physical circuit to the simulated circuit. With the largest percent error coming to be around 2%. This gave reassurance that this circuit was in fact built and measured correctly.

This lab was fairly enjoyable. With this further transistor knowledge, it will be much easier to understand each of these circuits and their practical application of them when the time is needed for them.

POST LAB QUESTIONS

1. Use LTSpice to observe and explain (where necessary) the outcomes of the followings:

a. Doubling the size of the NMOS transistor in the DC biasing circuit, shown in Fig. 5.3.

From analisis of utalizing LTSpice it seems that when (W/L) is doulbled the current Id is also doubled. Along with the transcunducatnce paramewters changing.

b. Having a load resistor RL=3kΩ instead of 1MΩ in the CS, CG, and CD amplifiers shown in Figs. 5.4, 5.5 and 5.6.

Common-Source Amplifier with Rl = 3kΩ

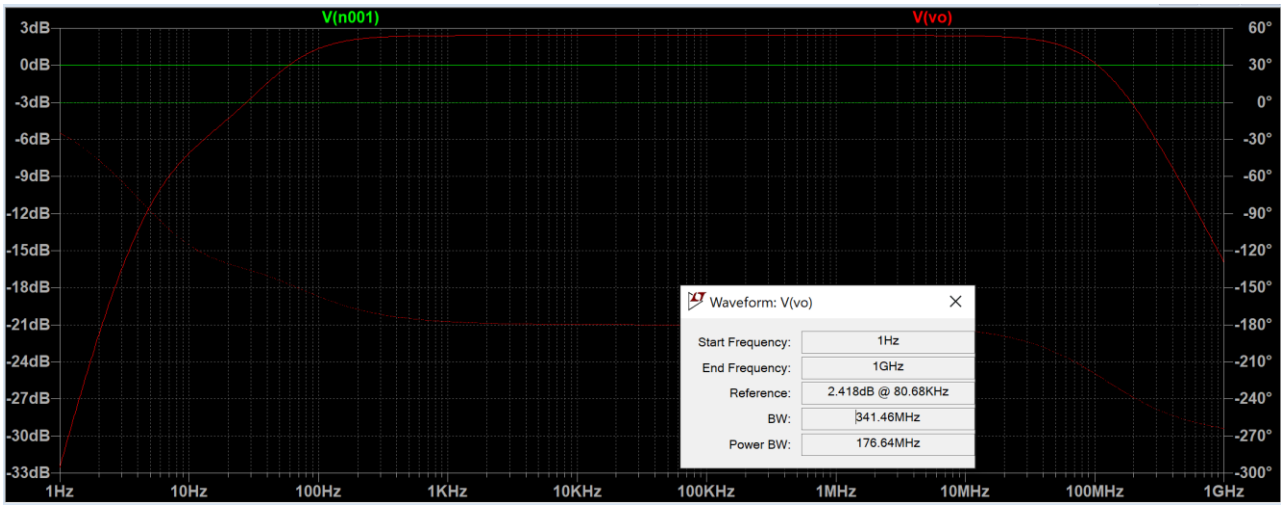


Figure 42 Common-Source Amplifier with Rl = 3kΩ

Common-Gate Amplifier with Rl = 3kΩ

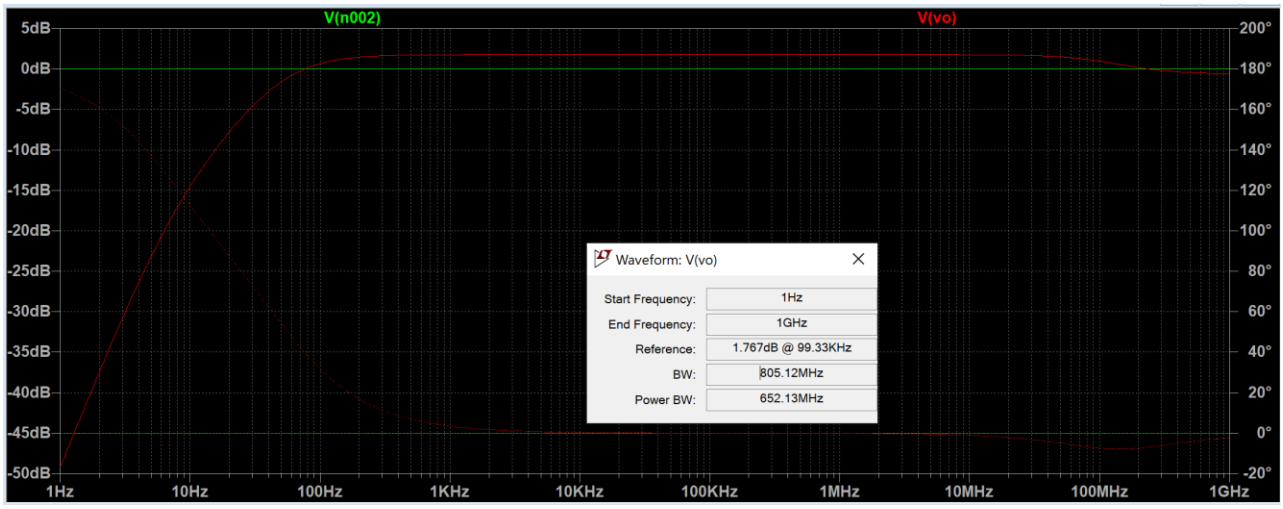


Figure 43 Common-Gate Amplifier with Rl = 3kΩ

Common-Drain Amplifier with Rl = 3kΩ

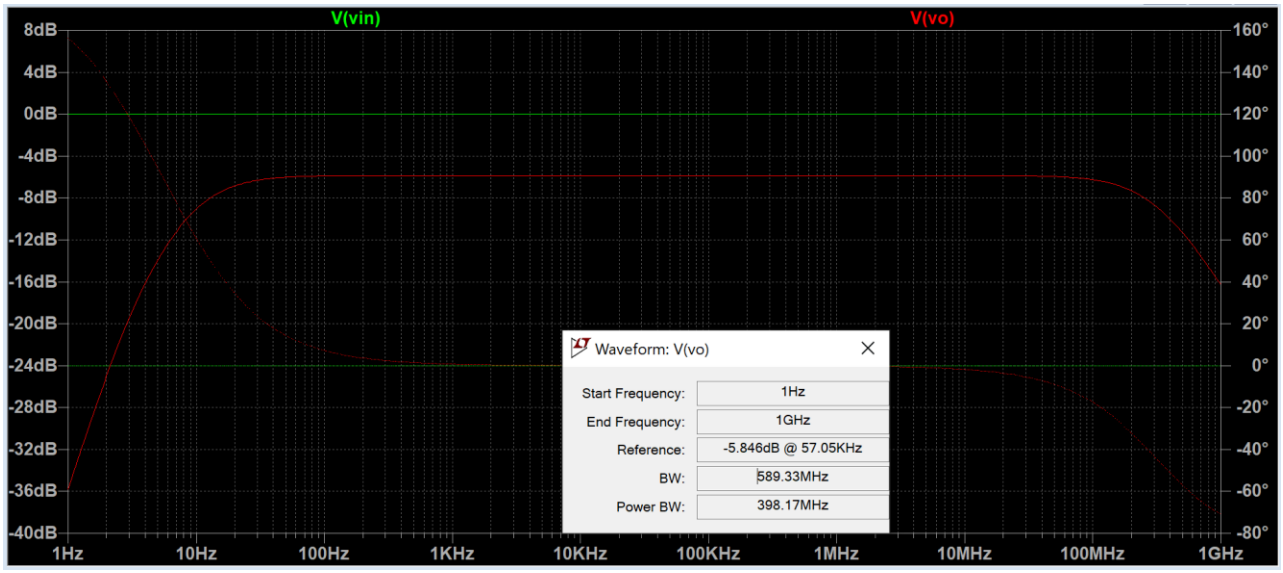


Figure 44 Common-Drain Amplifier with Rl = 3kΩ

When comparing these figures above with the original results in the lab it can be seen that the maximum gain has decreased across the board on all of them. Due to the decreased load on the circuit the Vo value will decrease thus resulting in an overall decrease in gain for each of the three circuits.

c. Placing capacitors, CC1, CC2, and CS, as 1000μF in the CS amplifier shown in Fig. 5.4, instead of 1μF.

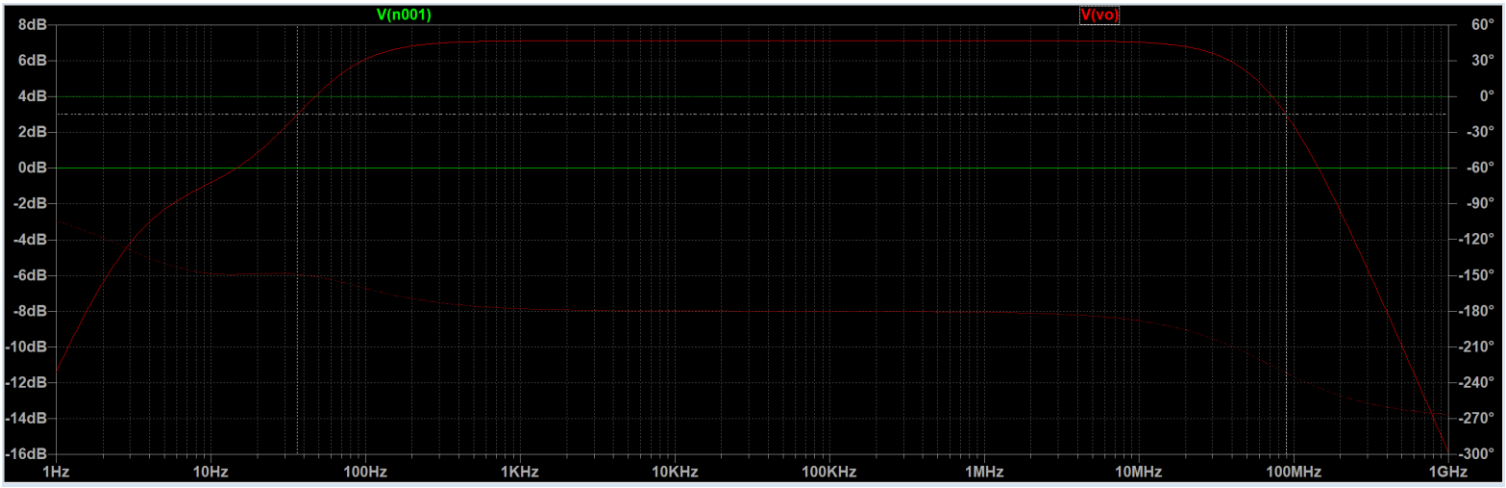


Figure 45 Frequency response of Common Source (CS) Amplifier Original

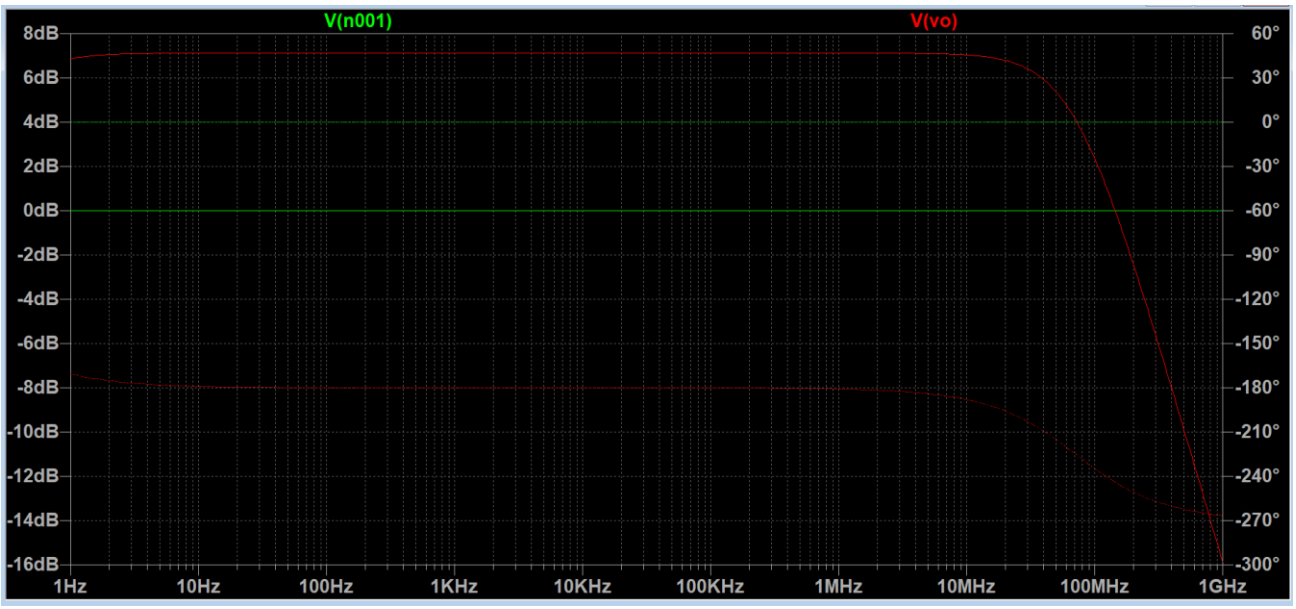


Figure 46 Frequency response of Common Source (CS) Amplifier Modified

From analyzing the two figures above when modifying the capacitors to all be higher capacitance and the same it seems to filter out all the lower frequencies. This makes sense due to the equation 1/jωC. As you increase the capacitance the overall value will tend to 0 thus resulting in the transfer function going to infinity. With this infinite capacitance it can filter out all lower frequencies and drastically reduces noise.

d. Removing the bypass capacitor CS in the CS amplifier shown in Fig. 5.4.

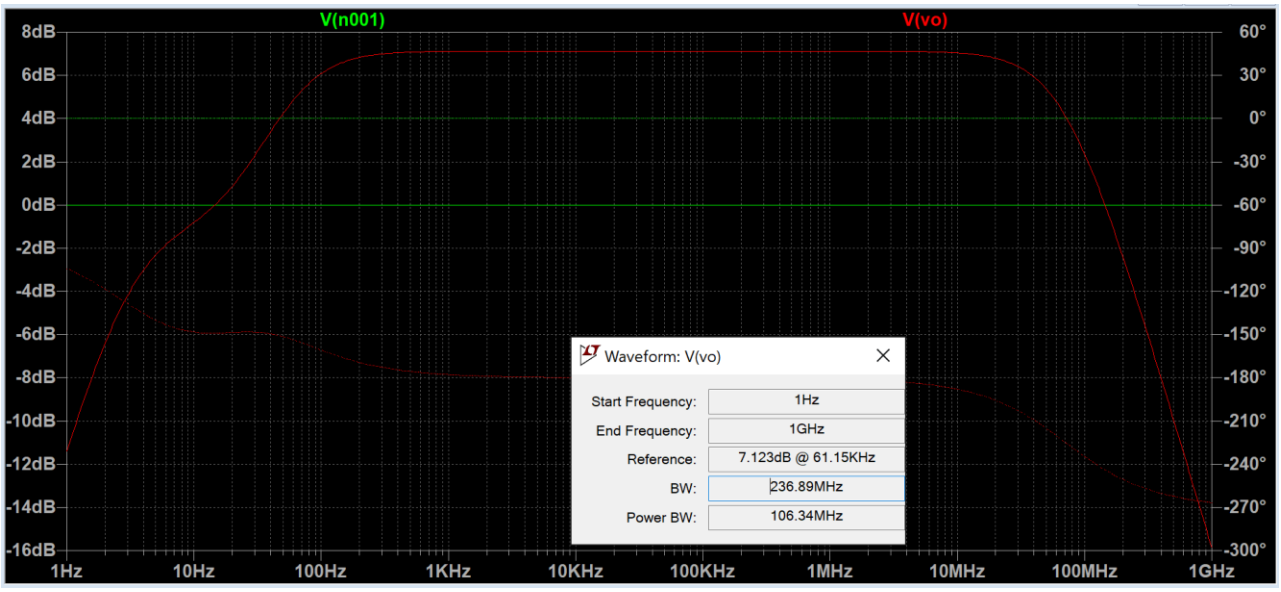


Figure 47 Frequency response of Common Source (CS) Amplifier with Bypass Filter

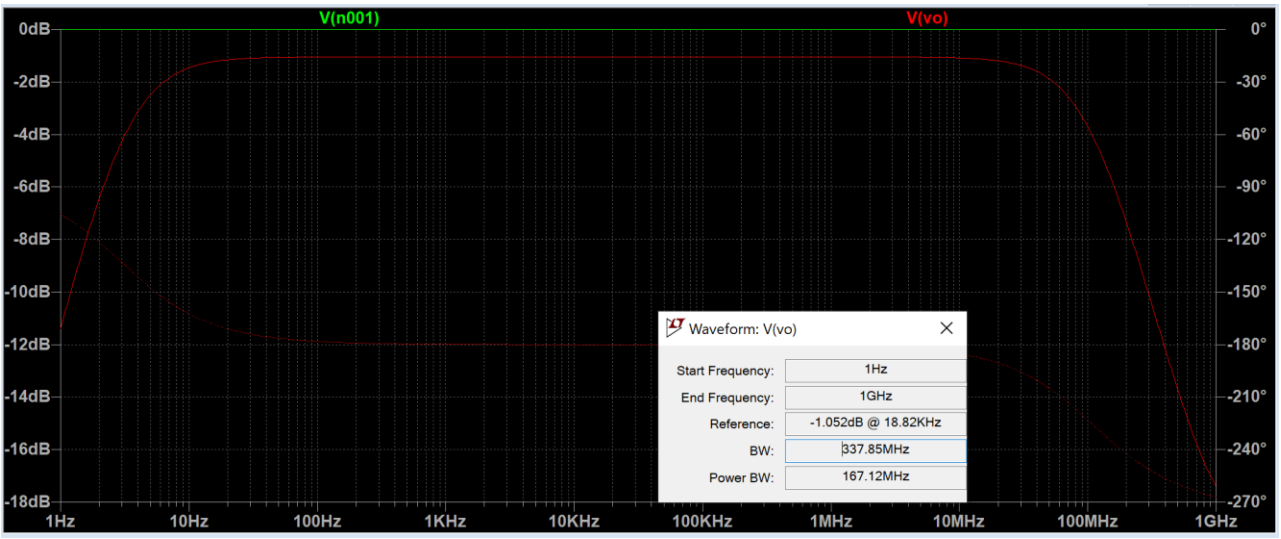


Figure 48 Frequency response of Common Source (CS) Amplifier without Bypass Filter

From the results of the two figures above it seems that the circuit without the bypass filter drops below the unity gain but the bandwidth increased. This bypass filter acts like a short which allows the AC signal a path to ground. If this short was not in place the noise would cause issues with the DC signal hence figure 48.

2. Based on your results, discuss the main differences between the Common-Source (CS) amplifier, Common-Drain (CD) amplifier, and Common-Gate (CG) amplifier.

From the lab experiment data, it indicates that both Common-Source (CS) and Common-Gate (CG) amplifiers exhibit a gain that exceeds unity. The Common Source Amplifier demonstrates amplification with a reverse phase of 180 degrees, whereas the Common Gate Amplifier, while also amplifying, maintains the original phase with a 0-degree shift. When comparing all amplifiers, it's observed that the Common Drain amplifier, although having a similar gain as the Common Source, offers a wider bandwidth. The Common-Gate amplifier, functioning as a source follower, seems to primarily serve as a voltage buffer and does not enhance voltage gain. In these lab experiments, it showed a comparatively lower maximum gain, even registering as negative. This type of amplifier, being a source follower, retains the phase of the input signal, as evidenced by the 0-degree phase shift in the final results.