Introduction to Digital Circuits

Lab 6

EEE 334
Circuits II

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Report Completed on: **12/05/2023**

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INTRODUCTION

This labs' main focus is to allow the student to gain a deeper understanding of fundamental logic gates and the characteristics behind them. The lab will focus on studying the characteristics of a CMOS inverter and then shifting to getting a deeper understanding of CMOS, NAND, and NOR gates.

Figure 1 was removed due to it only being a photo of myself

Figure 1 Lab Set-Up Selfie Photo

EQUIPMENT and COMPONENTS USED

For this lab the following items were used to conduct the experiments and findings:

- *Digital Multimeter*
- *ADK (Analog Discovery 2)*
- *Large Breadboard*
- *Analog Parts Kit*
- *TI-nspire CX II Calculator*
- *Capacitors used: 1x 100pF, 1x 1µF*
- *Transistor used: 1x CD4007*

Course of Action

This section covers the processes that need to be done for each part. There will be a detailed description of what needs to be found and accomplished. The completed results mentioned in this section will be found in the results section.

6.1 Voltage Transfer Characteristics of the CMOS inverter "Static Operation"

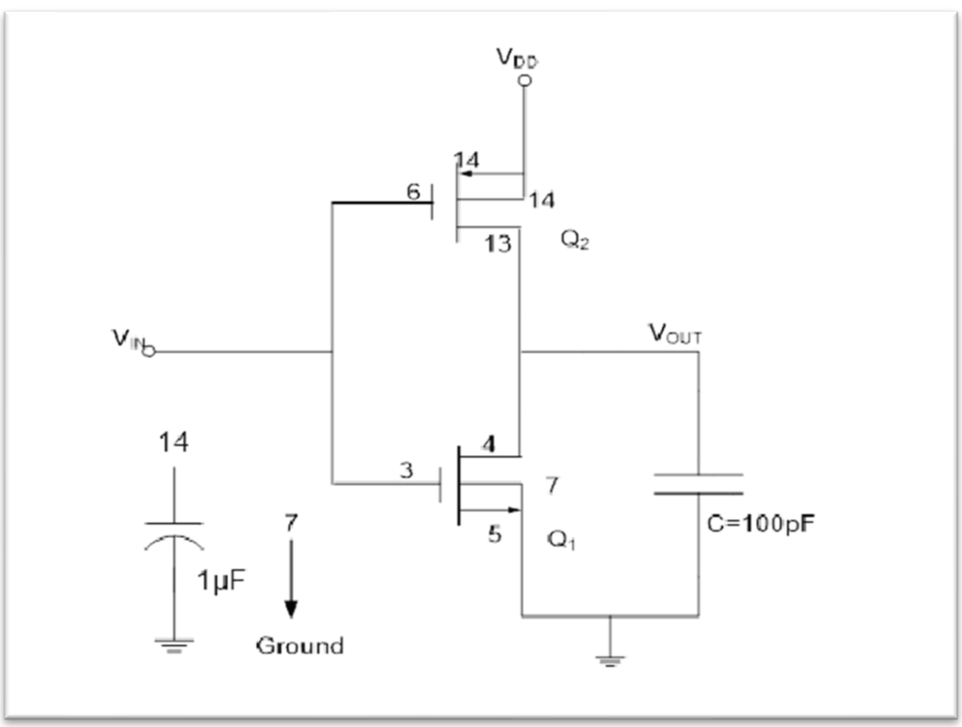


Figure 2 Circuit Diagram for CMOS Inverter

For the first section of the lab, the focus will be on hand calculating the theoretical values of NMh and NMl for the circuit displayed above. Once the hand calculations are complete the physical circuit will be built on the breadboard. The 100pF capacitor will also be checked for accuracy. Next, a DC voltage will be applyed to the input (Vin), incrementing it from 0 to 5V in 0.5V steps. Pay close attention to the range between 2.4-2.5V, making finer adjustments in this region to accurately measure the corresponding output voltage (Vout). Once this is done the data will be plotted with Vout against Vin. The focus being on the slope near Qn/Qp in the saturation area to determine the transfer characteristic gain. This data will then be used to calculate actual NMh and NMl values. This will be done by visually estimating the values from the plot, using the relevant equation for accuracy.

For the last part of this section the circuit will be simulated using LTSpice with NMOS4 and PMOS4, using the same transistor parameters as in lab 4.4. Then a DC sweep of Vin from 0 to 5V in 0.1V increments will be run. The simulation results will then be analyzed to determine the slope, NMh, and NMl, thereby confirming the practical results against the theoretical predictions.

6.2 Dynamic Operation of the CMOS Inverter

To start this section, the circuit will be modified for dynamic analysis, this will be done by disconnecting the DC input and instead applying a square wave ranging from 0 to 5V at a frequency of 1kHz. Then hand calculations will be done to calculate the propagation delay (tp), power dissipation (Pd), and the delay-power product (DP), considering an alpha value of 1.7.

Then the output voltage (Vo) and input voltage (Vin) will be observed on the ADK oscilloscope. Measuring the high-to-low propagation delay (tphl), overall propagation delay (tp), fall time (tf), and rise time (tr). While reading the oscilloscope and estimating the values while disregarding any minor oscillations that may occur.

Finally, the circuit will be simulated in LTSpice simulation software. Where the same value for the load capacitor will be used as in the practical setup. The Vpulse will be set up in the simulation as 0 to 5V with rise and fall times of 5ns and pulse width and period of 0.5ms and 1ms, respectively. Ensuring both DC and AC values are set to 0. From LTSpice the data will be recorded for the same time-related values (tphl, tplh, tp, tf, tr) to compare and validate against the oscilloscope measurements.

6.3 CMOS characterization of NAND and NOR gates(SPICE ONLY)

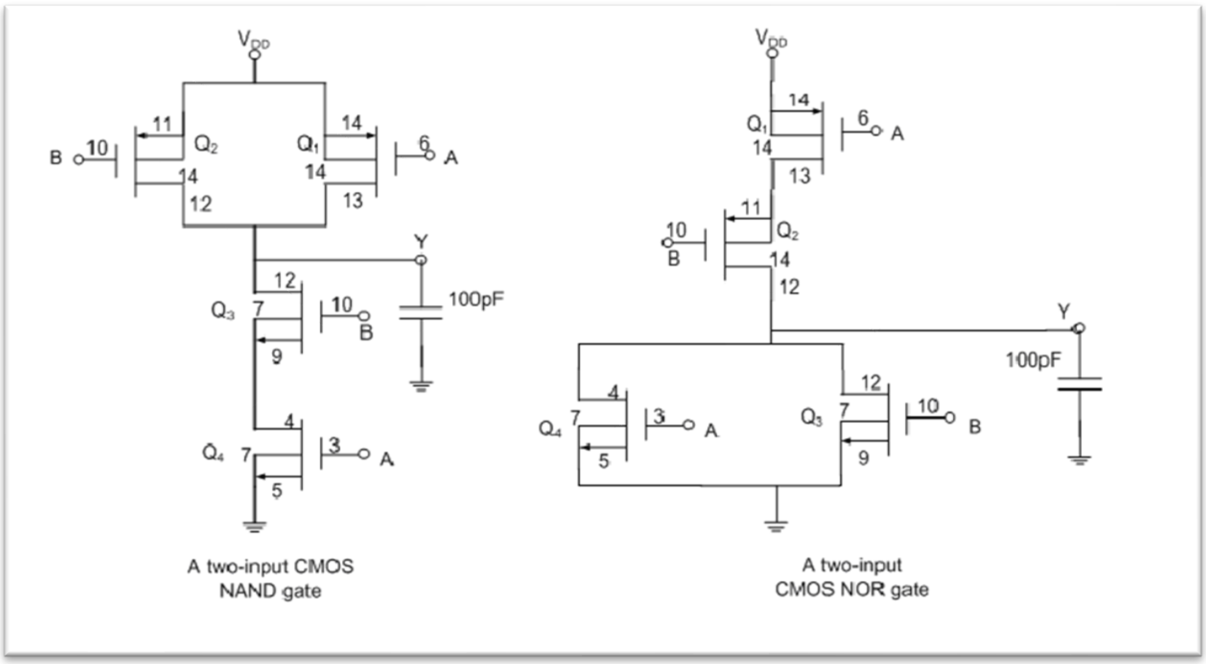


Figure 3 Circuit Diagram for NAND and NOR Gates

For the last section of this lab, the intricacies of NOR and NAND gates will be analyzed. To start the truth tables for each gate will be done by hand. After this the Booleab expression for the NOR and NAND will be displayed in the results.

Once the hand calculated items are done, each gate will be simulated using LTSpice, ensuring a 100pF capacitor at the output terminal for both circuits. The test of the NAND gate will come first. The test will be run with a 1kHz VPULSE, set to a 5V peak-to-peak voltage, on input A, while switching input B between 0V and 5V. The VPULSE settings will be set – 0 to 5V with 5ns for both rise and fall times, and pulse set at 0.5ms for width and 1ms for period, with DC and AC values at 0. Two tests will be run: initially, with input A receiving the pulse and input B locked at 5V, followed by a second test with input A pulsing and input B at 0V. The goal is to closely examine the input and output waveforms, focusing on calculating the propagation delay from the transient analysis. Lastly, the same test will be run for the NOR gate.

RESULTS

6.1 DC biasing of an NMOS transistor

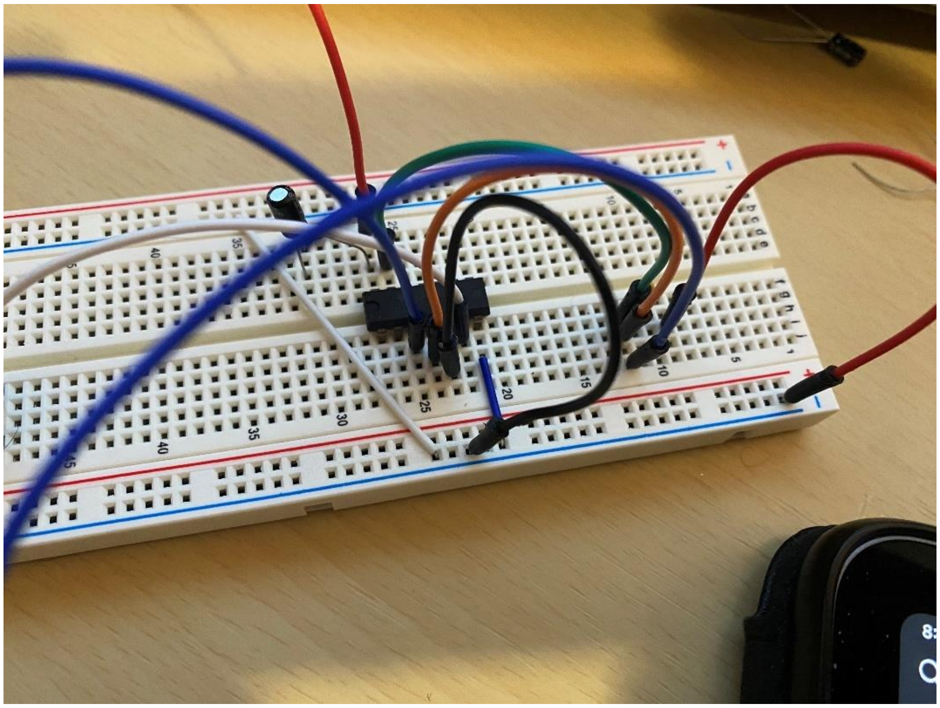


Figure 4 Physical Built Circuit for DC Biasing Circuit

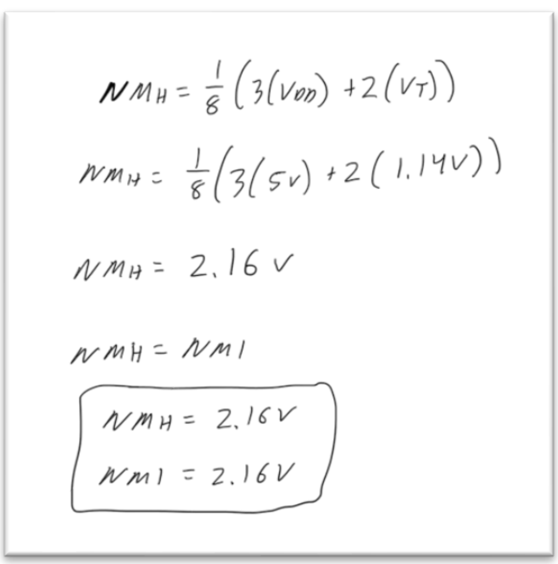


Figure 5 Hand Calculations for Part 1

Verified Component Measured Values:
Capacitor for pin 14 = 1.05μF
C = 105pF

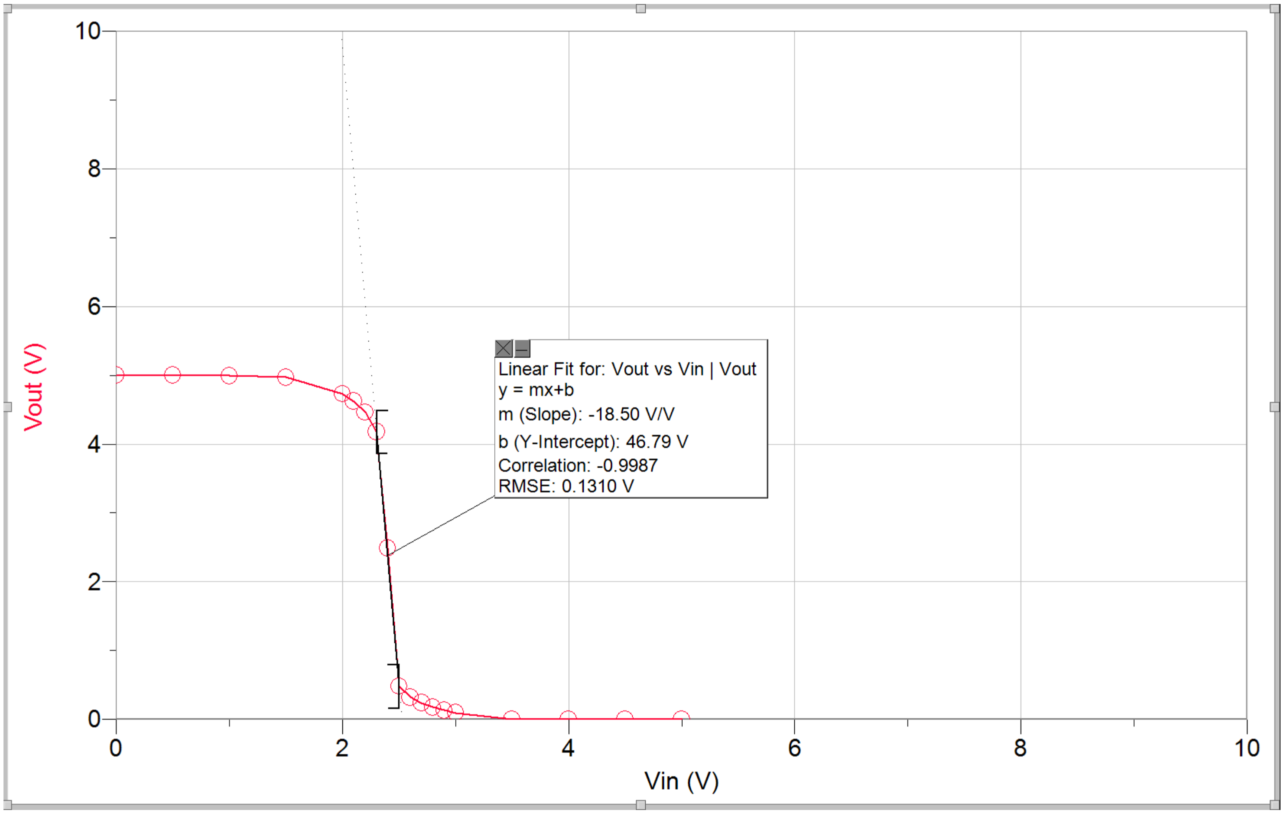
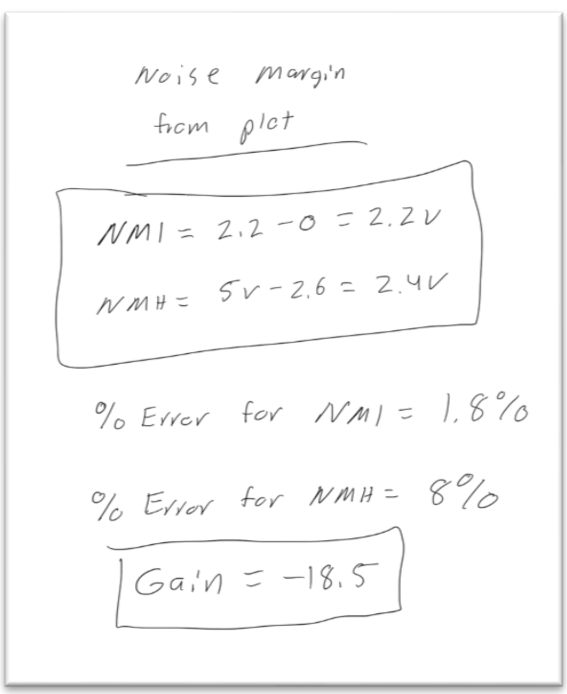


Figure 6 Plot for Part 1



Noise margin from plot

NMl = 2.2 − 0 = 2.2V

NMH = 5v − 2.6 = 2.4V

% Error for NMl = 1.8%

% Error for NMH = 8%

Gain = −18.5

Figure 7 Calculations from Plot

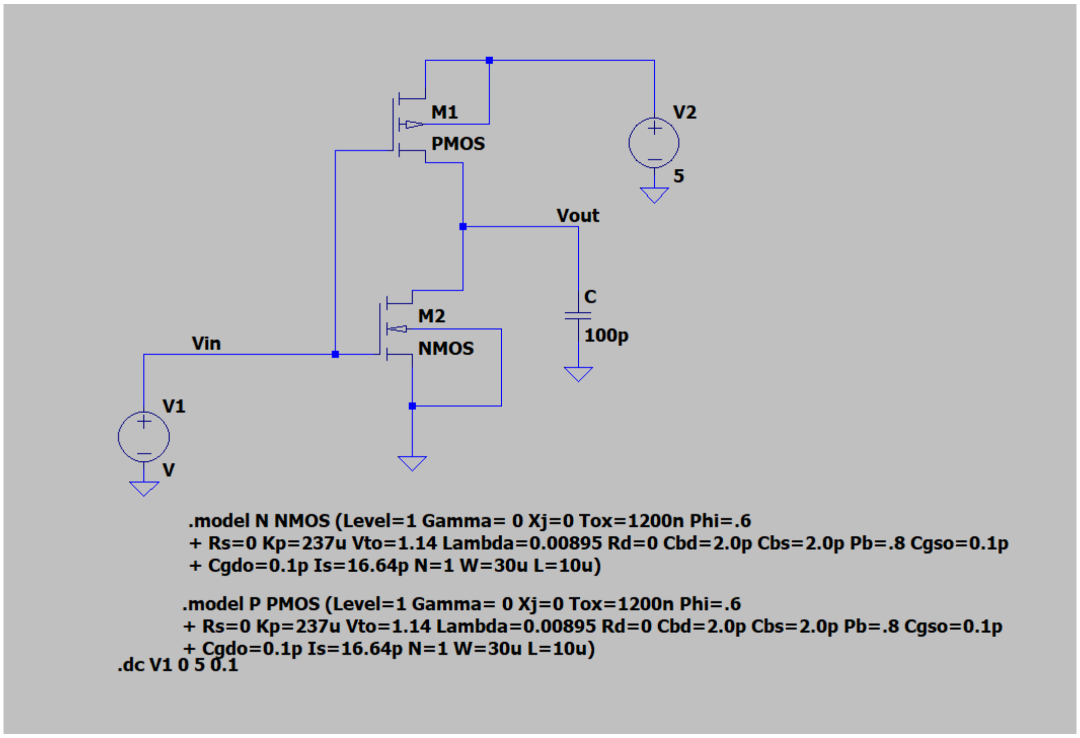


Figure 8 LTSpice Circuit Diagram for Part 1

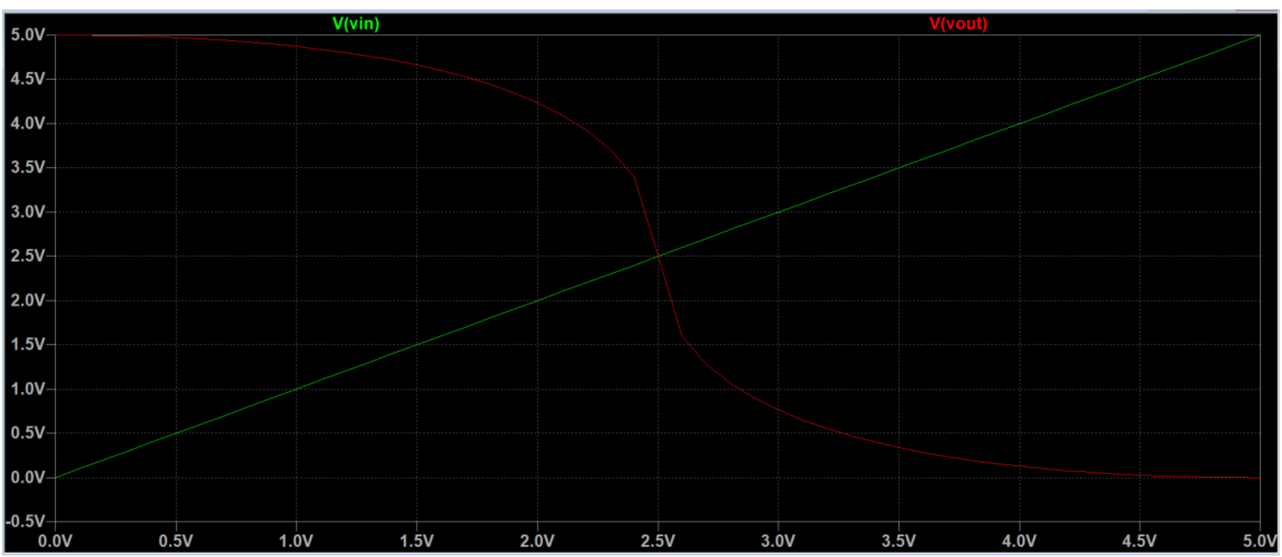
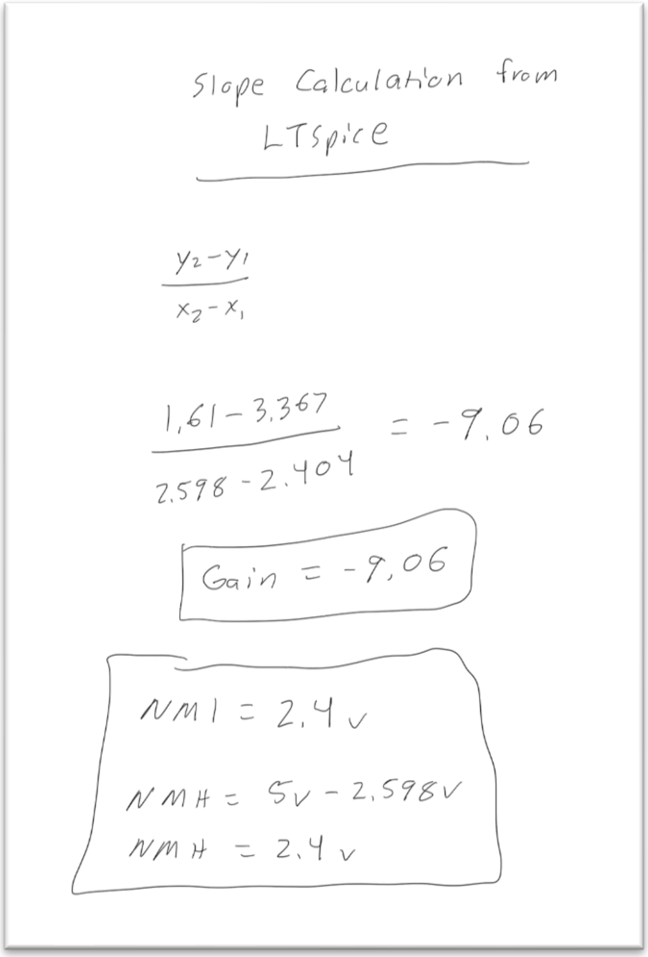


Figure 9 LTSpice Analysis for Part 1



Slope Calculation from
LTSpice

$$\frac{y_2-y_1}{x_2-x_1}$$

$$\frac{1.61-3.367}{2.598-2.404} = -9.06$$

$\boxed{\text{Gain} = -9.06}$

NMl = 2.4v

NMH = 5v - 2.598v
NMH = 2.4v

Figure 10 Hand Calculations for LTSpice Analysis

6.2 Dynamic Operation of the CMOS Inverter

$$t_{phl} = \frac{1.7C}{K'_p(\frac{W}{L}) \cdot V_{DD}}$$

$$t_{phl} = \frac{1.7(100 \cdot 10^{-12} F)}{(0.33 \frac{mA}{V^2})(5V)}$$

$$t_{phl} = 10.3\ ns$$

$$t_{plh} = \frac{1.7C}{K'_n(\frac{W}{L}) \cdot V_{DD}}$$

$$t_{plh} = \frac{1.7(100 \cdot 10^{-12} F)}{(0.711 \frac{mA}{V^2})(5V)}$$

$$t_{plh} = 47.82\ ns$$

$$P_D = f C_L V_{DD}^2$$

$$P_D = (1kHz)(100pF)(5V)^2$$

$$\boxed{P_D = 2.5 uW}$$

$$t_p = \frac{t_{phl} + t_{plh}}{2}$$

$$t_p = \frac{47.82ns + 10.3ns}{2}$$

$$\boxed{t_p = 29.06ns}$$

$$DP = P_D \cdot t_p$$

$$\boxed{DP = 72.65\ \underset{\text{femto}}{f} W \cdot s}$$

Figure 11 Hand Calculations for Part 2

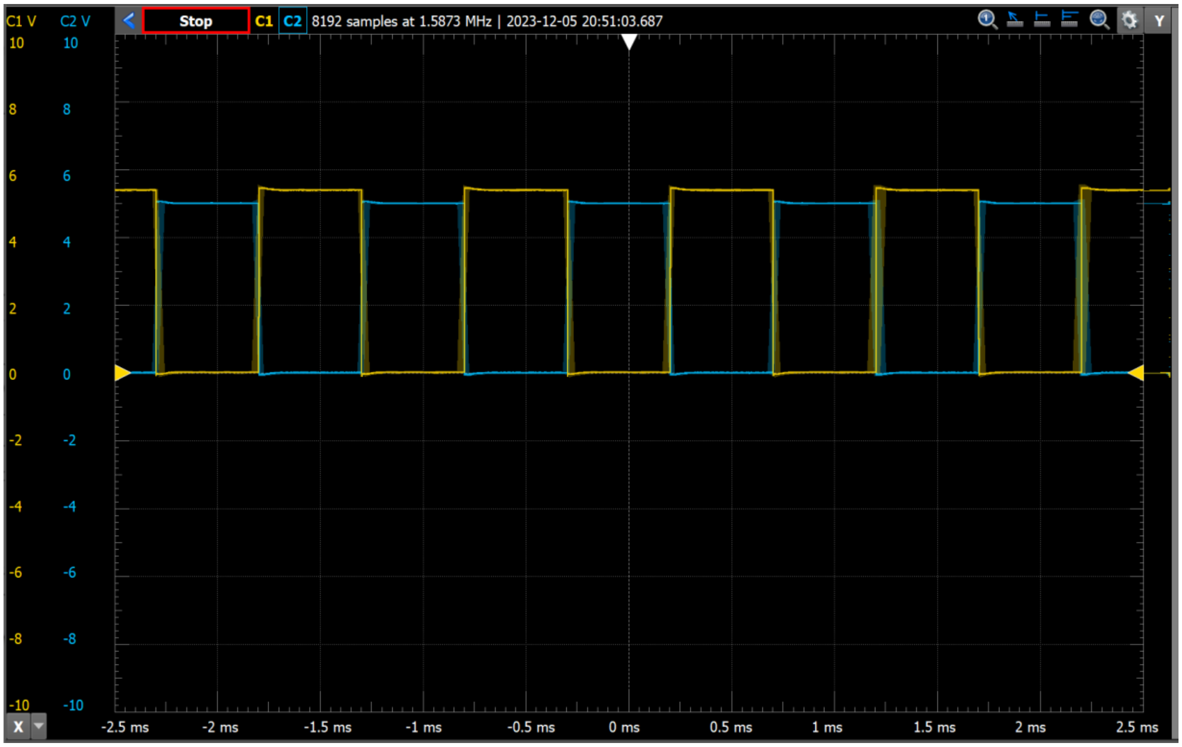


Figure 12 WaveForms for Part 2

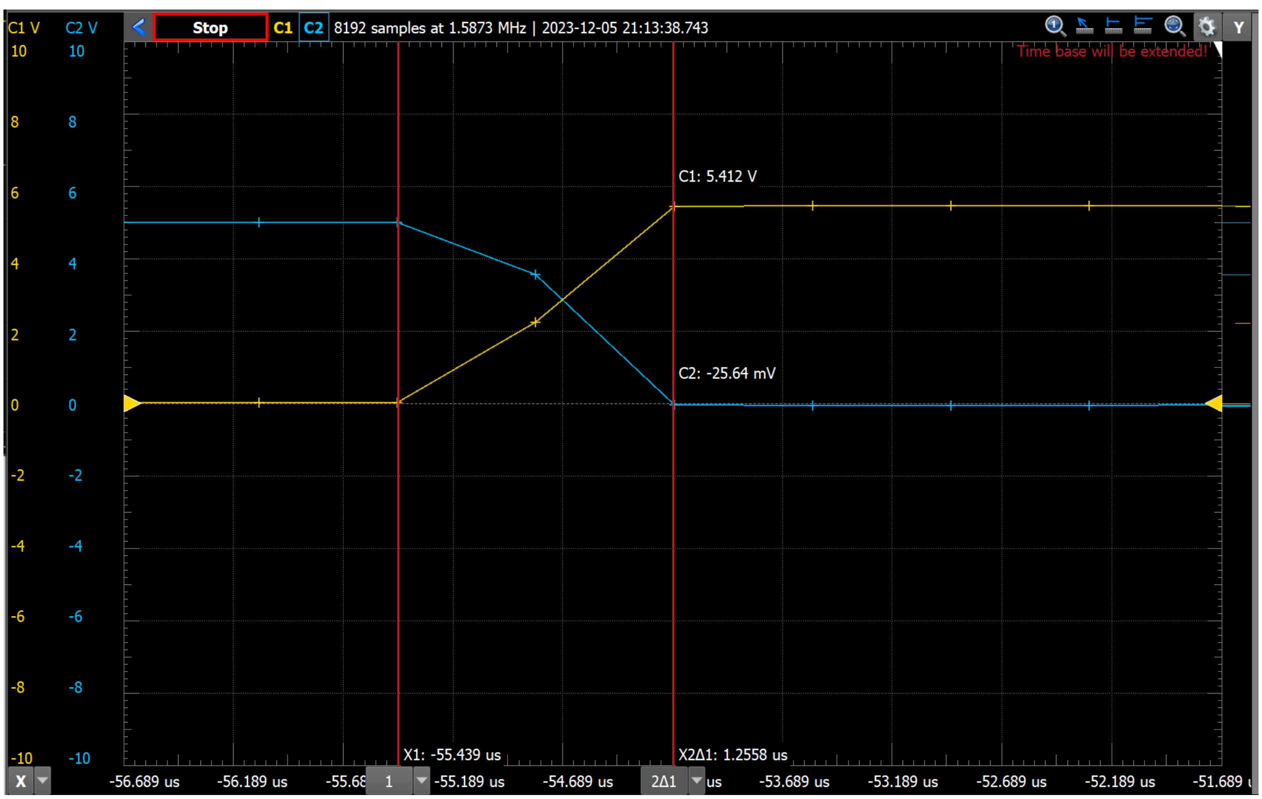


Figure 13 Finding Tr in Waveforms Part 2

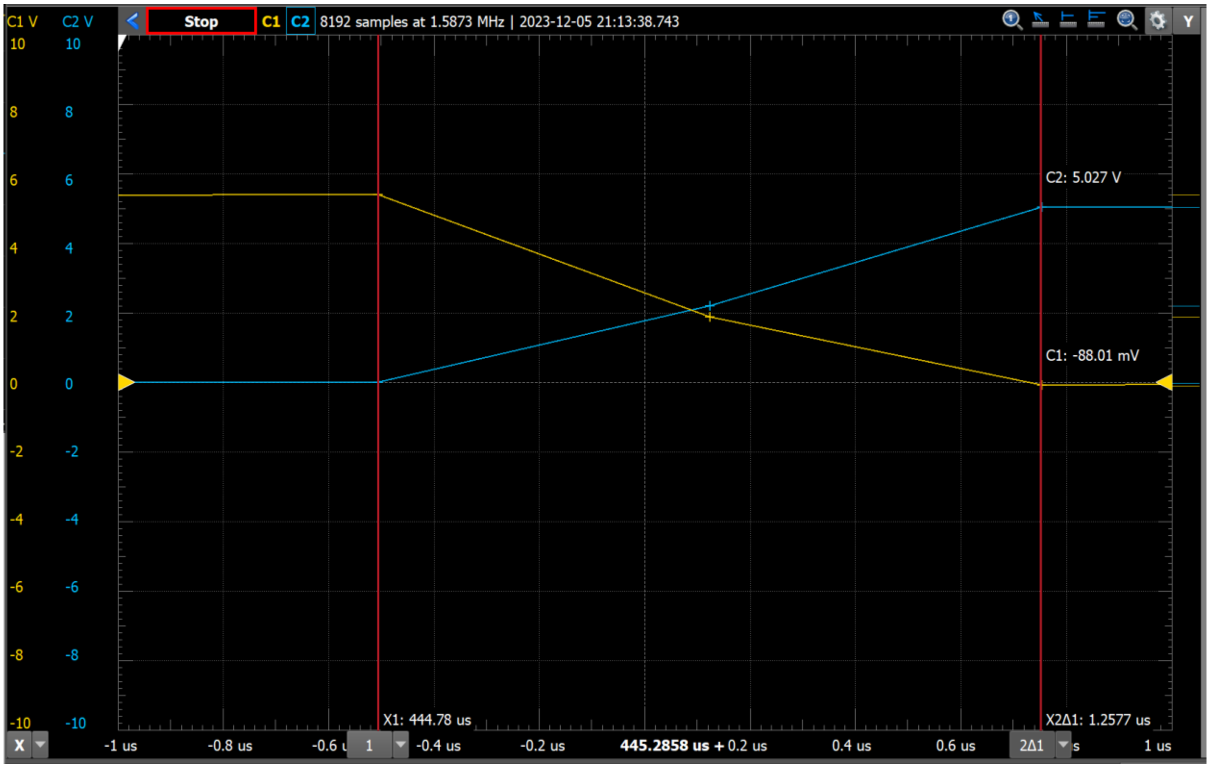


Figure 14 Finding Tf in Waveforms Part 2

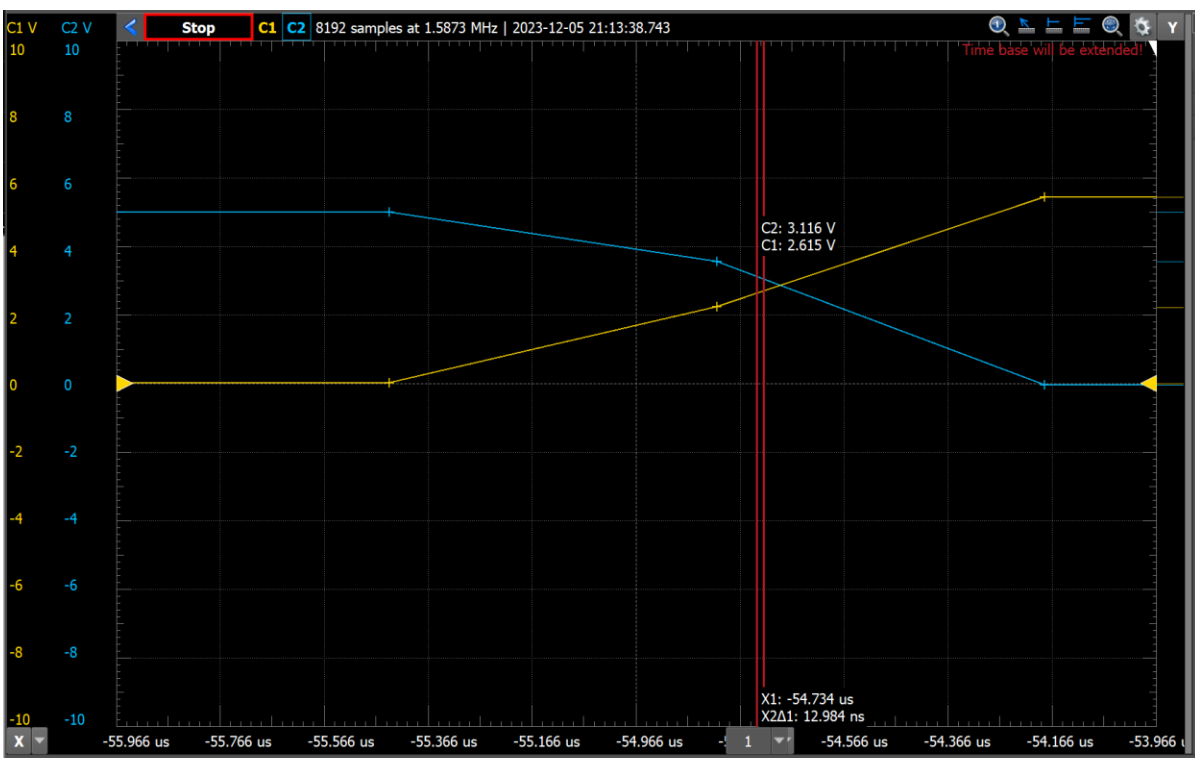


Figure 15 Finding Tphl in Waveforms Part 2

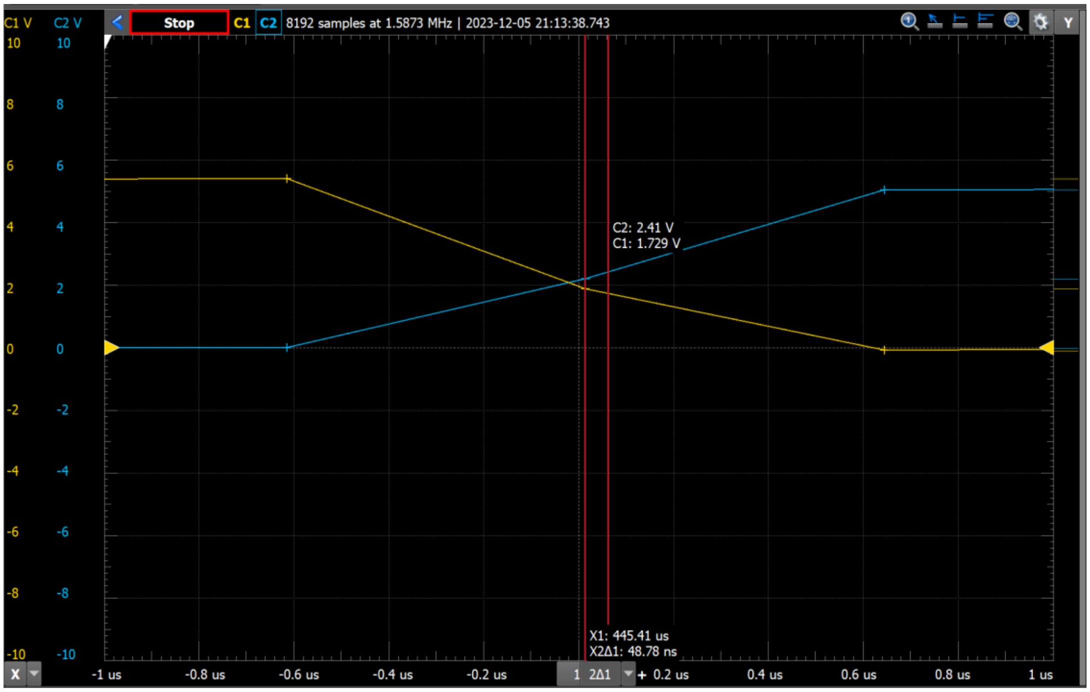
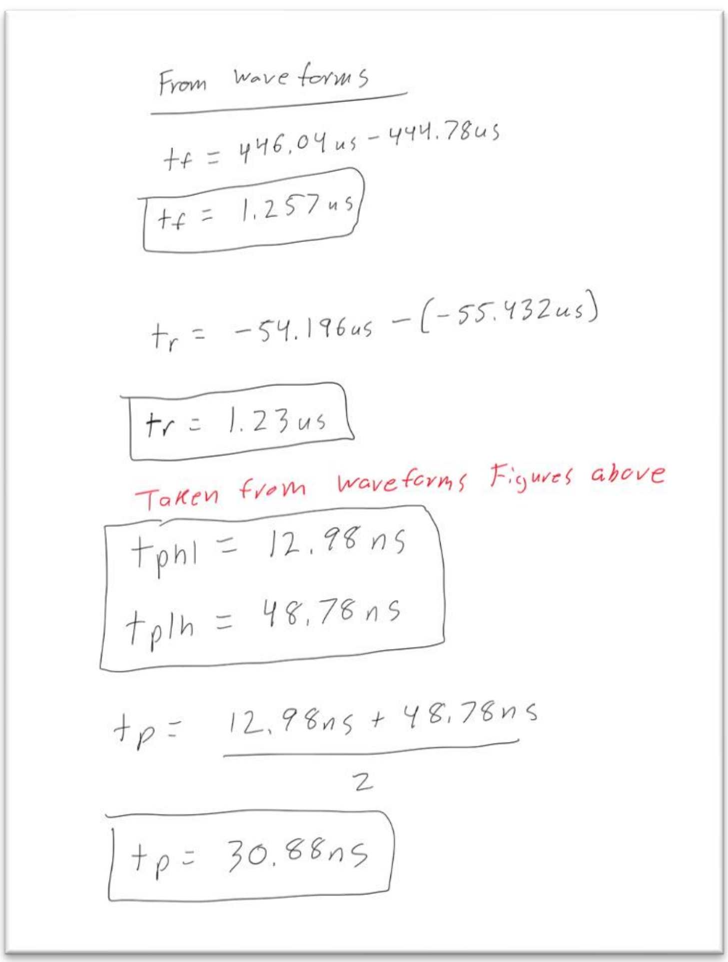


Figure 16 Finding Tplh in Waveforms Part 2



From waveforms

$t_f = 446.04us - 444.78us$

$\boxed{t_f = 1.257us}$

$t_r = -54.196us - (-55.432us)$

$\boxed{t_r = 1.23us}$

Taken from waveforms Figures above

$tphl = 12.98ns$

$tplh = 48.78ns$

$$t_p = \frac{12.98ns + 48.78ns}{2}$$

$\boxed{t_p = 30.88ns}$

Figure 17 Results for Waveforms Required Items to Find

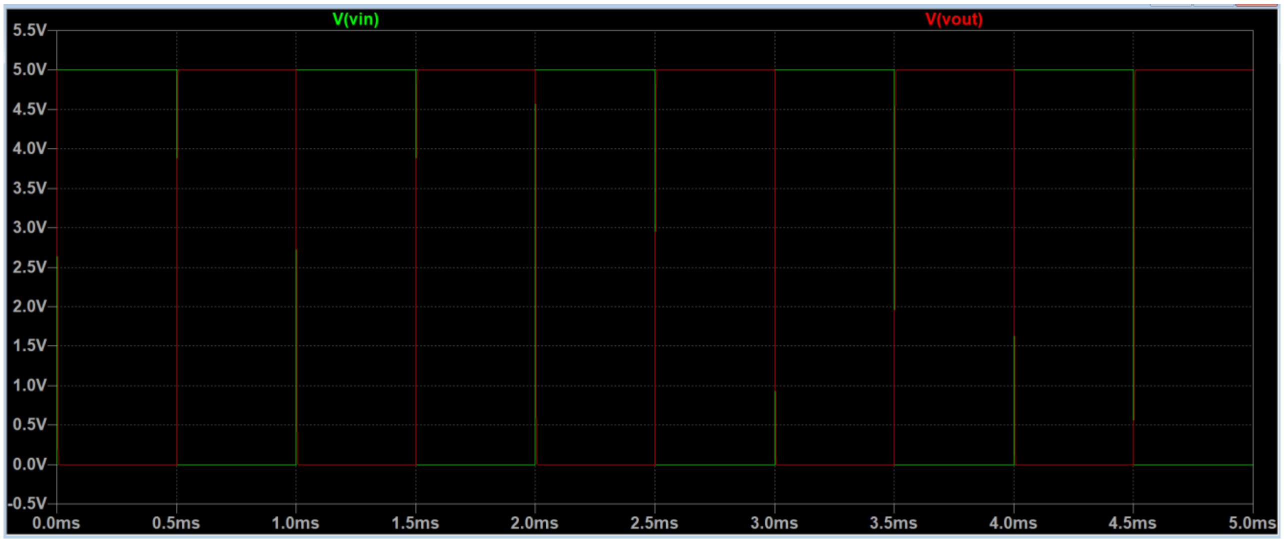
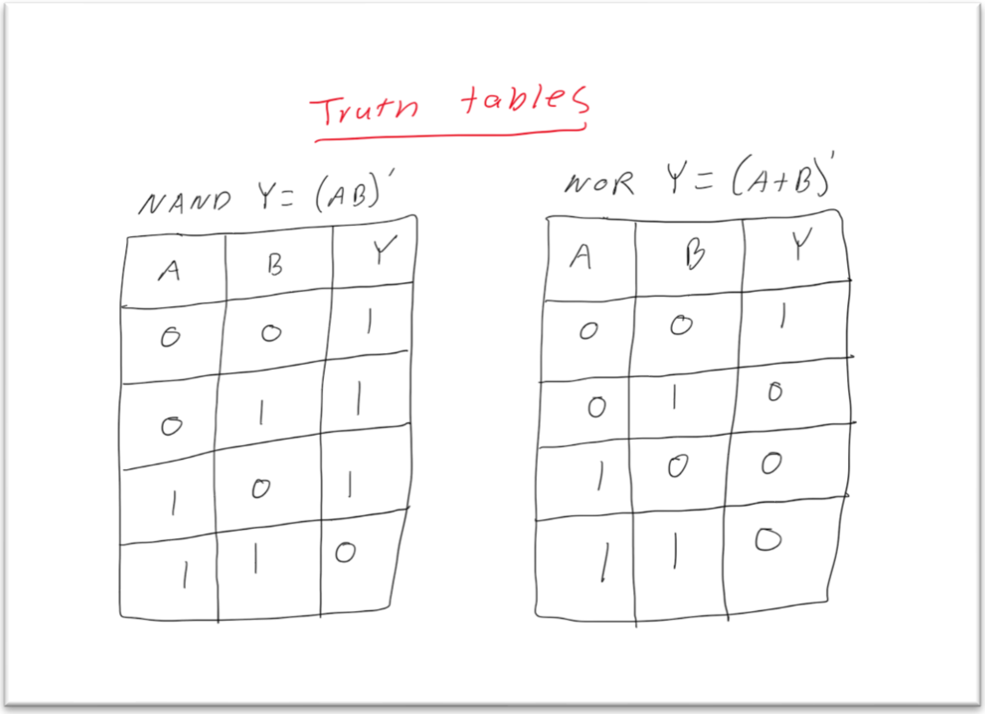


Figure 18 LTSpice Simulation Transient Analysis Results

```
tphl=1.1784e-006 FROM 0.002 TO 0.00200118
tplh=1.1784e-006 FROM 0.002 TO 0.00200118
tr=2.97672e-006 FROM 0.00250021 TO 0.00250319
tf=2.76758e-006 FROM 0.0020002 TO 0.00200297
tp: (tplh+tphl)/2=1.1784e-006
```

Figure 19 LTSpice Simulation Analysis Results

6.3 CMOS characterization of NAND and NOR Gates



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Figure 20 Truth Tables for Part 3

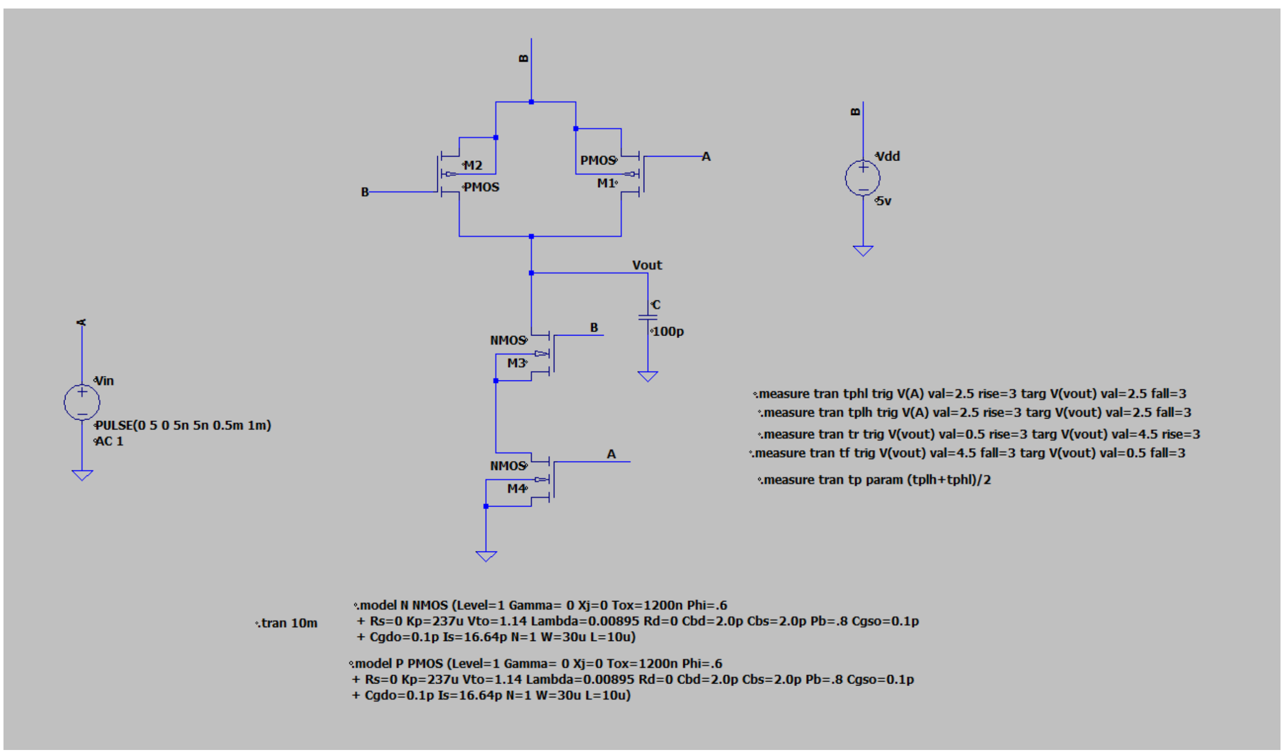


Figure 21 LTSpice Diagram for NAND Gate

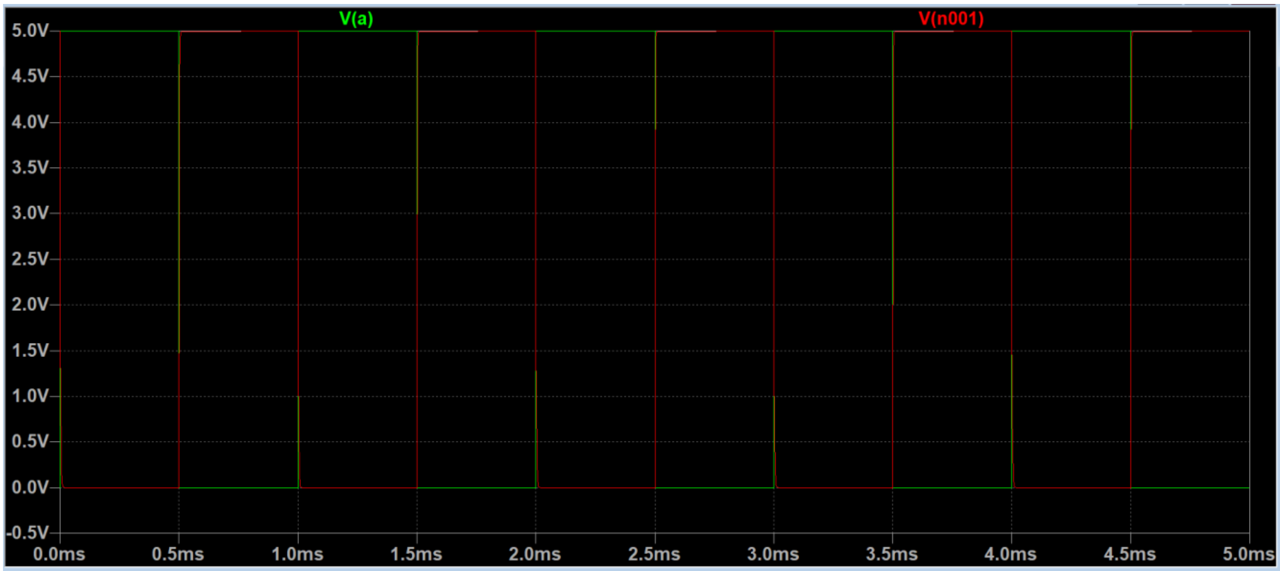


Figure 22 First Case NAND Gate Analysis

```
tphl=2.35882e-006 FROM 0.002 TO 0.00200236
tplh=2.35882e-006 FROM 0.002 TO 0.00200236
tr=2.9894e-006 FROM 0.00250021 TO 0.0025032
tf=5.54493e-006 FROM 0.00200041 TO 0.00200595
tp: (tplh+tphl)/2=2.35882e-006
```

Figure 23 First Case NAND Gate Analysis Results

From analyzing the LTSpice simulation for the first case everything seems to be behaving as expected. For the first case B is on and the only way for the gate to be True A has to be off. From the truth table at the beginning of this section if either one is false then the result will be false for AB, so true for the opposite. When the gate is represented to be on then the red one (output) is off and if the red one (output) is on then the green one is off. These conditions satisfy the gates logic.

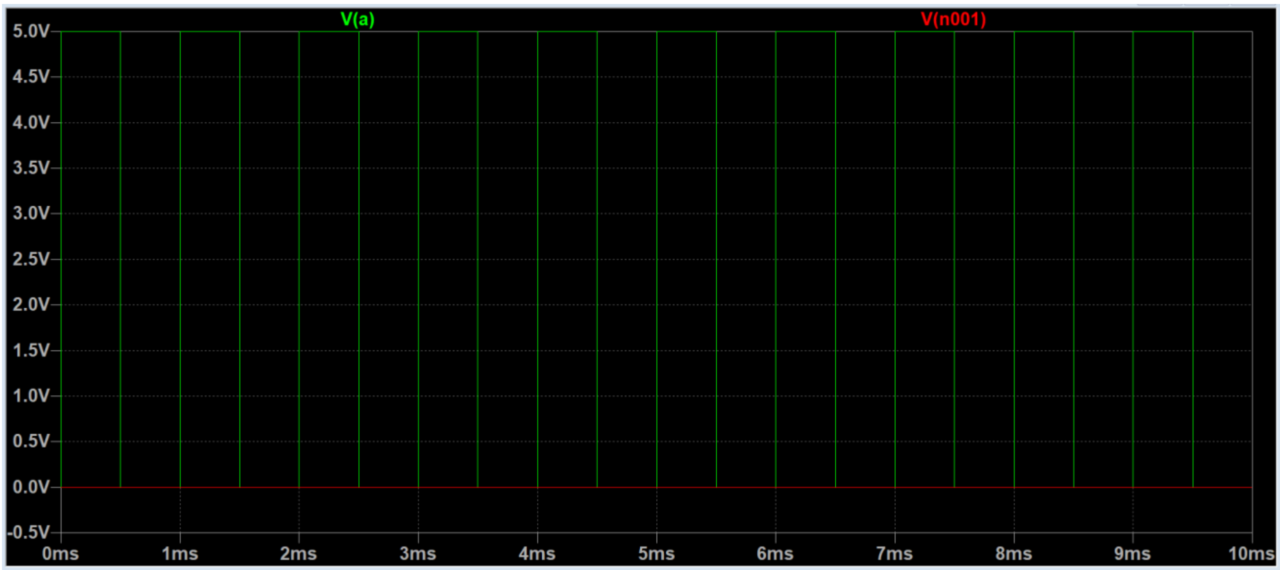


Figure 24 Second Case NAND Gate Analysis

```
Measurement "tphl" FAIL'ed

Measurement "tplh" FAIL'ed

Measurement "tr" FAIL'ed

Measurement "tf" FAIL'ed

Measurement "tp" FAIL'ed
```

Figure 25 Second Case NAND Gate Analysis Results

*** The reason for the failure above is due to the ability to not find tp for all cases as mentioned in the manual.

For the second case when B is 0V the not part of the gate will result in true. This is due to there never being A and B and there is always a NOT.

Steps Repeated for NOR Gate:

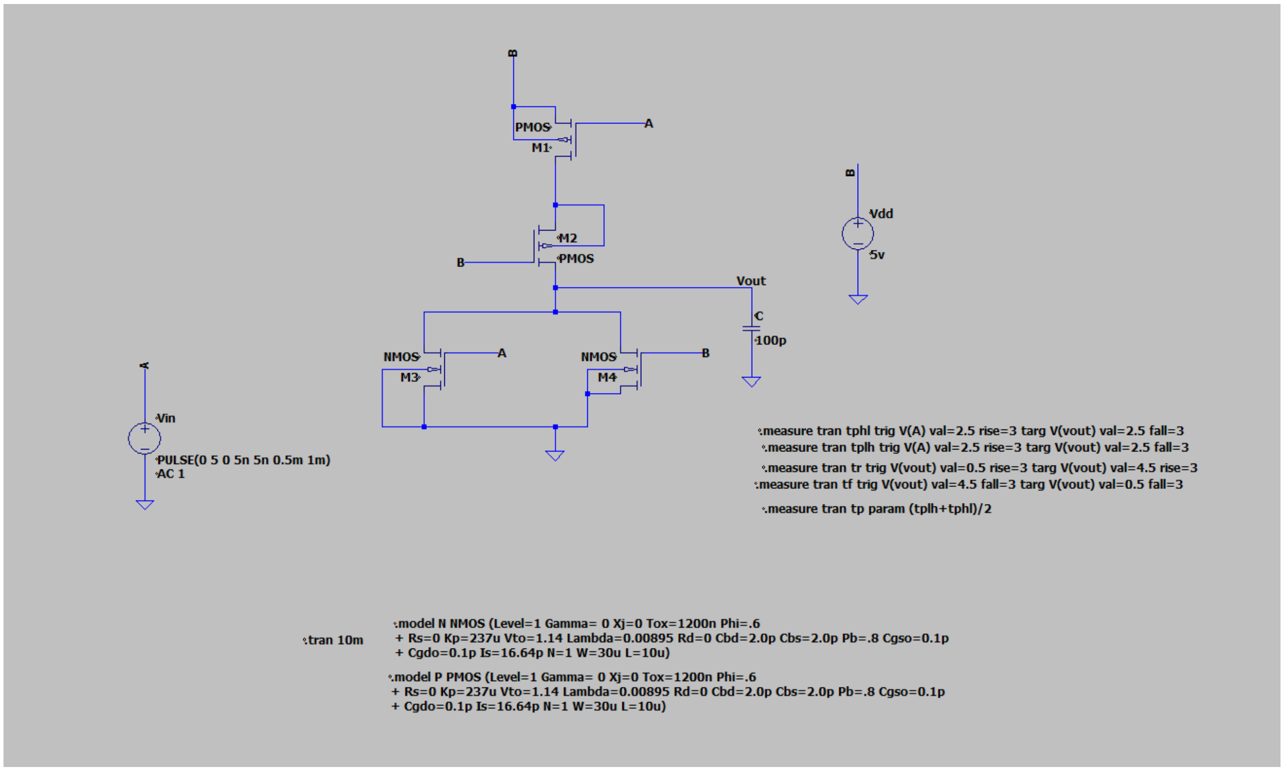


Figure 26 LTSpice Diagram for NOR Gate

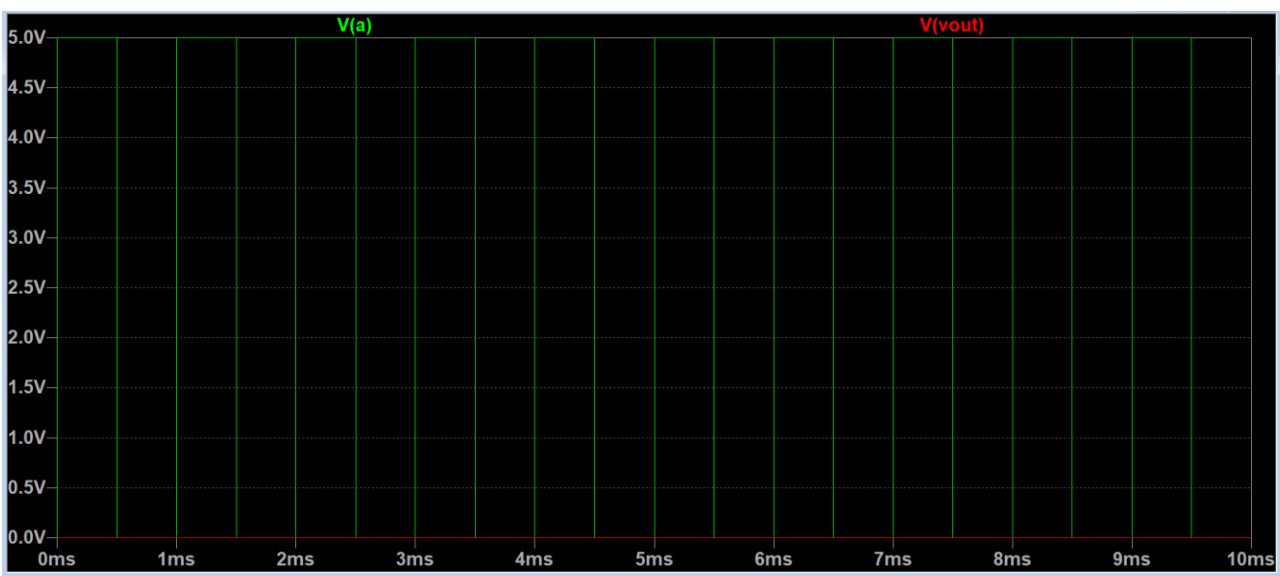


Figure 27 First Case NOR Gate Analysis

```
Measurement "tphl" FAIL'ed

Measurement "tplh" FAIL'ed

Measurement "tr" FAIL'ed

Measurement "tf" FAIL'ed

Measurement "tp" FAIL'ed
```

Figure 28 First Case NOR Gate Analysis Results

For the analysis of the NOR gate first case when B = 5v, the device never is on it always stays off. From the fundamentals of a NOR gate this makes sense due to if there is ever a true statement then the result would be off.

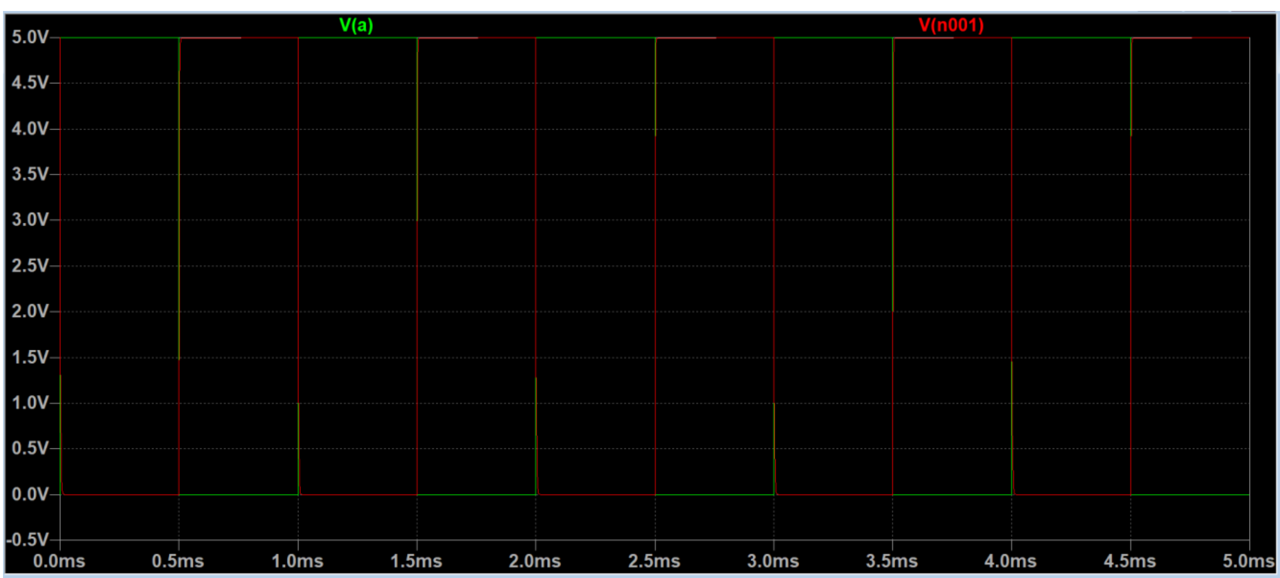


Figure 29 Second Case NOR Gate Analysis

```
tphl=2.35882e-006 FROM 0.002 TO 0.00200236
tplh=2.35882e-006 FROM 0.002 TO 0.00200236
tr=2.9894e-006 FROM 0.00250021 TO 0.0025032
tf=5.54493e-006 FROM 0.00200041 TO 0.00200595
tp: (tplh+tphl)/2=2.35882e-006
```

Figure 30 Second Case NOR Gate Analysis Results

For the analysis of the second case when B= 0V the result is only on and true when both the A and B are off. This is what is happening so the gate is behaving as expected.

CONCLUSION

This labs' main focus is to allow the student to gain a deeper understanding of fundamental logic gates and the characteristics behind them. The lab will focus on studying the characteristics of a CMOS inverter and then shifting to getting a deeper understanding of CMOS, NAND, and NOR gates.

For the first section 6.1, the focus was on Voltage Transfer Characteristics of the CMOS inverter. First the NMH and NMl were calculated by hand. Once completed the circuit was built and analysized with the ADK Waveforms oscilloscope. From the measure values they were logged onto a plot to find the slope and the NMH and NMl values. From there the circuit was then simulated in LTSpice where an analysis was run to find the same items from the physical part. Comparing the two they were relatively close but with a little error of 8% from the NMH and about half the gain as compared to the oscilloscope values.

As for the second section 6.2, this section shifted to the Dynamic Operation of the CMOS Inverter. In this section the transient analysis was run on the CMOS inverter. From that analysis the pulse response could be seen and analyzed. This part was a little tricky but zooming way into the oscilloscope values the values of tphl, tplh, tr, and tf were calculated. Once these values were gathered, they were compared to the LTSpice results where they were fairly close to each other with little error. These can be confirmed to be done correctly.

As for the second section 6.3, the NAND and NOR gate were analyzed on LTSpice. At the start of each part the circuit was built and then tested against all truth table options such as setting A to the pulse and B to 5v for the first case. For the second case the B was then set to 0V. From these different cases the NAND and NOR gate behaved as they should as mentioned in the results section.

This lab was pretty cool. With even further transistor knowledge of where this eventually goes. I like seeing the progression into modern day electronics.

POST LAB QUESTIONS

1.

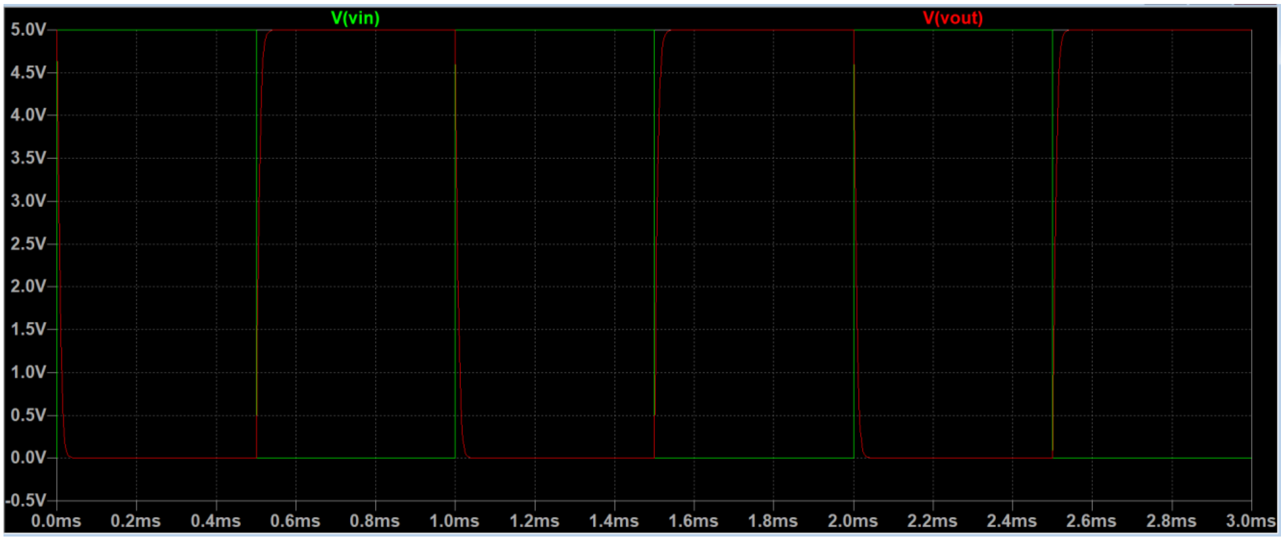


Figure 31 Post Lab Question A

a. When the output capacitor is changed to 500pF not much changes besides the output transitions seem to be delayed when compared to the pervious one earlier in the experiment.

b. From the analysis of adjusting the frequency up to 10kHz it seems that the CMOS inverter is switching at a faster rate than the previous one along with the rise and fall times being shorter which makes sense but not much else changes.

c. When the transistors (W/L) were matched this seems to make the overall circuit perform better than the previous one with nonmatching values. This makes sense due to having all transistors in symmetry with each other and no mismatch will result in better operation.

2.

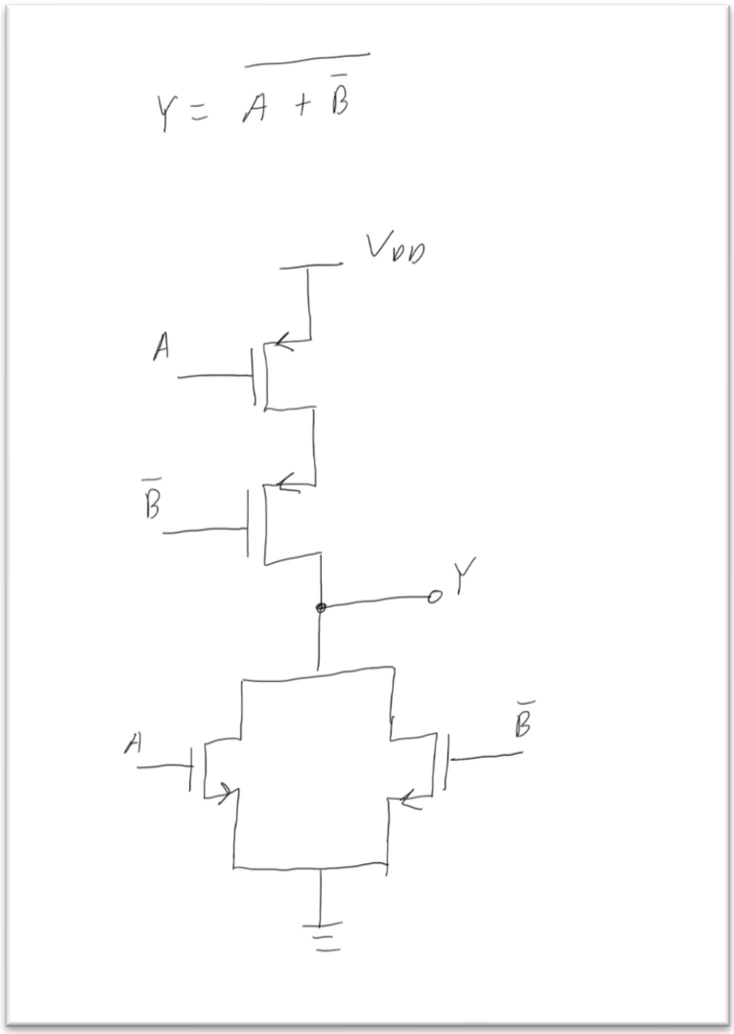


Figure 32 Hand Circuit Drawing