OPS Online Power Solutions

OPS56012V210

AC Solid State Relay with 60 Amp Current Limit and 1200V peak Operating Voltage

- **Silicon Carbide Power Transistors**
- **1200V Peak operating Voltage**
- **Less Power loss than Triac or SCR based SSRs**
- **Pulse OFF at current limit non-latching**
- **Feedback to Control side of Isolation**
- **Over Temperature Protection**
- **5kVRMS reinforced isolation**

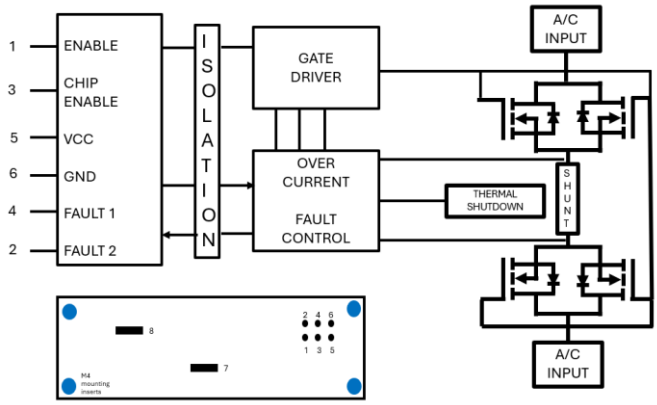
Product Description

The OPS56012V210 Is a fully integrated AC Solid State Relay with Current Limiting Capability. Based on Silicon Carbide Power Transistors the OPS56012V210 is able to operate at significantly lower Forward Voltage drops than Triac or SCR based AC SSRs dissipating less power and reducing the need for large and expensive head sinks. The package design allows for radiative cooling or water cooler to be mounted.

1. Applications

- Power distribution
- Over Current Event Prevention
- Power Supply Soft Start
- Battery management systems
- Building automation
- Factory automation and control

2. Pin Configurations



Silicon Carbide Transistors

Infineon

IMCQ120R004M2H

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	EN	I	—	Active high driver enable. Internal 500 kΩ pull-down to VSSP.
2	$\overline{\text{FLT2}}$	O	—	Fault 2 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
3	CE	I	—	Active high input. When asserted low, device is disabled. Tie to VDDP when not used. Internal 500 kΩ pull-down to VSSP.
4	$\overline{\text{FLT1}}$	O	—	Fault 1 indicator. Open-drain output. When being used, requires external pull-up to VDDP. Float or tie to VSSP when not used.
5	VDDP	—	P	Power supply for the primary side.
6	VSSP	—	GND	Ground supply for the primary side. All VSSP pins must be connected to the primary side ground.

3. Insulation Specifications

PARAMETER / SECTION		TEST CONDITIONS	VALUE	UNIT
CREEPAGE AND TRACKING				
CLR	External clearance (1)	Shortest terminal-to-terminal distance through air	≥ 8	mm
CPG	External creepage (1)	Shortest terminal-to-terminal distance across the package surface	≥ 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 120	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I–IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I–III	
DIN EN 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1697	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave)	1200	V_{RMS}
		DC voltage	1697	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7070	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$; t = 1 s (100% production test)	8484	V_{PK}
V_{IMP}	Maximum impulse voltage (2)	Tested in air; 1.2/50 µs waveform per IEC 62638-1	9230	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	Tested in oil (qualification test); 1.2/50 µs waveform per IEC 62638-1	12000	V_{PK}
q_{pd}	Apparent charge (4)	Method a: After input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM} = 2036V_{PK}$, t_m = 10s.	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM} = 2715V_{PK}$, t_m = 10s.	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM} = 3139V_{PK}$, t_m = 1s.	≤ 5	
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.4 × sin(2πft), f = 1 MHz	3	pF
R_{IO}	Insulation resistance, input to output (5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{8}	
	Pollution degree		2	
	Climatic Category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000V_{RMS}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000V_{RMS}$, t = 1s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.

(2) Testing is carried out in air to determine the intrinsic surge immunity of the package.

(3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier tied together creating a two-pin device.

4. ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 8, 9, and 16)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

5. Safety-Related Certifications

VDE	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify under UL 1577 Component Recognition Program
Reinforced insulation; Maximum transient isolation voltage, 7070 V_{pk}; Maximum repetitive peak isolation voltage, 1697 V_{pk}; Maximum surge isolation voltage, 12000 V_{pk}	Single protection, 5000 V_{RMS}
Certificate planned	Certificate planned

6. Maximum Rated Values - SSR

Parameter	Symbol	Note or test condition		Values	Unit
AC voltage	V_{AC}	T_{vj} ≥ 25 °C		850	Vrms
Continuous current if Current limit Disabled	I_{NLC}		T_c = 25 °C	200	A
			T_c = 100 °C	150	
RMS current Limit	I_{CL}			60	A

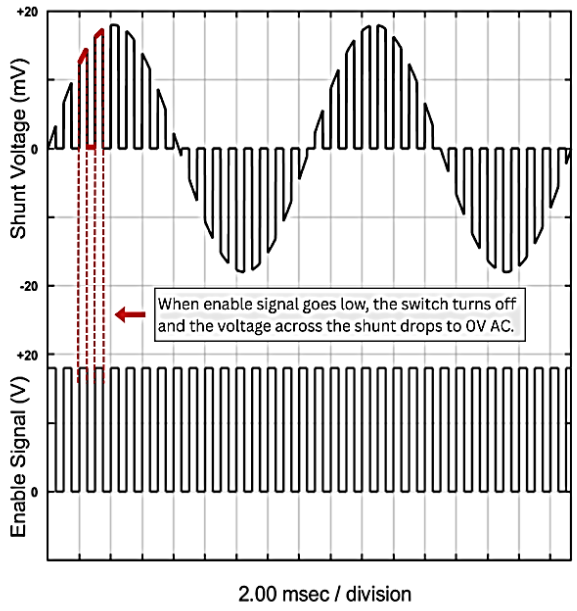
(1) Verified by design.

7. Characteristic Values - SSR

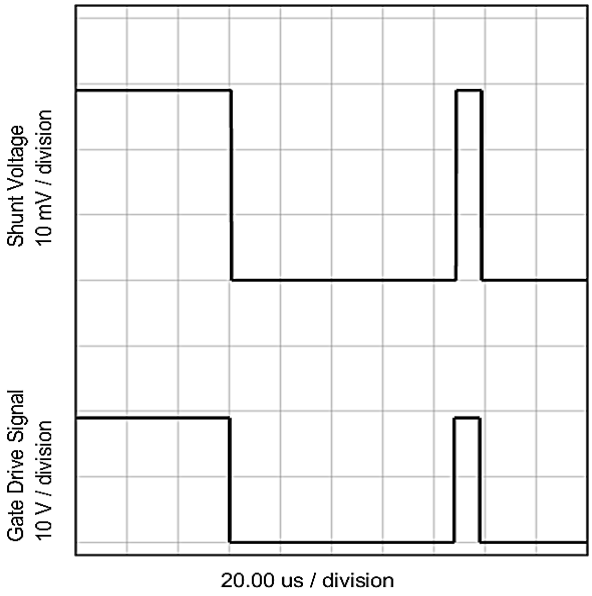
Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
on-state resistance	$R_{DS\ (on)}$	I_D = 50A	T_{vj} = 25 °C		3.7		mΩ
			T_{vj} = 150 °C		7.6	10.4	
			T_{vj} = 175 °C		8.9		

8. Characteristic Diagrams

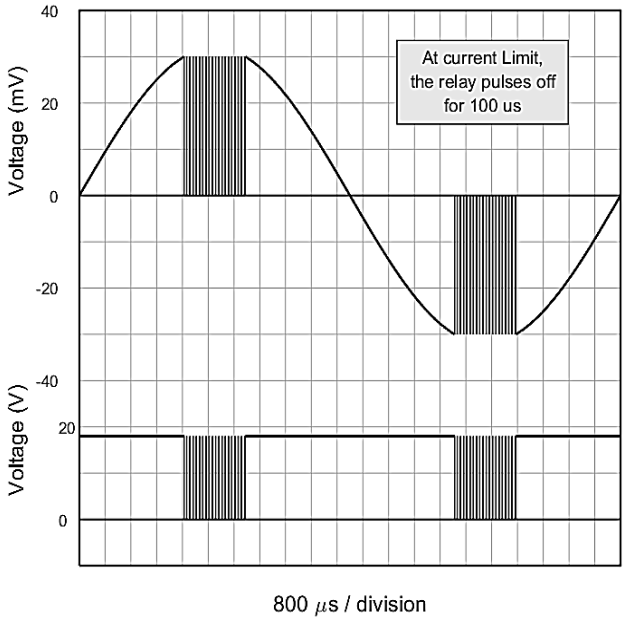
Voltage Across Shunt Resistor When Enable Signal Pulsed On/Off



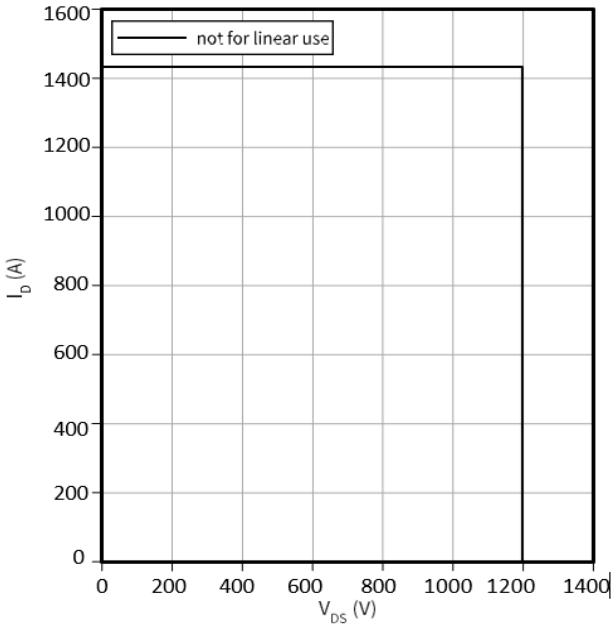
Voltage Across Shunt Resistor and Gate Drive Signal During Current Limit Event



Behavior during the current limiting event of the SSR



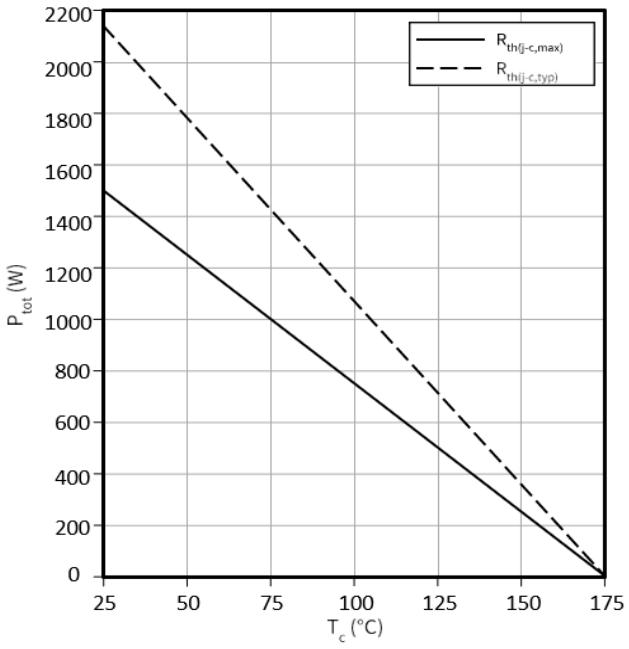
Reverse bias safe operating area (RBSOA)
$I_D = f(V_{DS})$, $T_{vj} \leq 200$ °C, $V_{GS} = 0/18$ V, $T_c = 25$ °C



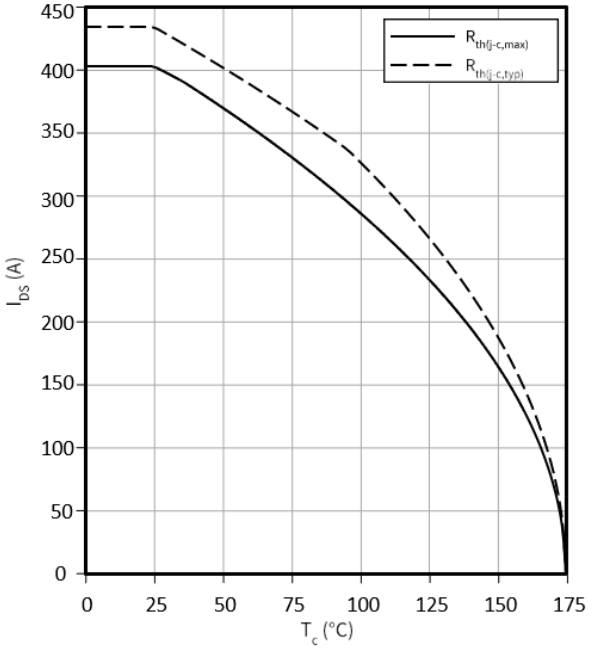
Characteristic Digarams – SSR, Ctd…

Power dissipation as a function of case temperature

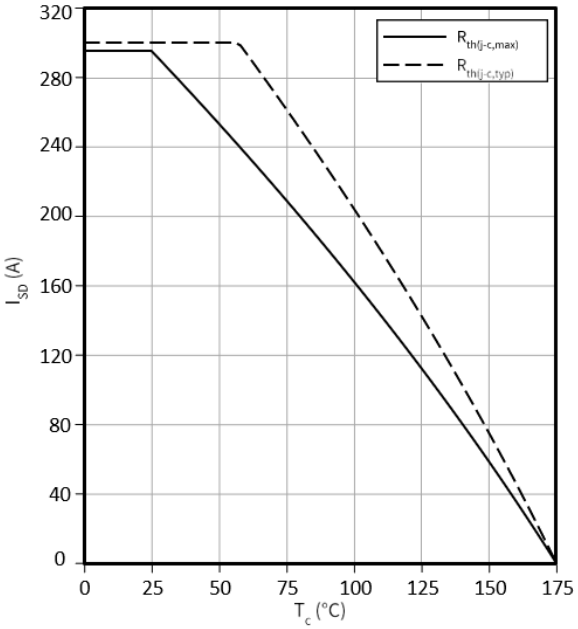
$P_{tot} = f(T_c)$



Maximum DC current as a function of case temperature limited by bond wire $I_D = f(T_c)$



Maximum current as a function of case temperature limited by bond wire $I_{SD} = f(T_c)$ $V_{GS} = 0$ V



Typical on-state resistance as a function of junction temperature $R_{DS(on)} = f(T_{vj})$ $I_D = 60$ A