The Role of High Thermal Conductivity Substrates in Future CMOS Technologies

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sp³ Diamond Technologies

Outline of Presentation

- Current Trends – Moore's Law
- Silicon and SOI Thermal Limits
- Diamond based SOI (SOD)
- Performance Benefits and Results
- Current Status and Application Areas
- Summary

Device Density Trends

Moore's Law continues to be the benchmark

Transistors Per Die

10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10^{1}
10^{0}

1965 Actual Data
MOS Arrays
MOS Logic 1975 Actual Data
1975 Projection
Memory
Microprocessor

1K
4K
16K
64K
256K
1M
4M
16M
64M
128M
256M
512M
1G
2G
4G

4004
8080
8086
80286
i386™
i486™
Pentium®
Pentium® II
Pentium® III
Pentium® 4
Itanium™

1960
1965
1970
1975
1980
1985
1990
1995
2000
2005
2010

(Courtesy: Intel© Corporation)

Power Density Trends

Moore's Law continues to be the benchmark

Transistors Per Die

10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
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Memory
Microprocessor

Bipolar
NMOS
Bulk CMOS
SOI CMOS

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4K
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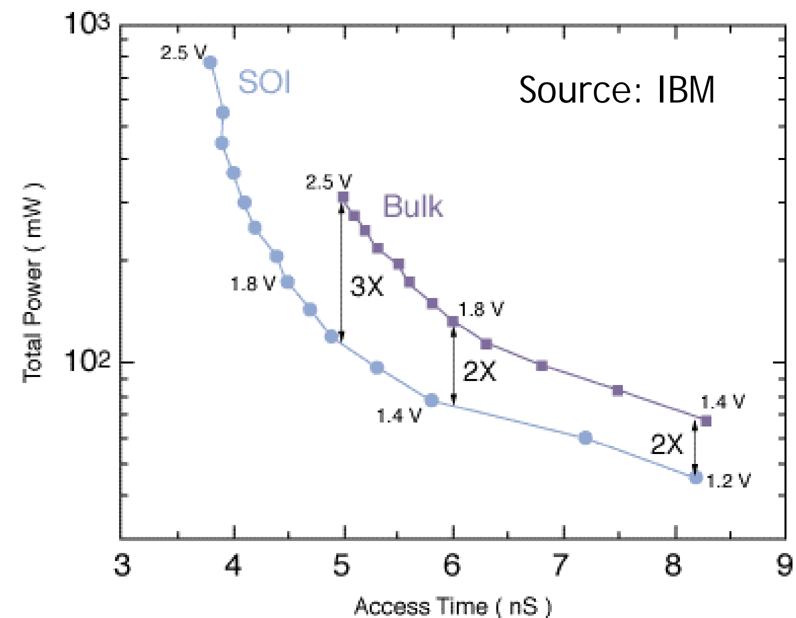
One Fallacy of Moore's Law-Thermal Limitations

- Increased Device Densities Cause Increased Thermal Energy
- Device Performance Limited by Heat Removal Rates
- Causes for Increased Power Densities
  - Higher Packing Densities
    - More gates per square centimeter
  - Channel Off Leakage Currents
    - Short Channel Effect
  - Dynamic Switching Currents
    - Shorter channels result in higher currents

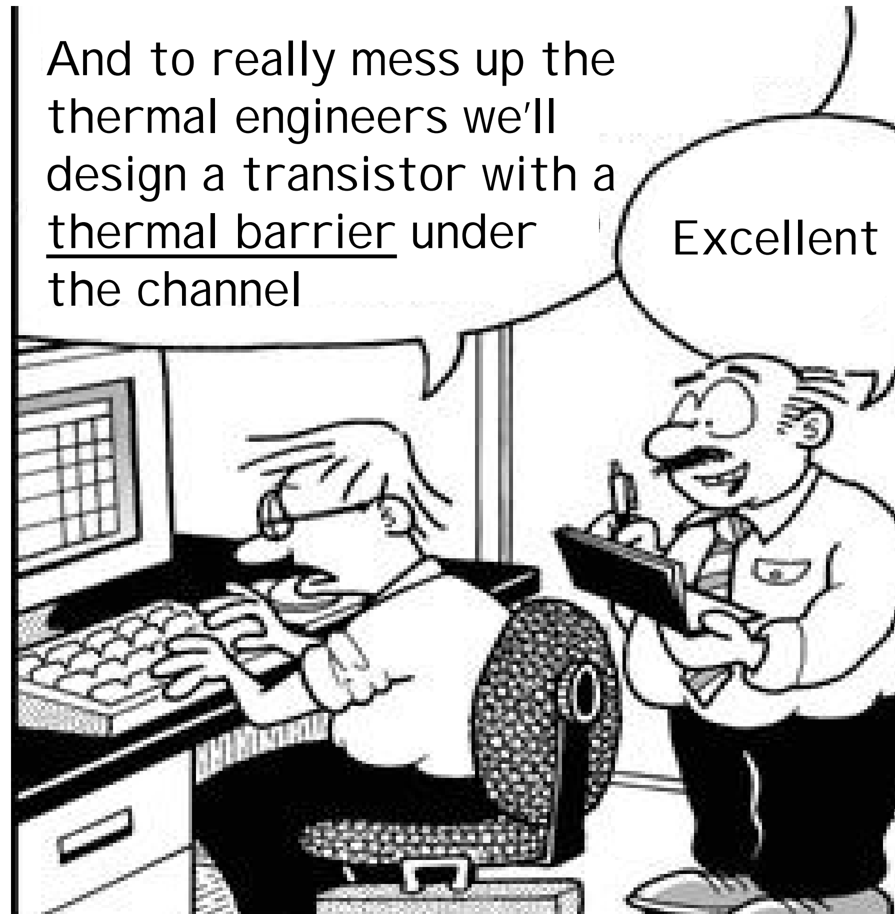
SOI – Half of the Cure

- Reduces Channel Off Leakage
- Reduces capacitance which reduces power/gate for a fixed speed

BUT!



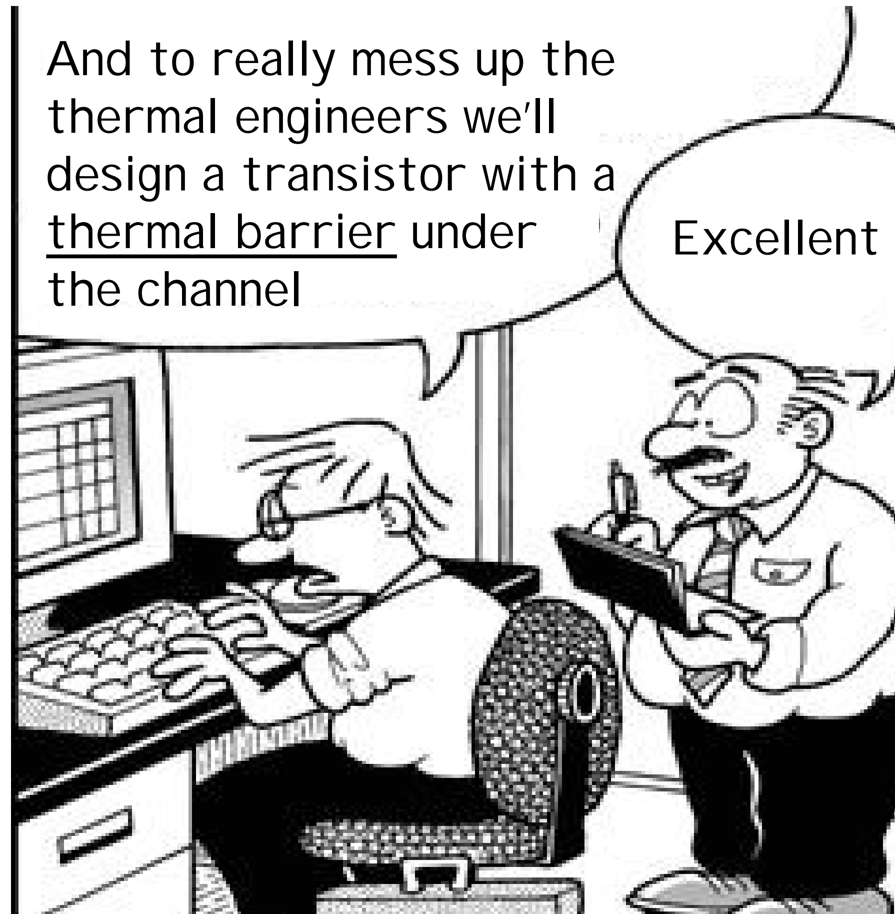
What Have We Done to Ourselves?



What Have We Done to Ourselves?

SiO_2 has a thermal conductivity of 1.4 W/m-K or ***1%*** of Silicon

Oops!



Even Low Power CMOS and Analog CMOS on SOI Can Have Issues

- Localized high activity can lead to local temperature non uniformity
- Oxide layers make the problem worse
- V_T and β are very sensitive to temperature.
- Large blocks dissipating a lot of power on a chip can induce differences in devices which are not on the same isothermal curve leading to severe device mismatch.

Non Uniform Temperature Effects on Digital Circuits

- Examples of digital circuits sensitive to mismatch are memory cells and clock distribution circuits.
- In the case of memories, the difference in the threshold voltages of two transistors of the same memory can be of the order of 100mV or more.
- Mismatch in general reduces the immunity to noise in digital circuits.

Non Uniform Temperature Effects on Other Circuits and Devices

- Analog CMOS circuits suffer from offset problems, nonlinearity, and general noise issues in very low noise devices.
- Power devices such as LDMOS can have significant current nonuniformity due to local gain variations

Solving the Other Half

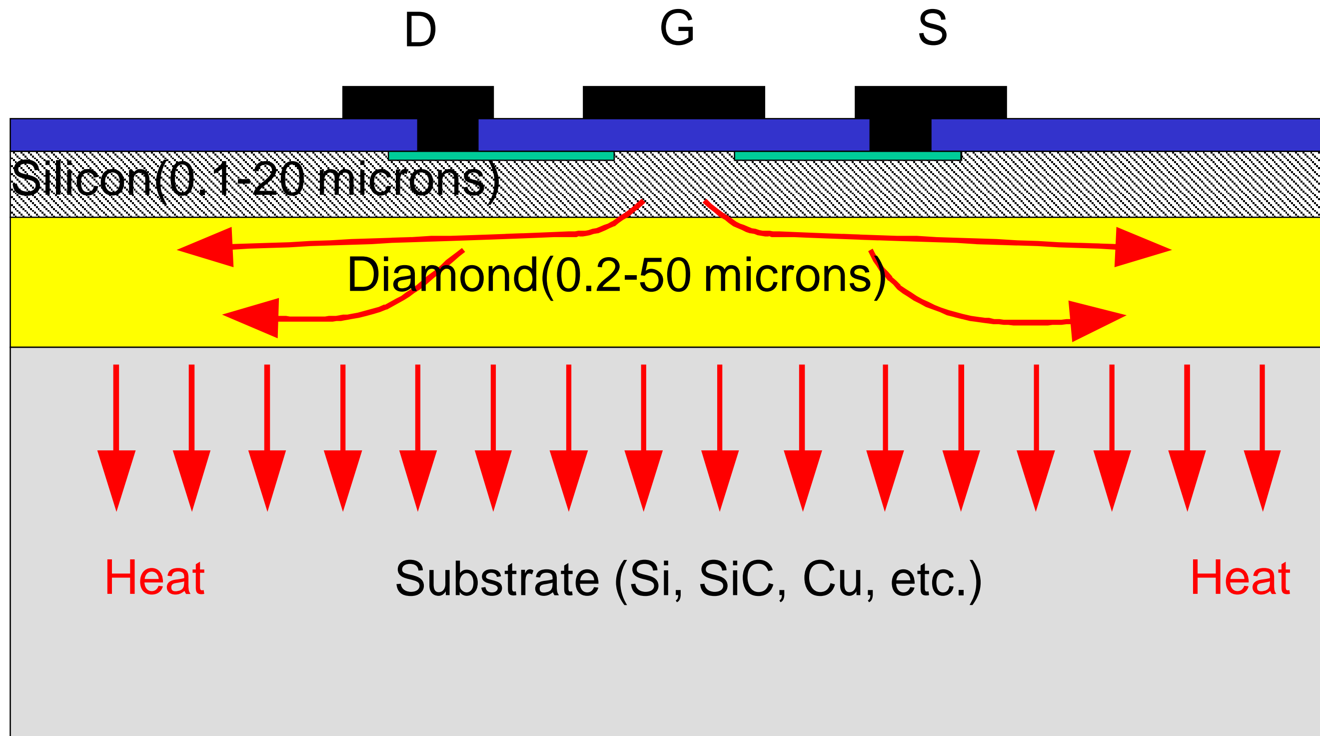
- Remove All Thermal Barriers and Add Heat Spreading
- Replace the I (SiO_2) in SOI with a high thermal conductivity material like diamond
- The resulting silicon on diamond (SOD) structure has no thermal barriers.
- Why Diamond?

Why Diamond?

- Highest possible thermal conductivity
  - 1000X SiO_2, 10X Si or thick AlN, 2-4X SiC or Cu
- High Young's modulus
  - 10X Si – 5 microns Diamond = 50 microns Si
- Low loss tangent – Good for RF and Microwave Frequencies
- High Breakdown Voltage – 30X Si, 1X SiO_2
- Can be grown cost effectively on 300 mm wafers
- Can be doped to make conductive

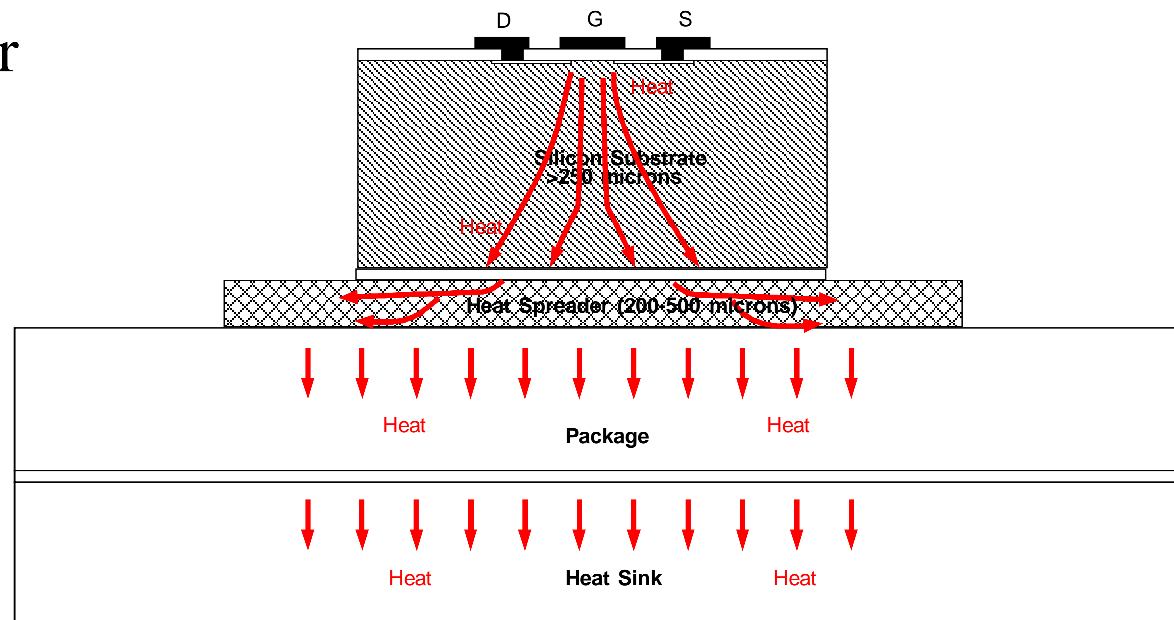
SOD Substrate

Silicon on Diamond (SOD) Technology



Heat Flow Path for Silicon Technology

- Device Layer
- Silicon Substrate
- TIM 1 layer
- Heat Spreader
- Package
- TIM 2 layer
- Heat Sink



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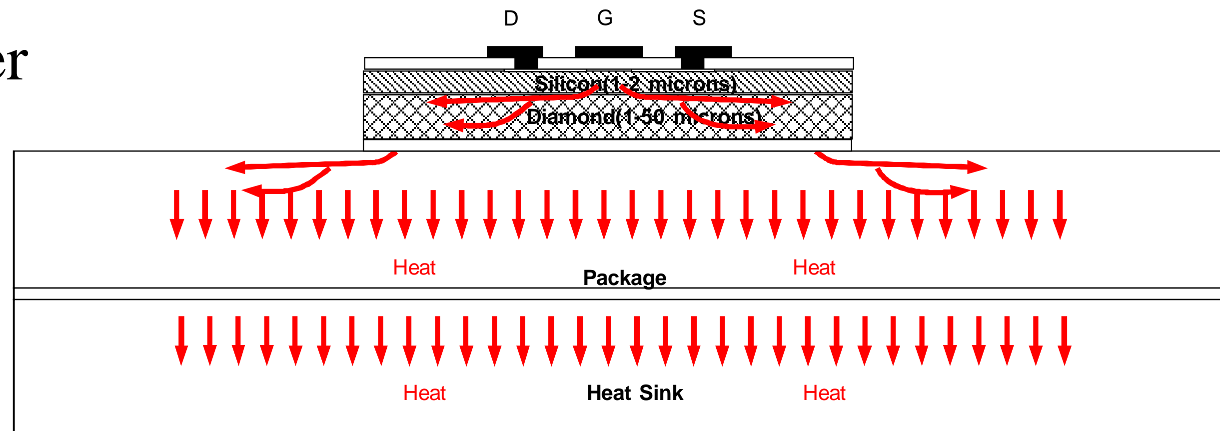


SOD Substrate Types

Thin SOD

- Substrate – 500 um
- Device Silicon
  - 100 - 2000 nm
- Diamond thickness
  - 150 - 500 nm
- Properties
  - High Vertical TC
  - Good Lateral TC
  - Moderate BV
  - Easiest to Fabricate

Thick SOD

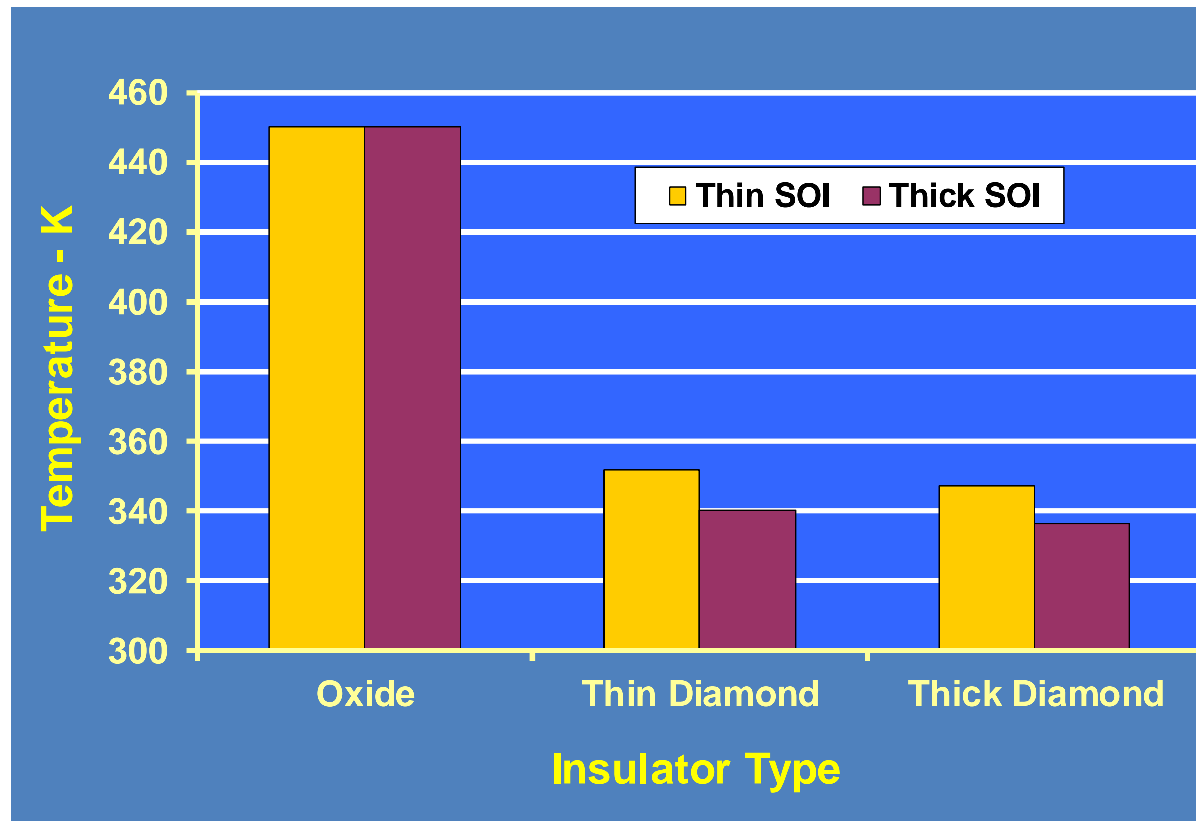
- Substrate – 500 um
- Device Silicon
  - 2 - 10 um
- Diamond thickness
  - 1 - 50 um
- Properties
  - High Vertical and Lateral TC
  - High BV
  - Free Standing at 10 um
  - Hardest to Fabricate

Application Areas

- Thin SOD - < 1 micron diamond
  - Microprocessors
  - SoC
  - Portable Wireless – RF
  - Low noise analog
  - HV analog and switching
- Thick SOD - > 2 microns diamond
  - Base Station Wireless - RF
  - HV Power switching - Automotive
  - BiCMOS
  - LDMOS
  - Bipolar
  - Substrates for Compound Semi Epi Layers (GaN on SOD)

Effects of Diamond on Junction Temperatures

Constant Power



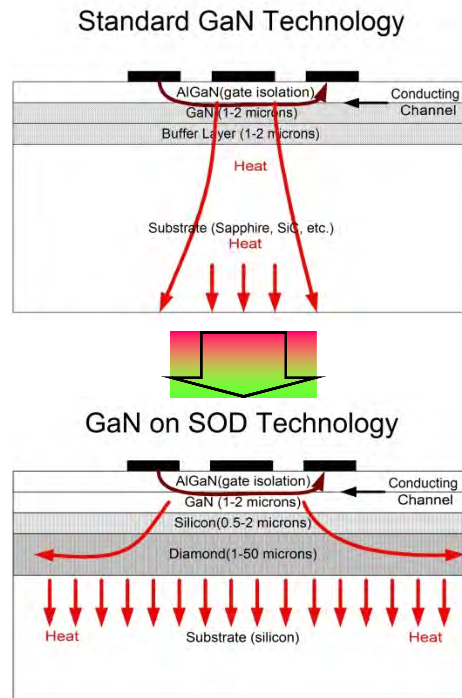
GaN on SOD (Silicon On Diamond)

The Solution to High Power Density Thermal Management

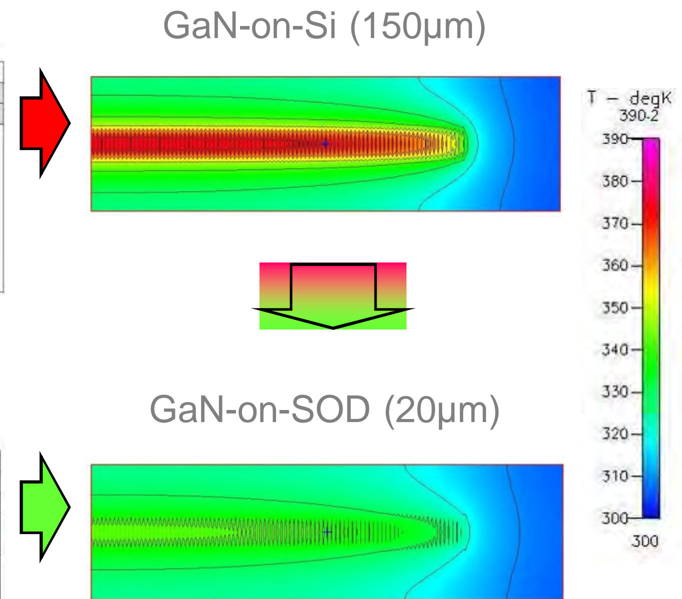
Benefits

- Diamond Heat spreading directly under the junction
- W/mm increase at fixed T_j
  - >100% vs. silicon
  - 50-80% vs. SiC
- T_j reduction at fixed power
  - >50 degrees vs. GaN on silicon or SiC.
- GaN growth on SOD yields films equivalent to GaN on silicon.
- Wafer size can be scaled to 300 mm.

Structure

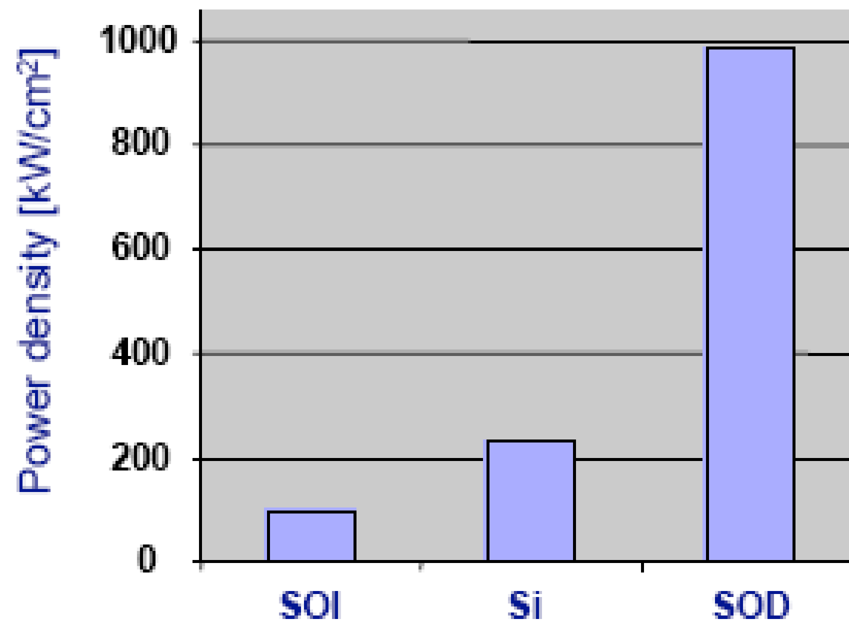


Thermal Improvement



Nitronex Data

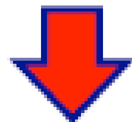
Measured Power Improvement for Constant Junction Temperature Thick SOD



Diamond- ~200 um

Silicon – ~2 um

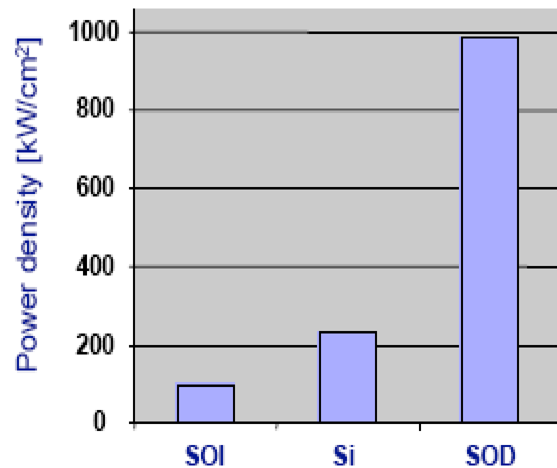
NCSU Data

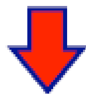


SOD power density input = 10 x SOI

Typical GaN on SOD Power Density Results

NCSU
Silicon Results



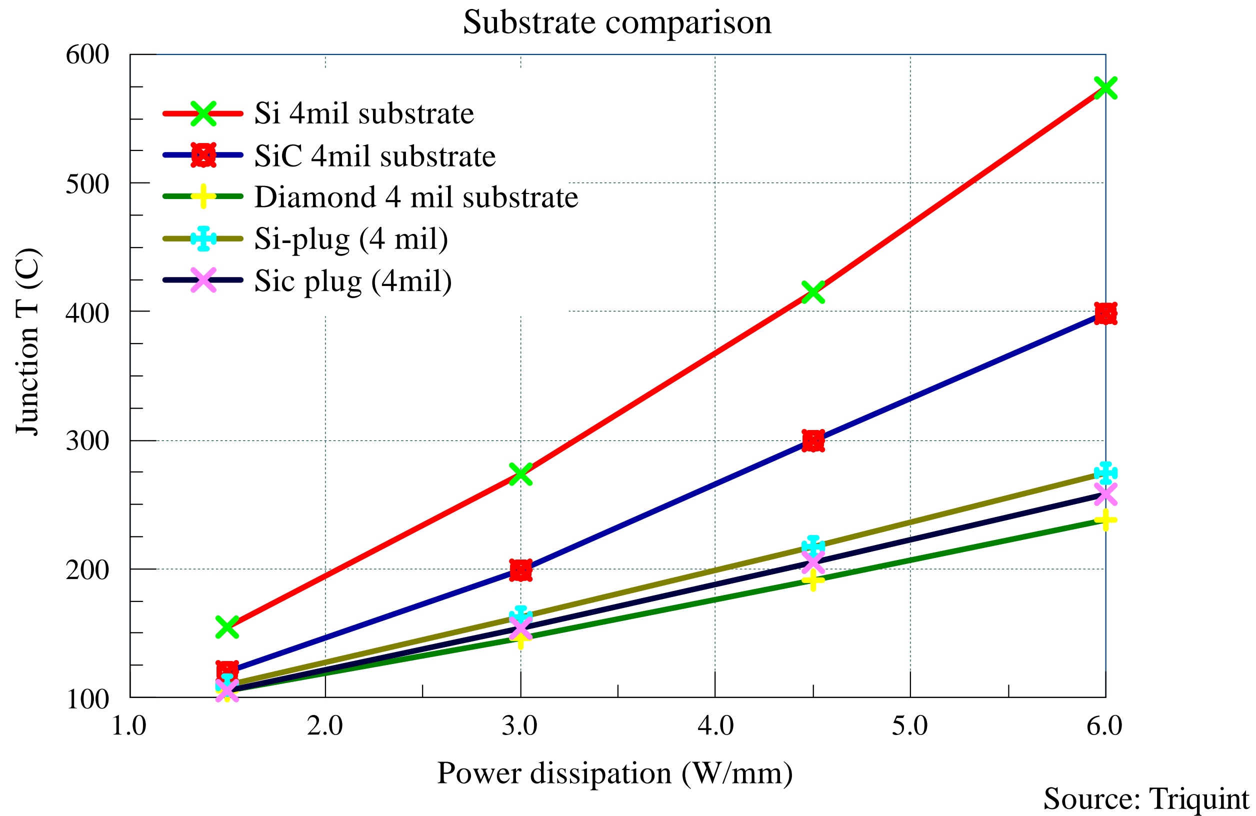


SOD power density input = 10 x SOI

GaN on SOD

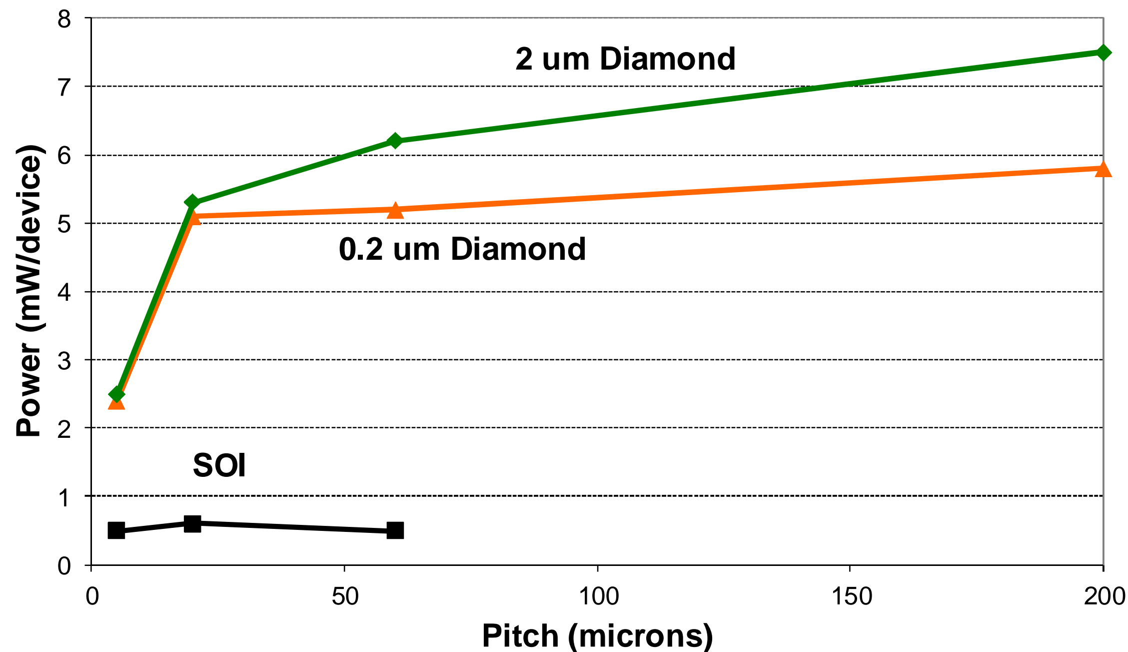
- 6 W/mm at T_j = 110C
- Power Density = 2000 kW/cm^2
- 5.5 micron Diamond

Modeled Thermal Improvements for GaN on SOD



Source: Triquint

Multi-gate CMOS Model



50 nm Silicon

200 nm Oxide

Diamond

Silicon Handle

Maximum power output for a 100C temperature rise

Feygelson, K.D. Hobart, J.E. Butler, Fabrication of Silicon-On-Diamond Substrates

Application Matrix- Where Can You Use It?

- CMOS Microprocessors
- Analog and RF CMOS
- Low noise analog
- HV and RF Power Devices – LDMOS, VDMOS
- Stacked Die Products – TSV interposers
- HV and RF GaN Devices
- VCSEL’s (Vert. Cavity Surface Emitting Laser)
- LED’s

Current Status of SOD

- GaN on Thick 100mm SOD is the best understood
- CMOS Level Silicon Quality/Purity has been verified
- CMOS processing on SOD is being investigated by sp^3 reactor customers
- 300 mm flat diamond on silicon substrates have been demonstrated
- 300 mm SOD substrates have yet to be fabricated
- Thick SOD substrates are still expensive

Summary

- SOD substrates provide heat spreading directly under the junction not several hundred microns away.
- Efficient heat spreading close to the device can provide performance improvements of 2-5X compared to silicon and up to 10X compared to SOI substrates.
- Works equally well on both silicon and compound semiconductor devices.

Questions

Single Chamber
Hot Filament Reactor

Dual Chamber Hot Filament Reactor