SOD Substrates – The Next Step in Thermal Control

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Today's semiconductor industry faces significant challenges in continued implementation of Moore's law due to the impact of increasing power densities on logic chips resulting from device density increases coupled with power increases to achieve faster and faster speeds. Both of these lead to increasing thermal loads on packages which do not have adequate thermal pathways for removing the heat. This same scenario is true in both the silicon world and the compound semiconductor world where RF power devices and high luminance LED's and laser diodes create similar heat flow problems. Historically, devices were mounted into packages using soft or hard solders and packages were attached to heat sinks using thermal grease as an interface material. Package materials were typically poor thermal conductors in the case of logic circuits and the thermal grease represented yet another significant thermal resistance in the system. The resulting thermal path included both the full thickness of the die as well as the other components just discussed. As chips areas increased the die attach method moved to epoxies to manage stresses at the interface and this resulted in even higher thermal resistances. Eventually the packaging industry moved to solder bump flip chip bonding and then the problems became even worse because neither side of the chip was in direct contact with the package. This problem was reduced by introducing another thermal interface material (TIM) between the chip and the package lid which is not as good as solder but better than nothing.

That general scenario of silicon chip, TIM, package, TIM, and heat sink defines current technology today for silicon devices. An additional problem is that heat is not generated uniformly on the chip so that some locations are significantly hotter than others. This is also true for devices in the compound semiconductor world such as RF power devices, LED's and VCSEL's. The current solution to this problem is to attach the device directly to a heat spreader so that heat is distributed across the entire area of the chip rather than being localized to specific areas. Unfortunately this still requires the heat to be extracted through the entire thickness of the silicon chip prior to reaching either a heat spreader or a heat sink. For some of the newer circuits being built on SOI substrates the problem becomes even worse because the heat has to pass through an oxide barrier in the SOI structure which has less then 1/100 the thermal conductivity of the silicon. The solution for all of these problems is to place a heat spreader as close to the heat generating areas as is physically possible. If this heat spreader layer is constructed of diamond then it can replace the oxide layer in an SOI structure and the device generated heat only has to move a few microns before it is spread across the entire area of the chip. The net result is to reduce both the local junction temperature as well as the overall chip temperature since the heat flow path is now the full area of the chip itself.

SOD wafers as shown in Figure 1 are basically equivalent to SOI wafers but the insulator (I) in SOI is diamond rather than silicon dioxide. The top layer silicon thickness is a micron to tens of microns thick depending on the specific application and the diamond layer is several microns thick again dependant on the specific application. The underlying substrate is a full thickness silicon wafer which serves as a handle for processing and can be either thinned or completely removed prior to packaging. Diamond at this thickness has a thermal conductivity that is 2-3 times greater than copper and 10 times greater than silicon.

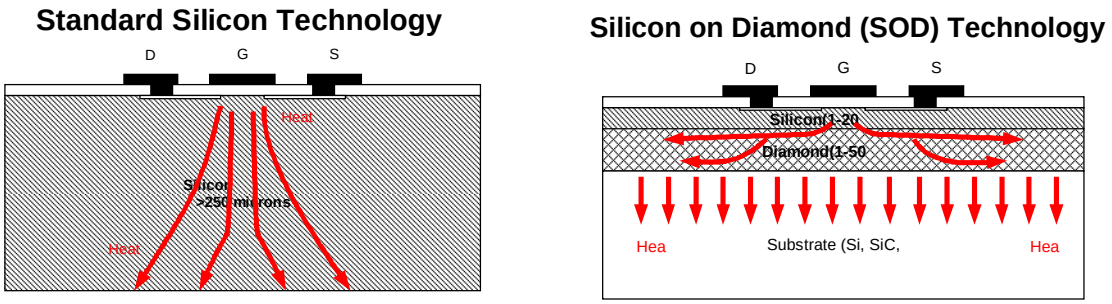

Figure 1

This high thermal conductivity means that several microns of diamond can effectively equalize temperatures across an entire chip at the device junction level. Local power densities of hundreds to thousands of watts per square mm in logic chips are spread quickly over the total area of the chip and reduced to a few hundred watts per square centimeter at most. Heat flux at this level can be handled much more easily by initial TIM layers and subsequent heat spreaders and heat sinks as shown in Figure 2.

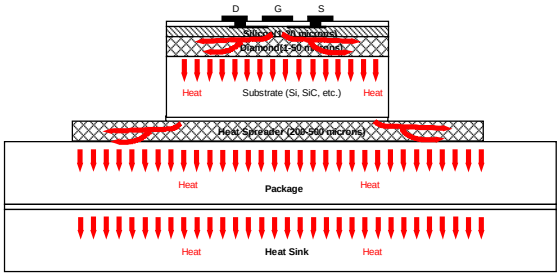

Figure 2
Heat flux in ideal packaged SOD device

The limit of this technology is determined by the ability of the TIM layers, package materials and heat sinks to remove heat from the diamond layer. Under actual measured conditions, power densities as high as 1000 W/cm2 with junction temperatures below 120C have been shown to be possible on silicon devices on SOD substrates. This compares to 200 W/cm2 for equivalent thicknesses of silicon substrates and less than 100 W/cm2 for SOI substrates. These results from work done at NCSU by Dr. Sitar are shown in Figure 3.

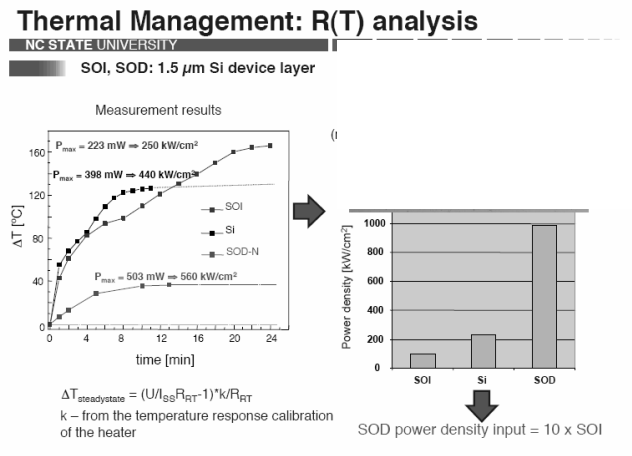

Figure 3
Measured Tj and performance as a function of substrate type

Application areas for this technology span a broad area of electronics. In the silicon world, high density, high speed logic chips such as microprocessors and video processing chips make up the most obvious area. Additional silicon product areas are discrete power devices, analog power IC's and MEMS devices such as DLP chips. There are also applications in stacked die devices where localized hot spots on one chip can affect performance on the adjacent chip. Applications in compound semiconductor devices are equally broad. The emerging market of high frequency RF power devices used in cell phone base stations and wireless applications are beginning to use GaN HEMT transistors where the GaN device layer is grown on either SiC or silicon substrates. Both of these can be replaced with SOD substrates with substantial improvements in device performance and/or reduced junction temperatures as shown in Figure 4. For the growing white light LED market, the color balance of the typical three color LED unit is determined by temperature stability between the devices. New GaN LED processes can produce all three colors on one chip which can be temperature stabilized using SOD substrates. Likewise the newest vertical cavity surface emitting laser diodes (VCSEL's) can be made on GaN on SOD substrates which allow much higher power densities and luminosity than standard products.

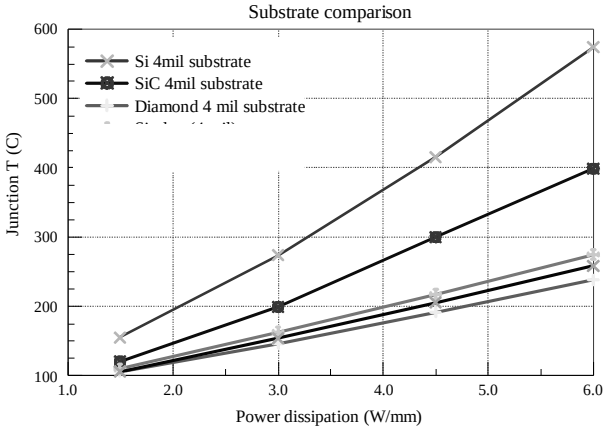

Figure 4
SOD performance on various substrates – courtesy of Triquint Corp.

All of these products are possible and will evolve over the next decade from concept to mainline production if Moore's law holds true for the silicon world and if high performance wireless devices and solid state lighting evolve as expected in the compound semiconductor world. Each substrate will be customized to the application to optimize the thermal performance so the substrate variations will be as broad as the product application areas. Eventually all high performance high efficiency semiconductor devices will require the use of a heat spreading material such as diamond as close to the junction as is possible.