Advances and Challenges in Large Diameter Silicon on Diamond Substrates

Jerry W. Zimmer and Gerry Chandler

sp3 Diamond Technologies, Santa Clara, CA jzimmer@sp3inc.com, gchandler@sp3inc.com

INTRODUCTION

Today's semiconductor industry is constantly grappling with the challenges of good thermal management in a wide variety of devices including high speed microprocessors, RF power devices, power switching devices, high luminance LED's and laser diodes. High thermal conductivity packages, heat spreading sub mounts and other techniques have been in use for many years to control heat at the package level. More recently technologies using thinner die and higher thermal conductivity substrates have been implemented as chip power is pushed to higher and higher limits. Silicon carbide is now a common substrate for GaN RF devices and diamond which is the ultimate in high thermal conductivity substrates has also been used as a thermal substrate for GaN HEMT devices in small sizes [1] [2].

Many devices such as microprocessors, RF power and power switching devices require large area substrates to be economically viable however. To date, no one has reported fabrication of any active semiconductor devices on diamond based substrates larger than two inch diameter. Nor has anyone demonstrated that devices can be made with reasonable yield over large areas. Issues of the cost of thick diamond substrates and flatness of thinner diamond substrates have limited existing work to relatively small sizes but the use of SOD (silicon on diamond) substrates directly for silicon or SiGe technologies or with GaN epi layers for compound semiconductor devices has largely circumvented this limitation. SOD substrates can now be made in 100 mm diameters and can be potentially be scaled to sizes up to 300 mm diameters. GaN epilayers have been successfully deposited on these substrates and active devices have now been fabricated which show the viability of the technology as well as the potential for reasonable production yields over large areas.

DISCUSSION

100 mm SOD substrates were fabricated using hot filament diamond deposition on high resistivity float zone silicon wafers and subsequently flipping and grinding the original substrate to create a thin single crystal silicon layer suitable for silicon or SiGe technologies or in this case as a seed layer for the GaN epi layer. Figure 1 shows the structure of the SOD wafer where the thickness of the silicon layer is a function of the particular process technology.

Silicon on Diamond (SOD) Technology

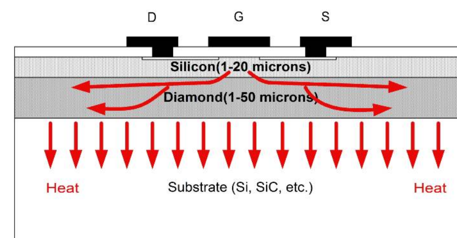

Figure 1

For compound semiconductor applications the silicon layer is minimized and MOCVD technology is used to grow the buffer, GaN and AlGaN device layers in the case of an RF HEMT device. This is shown in Figure 2. In this particular work GaN devices layers were shown to be of sufficient quality to make functional HEMT transistors as reported previously [3].

GaN on SOD Technology

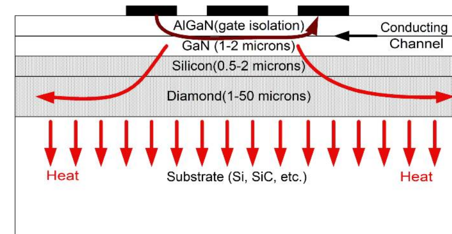

Figure 2

Subsequent to GaN growth, devices were fabricated using a standard mask set and process for HEMT devices. Prior to fabrication it was decided to cut one wafer down to 50 mm diameter to allow making a smaller gate length device. Devices were then fabricated on both wafers and electrically tested in whole wafer format with the handle wafer attached. The handle wafer was then removed from one wafer and that wafer will be mounted on a copper heat sink to allow further testing of thermal performance.

RESULTS

Both wafers were processed without significant problems and yielded functional HEMT devices. Figure 3 shows the finished 100 mm wafer which has a 3x4 inch functional area as a result of a polishing defect in the silicon layer.

Figure 3
100 mm GaN on SOD Wafer

Figure 4 shows the finished 50 mm wafer. The primary device which was characterized on these wafers consisted of a 2 gate transistor with 0.35 micron gate lengths and 150 micron gate width. This is shown in Figure 5 and Figure 6 which is a cross section showing the 0.35 micron gate length.

Figure 4
50 mm GaN on SOD Wafer

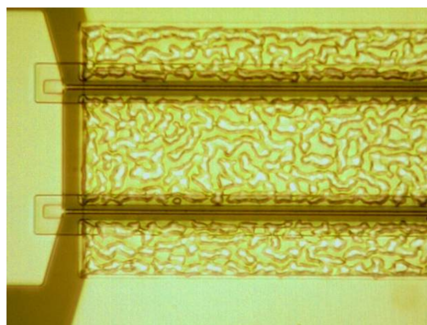

Figure 5
Portion of tested HEMT device

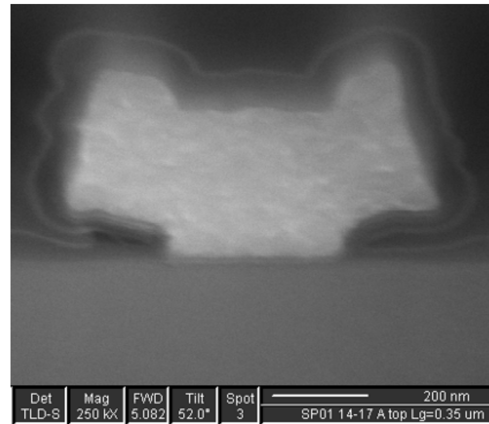

Figure 6
Cross Section of 0.35 micron transistor

Approximately 160 of these devices were electrically characterized in the functional area of the first wafer and a slightly smaller sample on the second wafer. Table 1 is a summary of the average results of that characterization. The data shows that functional devices can be made on these wafers and that the basic parameters are consistent with the geometry of the device and the characteristics of the GaN epi layer. The more important question however is whether or not this can be duplicated across the whole wafer and on more than one wafer. To answer that question requires examination of the distribution of the parametric data both statistically as well as spatially on the wafer.

Table 1
Summary of Wafer Test Results

Parameter	Wafer 1 Passivated	Wafer 2 Passivated
gmp (mS/mm)	213	223
IDS,max (mA/mm)	644	512
IGL (mA/mm)	-7.0x10-5	-2.6x10-6
fT@Gmp (GHz)	24.9	31.4
fMAX (MAG) @Gmp (GHz)	45.8	44
Device VBR (V)	50	47
Vth (V)	-1.35	-1.0

Figures 7 through 11 show the wafer maps and statistical distributions for selected device electrical parameters. Verification of the general quality of the GaN layer can be achieved by looking at the breakdown voltage of the devices on wafer 1(Figure 7). The maximum tested value was 50 volts for this parameter and virtually all devices had values above this level regardless of position on the wafer. The low level and random distribution of bad devices indicates that there are minimal fundamental structural problems with the GaN epi layer. This is supported by the gate leakage data for wafer 1 shown in Figure 8 where the distribution of high

leakage devices is again fairly random although some clustering does exist toward the edges of the tested area.

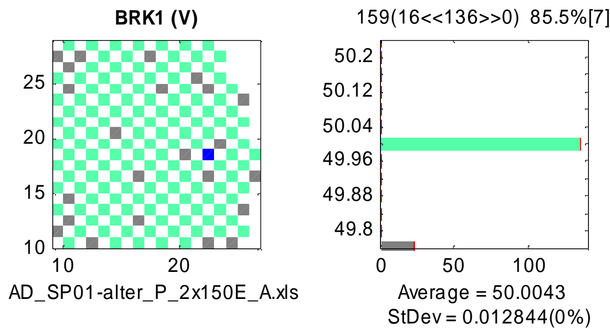

Figure 7
Breakdown voltage

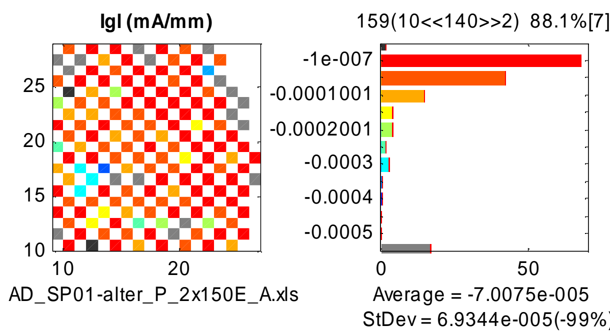

Figure 8
Gate Leakage Current

Given the consistency of the most basic parameters it is now practical to examine the actual device performance characteristics. Figure 9 shows the maximum source drain currents for the device which is a standard measure for device channel quality. Maximum values are again clustered towards the edge of the wafer and the 90% yield shows the potential for high yields over large areas. Compared to equivalent devices built on GaN on silicon wafers the values are slightly low which may be due to differences in composition of the channel layer or stress in the films. This issue remains to be investigated in detail.

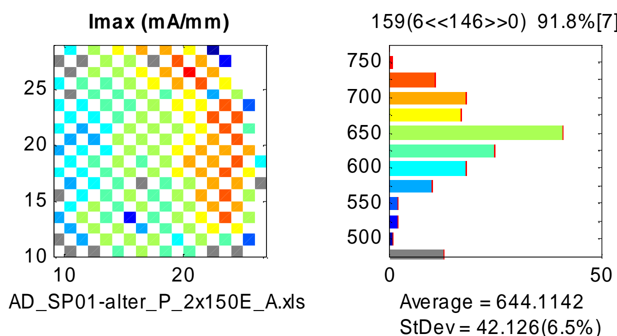

Figure 9
S/D Imax – ma/mm

Finally, if the frequency response of the devices is measured, we find that the values are consistent with the measured device geometry. Figures 10 and 11 show values and distributions for f_{max} and f_t. Again, defective die are randomly distributed and lower values are clustered toward the edge of the wafer where gate lengths were slightly longer.

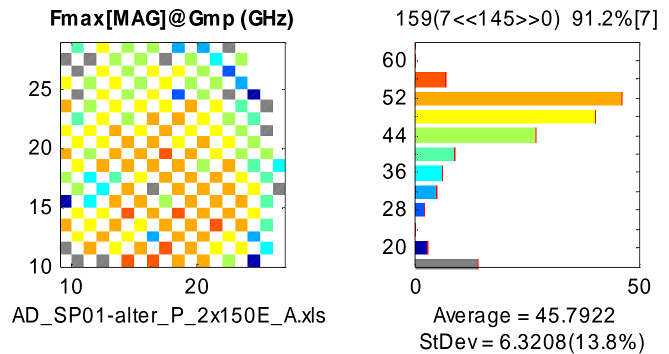

Figure 10
f_{max}

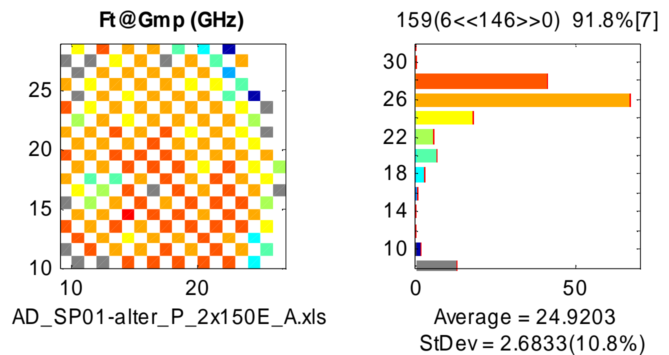

Figure 11
f_t

Values and distributions of these parameters for wafer 2 were similar although slightly lower but still demonstrated that reasonable yields of functional devices could be achieved.

Significant work remains however. Figure 12 shows the DC and pulsed IV characteristics of a device where significant thermal droop is evident in the DC data. This measurement was done on a full wafer which had not yet had the silicon handle wafer removed but it clearly shows the necessity of performing this step so that the diamond layer is in direct contact with a cooled surface.

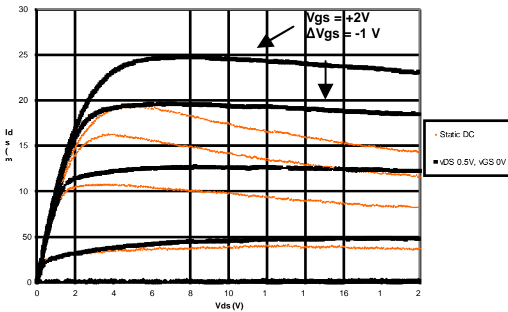

Figure 12
DC and pulsed IV plot showing thermal droop

The high Young's modulus of diamond allows the complete removal of the silicon handle wafer which was used for processing the wafer and this leaves only three layers between the device junction and the package. Figure 13 shows a FIB cross section of the wafer before the silicon handle was removed and 14 shows a cross section of the structure after handle removal where the stack consists of the GaN epi layer, the silicon buffer layer used for the GaN growth, and the diamond substrate.

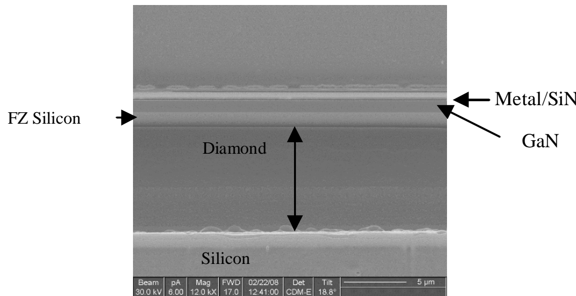

Figure 13
FIB Cross Section of Wafer

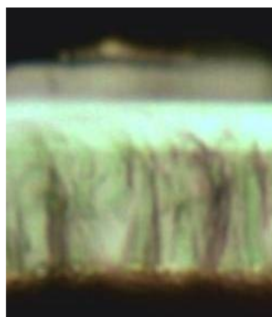

Figure 14
Cross section after handle removal showing all layers

In full wafer form the thermal performance can be measured and compared to models to determine the expected performance after silicon handle removal. Figure 15 shows that comparison where the junction temperature is modeled for both the device including the silicon handle and with the silicon handle removed. This is compared to actual temperature measurements of the device with handle silicon attached and an equivalent device on a thermally conductive silicon carbide substrate. The results show that for this particular substrate stack the device performance will be substantially better than GaN on silicon and roughly equal to GaN on silicon carbide performance.

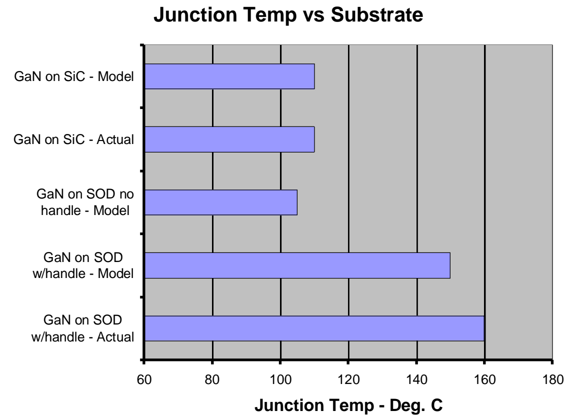

Figure 15

CONCLUSIONS

Silicon on thermally conductive diamond substrates provides a path for increasing both power dissipation and reliability on silicon and compound semiconductor technologies such as GaN. The substrates must be fabricated at high quality levels and at large diameters to meet manufacturing economic goals however. This work has now demonstrated that for high power GaN technology where 100 mm wafers are just evolving these devices can be fabricated on 100 mm SOD wafers with yields sufficient to meet manufacturing goals. Much remains to be done to reach full manufacturing readiness but there do not appear to be any blocking issues in implementing this technology on a variety of compound semiconductor devices including power RF, power switching, high luminance LED's and VCSEL laser diodes. In addition, the technology can be scaled to 200 and 300 mm wafers where silicon and SiGe technologies can benefit from the improved thermal performance.

ACKNOWLEDGEMENTS

The authors would like to thank the staff at AFRL including Gregg Jesson, James Gillespie, and others for the device processing and electrical testing and Edwin Piner and John Roberts at Nitronex for the GaN deposition.

REFERENCES

[1] GaN-HEMT Epilayers on Diamond Substrates: Recent Progress, D. Francis, J. Wasserbauer, etal., CS Mantech 2007, pp 133-136.

[2] Comparison of GaN HEMT's on Diamond and SiC Substrates, L. Eastman, etal., IEEE Electron Device Letters, 2007.

[3] GaN on SOD Substrates – The Next Step in Thermal Control, J. Zimmer and G. Chandler, CS Mantech 2007, pp 129-132.