VELOCITY

Faster TTM with Velocity

- One Common interface
- Parallel Conversions
- Customizable & Flexible
- Pre-Silicon Validation with REPLAY
- Burn-In Links
- Same Day Support
- 1 day Training
- No Perl scripts required
- Automated setup
- Built-in Intelligence

Velocity Features

- ATE Rules Checking
- Design File Analysis
- MultiPort/MultiTime Domain
- DataRate/XMODES
- Port Tracking
- Optimized Vector Compression
- Automated Editing Language
- Logical Masking
- Pattern Bursting
- Multi-Simulation merging (MCM)
- REPLAY to Design with Verilog
- Simulation Resampling
- Vector size analysis
- Scan Flop logging links
- GUI & Batch Interfaces

Velocity – Smarter, Faster, Easier!

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VELOCITY CAE TESTING AT THE SPEED OF LIGHT

VELOCITY
EDA & ATE Specifications

Testers

- Advantest
  - XSCALE, 93K, 83K
  - T2000, CTS
  - EVA
- Teradyne
  - Flex, UltraFlex, UltraFlexPlus, J750
  - ETS
  - Magnum, Catalyst
- LTX/Credence
  - Fusion, ASL, Quartet, Diamond
- Test Evolution TEV
- National Instruments
- YTEC V50/100

EDA

- Simulator formats
  - WGL, STIL, EVCD/VCD & SVF
  - Verilog
  - User Defined
- Simulators
  - Mentor, Synopsys, Cadence
  - ModelSim, Icarus & Others
  - Custom

Lab-Links

- Protocols: JTAG, I2C, SPI & SMB
- Excel Spreadsheets, CSV
- XML
- User Defined Formats

Burn-In

- MMC, INCAL, Sierra & AehrTest
- Custom

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