

THE HIGH TECH TRIBUNE

The Evolution of the IC FET Technology

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Introduction: Transistors are the fundamental building blocks of modern electronics, enabling the operation of everything from microprocessors to memory chips, to networking all the way to advanced AI systems. The IC transistor technology follows Moore's Law (1965) guidelines pressing the IC transistor technology to advance, and it is leading to the exponential increase in computing power and the decrease in size and relative cost. Over As transistor sizes approach atomic scales in recent years, novel transistor architectures have evolved from conventional *planar FET* suited upto 28 nm nodes, to modern *FinFET that is suited for upto 7nm nodes*, and to the more recent and advanced *gate-All-Around FET* (*GAAFET*) that is suited for all the way to sub 2nm nodes.

In this article, we intuitively explore the evolution of FET transistors within IC fabrication technology. We gradually illustrate the transistor's progression starting from the PN junction as a fundamental block, and then we develop an understanding to the basic operation of the field effect transistor (FET), before exploring the advancement in the FETs IC technology from planar FET, to FinFET, and finally to GAAFET. We will highlight the reasons for each transition, the differences in fabrication processes, and the current state-of-the-art fabrication manufacturing.

The PN Junction as A Fundamental Block: The PN junction is a diode that is made by joining heavily doped p-type and n-type semiconductor. At the interface, a depletion region is created which acts as a barrier that blocks the current to flow in the reversed direction (from the n-type to the p-type), but it allows the current to flow in the forward direction, a voltage drop is observed across the diode. The forward voltage drop allows the charges within the pn junction to overcome the depletion region. If a reverse voltage is applied across the PN junction, the depletion width increases, thus preventing the current from flowing in the reversed direction. We can simply say that the PN junction is an uncontrolled switch, which allows the current to flow in the forward direction and block the current from flowing in the opposite direction. Understanding the basic behavior of the diode is essential to understand the operations of the FET transistor and its evolution within IC technology.

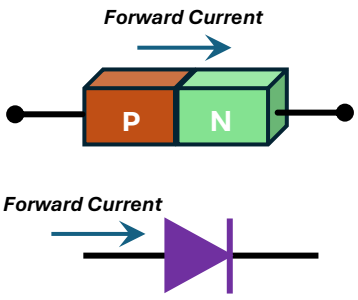

Fig. 1 Basic PN junction is a diode that passes current in one direction.

Two Back-to-Back Diodes: The Basic module of the FET is to have two back-to-back diodes. Two back-to-back diodes can be made by horizontally joining three layers of npn material, or pnp material, in consecutive order as shown in the figure. By joining two back-to-back pn junctions, there is not any current flowing the material, as each of pn junctions blocks the current from flowing in one of the two opposite directions. For example, if one diode is forward biased, the other diode will be reversed biased. Therefore, the two back-to-back diodes represent a normally closed switch that does not allow the current to flow in both directions.

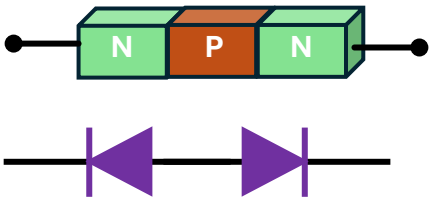

Fig. 2 Basic NPN back-to-back diodes that block the current in both directions.

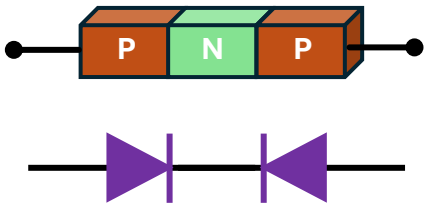

Fig. 3 Basic NPN back-to-back diodes that block the current in both directions.

Creating a Channel Using an Electric Field: From semiconductor physics, we also know the standalone n-type and the p-type material conduct current. By

adding impurities to the pure silicon and this process is called doping. In n-type material, Phosphorus is added to increase the number of free electrons, and the electrons are the majority carriers that carry current. Conversely, Boron is added to the p-type material to increase the number of free holes, thus holes become the majority carriers that carry the current. Thus, the conductivity of the dopped semiconductor material can be controlled by adjusting the amount of doping added to the pure silicon.

Also, we know that the two back-to-back diodes block the current in both directions, and let's call one terminal source and the other terminal drain. Now, the middle material can be inverted using electric from the middle layer to the source. As shown in the figure, applying a strong enough electric field from the middle p-type to the source, an n-channel is created in the middle p-type material as the electric field would attract free electrons from the n-type source. Once the channel is created, the current will flow across the drain source terminal. The channel behaves as a conductor that allows the current to flow. The conductivity of the channel is a function of the doping and intensity of the electric field. Now, the drain to source becomes a controlled switch such that when the electric field is strong enough, a channel is created allowing the current to flow. If the electric field is removed, then the channel disappears and the current stops from flowing.

Similarly, the electric field is now applied from the source to the middle n-type layer in the pnp back-to-back diodes. Here the holes in the source will be repelled by the electric field from the source to the middle layer. Thus, creating a p-channel from the source to the drain. This channel will allow the current to flow from the drain to the source. In the next section, we will show how the electric field is created using the concept of capacitor. The capacitor is two conductors that are separated by an insulator. When a voltage is applied across the capacitor, opposite charges accumulated on its conductors which creates an electric field within the capacitor.

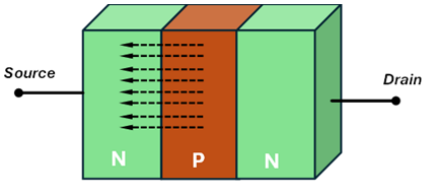

Fig. 4(a) Applying electric field from the middle material to the source of the npn junctions.

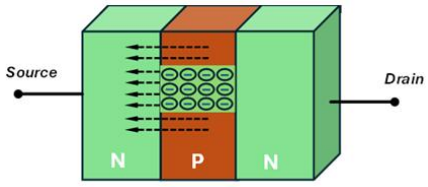

Fig. 4(b) The electric filed attracts electrons from the source to middle material creating a n-channel from the source to the drain

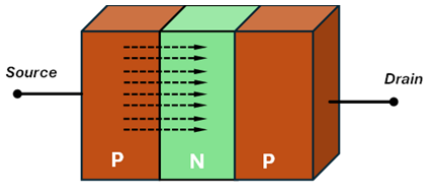

Fig. 4(c) Applying electric field from the source to middle material of the pnp junctions.

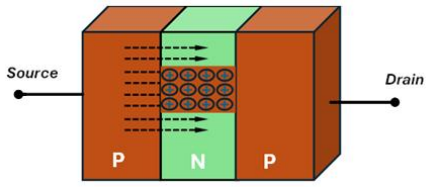

Fig. 4(d) The electric filed attracts holes from the source to middle material creating a p-channel from the source to the drain

The goal is to make the back-to-back diodes act as a controlled switch using a control voltage source. Such that the current would pass through the back-to-back diodes when a control voltage is applied. Basically, the back-to-back diodes conduct when a controlled voltage is applied, and it will turn off when the voltage is not applied.

Basic Structure of Planar FET Transistor: The basic structure of the FET transistor contains a capacitance that is used to create the electric field between the middle material and the source. The capacitor is created by adding an insulator (SiO_2 or high K material) on the top of the middle layer, and then by a conductor is on the top of the insulator. This conductor becomes the third terminal of the FET, and it is called the gate. The capacitor is used to create an electric field from the gate to the source. By applying a voltage from the gate to the source, an electric field is created. If the electric field is large enough it will attract electrons from n-type source (or attracts holes for the p-type source), thus creating a channel underneath the gate that links the source to the drain. Therefore, the gate to source voltage is used to turn the FET on or off. Note that the source and the drain are made of heavily doped material, to ease the creation of the channel.

Basically, by applying a voltage from the gate to the source, a channel is created making the transistor and allowing the current flow from the drain to the source. For the n-channel FET, the higher the gate to source voltage the more electrons are attracted to the channel. Hence, it has better conductivity. Equally for the p-channel FET, the higher the source to gate voltage, the more holes are repelled from the source to p-channel, the better the conductivity of the transistor. Thus, you can think of the channel as a variable resistor. The conductivity of the channel increases by increasing the gate to source voltage, the number of free charges increases which decreases its resistance. How the gate is manufactured positioned at the heart of IC technology evolution.

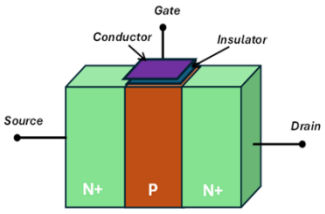

Fig. 5(a) The n-channel Planar FET with the gate, source and drain.

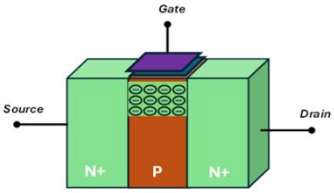

Fig. 5(b) The n-channel links the drain to the source, by applying a voltage form the gate to the source.

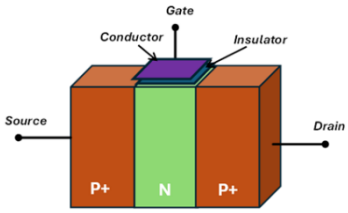

Fig. 5(c) The p-channel planar FET with the gate, source and drain.

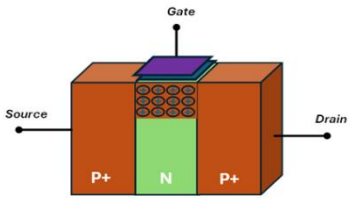

Fig. 5(d) The p-channel links the drain to the source, created applying a voltage form the source to the gate.

Basic FET Transistor Operation: The FETs are voltage-controlled switches with two types, n-channel and p-channel. When the FET is one, a channel is created from the drain to the source. The channel allows the current to flow in either direction. To create the channel, the gate-to-source Voltage must exceed some threshold value. This creates a strong enough electric field, within the gate-source junction, to move the majority carriers, electrons for n-type, holes for n-type, to the gate region. By increasing the gate-to-source voltage, more charges are moved to the channel. This makes the channel more conductive and less resistive. If we hold the drain-to-source voltage constant and increase the gate voltage, then the drain to source current increases as the conductivity of the channel increases.

Now, if the gate-to-source voltage is kept constant above the threshold value, and the drain-to-source voltage is slowly varied. Initially, the drain current increases linearly according to Ohm's law. But the channel strength is constant as the gate voltage is held constant. The channel starts to get depleted as the drain-to-source voltage increases. Eventually, the channel will be fully consumed, and the current will not increase. At this point the channel is saturated, and the drain current will not increase by increasing the drain-to-source voltage. For small transistors, the channel length becomes small < 1micrometer, the increase in the current will slightly increase by increasing the drain-to-source voltage. This is called the channel modulation effect, which reduces the channel effect length by increasing the drain-to-source voltage.

It is important to mention that the gate acts as capacitor. Under static conditions, the gate current is zero, as the insulator prevents gate current from flowing into the transistor. Other parasitic capacitances exist within the FET transistors. Those capacitors need to charge (or discharge) when turning the FET on (or off). The time required to charge and discharge the capacitances puts limits on the maximum frequency and puts limits on the maximum frequency handled by the FETs. The time required is often modeled by first order RC circuit.

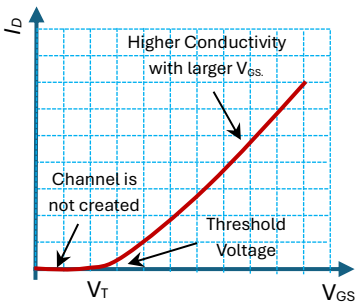

Fig. 6(a) increasing the gate to source voltage and holding the Drain to Source voltage constant, It shows a higher current at larger Gate-to-Source voltage.

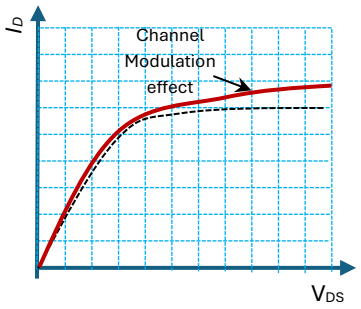

Fig. 6(b) Varying the gate to source voltage and holding the Drain to Source voltage constant, The conceptual inverted S-shape curve between inflation and interest rate.

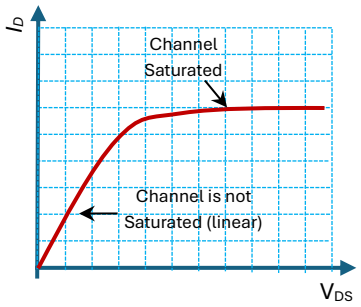

Fig. 6(c) Varying the gate to source voltage and holding the Drain to Source voltage constant, The conceptual inverted S-shape curve between inflation and interest rate.

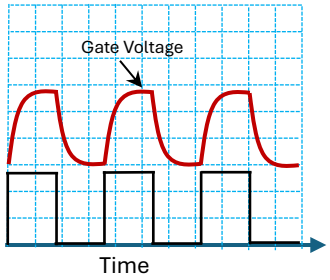

Fig. 7 The gate voltage has a time delay due to the gate equivalent capacitance.

Fabrication of Planar FETs on ICs: FETs are at the core of IC fabrication. FETs are the building blocks in digital circuits as well as in analog circuits. This was made possible by using CMOS

circuits on the same wafer (or die). CMOS technology enables the fabrication of both n-channel and p-channel FETs on the same die. The n-channel transistor is fabricated on a substrate that is made of lightly doped p-type material. The substrate is connected to the lowest voltage on the die. The source (S) and the drain (D) are made of highly doped n-type material. The highly doped source and drain are better conductors; but more importantly, this makes it easier for the gate to attract electrons from the source to create the n-channel. The substrate must have a solid connection by adding a heavily doped p+ material to the body (B) terminal. The body terminal is connected to the lowest voltage on the die. Similarly, the P-channel source uses a lightly dopped substrate that is connected to the highest voltage on the die. The source and the drain are made of heavily doped p+ material. When it comes to the planar FETs, the doping concentrations, as well as the geometric size of the channel, the length (L) and the width (W) as well as the thickness of the oxide (t), are very critical values. Planar FETs have dominated semiconductor technology for decades, featuring flat channel structure where the gate controls the current flow from one side that is the top.

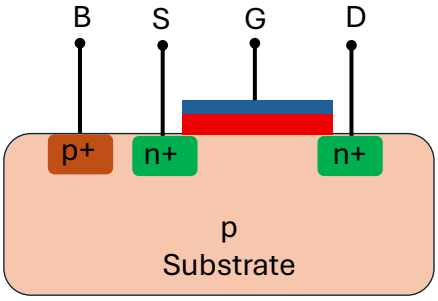

Fig. 8(a) The basic idea of fabrication n-channel FET on lightly doped p substrate.

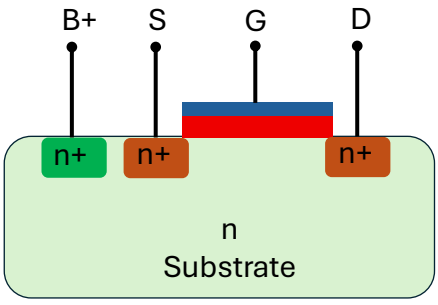

Fig. 8(b) The basic idea of fabrication p-channel FET on lightly doped n substrate.

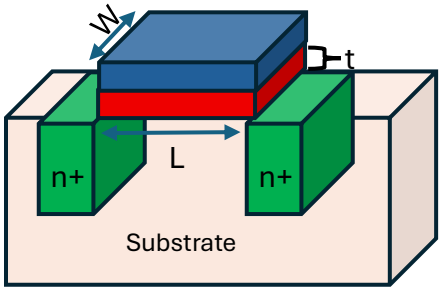

Fig. 8(c) A 3-D structure of n-channel FET with its physical dimensions of the channel length (L), the channel width (W) and the thickness of the oxide layer (t).

Most digital and analog IC chips use CMOS technology, in which n-channel and p-channel FETs are fabricated on the same die. The wafer uses lightly doped p material on which the n-channel transistors are added directly on the die. The p-channel transistors are fabricated on n-wells. So the n-well is implanted before creating the p-channel transistors.

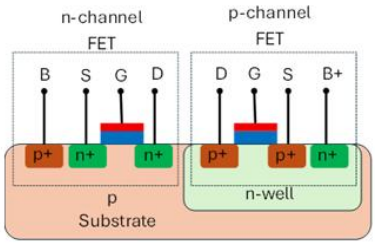

Fig. 9 The COMS technology is to fabricate the n-channel and the p-channel on the same die.

The fabrication of a planar FET begins with a polished silicon wafer; each wafer is divided into smaller dies. Depending on the size of each chip, a wafer may contain up to 70000 different chips. The wafer, also called the substrate or body or die, is made of lightly doped p type material. The die (substrate) must be connected to the lowest voltage on the chip. The transistor is fabricated using lithography, ion implantations and thermal oxidation. Lithography is the process of transferring circuit patterns onto a silicon wafer with a nanometer precision. First, the wafer is coated with photoresist material. Then, ultraviolet (UV) light, or extreme ultraviolet (EUV) light, is passed through a highly précised mask. The area of the wafer that is exposed to light will be hardened, the area that was not exposed to light will be easily removed. This creates a stencil on the wafer process that defines the desired areas to be used for doping. Ion implantation is used to add impurities n-type or p-type areas. Thermal oxidation is used to create a thin layer of silicon dioxide on the surface of the gate. On top of this oxide, a conductive polysilicon is deposited defining the gate electrode. Lithography includes additional steps such as annealing, depositing insulating layers, and formation metal contacts, as well metal routing layers are included. This planar manufacturing approach was straightforward, scalable, and became the backbone of the integrated circuit revolution.

Planar FET Drawbacks: During the past decades, the planar FET aggressively advanced its technology by scaling down its size devices to reduce its capacitance, reducing its operating voltages, and minimizing its power consumption. As the transistor size continued to scale down, the fabrication technology reached its limits around the30 nm ~ 20 nm node. Some of the serious drawbacks of the planar FETs below the 20 nm technology include:

1. Short-channel effects – As the channel length shrinks, the gate loses control over the channel, leading to problems like drain-induced barrier lowering (DIBL) and threshold voltage roll-off.
2. Increased gate leakage currents – Thin gate oxides and small geometries cause

higher leakage, raising static power consumption.
3. Poor electrostatic control – With only one gate sitting on top of the channel, it becomes difficult to effectively control the current in very small devices.
4. Heat dissipation challenges – The power dense (watts/unit area) became challenging to control.

The Transition to FinFET: The demands for high-performance low-power CPUs, GPUs, and mobile SoCs have pushed beyond the planar FETs limit of 20 nm. At the 20 nm node, planar FETs began to suffer from severe short-channel effects, leakage currents, and power inefficiencies. To keep aligned with Moore's Law, the semiconductor industry turned to solving these issues. Once the technology reached the 20 nm limit, it became apparent that the short channel effect is a serious problem that needs to be overcome. The gate structure of the planar FET was once considered advantageous due to its fabrication simplicity, but now the gate structure is severely contributing to its limitation at 20 nm node. The gate of the planar FET creates the channel by having one side electrode that is placed on the top between the drain and the source. The channel would be better controlled if the gate's electrode covers the channel from multiple sides. This has pushed for FinFET technology, a three-dimensional transistor architecture that revolutionized chip design. While not without challenges, FinFETs performance and efficiency gains have made them indispensable in modern IC designs.

When FinFETs were first proposed, manufacturers faced daunting challenges. The 3D structure required extremely precise lithography and etching to form narrow fins with uniform height and width. Integrating these fins with existing CMOS fabrication lines demanded new process steps, materials, and tools. Yields were initially low, and cost was a significant concern until its technology matured. By the mid-2010s, commercial CPUs and SoCs featuring FinFETs were shipping in volume, powering everything from data centers to smartphones.

The Structure of FinFETs: FinFETs feature a three-dimensional fin-like structure in which the gate wraps around the channel on three sides. This design provides better electrostatic control, reducing leakage and improving performance at smaller nodes. The fin is a thin vertical silicon that rises above the substrate. The gate wraps around the midsection of the fin, and the end sections are the heavily doped source and drain. Now, the current flows through the fin, from the drain to source through the channel. Because the gate sounds the channel from three sides, the gate provides excellent electrostatic control over the channel.

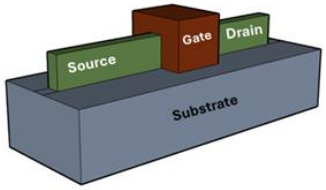

Fig. 10(a) The basic structure of the FinFET that is made of a 3D fin and the gate is wrapped around it from three sides.

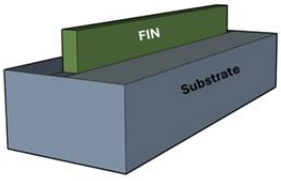

Fig. 10(b) The 3D Fin is etched by carving the silicon around it.

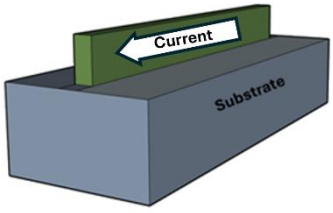

Fig. 10(c) The fin is the channel where the current flows through it.

The Fabrication process of FinFETs: The fabrication lithography steps of the FinFET have evolved from the conventional planar FETs. The fabrication of a FinFET involves the following steps:

1. *Fin Formation* which creates the fins regions and etches the wafer to create narrow thin fins.
2. *Shallow Trench Isolation (STI):* Filling gaps between fins with oxide to isolate devices.
3. *Gate Stack Deposition*: Forming the gate materials that wrap around the fin.
4. *Source/Drain Implantation:* Adding dopants to define transistor terminals.
5. *Contacts and Metallization*: Adding contacts to the transistors terminals and connecting transistors with interconnect metal layers.

The fin formation steps start with the substrate which is the silicon wafer with a layer of insulator (e.g., silicon nitride Si_3N_4 or silicon dioxide SiO_2). This protects regions during etching. Lithography uses extreme ultraviolet light (EUV) to define where the fin is etched or carved. Anisotropic reactive ion etching (RIE) is used to etch away exposed silicon, leaving behind narrow, tall silicon "fins". The shallow trench isolation (STI) fills the gaps between the fins with silicon dioxide. The oxide is then planarized using chemical-mechanical polishing and fin height precisely adjusted, the fin height controls the effective channel thickness. The gate stack deposition step is critical, because it determines how well the gate controls the fin channel. Which includes a stack of the gate dielectric, gate electrode, and gate cap. The gate dielectric is made of high-k material (hafnium oxide HFO_2) that is combined with a thin interfacial layer of SiO_2. The Gate electrode is a metal that is made of titanium nitride, tantalum nitride or tungsten. The gate cap is a spacer the is used to protect and isolate the gate, and it is made of silicon nitride. The source and the drain are located at the fins end sections. Their implementation steps start

with lightly doped drain (LDD) light dose of dopants (phosphorous for the n-channel FETs, and Boron for the p-channel FETs) at the drain near gate to lower the hot-carrier effects. The hot carrier effect is caused by the high current in the saturation region. The gates are covered by dielectric spacers (Si_3N_4 or SiO_2) to protect the channel during deeper source/drain implantation. Heavy doping is introduced to form the highly conductive source/drain terminals. The n-channel uses phosphorus, arsenic or pure silicon may, and the p-channel uses boron or SiGe. Repeated thermal annealing is applied where high temperature annealing is used to activate the dopants and repair the lattice damage. Silicidation, which is a metal layer deposited to the drain and source, which creates a low resistance silicide contact. The final step is to make contacts to connect to the transistor (gate, source, drain) vertically to the wiring network, and metallization which interconnect transistors using multilayers of metals (Cu/Co) and low-k dielectrics. The contact formation starts by separating each FET by depositing thick dielectric material, then it uses lithography and etching to open contact vias to the gate, source and drain of each transistor. Barrier layer is added, followed by filling the contacts with tungsten, cobalt or ruthenium. The metallization is made of multiple layers of metals that are separated by insulations. The first (lower) three metal layers are used for direct contact with the transistors, and short runs, intermedia metal layers are used for routing and the upper metal layers are thicker used for signal distribution and power signals. The last step of the IC fabrication is passivation, in which seals the chip with a dielectric layer that protects the IC from moisture, contamination and mechanical stress.

Challenges in Adopting FinFETs: While FinFETs have solved the scaling problem of planar FETS below the 20 nm, they have drawbacks and challenges. Fabricating the FinFETs is complex and requires extremely precise lithography, etching and alignment processes. Thus, it requires advanced equipment, and repetitive patterning steps as well as new materials, which raised the overall production costs per wafer. The performance sensitivity to the fin's height and width is another drawback FinFETs. The 3-D geometry added stricter design rules which made circuit layout design more challenging. FinFET technology has reached its scalability limits at 3nm due to short-channel effects and leakage. The tall, narrow fins make heat dissipation less efficient, which can impact reliability. Nevertheless, the promise of superior performance and efficiency proved irresistible. Industry leaders such as TSMC, Intel and Samsung have dedicated enormous resources to bringing FinFETs to production.

Transition to the Gate-All-Around FETs (GAAFETs): While FinFETs improved transistor electrostatic control, scaling the FinFET transistor below 5nm has serious drawbacks. The FinFET suffers from the short channel effect, gate leakage current and electrostatic control. This led to the new development of gate-all-around FET (GAAFETs.) The GAAFET is the next step in transistor evolution, designed to overcome the scaling limits of FinFETs. The gate of the GAAFET surrounds the channel on all sides, the gate is all around the channel. This provides better electrostatic control, drastically reducing leakage and allowing transistors to scale beyond the 3nm and 2nm nodes.

The GAAFET uses multilayers of nanosheets that are stacked horizontally (in parallel). Each sheet acts as a channel, so parallel channels have better overall conductivity. Each sheet is fully enclosed by the gate, which improves the electrostatic control and minimizes the gate leakage, hence improving performance and energy efficiency. By adjusting the width of these nanosheets, designers can fine-tune drive current, offering flexibility than FinFETs.

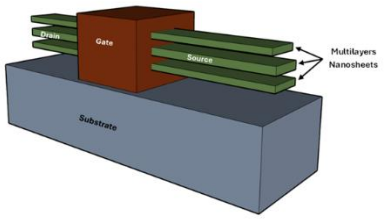

Fig. 11(a) The structure of the GAAFET is made of multilayer nanosheet. The gate is wrapped around the nanosheets from all sides. The end terminals of the nanosheets are heavily doped making the source and the drain.

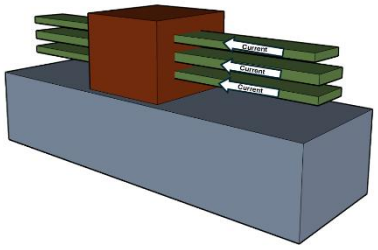

Fig. 11(b) The gate is used to create the channel from the drain to source of each layer. Once the channel is created, the current flows through the channel.

The main advantage of GAAFETs is their superior control of short-channel effects, reduced leakage, and better scalability for advanced nodes. However, they also introduce new fabrication challenges, such as forming uniform nanosheets and precisely wrapping the gate around them at the atomic scale and aggregated capacitances. Despite these hurdles, leading chipmakers like TSMC, Samsung, and Intel are transitioning to GAAFETs to power the next generation of high-performance, low-power chips.

GAAFETs have already moved from research labs into real products. Samsung became the first to mass-produce 3nm GAAFET chips, powering mobile processors and even wearables like the Exynos W1000, where efficiency and compact design are crucial. Other chipmakers, including TSMC and Intel, are preparing to adopt GAAFETs at the 2nm generation for high-performance computing, AI accelerators, and data-

center processors that demand maximum density and minimal power loss. With their ability to tame leakage and operate at lower voltages, GAAFETs are also poised to expand into edge devices, IoT, and eventually automotive systems—marking them as the next universal workhorse of advanced electronics.

Th Fabrication steps of GAAFETs: To build multilayer nanosheets, the fabrication process has evolved from the FinFET process. Starting with a silicon wafer, alternating layers of Si and SiGe are grown epitaxially, generating alternating layers of Si/SiGe. The Si layers will form the transistor channels, and the SiGe layers are sacrificial layers and will be etched away later.

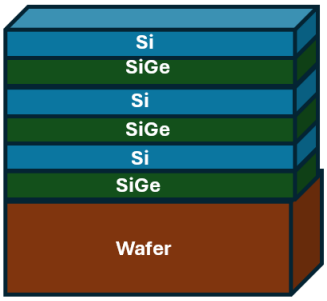

Fig 12(a) The fabrication of the GAAFETs starts by making a multilayers stack of Si/SiGe added on the top of the substrate (wafer).

The Next step is the sheet patterning which defines the areas of the nanosheets. Lithography is used with EUV to define the narrow fins that contain the alternating Si/SiGe. Thin hard mask of SiO2 is deposited to protect the designated layers.

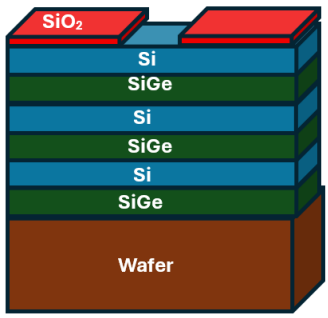

Fig 12(b) The pattern for each nanosheet segment is defined using SiO_2 protection layer. Unprotected regions will be etched away.

Anisotropic etching is implemented by using repetitive steps of reactive ion etching (RIE) process to etch away all the Si/SiGe layers on the exposed regions.

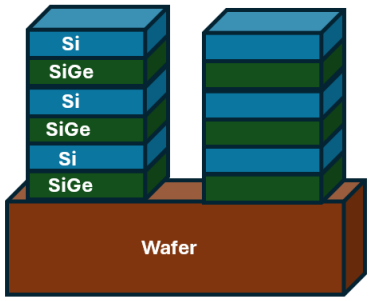

Fig 12(c) Anisotropic etching removes the layers of the unprotected region.

The next step is removing the sacrificial SiGe layers by selectively etching them away, leaving behind the suspended silicon nanosheets.

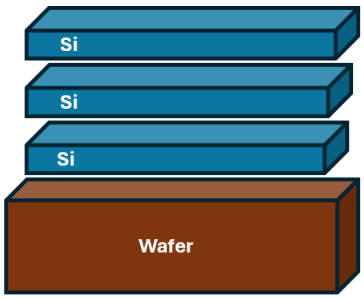

Fig 12(d) Obtaining the multilayer silicon nanosheets after removing the sacrificial SiGe layers.

The next step is the gate stack deposition to form the gate all around by depositing high-k dielectric around the nanosheets. Then, a metal gate (TiN) is deposited to completely wrap around the nanosheets followed by spacer formation to protect the gate during subsequent steps.

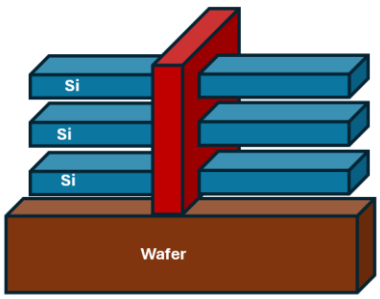

Fig 12(e) Depositing the gate all around the nanosheets from all sides.

The next step is the source/drain formation by adding heavy dopant on both sides of the nanosheets for the n-channel and the p-channel, and this is followed by dopant activation (annealing).

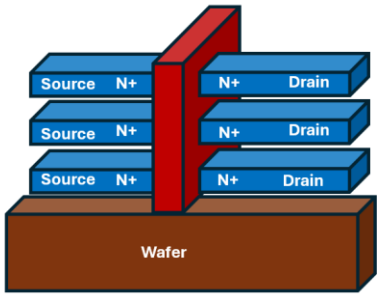

Fig 12(f) Doping the ends of the multilayers with n dopants to create n-channel GAAFETs.

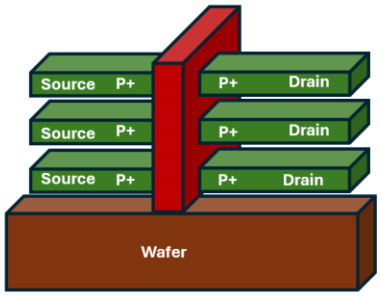

Fig 12(g) Doping the ends of the multilayers with p dopants to create p-channel GAAFETs.

The next step is to add contacts to the gates, sources and gates using tungsten, cobalt, or ruthenium, followed by the metallization step where multiple layers of copper are deposited for routing and interconnects.

Drawback of the GAAFETs: The Gate-All-Around FETs deliver superior electrostatic control but at the price of tougher manufacturing and integration hurdles. The fabrication is far more complex, requiring stacked Si/SiGe layers, precise nanosheet release, and conformal gate deposition. Each has raised costs and risk defects. The ultrathin nanosheets are mechanically fragile, making yield harder to maintain, and material strain adds further reliability concerns. Variability in nanosheet thickness or etch uniformity can shift

device performance, while the dense stacking of channels creates power and heat dissipation issues.

Summary: For decades, the planar FET dominated the IC technology, its flat channel and simple one-sided gate design had pushed the rise of microprocessors and consumer electronics. As transistors shrank below 30 nanometers, leakage currents and short-channel effects threatened to stall progress. The shift to FinFET technology, with its three-dimensional fin structure and three-sided gate, has delivered stronger control enabling the explosive growth of smartphones, cloud computing, and AI in the 2010s. Today, as scaling pushes into the 2nm frontier, the industry has embraced the Gate-All-Around FET. By surrounding stacked nanosheets with a gate surrounding the channel from all sides, GAAFETs deliver the ultimate electrostatic control, squeezing out more performance and efficiency. Together, these milestones mark the relentless innovation that keeps Moore's Law alive.

Table1. Comparison between planar FET, FinFET and GAAFET.

Feature	Planar FET	FinFET	GAAFET
Structure	Flat channel with gate on top	3D fin with gate on three sides	Stacked nanosheets with gate all around
Electrostatic Control	Weak at small nodes	Stronger than planar	Strongest, full gate wrap
Scalability	Limited below ~28nm	Effective down to ~5nm	Enables <2nm technology nodes
Fabrication Complexity	Relatively simple, mature	More complex (fin etching, 3D gate deposition)	Most complex (stacked epitaxy, nanosheet release, conformal gate)
Performance	Adequate at larger nodes	High drive current, reduced leakage	Even higher drive current, best leakage control
Power Efficiency	Moderate	Improved vs planar	Best power efficiency
Threshold voltage Variability	Threshold voltage variation at small nodes	Reduced but still present	Improved, but new nanosheet variability introduced
Thermal Issues	Easier to dissipate heat	Moderate heat challenges	Higher heat density due to stacked channels
Adoption Era	Dominant up to 28nm (2011 and earlier)	Mainstream from 22nm to 5nm	Entering mass production at 3nm → 2nm (TSMC, Samsung, Intel)