DE LA RECHERCHE À L'INDUSTRIE

Full 300 mm Electrical Characterization of 3D Integration Using High Aspect Ratio (10:1) Mid-Process Through Silicon Vias

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OUTLINE

- **Introduction**
  - 3D Integration and why increasing aspect ratio
- **New metallization of High aspect ratio TSV**
  - MOCVD TiN barrier
  - Electrografted seed layer : eG^{3D}
    - ✓ Characterization
    - ✓ Transfer on 300 mm platform
- **Integration and electrical results**
- **Conclusions and perspectives**

WHY 3D INTEGRATION ?

- In the near future, the electronic circuit will probably be looking like this and will integrate complex electronic systems on silicon

SIM slot
App Processor/DDR SDRAM
Accelerometer
Power Amp
Transceiver
Power Amps
NAND Flash
GPS
PMIC
BB-PMIC
SRAM
BaseBand Processor

System on board
(Smartphone PCB)

Stacked 3D ICs

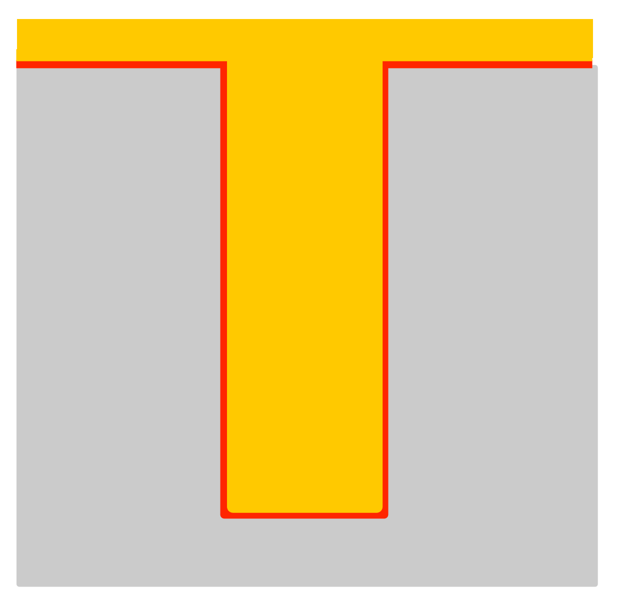
A silicon interposer

With very heterogeneous dice on it (various substrates, various technologies co-existing, various chip makers…).

Smaller - More Performance with higher functionalities - Cheaper

HIGH ASPECT RATIOS – CHALLENGES FOR METALLIZATION

- Higher and higher aspect ratios are today forecasted
- TSV Mid-process
  - From 10x100 µm today to 10x150 µm or 5x80 µm depending on application
- Where are the challenges for metallization of these TSVs?



Barrier

- Conformal deposition
- Good barrier properties for process temperature

Seed

- Conformal deposition, continuous on sidewalls
- Low resistance

Plating

- Void free deposition in whole TSV
- Low overburden

HIGH ASPECT RATIOS – ALTERNATIVE SEED LAYER

- Electrografted seed layer
  - Process developed by aveni: eG^{3D}

High adhesion
High nucleation density
Reduced terminal effect

2+

Cu

L

e^-

2+

Cu

Copper with complexing agent
+
Adsorbed copper via ligands

$2e^-$

L_1 + L_1

Cu

$1/2Cu^0$ + $1/2Cu^{2+}$

Disproportionation

Cu^0

L_2

Two e^- reduction
Adsorption

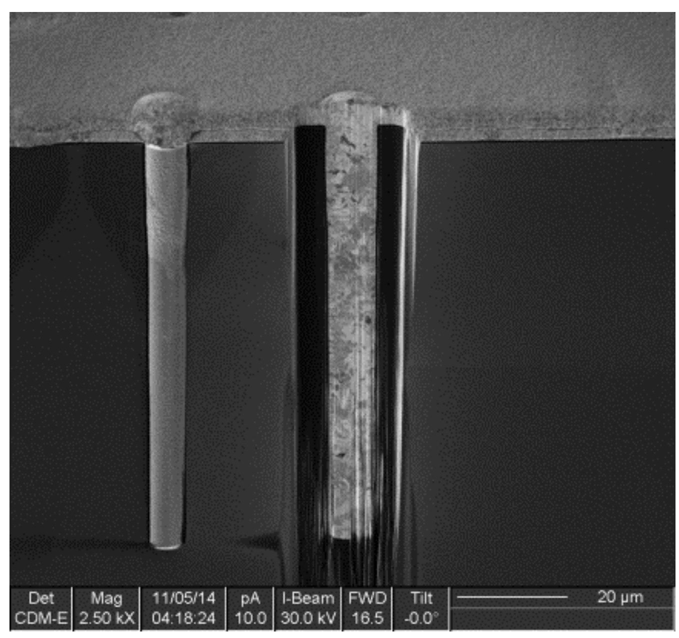
Thickening
Metal-to-metal bond
No carbon in the film

Can be used as a PVD seed repair or directly as DoB (Direct on Barrier)

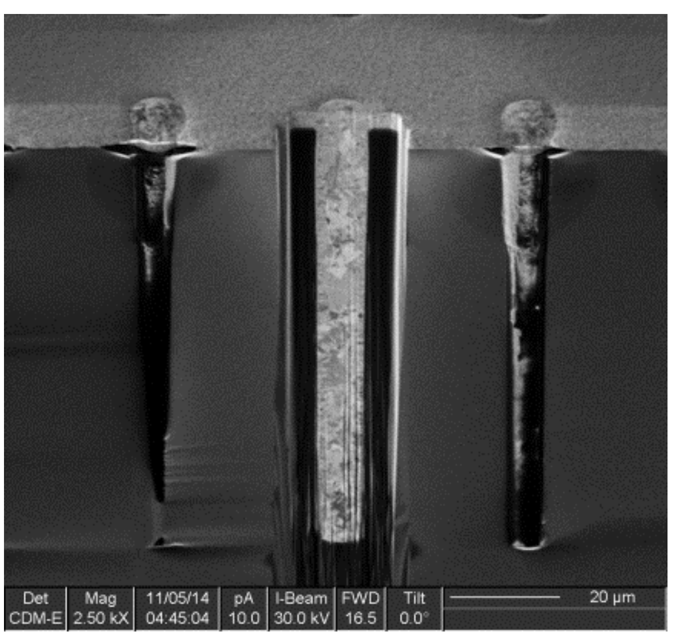
HIGH ASPECT RATIOS SEED LAYER – eG^{3D}

- Transfer to 300 mm scale
  - Copper filling

10x100 µm TSVs filled with the 2 selected options: seed repair or direct on barrier seed



PVD barrier + Cu seed layer
+ eG^{3D} repair process

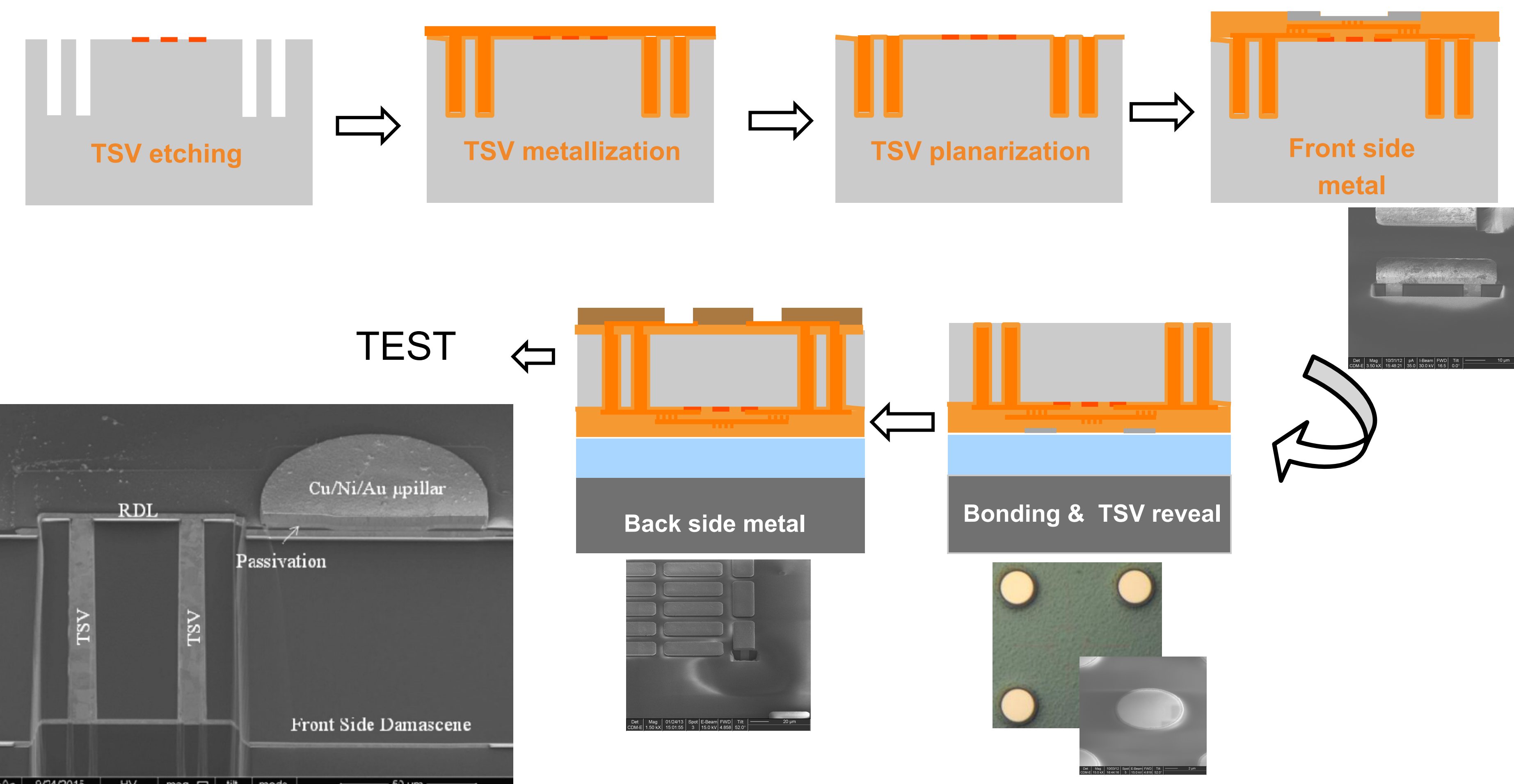


MOCVD TiN barrier + Cu seed flash
+ eG^{3D} seed layer process

Void free filling obtained on both metallization options

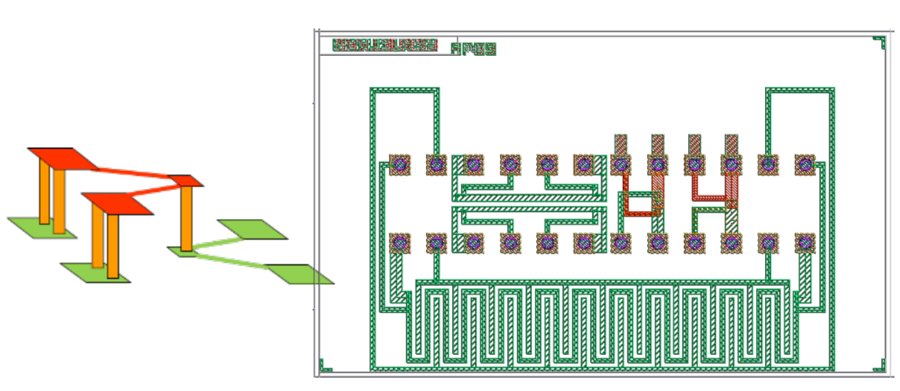
INTEGRATION

- Complete integration was performed using TSV mid process flow

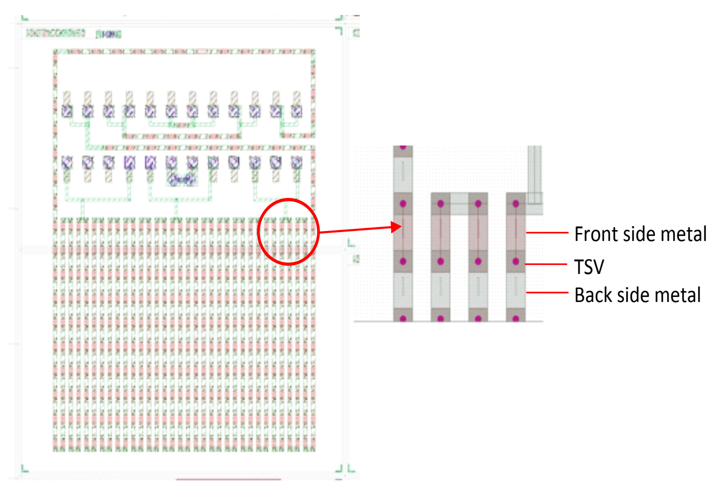


TEST STRUCTURE

Test structure : Kelvins and daisy chains



10x100 µm Kelvin TSV

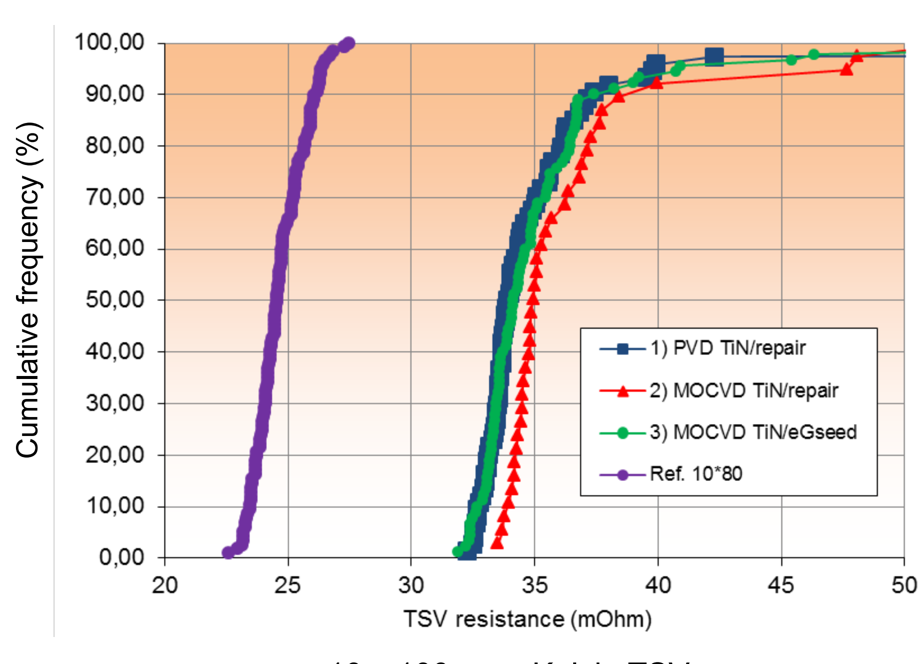


10x100 µm : 2 to 754 TSVs Daisy Chain

Metallization splits for comparison

Split 1 : PVD barrier/seed repair option
Split 2 : MOCVD TiN barrier/seed repair option
Split 3 : MOCVD barrier/Flash PVD Cu/eG3D seed layer

Electrical results



10 x 100 µm - Kelvin TSV

100,00
90,00
80,00
70,00
60,00
50,00
40,00
30,00
20,00
10,00
0,00
40
50
60
70
80
TSV resistance (Ohm)
1) PVD TiN/repair
2) MOCVD TiN/repair
3) MOCVD TiN/eGseed
Ref.PVD- 10*80

10 x 100 µm - 754 TSV daisy chain

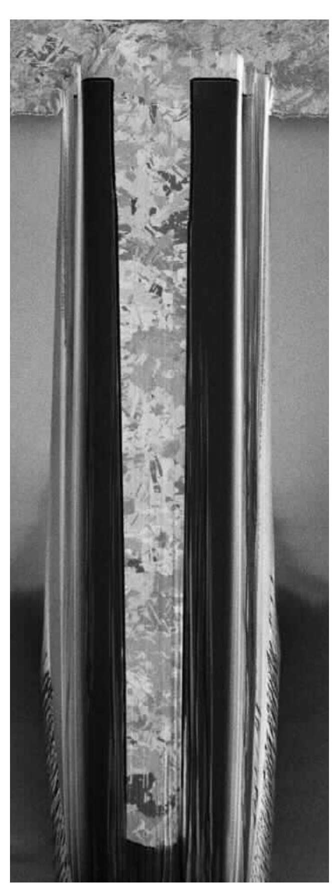
- Excellent yield whatever metallization conditions
- Sharp distribution
- No clear difference between the splits
- Same distribution as 10x80 µm full PVD reference, difference is due to TSV height

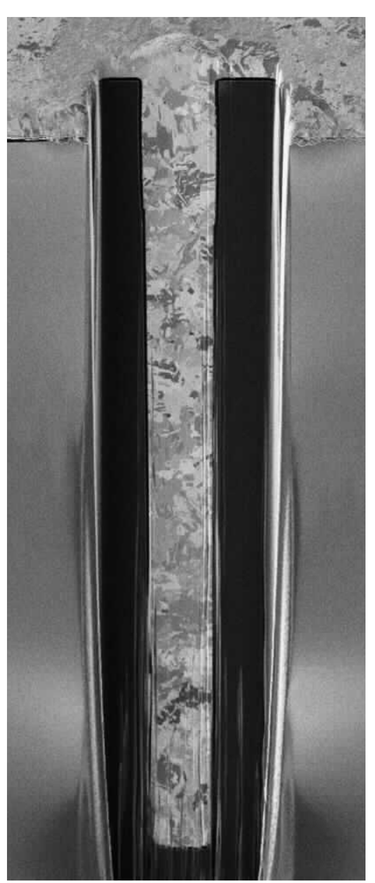
INTEGRATION

Process extendibility to higher TSV

- Same process was applied to 12:1 aspect ratio TSV (10 x 120 µm)

Option 1
MOCVD TiN –
1.5 µm PVD seed-
200 nm eG^{3D} repair





Option 2
MOCVD TiN –
Flash Cu PVD 200 nm -
200 nm eG^{3D} seed

- Both presented metallization options are extendible to 12:1 aspect ratio

CONCLUSIONS

- A new metallization process has been demonstrated enabling copper filling of high aspect ratio TSV based on :
  - A low temperature MOCVD TiN barrier material
  - An Electrografted seed layer that can be used in stand alone or as a seed repair option
- Process development was performed and transferred on a 300 mm platform
- Electrical integration was realized showing no degradation of TSV performances compared to reference iPVD metallization
- Extendibility of this process for higher aspect ratio has been demonstrated and integration is on going on 12:1 AR
- Adhesion is still under investigation through process and hardware optimization to remove the copper flash PVD

I would like to acknowledge :
- The 300 mm plating team
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- aveni process team
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