Power, Isolation and Signal Integration:

The SiP Gateway to Future Power Conversion Systems

Presented by MPics Innovations

Richard Lum, CEO

POWER

ISOLATION

SIGNAL INTEGRATION

FUTURE READY

A Confluence Reshaping Power Conversion

Technology Push

- WBG Devices (SiC / GaN)
- Higher Switching Speed
- Higher Power Density
- Smaller Form Factor
- Increasing System Complexity

Market Pull

- Better Efficiency
- Higher Reliability
- Smarter Monitoring & Management
- Faster Development Cycles
- Cost-Performance Pressure

Next-Generation Power Conversion

Technology push + market pull are driving a new integration era.

Why Integration Matters:

Key Benefits for Next-Gen Power Systems

Our integrated SiP delivers system-level advantages that drive performance, reliability and time-to-market.

Higher Power Density

- Up to 60% smaller solution size
- More power in the same footprint
- Ideal for space-constrained designs

Lower Cost

- Reduced BOM count
- Fewer external components
- Lower assembly and system cost

Higher Performance

- High CMTI and low propagation delay
- Reduced parasitics
- Improved efficiency and system dynamics

Enhanced Reliability

- Reinforced isolation for higher safety
- Better noise immunity
- Fewer points of failure, longer system life

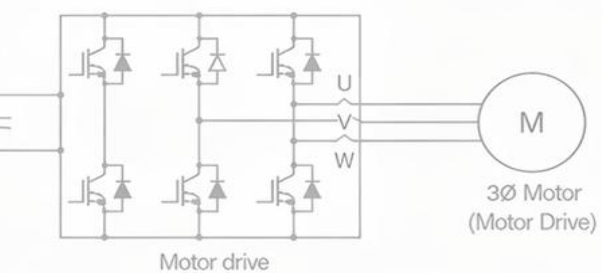
One Integrated Solution. Many System Advantages.

Enabling higher power, higher efficiency and faster innovation.

MPiCS INNOVATIONS

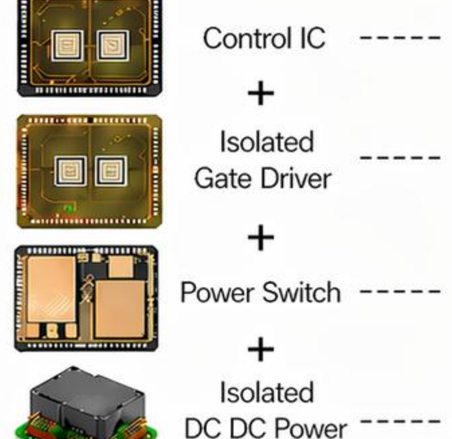
High Voltage Integrated Power + Signal Isolation in One SiP

Replacing multiple components with a single, high performance SiP



TRADITIONAL APPROACH

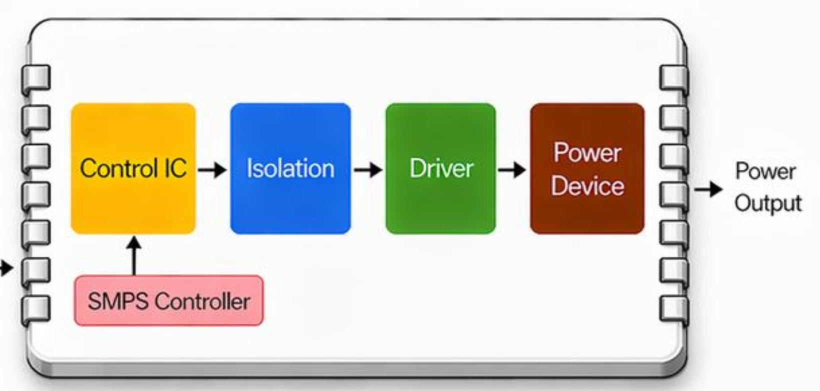
Multiple Components



- Larger solution size
- Higher BOM cost
- More design complexity
- Lower reliability

OUR SOLUTION

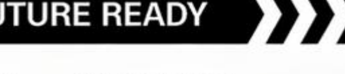
One Integrated SiP

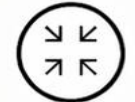


LLC DC-DC Converter

Smaller, Simpler, Smarter,
Built for Performance and Reliability

Isolation
(High Voltage)





COMPACT
Up to 60% smaller solution size

COST EFFICIENT
Lower BOM and system cost

HIGH PERFORMANCE
High CMTI, low propagation delay, high efficiency

HIGH RELIABILITY
Fewer components, higher robustness

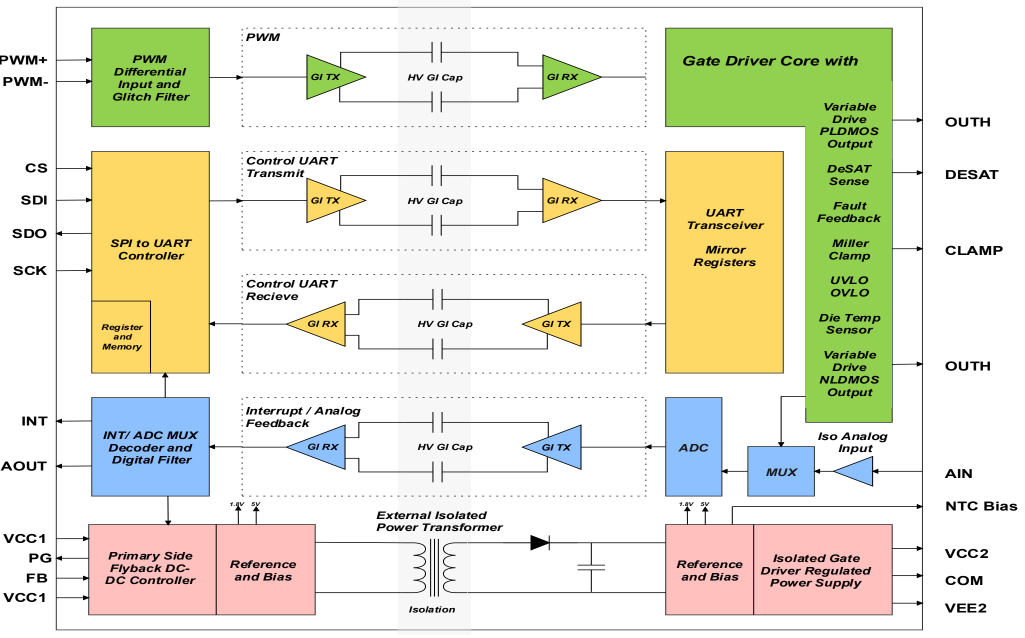
FASTER TIME TO MARKET
Simplified design and faster development

Silicon Proven Driver IP and SiP Integration Platform

GaN + Isolation Design IP

All IP blocks are silicon proven, can be customized and integrated to custom specifications

Advanced Gate Driver Integration Platform using Silicon Verified IP in XP018 40V Process with On Chip Galvanic Isolated HV Capacitors



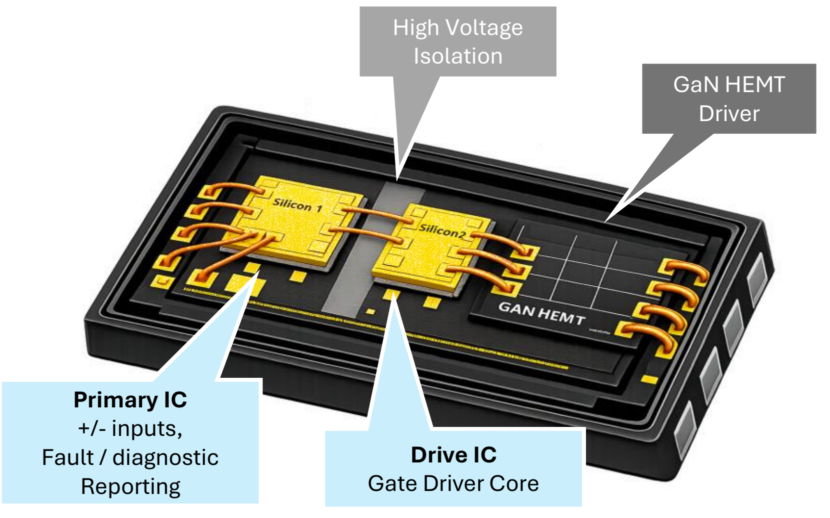
Scalable Isolated Gate Driver Core IP

Isolated SPI Controller

Analog/High Speed Interrupt Feedback Channel

Isolated DCDC / Common Reference and Bias IP

Gallium **N**itride **P**ower **I**solation **C**ontrol **S**ense



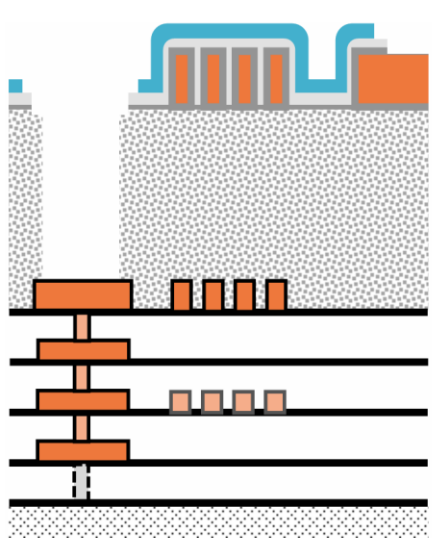
Integrated GaN Package

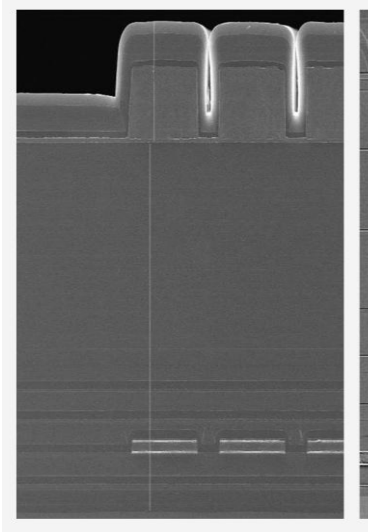
- Small form factor
- Reduced parasitic inductance between package and PCB
- Faster switching frequency
- Improved power efficiency
- Integrated diagnostics and control
- Predictive Analytics for mission critical systems

Customizable GaN with Monolithic Integration (R, C, LVT, Diodes)

xfab Galvanic Isolation Solutions + xfab GaN Solutions

- VISO isolation withstand voltages up to 5000 Vrms for 1 minute
- Designed for operating temperatures of up to 175 °C
- Allows integrated coupler devices
- Fully IATF-16949:2016 automotive qualified

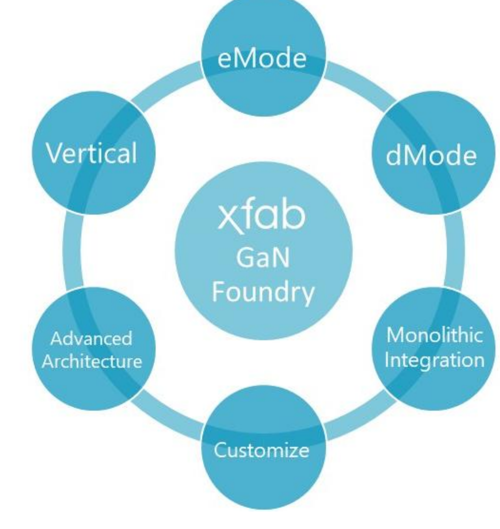


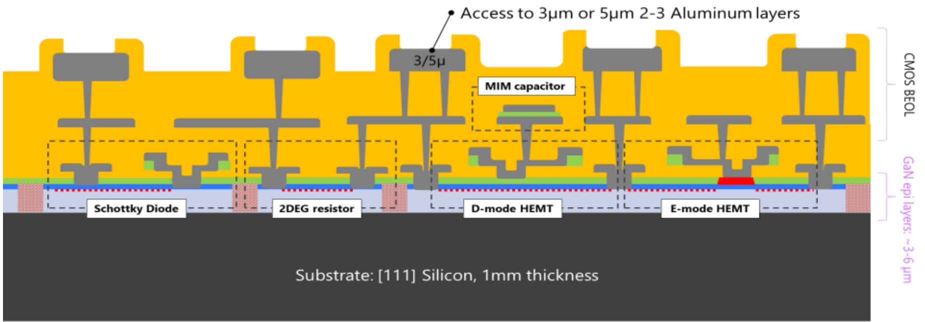


eMode
- 650V-750V HEMT
- 100V-200V HEMT
- Schottky Diode

dMode
- 650V-750V HEMT
- Schottky Diode

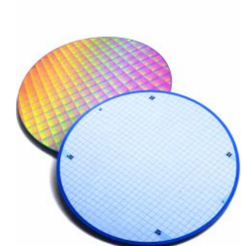
Monolithic Integration
- Capacitors
- Resistors
- Diodes
- LV transistors

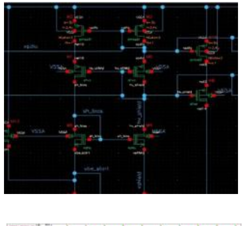


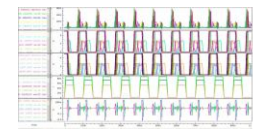


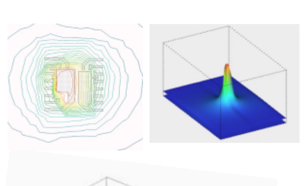
Work with our Team – Engineer your Ideas into Production

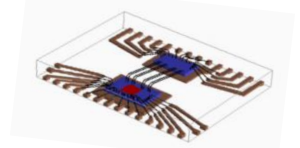
Foundry	Design & Verification	Package Design	Field Solver Tools	Electrical Verification	QMS	Mass Production
	MPiCS INNOVATIONS	MPiCS INNOVATIONS	MPiCS INNOVATIONS	MPiCS INNOVATIONS	MPiCS INNOVATIONS	
Collaborate with several foundries: X-FAB, TSMC, Global Foundry, HHGrace, UNT	Custom Analog/ Mixed signal full chip development Design, Layout Simulation, and Verification	Package design combining Precision Field Solver and Thermal Optimization	E-Field High Voltage Study on GI Cap Electro-Magnetic Field Study	Verification across Temperature HV Reliability/ Verification TDDB e-model lifetime	IATF-16949, ISO9001 System Qual/ Rel AEC-Q / JEDEC Safety Standards UL (US); CSA (Canada) CQC (China) IEC60747 (EUR)	Wafer Probing Front to End Full Line Assembly Final Testing with Over Temperature Capability

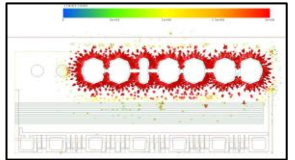


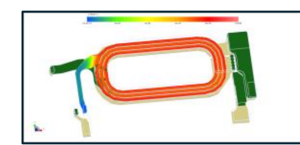


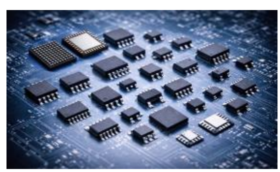












Thank You !

Do visit us at Hall 5,

BOOTH 3149

for discussion and demo !

Scan to visit our Corporate Home Page to download these slides

semi | SEMICON® SOUTHEAST ASIA

MAY 5-7, 2026 | MITEC, KUALA LUMPUR, MALAYSIA

We're exhibiting at SEMICON Southeast Asia 2026!

JOIN US AT
BOOTH 3149
HALL 5

MPiCS INNOVATIONS

MPics Innovations
Specialty Analog IC Design

TRANSFORM TOMORROW