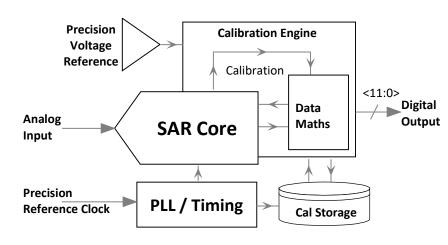## CaptiVade™
12 Bits Self Calibrating Successive Approximation Analog to Digital Converter Core

The CaptiVade™ A to D converter is based on a proprietary Self Calibrating Successive Approximation Charge Re-distribution technique that allows easy porting to various CMOS technologies. Because of its moderate analog content and usage of fast digital computation for self calibration, it is most suited for technologies with dimensions less than 65nm.

Starting at conversion rates of up to 80Msps and achieving linearity at 12-bits resolution, these cores can also be configured in a time interleaved arrangement to achieve Gsps operations which is suitable for 5G communications front end and high speed data acquisition systems.

While we have started circuit design and also in the process of filing for IP Protection, we are actively seeking collaborators who have a need for such performance IP to work with us towards a silicon verified IP status. We can work out a business arrangement where our collaborators who bears some risk with us gain early access to the silicon verified core at preferential pricing.

Block Diagram of Self Calibrating High Speed ADC

Features

- ☐ Small area utilization for Analog portion of the ADC

- ☐ Synthesizable digital control and calibration algorithm

- ☐ ADC core can be time interleaved for higher throughput

- ☐ Common Blocks can be shared for minimizing power dissipation

- ☐ Suitable for IQ ADC for Communications Transceiver Front End

- ☐ Ease of migration to smaller geometry processes for product / technology costs down

Disclaimer: This is a product currently under R&D development. MPics Innovations reserves to right to make any changes to the information provided here within this documentation without notifications. All Rights Reserved. CaptiVade® and its stylized representation is a registered trademark of MPics Innovations.

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Ideate ■ Collaborate ■ Create

Multi-Physics Integrated Circuits and Systems

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