



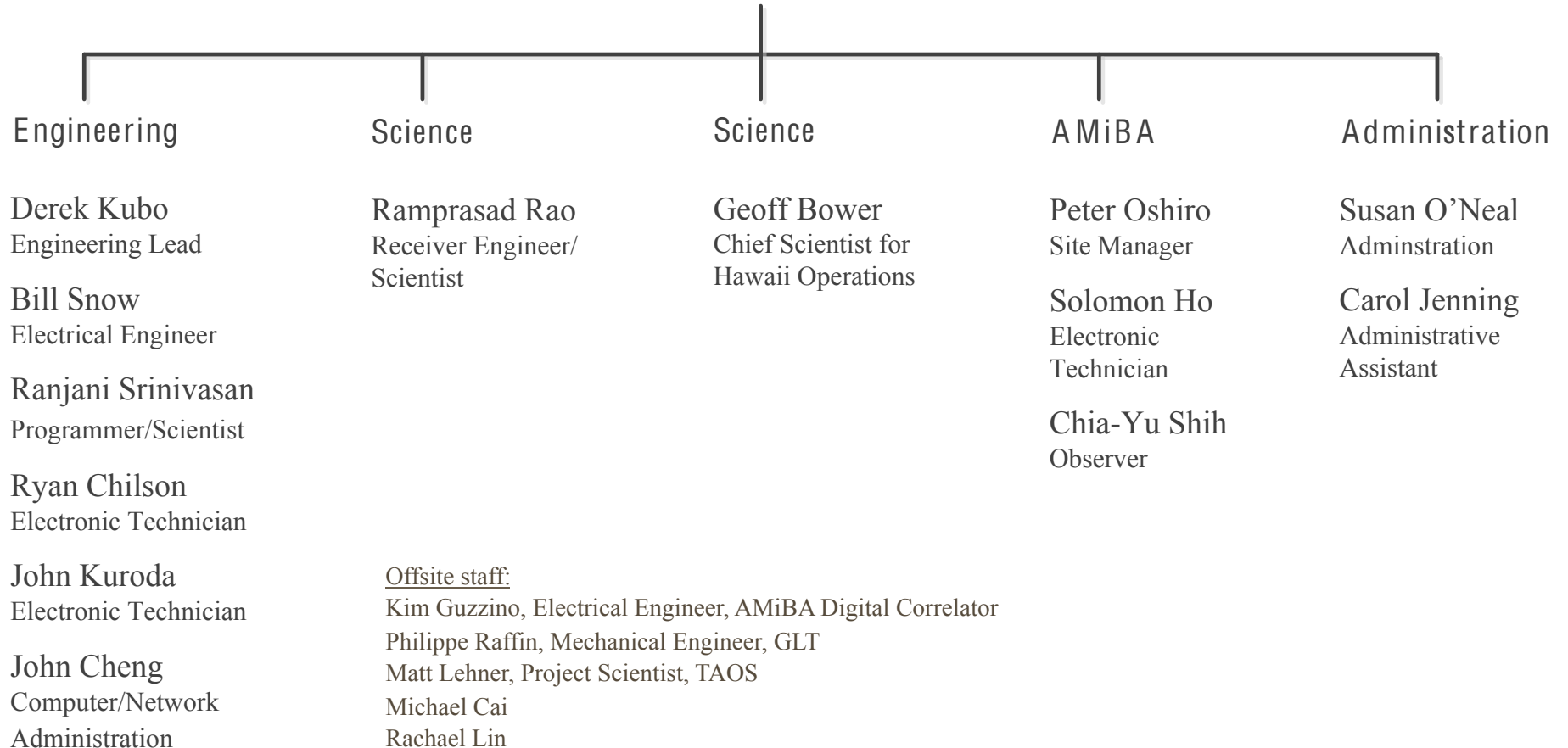
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HARDWARE DEVELOPMENT

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Filename = ASIAA_Hardware

HARDWARE DEVELOPMENT & OPERATIONS SUPPORT

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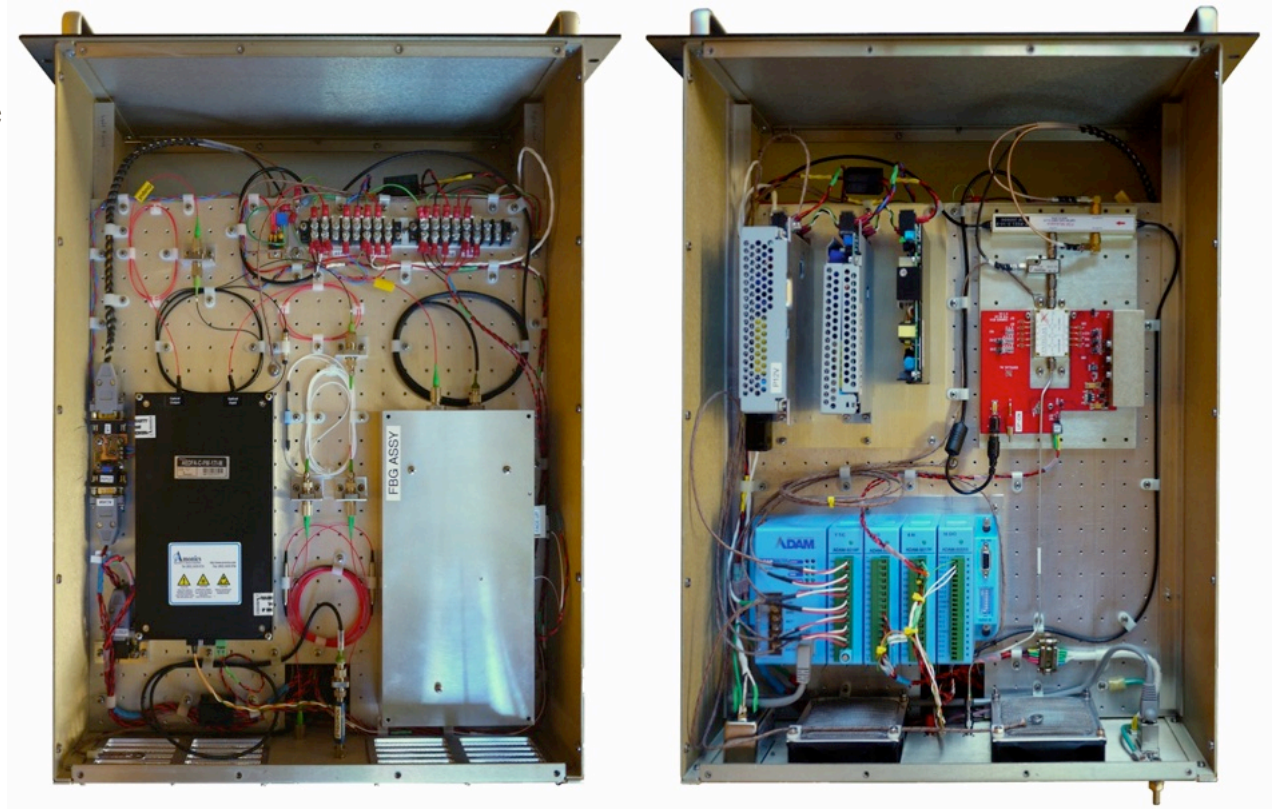


HARDWARE DEVELOPMENT

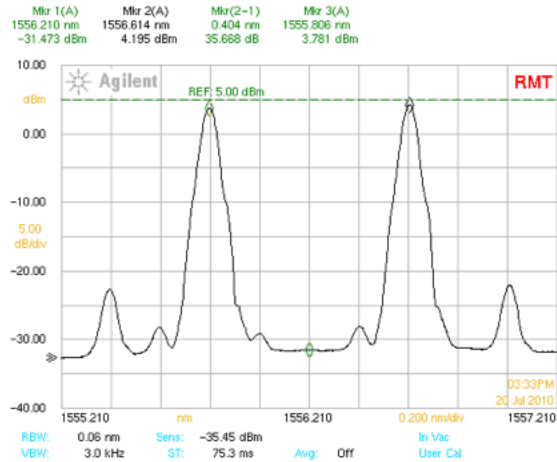
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ALMA ALTERNATE LASER SYNTHESIZER

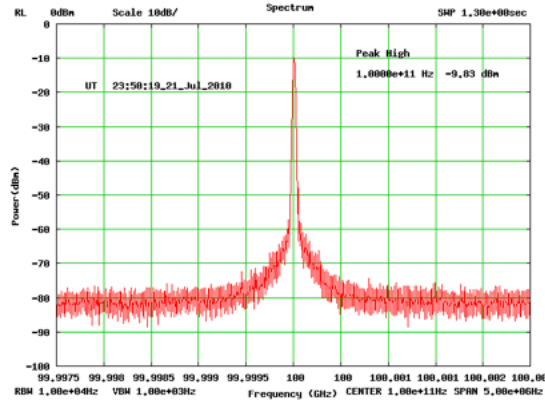
- Mach-Zehnder Modulator Laser Synthesizer (D. Kubo, R. Srinivasan, H. Kiuchi, M.-T. Chen, 2009-2010)
 - Laser Synthesizer is the primary instrument used to develop the optical Local Oscillator (LO) signal sent over fiber to the 66 ALMA antennas
 - TeraXion was awarded the contract to develop and deliver the Laser Synthesizer
 - Had difficulty meeting phase noise requirements during 2008 and posed a risk to the ALMA program
 - ASIAA – Hawaii, in collaboration with NAOJ, developed a unit based on a much simpler MZM architecture
 - Phase noise performance was significantly better
 - Integration with rest of system in Charlottesville VA revealed an incompatibility with Line Length Corrector (LLC) in Fast Frequency Switching mode
 - ALS was used in Charlottesville for ALMA receiver testing and returned to ASIAA after completed in 2012



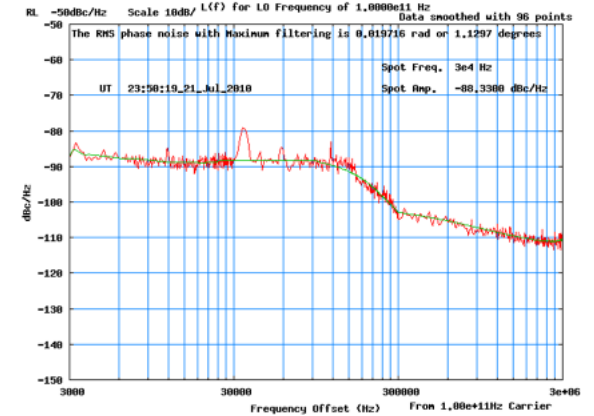
ALMA ALTERNATE LASER SYNTHESIZER



MZM LS J2 Optical Output, LO = 100 GHz



Photomixer RF output, LO = 100 GHz



L(f) Plot, LO = 100.0 GHz

• LS Residual Phase Noise Comparisons

(CVR contribution removed)

- Specification ≤ 27 fsec (1 kHz – 1 MHz)

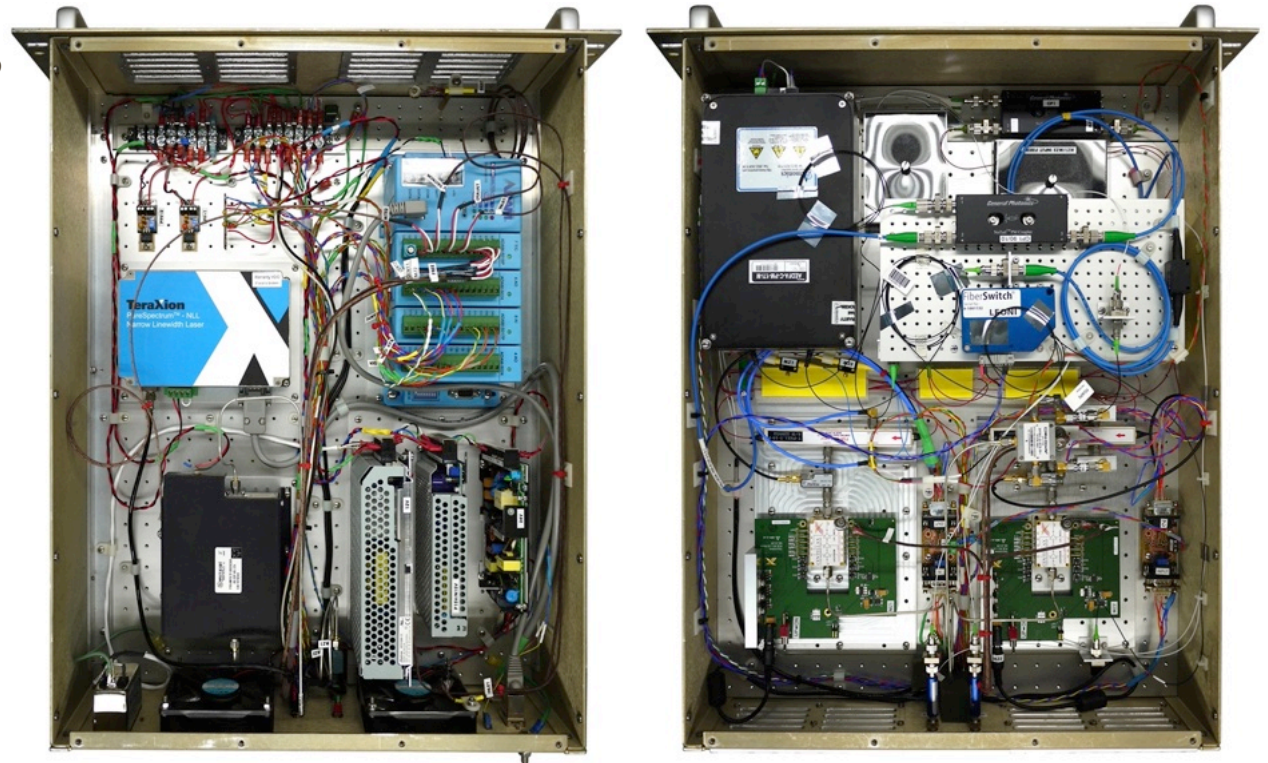
- MZM LS S/N 001: 11 fsec (3 kHz – 3 MHz)*
- Baseline LS S/N 001: 17 fsec (1 kHz – 1 MHz)
- Baseline LS S/N 002: 24 fsec (1 kHz – 1 MHz)
- Baseline LS S/N 004: 18 fsec (1 kHz – 1 MHz)

*integration bandwidth limited by test equipment in Hilo

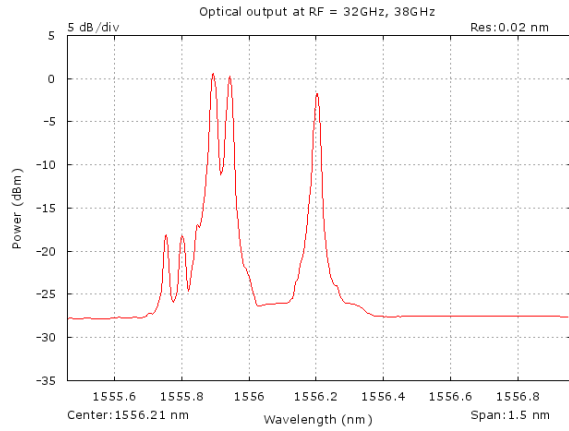
- MZM LS performance is ~35% better than the best performing baseline LS (at 100 GHz LO)
- However, other contributions to phase noise diminish the improvement provided by the MZM LS
- “*Development of a Mach-Zehnder Modulator Photonic Local Oscillator Source*”, IEEE Transactions on Microwave Theory and Techniques, VOL. 61, August 2013

ALMA LO REFERENCE TEST MODULE

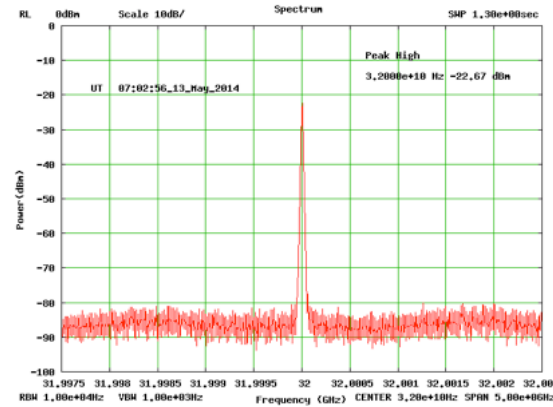
- MZM LORTM (D. Kubo, R. Srinivasan, J. Han, M.-T. Chen, 2010-2011)
 - Based on the previous Laser Synthesizer work, ASIAA-Hawaii took on the task to develop a MZM based LORTM for use at the ALMA East Asia Front End Integration Center (EA-FEIC) in Taichung, Taiwan
 - The unit was designed to support all bands with the exception of 1 and 5 (not required at EA-FEIC at the time)
 - The hardware and a substantial amount of software was delivered to EA-FEIC in August 2011
 - Software interface was through LabView
 - ASIAA-Taipei took on the role of developing ALMA band-1 in 2012
 - Sky coverage was 31-45 GHz but has been revised to 35-52 GHz
 - Existing TeraXion LS and LORTM do not cover the new frequency range
 - The MZM LORTM was modified March 2014 to support the new Band-1 requirements



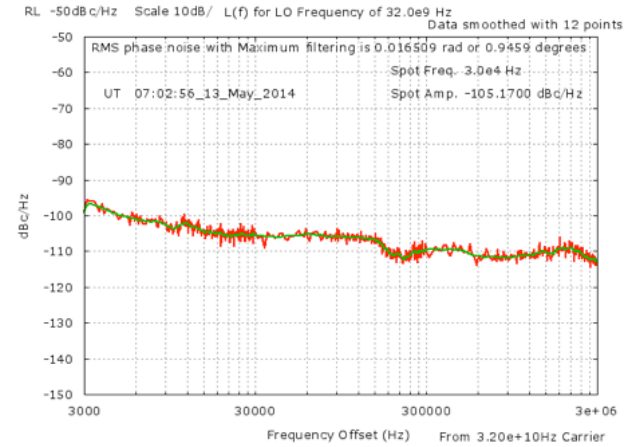
ALMA LO REFERENCE TEST MODULE



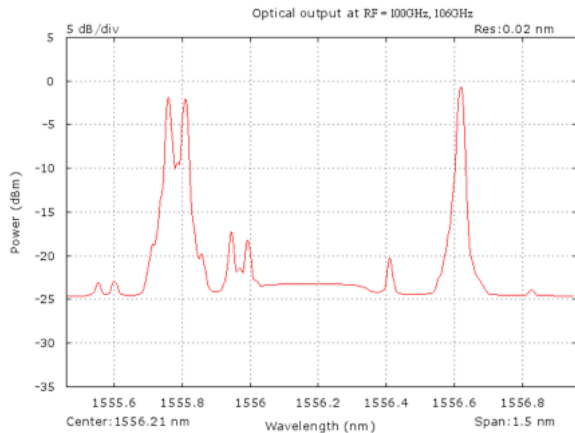
LORTM J2 Optical Output, LO = 32 GHz,
TS = 38 GHz



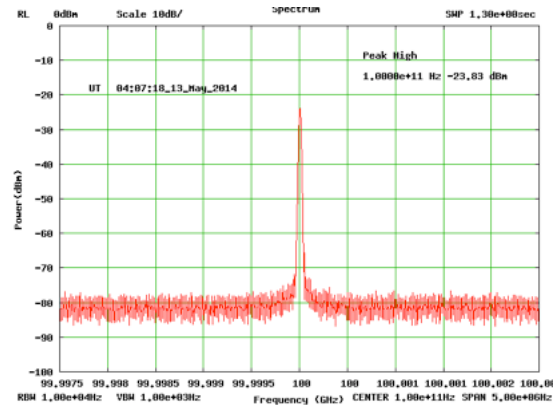
Photomixer RF output, LO = 32 GHz



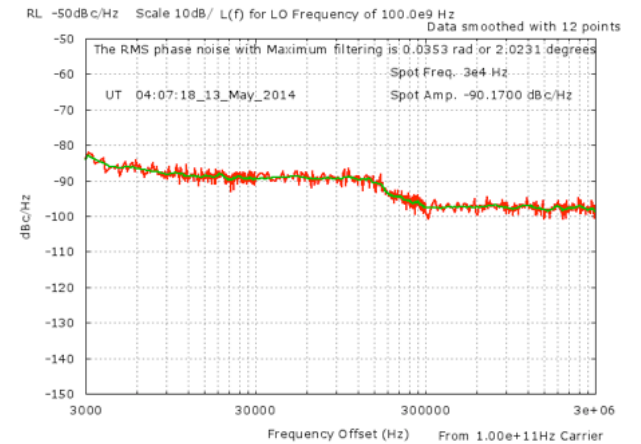
L(f) Plot, LO = 32.0 GHz



LORTM J2 Optical Output, LO = 100 GHz,
TS = 106 GHz

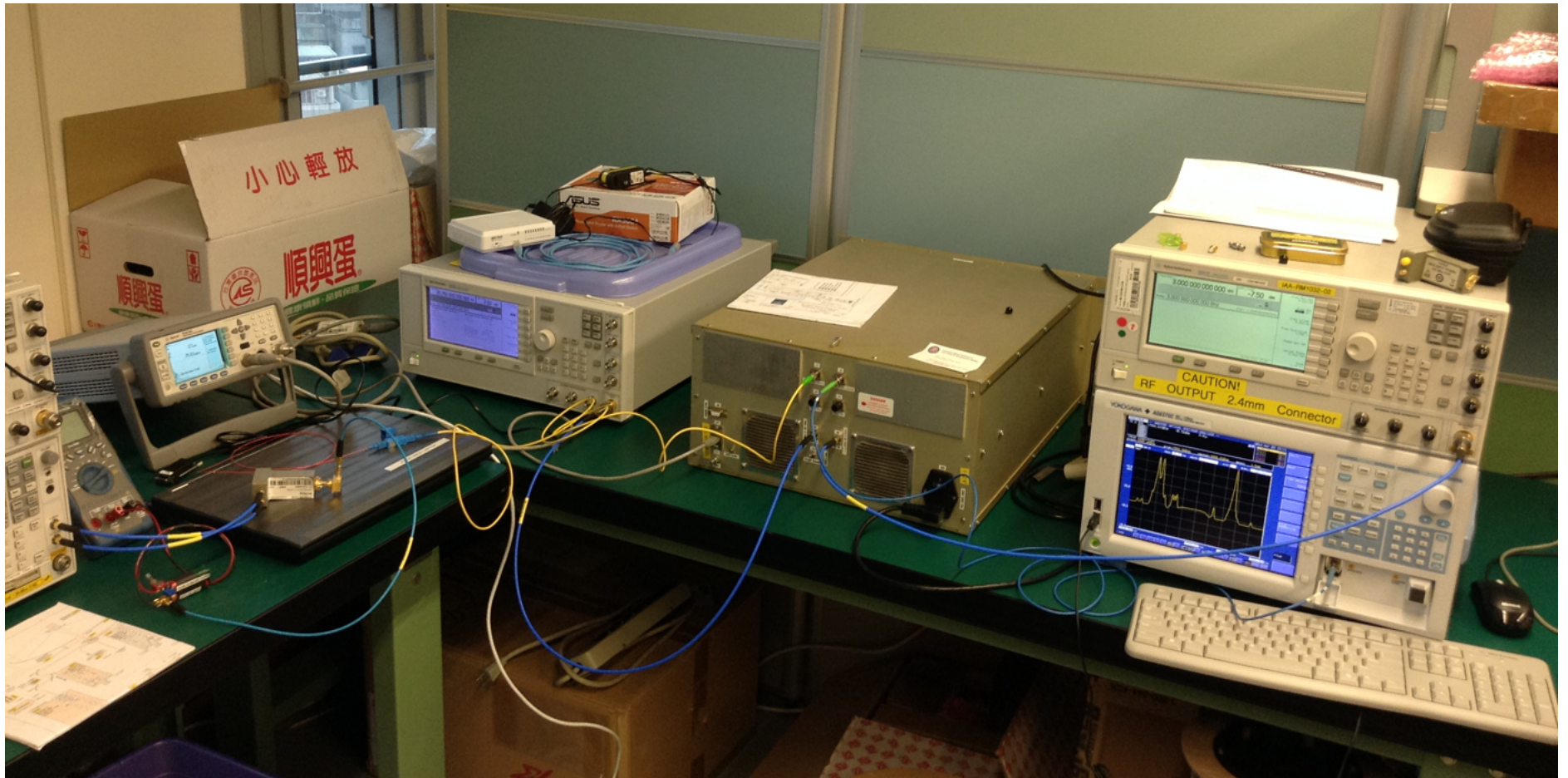


Photomixer RF output, LO = 100 GHz



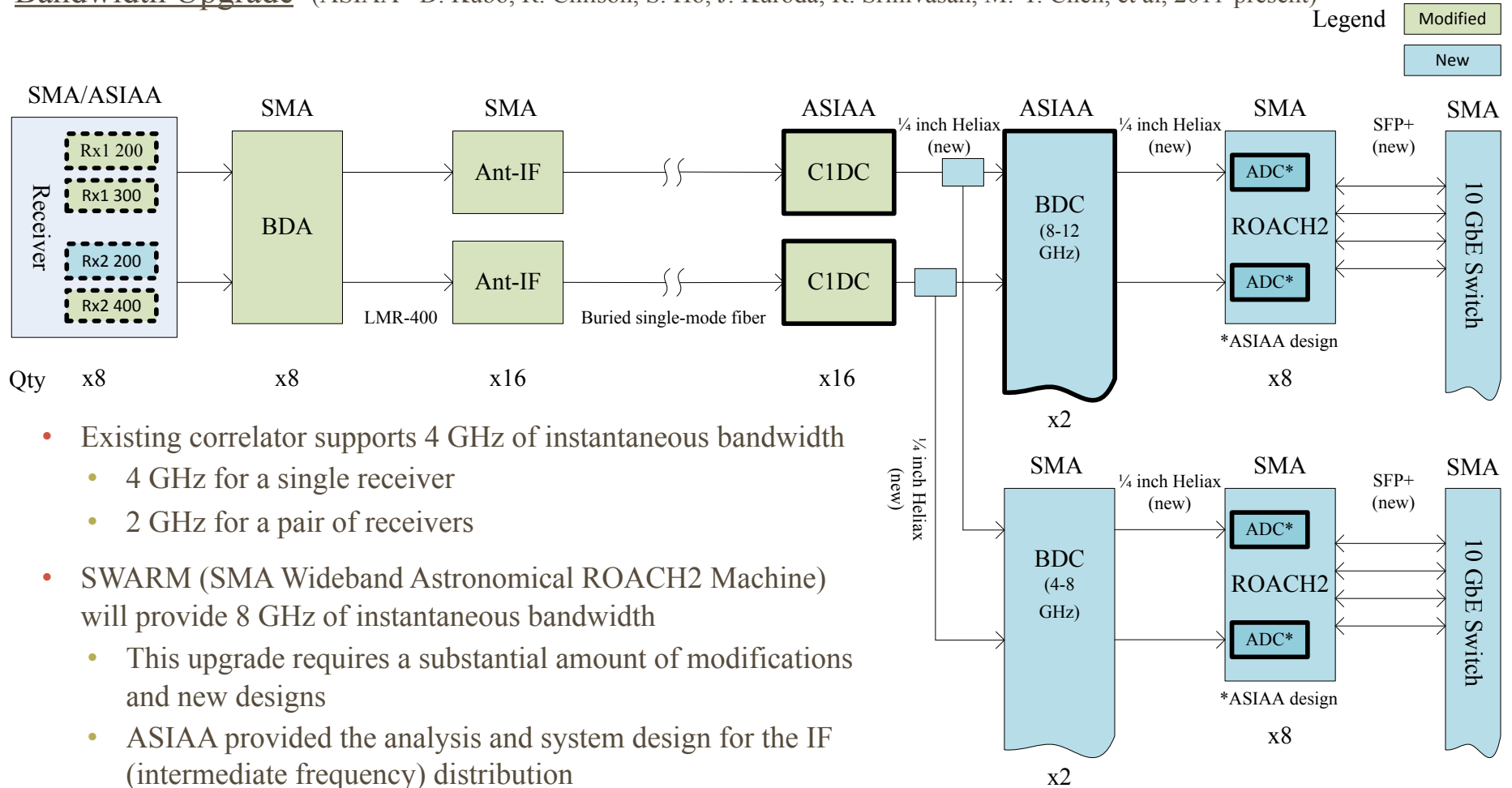
L(f) Plot, LO = 100.0 GHz

ALMA LO REFERENCE TEST MODULE



SMA WIDEBAND UPGRADE

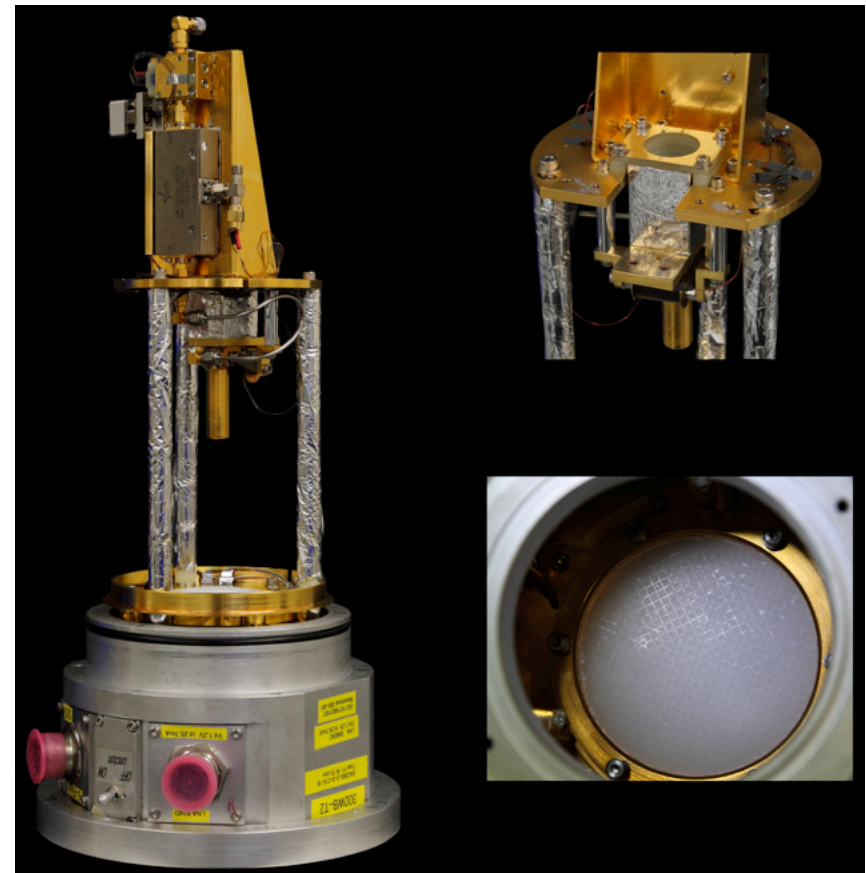
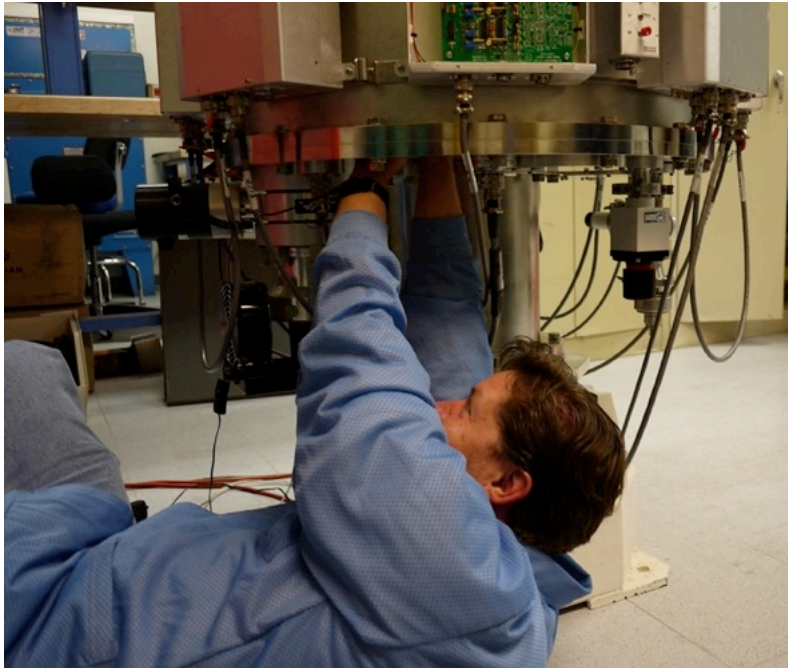
- Bandwidth Upgrade** (ASIAA - D. Kubo, R. Chilson, S. Ho, J. Kuroda, R. Srinivasan, M.-T. Chen, et al, 2011-present)



- Existing correlator supports 4 GHz of instantaneous bandwidth
 - 4 GHz for a single receiver
 - 2 GHz for a pair of receivers
- SWARM (SMA Wideband Astronomical ROACH2 Machine) will provide 8 GHz of instantaneous bandwidth
 - This upgrade requires a substantial amount of modifications and new designs
 - ASIAA provided the analysis and system design for the IF (intermediate frequency) distribution

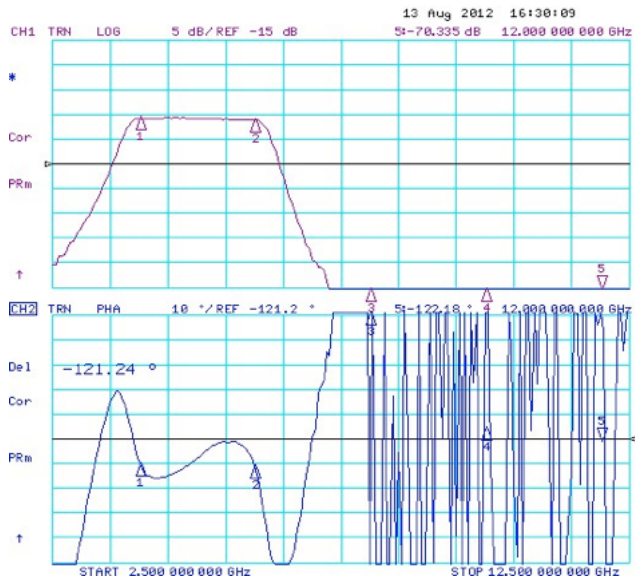
SMA WIDEBAND UPGRADE

- Receivers (x24 upgrade, x8 new) (J. Han, R. Chilson, M.-T. Chen, 2011-present)
 - Receiver-1 upgrades (IF output increased from 4-6 GHz \rightarrow 4-12 GHz)
 - 200 GHz receivers all complete (ASIAA 1, SAO 7)
 - 300 GHz receivers all complete (ASIAA 2, SAO 6)
 - Receiver-2 upgrades
 - 200 GHz receivers, 0/8 complete (new)
 - 400 GHz receivers, 3/8 complete (ASIAA 0, SAO 3)

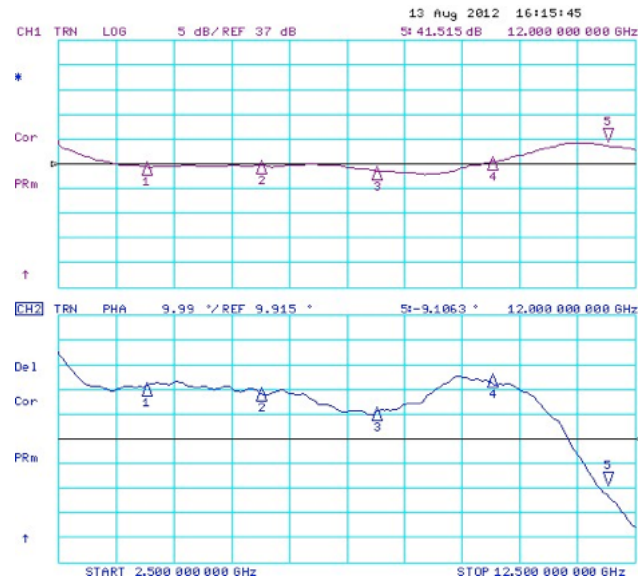


SMA WIDEBAND UPGRADE

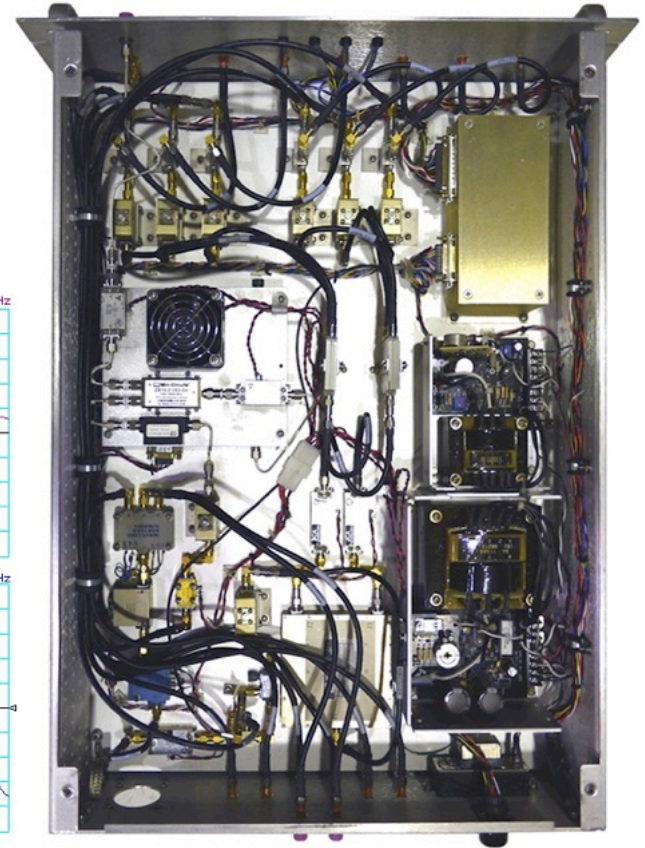
- Correlator 1st Down Converter (x16 upgrade) (S. Ho, J. Kuroda, D. Kubo, M.-T. Chen, 2012-present)
 - Each of the eight antennas require a pair of C1DCs to process the fiber optic signals
 - Ortel fiber optic transmitter & receiver provides 4-12 GHz of signal bandwidth
 - Only 4-6 GHz is used by existing legacy correlator
 - Upgrade consisted of the addition of wideband amplifiers, power divider, and band pass filter
 - Preserves the original function for the legacy correlator
 - Provides a new 4-12 GHz output for the SWARM correlator



4-6 GHz Legacy signal output

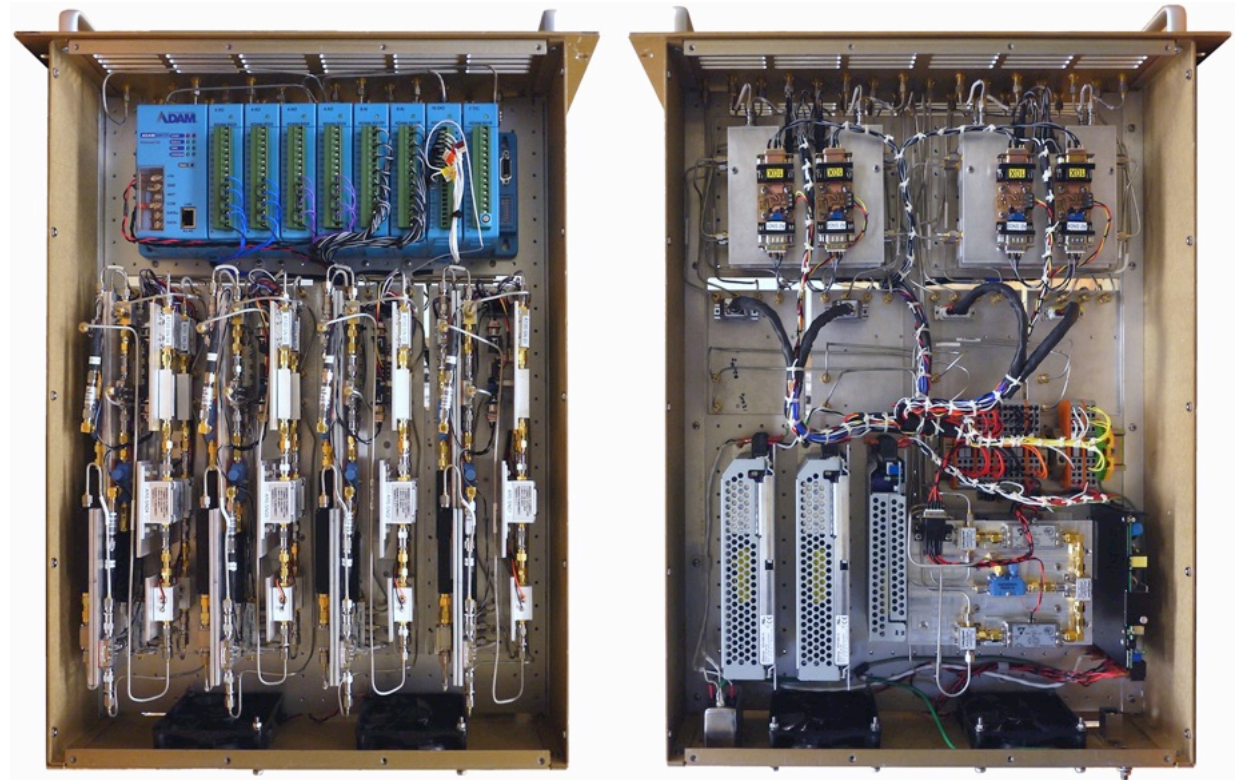


4-12 GHz SWARM output



SMA WIDEBAND UPGRADE

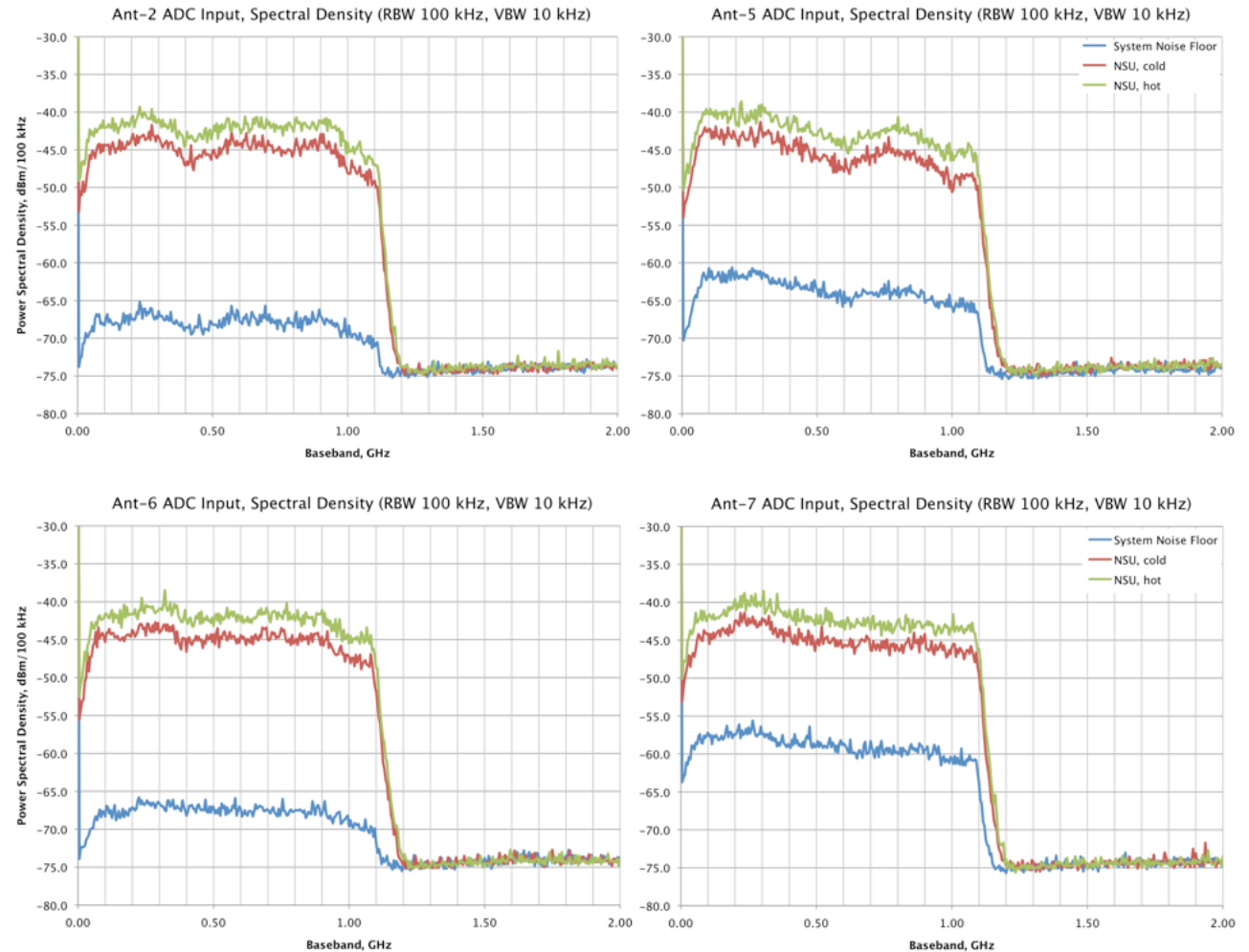
- Block Down Converter (x2 new) (R. Chilson, R. Srinivasan, D. Kubo, J. Kuroda, M.-T. Chen, 2011-2013)
 - The 4-12 GHz wideband IF signal from the C1DC requires frequency down conversion to baseband prior to digitization by the analog-to-digital converters (ADCs)
 - ASIAA developed and delivered two BDC units
 - Each BDC unit supports 4 antennas and 2 IF channels per antenna
 - 8-10 GHz portion is down converted to 0.05-2.15 GHz for digitization
 - 10-12 GHz portion is down converted to 0.05-2.15 GHz for digitization
 - For digitization
 - Additional signal leveling provided to optimize ADC input drive level



SMA WIDEBAND UPGRADE

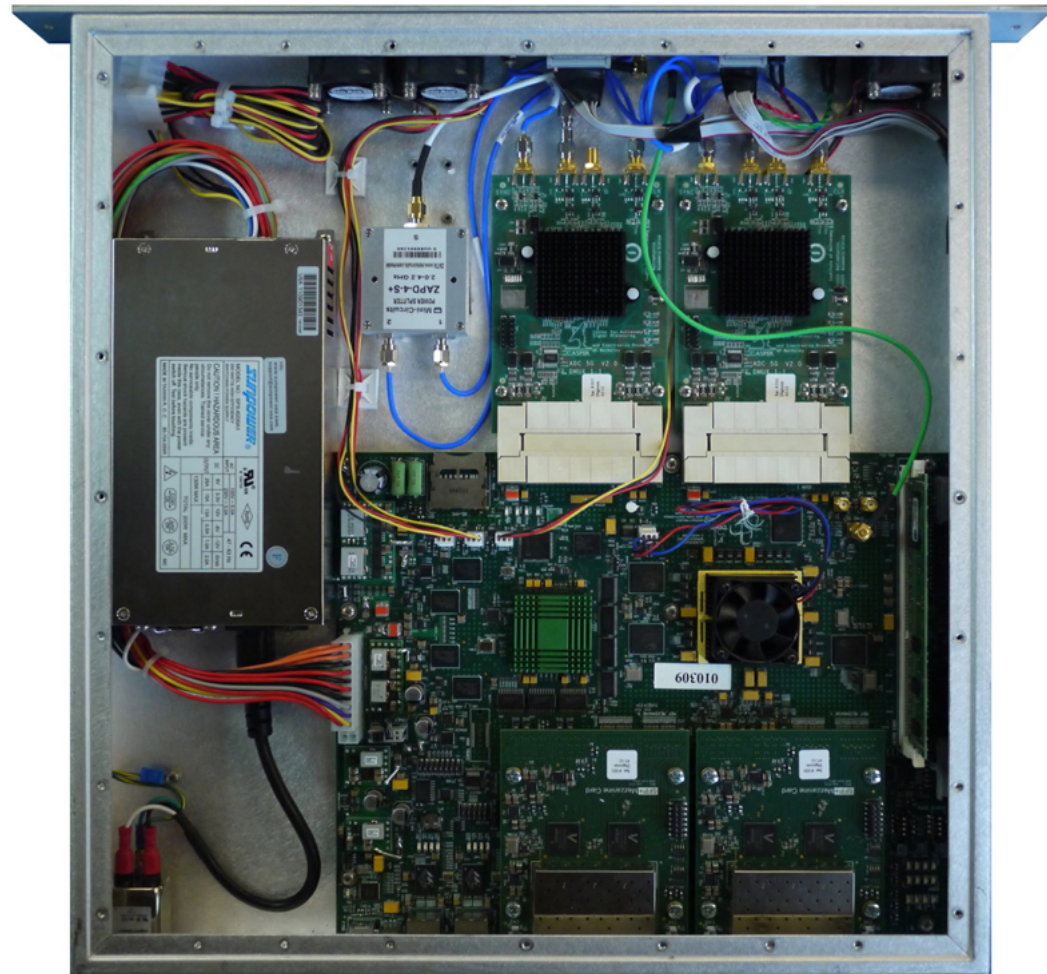
- Overall Cascaded Performance from Receiver Output to ADC input (D. Kubo, P. Yamaguchi, R. Chilson, M.-T. Chen, 2014)

- White Gaussian noise source was used in the antenna cabins to stimulate the IF system
 - 3 dB reduction in noise power represented by green to maroon change
 - Noise source removed represented by blue trace
 - 1 GHz low pass filter was purposely introduced at the BDC output to accommodate a lower ADC sampling speed



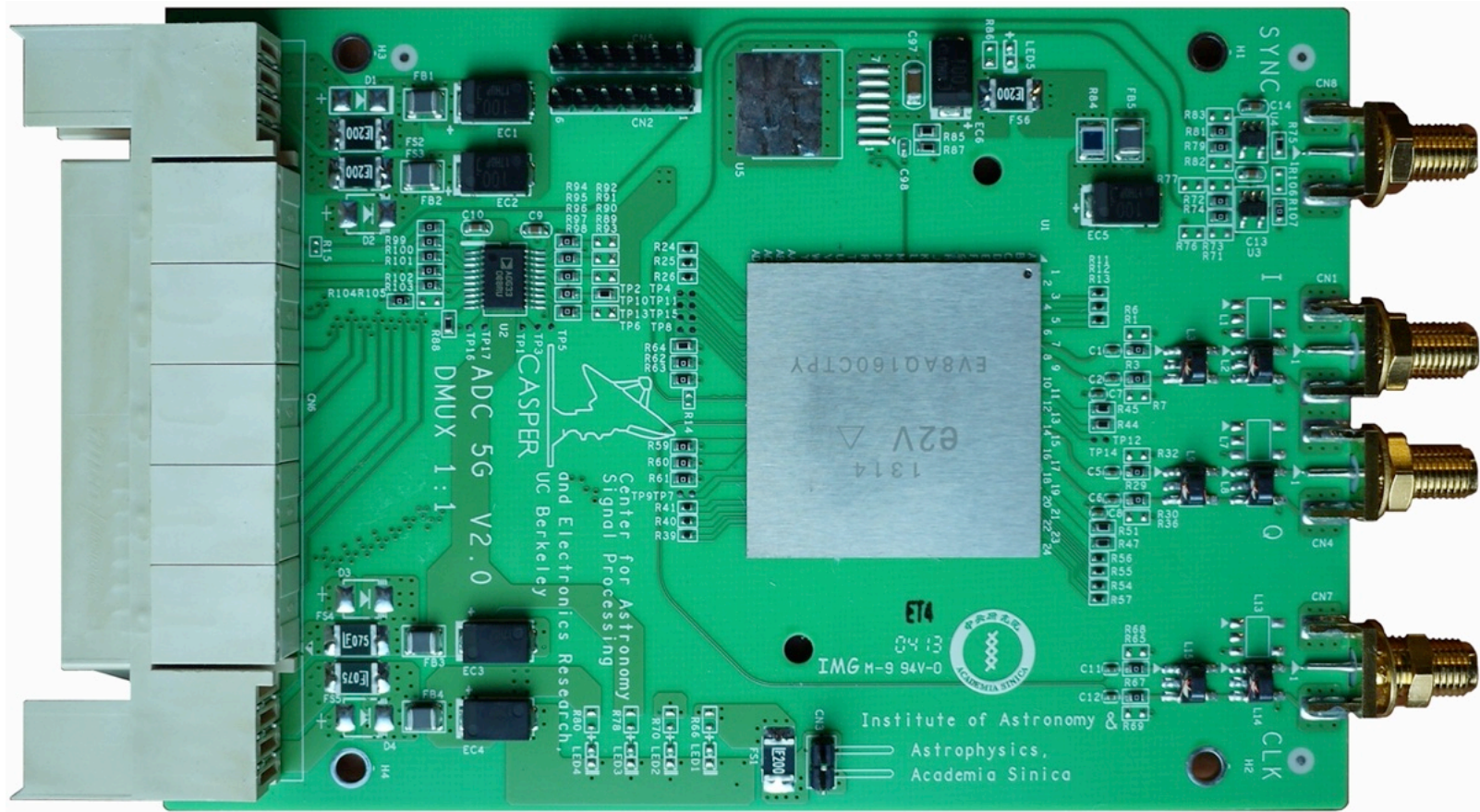
SMA WIDEBAND UPGRADE

- ROACH-2 with ASIAA Analog-to-Digital Converters (H.-M. Jiang, H. Liu, K. Guzzino, C.-T. Li, M.-T. Chen, et al, 2012)
 - Key enabling technologies:
 - ROACH-2 (Reconfigurable Open Architecture Configurable Hardware) provided by the CASPER consortium
 - Primary challenge of developing hardware has been replaced with the challenge of developing the FPGA code
 - 5 Gsps, 8-bit analog-to-digital converter (ADC) provided by ASIAA
 - SMA is currently clocking the two ADCs at 2.288 Gsps which produces an input rate of 36.608 Gbps into the ROACH-2
 - SMA's final targeted clock rate is 4.576 Gsps and will produce at total input rate of 73.216 Gbps



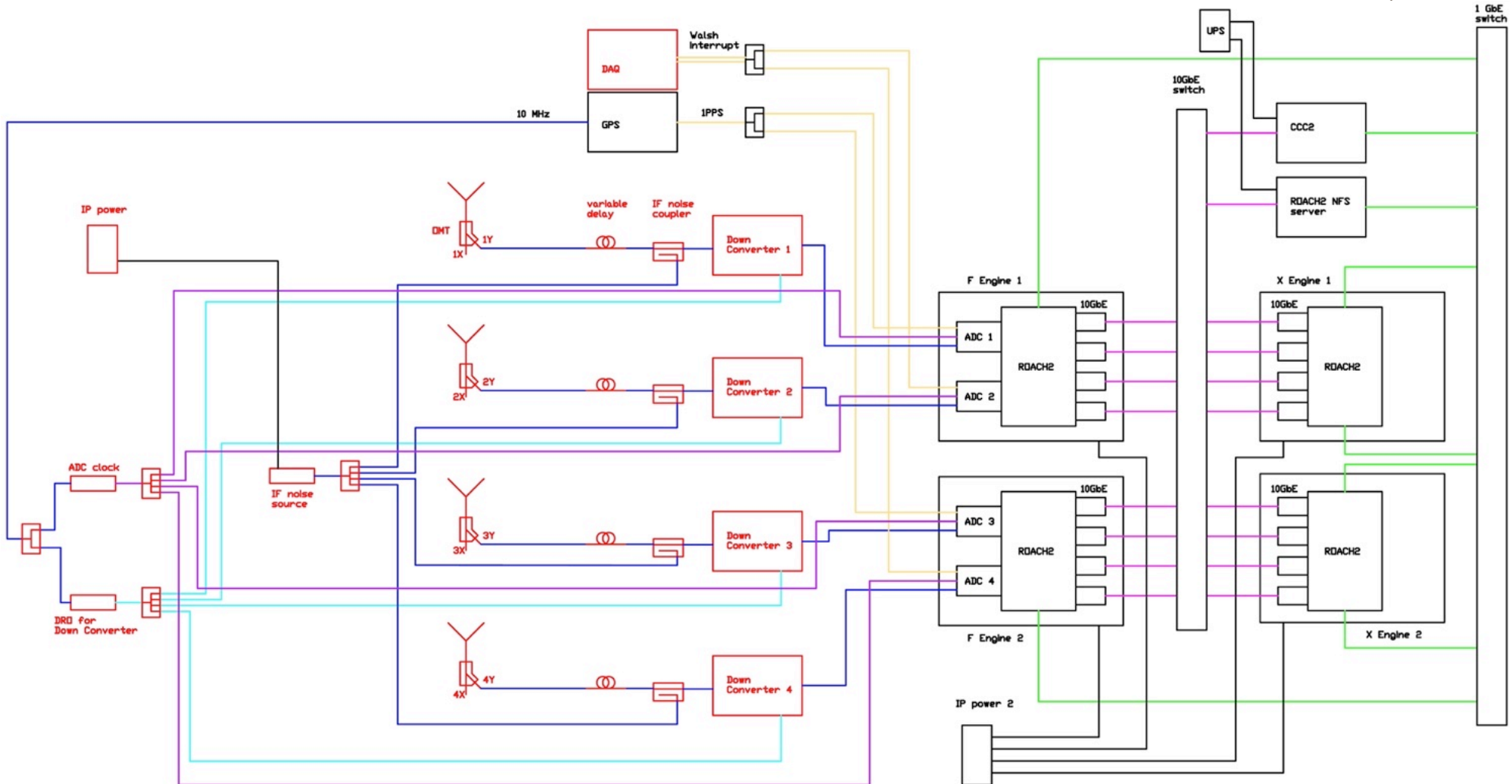
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AMIBA DIGITAL CORRELATOR

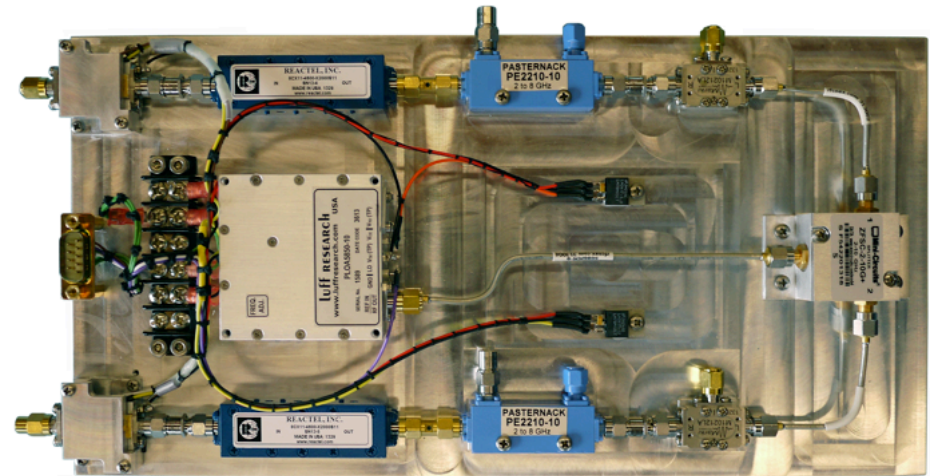
- 4-Element Prototype Digital Correlator (C.-T. Li, H.-M. Jiang, H. Liu, K. Guzzino, S. Ho, J. Kuroda, R. Srinivasan, D. Kubo, M.-T. Chen, 2014)



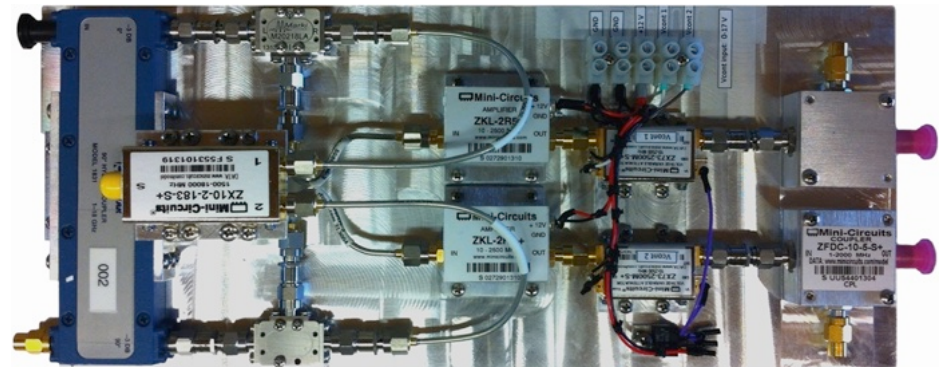
AMIBA DIGITAL CORRELATOR

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- Down Converter Plates
 - The prototype on Mauna Loa currently uses a pair of dual channel down converter plates to support 4 antennas
 - Observation fixed to 87.6-89.6 GHz band
 - Change in observing frequency requires changing Reactel filters
 - A prototype single channel I/Q down converter was made for testing in Taipei
 - Observation over any 4 GHz portion of the 86-102 GHz band
 - Requires twice as many ROACH-2s



Dual Channel Down Converter – Permits down conversion of any 2 GHz portion of the 2-18 GHz IF



Single Channel I/Q Down Converter – Permits down conversion of any 2 GHz portion of the 2-18 GHz IF

AMIBA DIGITAL CORRELATOR

- 4-Element Prototype Digital Correlator (C.-T. Li, H.-M. Jiang, H. Liu, K. Guzzino, S. Ho, J. Kuroda, R. Srinivasan, D. Kubo, M.-T. Chen, 2014)
 - Key enabling technologies:
 - ROACH-2 (Reconfigurable Open Architecture Configurable Hardware) provided by the CASPER consortium
 - Primary challenge of developing hardware has been replaced with the challenge of developing the FPGA code
 - 5 Gbps, 8-bit analog-to-digital converter (ADC) provided by ASIAA
 - We are currently clocking the two ADCs at 3.2 Gbps which produces an input rate of 51.2 Gbps into the ROACH-2
 - Our final targeted clock rate is 4.48 Gbps and will produce a total input rate of 71.68 Gbps

