Datasheet

X3G6509B8

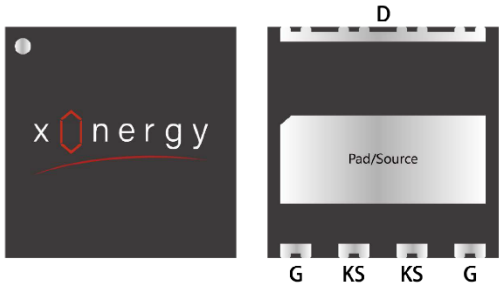
Contents

X3G6509B8

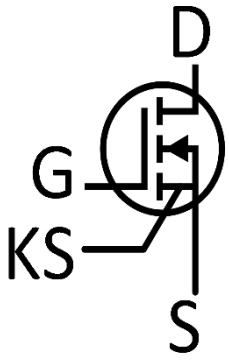
700V 82mΩ E-Mode GaN HEMT

Features

V_{DS}	$R_{DS(on)}$	I_{DS}
700V	82mΩ	20A



- High reliability
- High dv/dt capability
- Extremely low input capacitance
- Zero Qrr
- Outstanding switching performance
- Low system profile
- Dual gate pins



Applications

- Switching power supplies
- PC and server power supplies
- Adapters, quick chargers
- 5G power supplies

Description

- The X3G6509B8 is a 700V power GaN HEMT in DFN8x8 package with dual gate pins. Based on p-GaN enhancement mode (E-mode) GaN-on-silicon technology, it is a normally off and stand-alone device. Thanks to Xiinergy's proprietary design, the device can be switched at very high frequences in both soft-switching and hard-switching modes while still achieve high efficiency. In addition, Xiinergy's patented dual-gate-pin structure is designed to further improve switching performance and allow flexibility in PCB layout. Xiinergy adopts advanced packaging methods to obtain low thermal resistance and high device performance.

Type	Package	Qty
X3G6509B8	DFN8x8	3300

Device Characteristics

Static Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$V_{GS(th)}$	Gate threshold voltage	1	1.25	2.5	V	V_{DS}=V_{GS}, I_D=3.5mA, T_J=25°C
		0.7	1.15	2	V	V_{DS}=V_{GS}, I_D=3.5mA, T_J=150°C
BV_{DSS}	Drain-Source breakdown voltage	700			V	V_{GS}=0V, I_D=250μA, T_J=25°C
I_{DSS}	Drain-Source leakage current,		1		μA	V_{GS}=0V, V_{DS}=700V, T_J=25°C
			30		μA	V_{GS}=0V, V_{DS}=700V, T_J=150°C
I_{GSS}	Gate-Source leakage current		20		μA	V_{GS}=6V, V_{DS}=0V, T_J=25°C
$R_{DS(on)}$	Static drain-source on resistance		82		mΩ	V_{GS}=6V, I_D=5A, T_J=25°C
			195		mΩ	V_{GS}=6V, I_D=5A, T_J=150°C
V_{SD}	Reverse conduction voltage	1.6	1.7	2.1	V	I_{SD}=1A, V_{GS}=0V, T_J=25°C
R_G	Internal gate resistance		1.4		Ω	f=5MHz, open drain, T_J=25°C

Dynamic Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input capacitance		108		pF	V_{GS}=0V, V_{DS}=400V, f=1MHz T_J=25°C
C_{oss}	Output capacitance		32		pF	
C_{rss}	Reverse transfer capacitance		0.9		pF	
Q_g	Gate charge		3.9		nC	V_{DS}=400V, I_D=6A, V_{GS}=6V T_J=25°C
Q_{gs}	Gate to source charge		0.6		nC	
Q_{gd}	Gate to drain charge		1.8		nC	
Q_{rr}	Reverse recovery charge		0		nC	
DR_2/DR_1	Dynamic resistance ratio			1.1	-	V_{DS}=400V, T_J=25°C

Switching Performance

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(on)}$	Turn-on delay time		1.4		ns	V_{DS}=400V, I_D=10A V_{GS}=+6V/0V $R_{g(on)}$=15Ω, $R_{g(off)}$=3Ω L=70μH T_J=25°C
t_r	Rise time		2.2		ns	
$t_{d(off)}$	Turn-off delay time		3.7		ns	
t_f	Fall time		5.3		ns	
E_{on}	Turn on switching energy		11.2		μJ	
E_{off}	Turn off switching energy		5.3		μJ	

Absolute Max. Ratings

Symbol	Parameter	Value	Unit
$V_{DS\text{-}max}$	Breakdown voltage transient @T_J=25°C	850	V
$V_{GS\text{-}max}$	Gate to source max. transient voltage @T_J=25°C	-15 to +7	V
$I_{DS\text{-}max}$	Gate to source DC current @T_J=25°C	20	A
$I_{DS\text{-}max}$	Gate to source DC current @T_J=100°C	13	A
$I_{DS\ Pulse\text{-}max}$	Pulse drain current(Pulse width 50μs, V_{GS}=6V)	40	A
$dv/dt_{\text{-}max}$	Drain to source voltage slew rate	150	V/ns
$T_{J\text{-}max}$	Max junction temperature	150	°C
$T_{S\text{-}max}$	Storage temperature	-55 to 150	°C

Thermal Characteristics (Typical)

Symbol	Parameter	Typ.	Max.	Unit
R_{thJC}	Thermal resistance from junction to case	1.2		°C/W
R_{thJA}	Thermal resistance from junction to ambient		38	
T_{solder}	Reflow solding temperatre	260		°C

Characteristics Diagrams

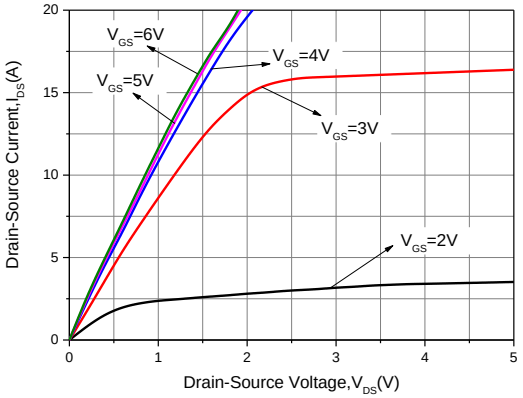


Figure 1.Output Characteristics T_J=25°C

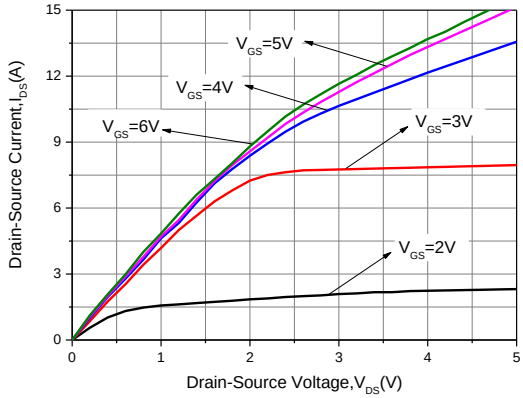


Figure 2.Output Characteristics T_J=150°C

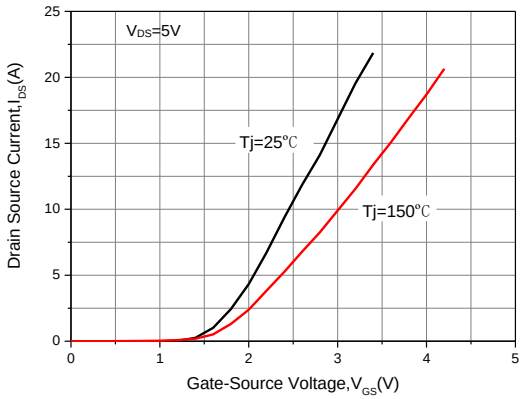


Figure 3.Transfer Characteristic for Vrious Junction Temperature

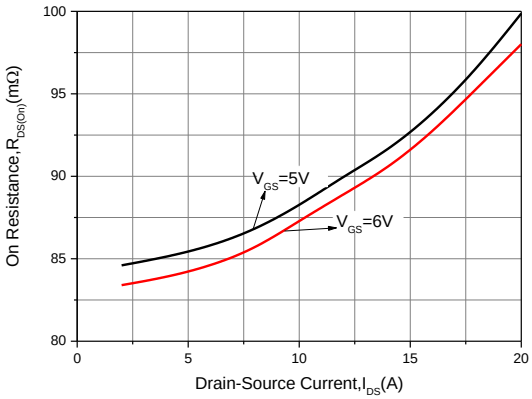


Figure 4.On-resistance vs.Drain Current For Various Gate Voltage @25°C

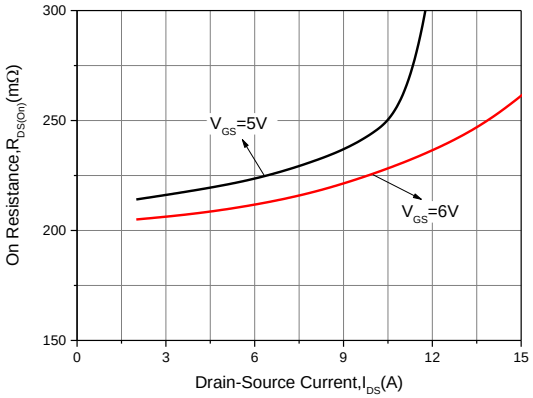


Figure 5.On-resistance vs.Temperature For Various Gate Voltage@150°C

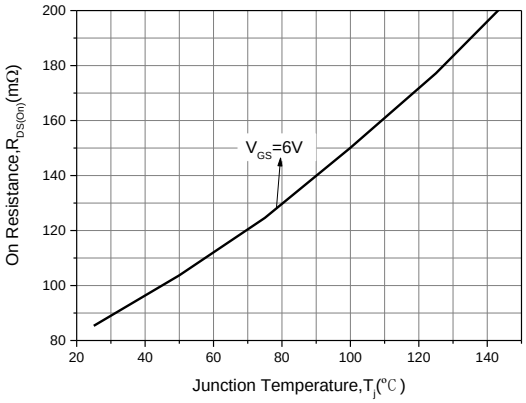


Figure 6. On-Resistance vs.Temperature

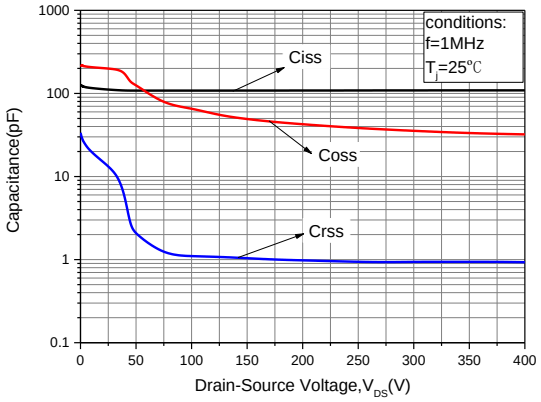


Figure 7.Capacitances vs.Drain-Source Voltage

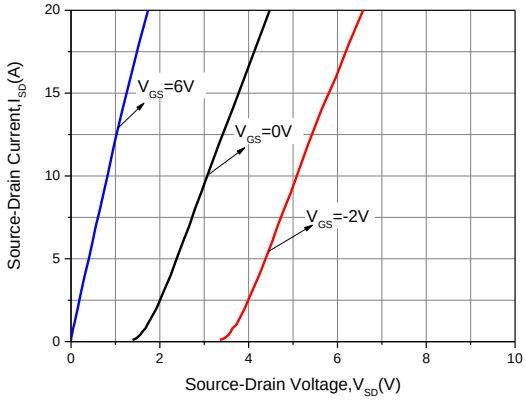


Figure 8.Channel Reverse Characteristic

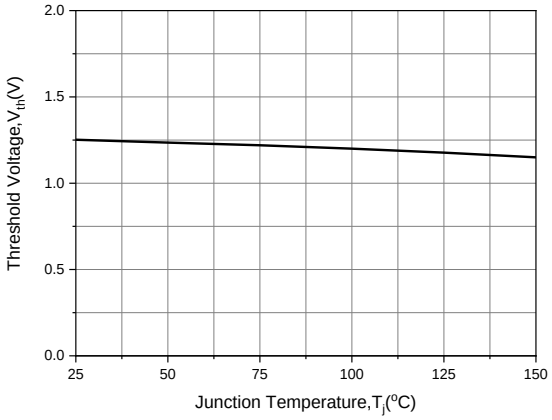


Figure 9.Threshold Voltage vs.Temperature

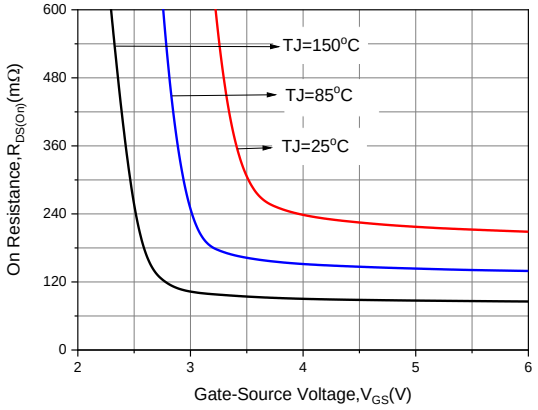


Figure 10.On-resistance vs.Gate Voltage @5A

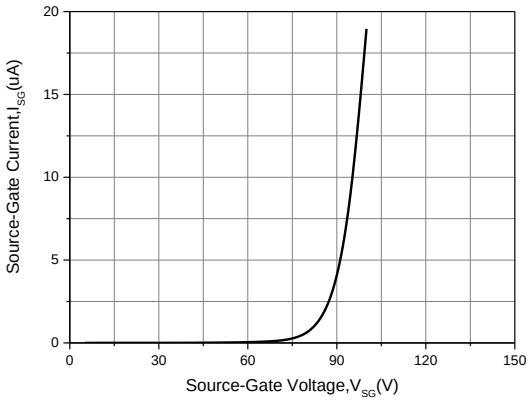


Figure 11.Reverse Gate Voltage

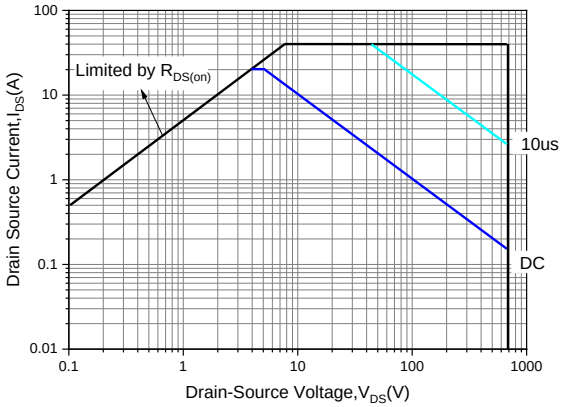


Figure 12.Safe Operating Area

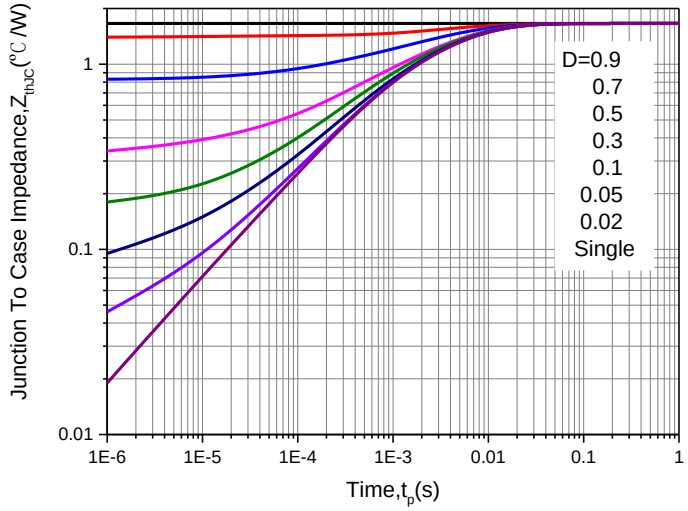
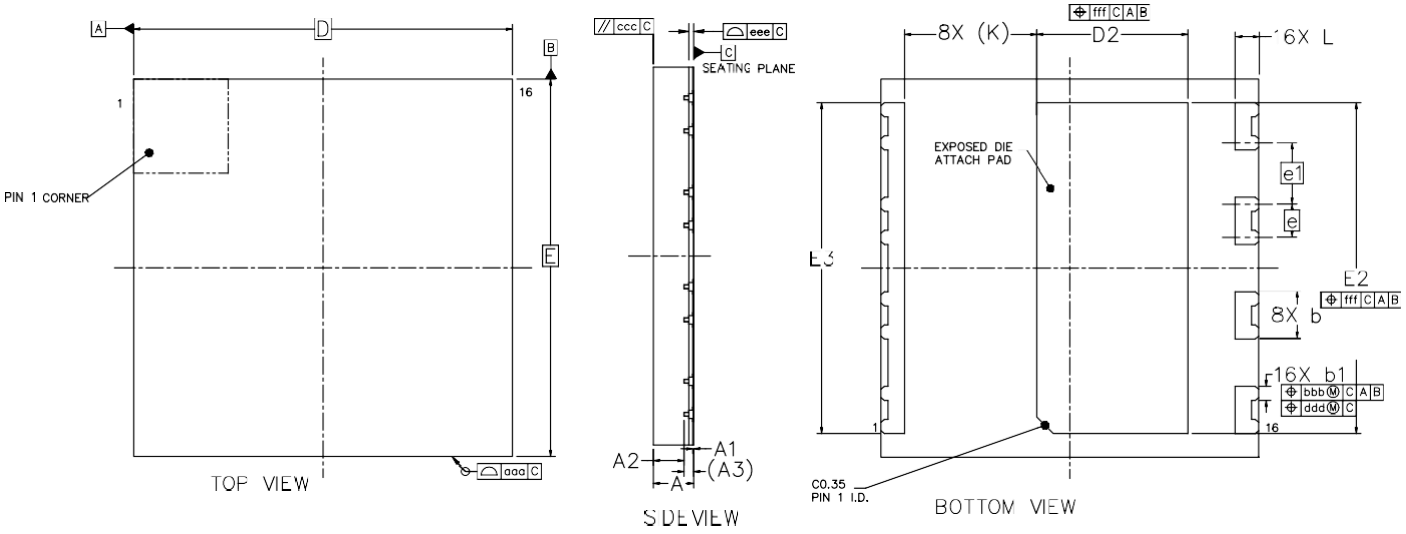


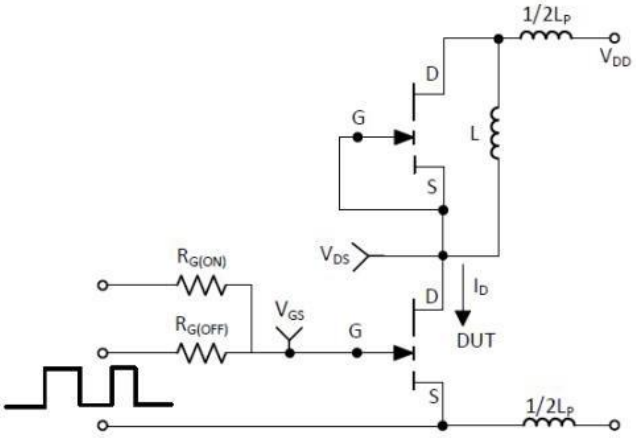
Figure 13.Transient Thermal Impedance(Junction-Case)

Package Dimensions

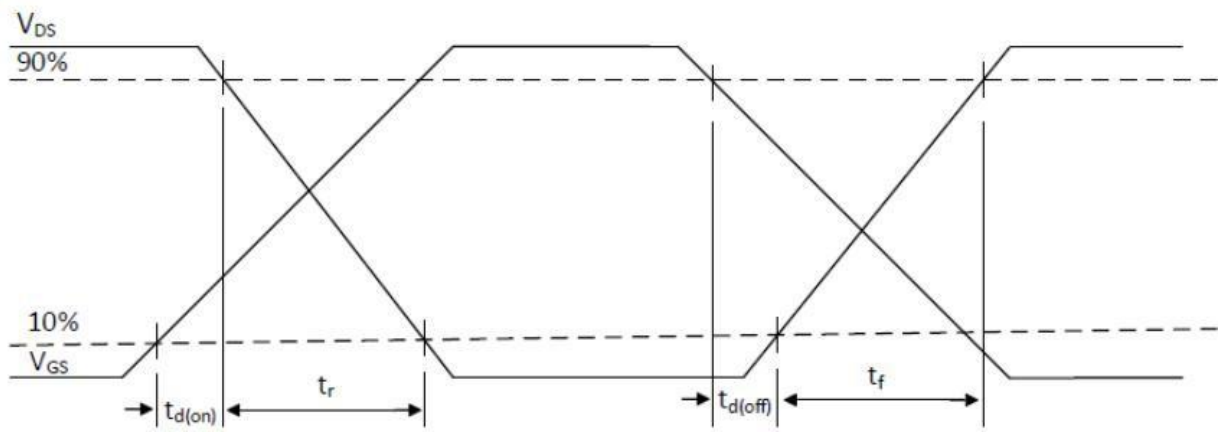


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.647	---
L/F THICKNESS		A3		0.203	
LEAD WIDTH		b	0.90	1.00	1.10
		b1	0.25	0.30	0.35
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.7 BSC	
		e1		1.3 BSC	
EP SIZE	X	D2	3.10	3.20	3.30
	Y	E2	6.90	7.00	7.10
	Y	E3	6.90	7.00	7.10
LEAD LENGTH		L	0.40	0.50	0.60
LEAD TIP TO EXPOSED PAD EDGE		K		2.8 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

Testing Conditions

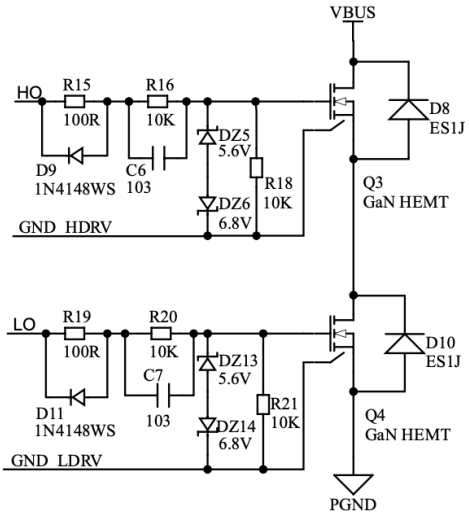


Switching Test Circuit

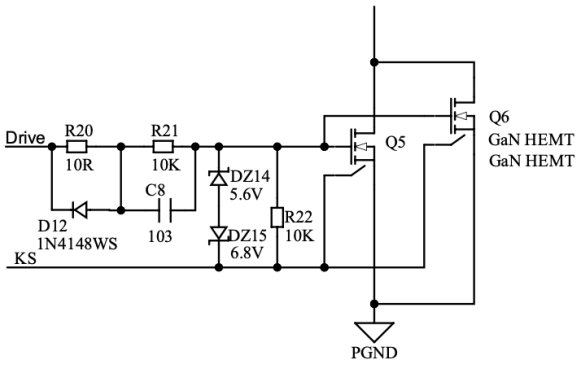


Switching Time Waveform

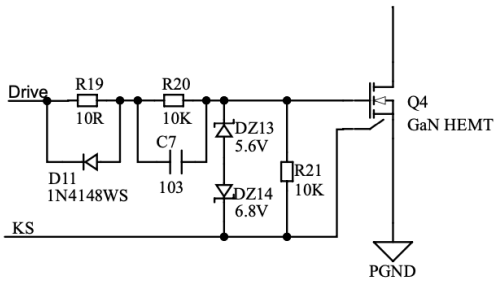
Gate Driving Examples



Half Bridge



Two Devices in Parallel



Single Device

Revision History

Document revision	Date	Description of changes
2.7	2023.10.27	Target datasheet
2.8	2023.12.26	Updated ordinate in Figure7
2.9	2024.3.28	Add Vth @150°C
3.0	2024.4.8	Add Dynamic Rdson

Important Notice

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