



# Datasheet

## X3G6509B8

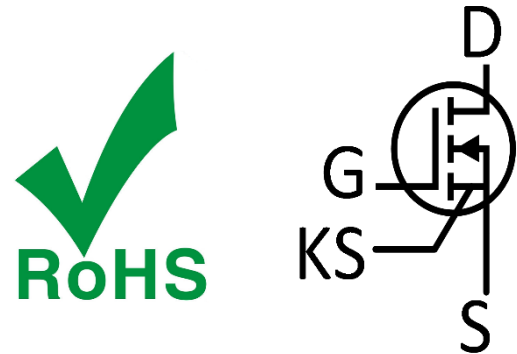
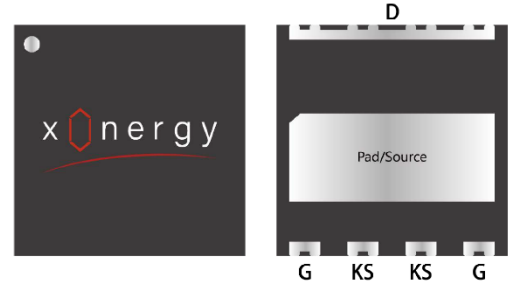
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## Features

$V_{DS}$	$R_{DS(on)}$	$I_{DS}$
700V	82mΩ	20A

- High reliability
- High dv/dt capability
- Extremely low input capacitance
- Zero Qrr
- Outstanding switching performance
- Low system profile
- Dual gate pins



## Applications

- Switching power supplies
- PC and server power supplies
- Adapters, quick chargers
- 5G power supplies

## Description

- The X3G6509B8 is a 700V power GaN HEMT in DFN8\*8 package with dual gate pins. Based on p-GaN enhancement mode (E-mode) GaN-on-silicon technology, it is a normally off and stand-alone device. The device can be switched at very high frequencies in both soft-switching and hard-switching modes while still achieve high efficiency. In addition, our patented dual-gate-pin structure is designed to further improve switching performance and allow flexibility in PCB layout. Advanced packaging methods are implemented to obtain low thermal resistance and high device performance.

Type	Package	Qty
X3G6509B8	DFN8*8	3300

## Device Characteristics

### Static Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$V_{GS(th)}$	Gate threshold voltage	1.2	1.6	2.3	V	$V_{DS}=V_{GS}$ , $I_D=3.5mA$ , $T_J=25^\circ C$
$BV_{DSS}$	Drain-Source breakdown voltage	700			V	$V_{GS}=0V$ , $I_D=250\mu A$ , $T_J=25^\circ C$
$I_{DSS}$	Drain-Source leakage current,		1	100	$\mu A$	$V_{GS}=0V$ , $V_{DS}=700V$ , $T_J=25^\circ C$
			30		$\mu A$	$V_{GS}=0V$ , $V_{DS}=700V$ , $T_J=150^\circ C$
$I_{GSS}$	Gate-Source leakage current		20	300	$\mu A$	$V_{GS}=6V$ , $V_{DS}=0V$ , $T_J=25^\circ C$
				500	$\mu A$	$V_{GS}=6V$ , $V_{DS}=0V$ , $T_J=125^\circ C$
$R_{DS(on)}$	Static drain-source on resistance		82	107	mΩ	$V_{GS}=6V$ , $I_D=5A$ , $T_J=25^\circ C$
			195		mΩ	$V_{GS}=6V$ , $I_D=5A$ , $T_J=150^\circ C$
$V_{SD}$	Reverse conduction voltage	1.6	1.7	2.1	V	$I_{SD}=1A$ , $V_{GS}=0V$ , $T_J=25^\circ C$
$R_G$	Internal gate resistance		1.4		Ω	$f=5MHz$ , open drain, $T_J=25^\circ C$

### Dynamic Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$C_{iss}$	Input capacitance		108		pF	$V_{GS}=0V$ , $V_{DS}=400V$ , $f=1MHz$ $T_J=25^\circ C$
$C_{oss}$	Output capacitance		32		pF	
$C_{rss}$	Reverse transfer capacitance		0.9		pF	
$Q_g$	Gate charge		3.9		nC	$V_{DS}=400V$ , $I_D=6A$ , $V_{GS}=6V$ $T_J=25^\circ C$
$Q_{gs}$	Gate to source charge		0.6		nC	
$Q_{gd}$	Gate to drain charge		1.8		nC	
$Q_{rr}$	Reverse recovery charge		0		nC	
$DR_2/DR_1$	Dynamic resistance ratio			1.1	-	$V_{DS}=400V$ , $T_J=25^\circ C$

### Switching Performance

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(on)}$	Turn-on delay time		1.4		ns	$V_{DS}=400V, I_D=10A$ $V_{GS}=+6V/0V$ $R_{g(on)}=15\Omega, R_{g(off)}=3\Omega$ $L=70\mu H$ $T_J=25^\circ C$
$t_r$	Rise time		2.2		ns	
$t_{d(off)}$	Turn-off delay time		3.7		ns	
$t_f$	Fall time		5.3		ns	
$E_{on}$	Turn on switching energy		11.2		$\mu J$	
$E_{off}$	Turn off switching energy		5.3		$\mu J$	

### Absolute Max. Ratings

Symbol	Parameter	Value	Unit
$V_{DS-max}$	Breakdown voltage transient @ $T_J=25^\circ C$	850	V
$V_{GS-max}$	Gate to source max. transient voltage @ $T_J=25^\circ C$	-15 to +7	V
$I_{DS-max}$	Gate to source DC current @ $T_C=25^\circ C$	20	A
$I_{DS-max}$	Gate to source DC current @ $T_C=100^\circ C$	13	A
$I_{DS\ pulse-max}$	Pulse drain current(Pulse width 50 $\mu s$ , $V_{GS}=6V$ )	40	A
$dv/dt-max$	Drain to source voltage slew rate	150	V/ns
$T_{J-max}$	Max junction temperature	150	$^\circ C$
$T_{S-max}$	Storage temperature	-55 to 150	$^\circ C$

### Thermal Characteristics (Typical)

Symbol	Parameter	Typ.	Max.	Unit
$R_{thJC}$	Thermal resistance from junction to case	1.2		$^\circ C/W$
$R_{thJA}$	Thermal resistance from junction to ambient		38	
$T_{solder}$	Reflow soldering temperature	260		$^\circ C$

### Characteristics Diagrams

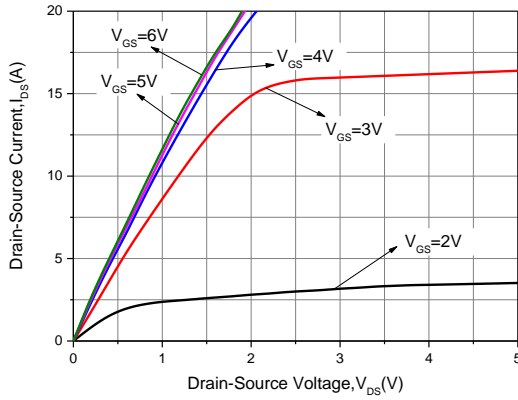


Figure 1. Output Characteristics  $T_j=25^\circ\text{C}$

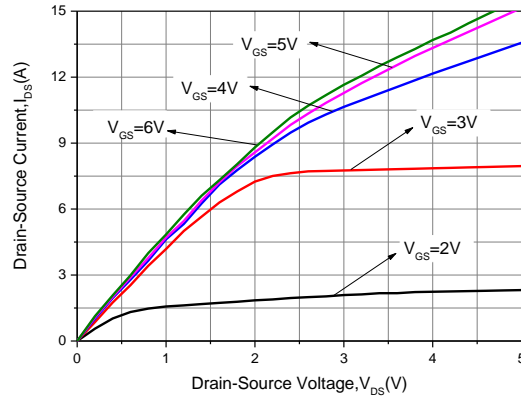


Figure 2. Output Characteristics  $T_j=150^\circ\text{C}$

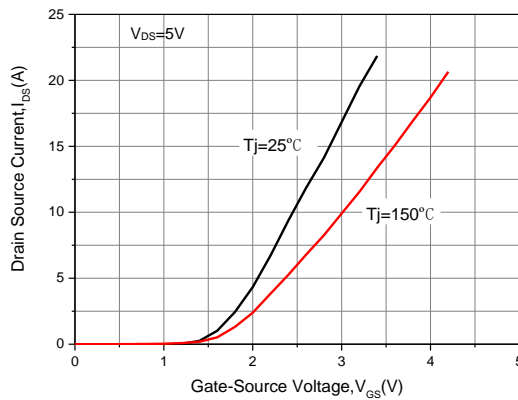


Figure 3. Transfer Characteristic for Various Junction Temperature

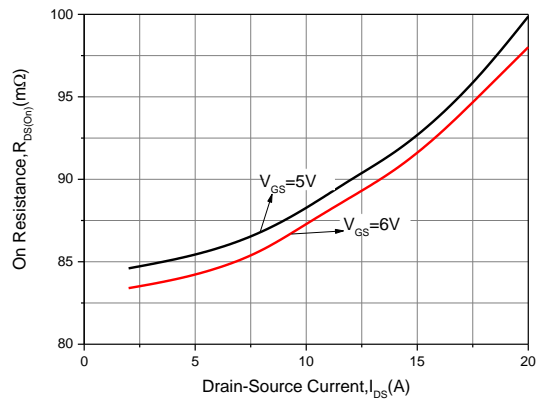


Figure 4. On-resistance vs. Drain Current For Various Gate Voltage @ $25^\circ\text{C}$

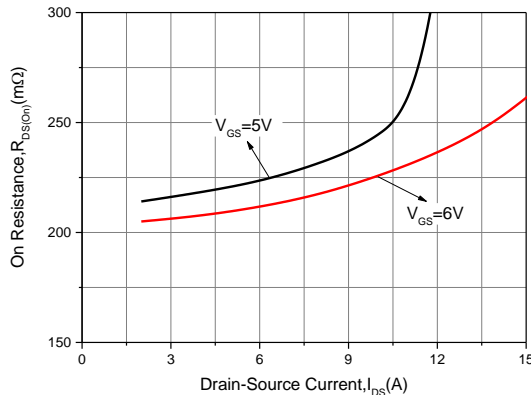


Figure 5. On-resistance vs. Temperature For Various Gate Voltage @ $150^\circ\text{C}$

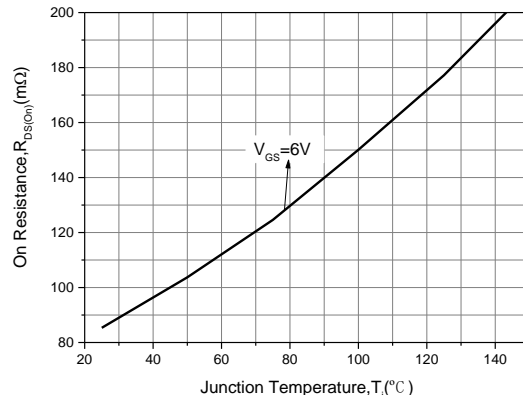


Figure 6. On-Resistance vs. Temperature

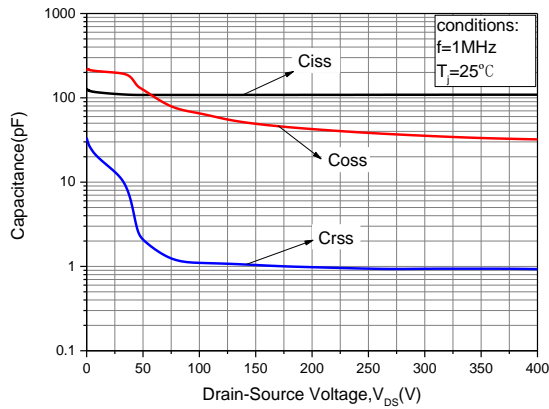


Figure 7. Capacitances vs. Drain-Source Voltage

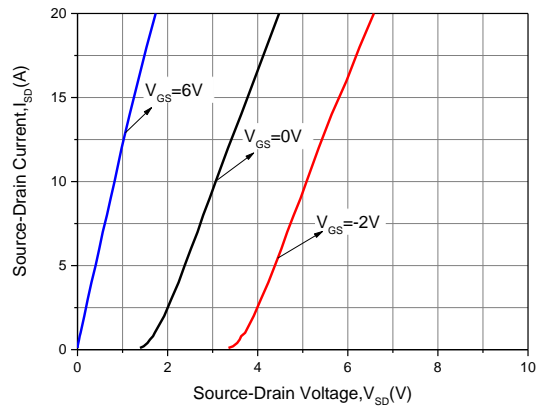


Figure 8. Channel Reverse Characteristic

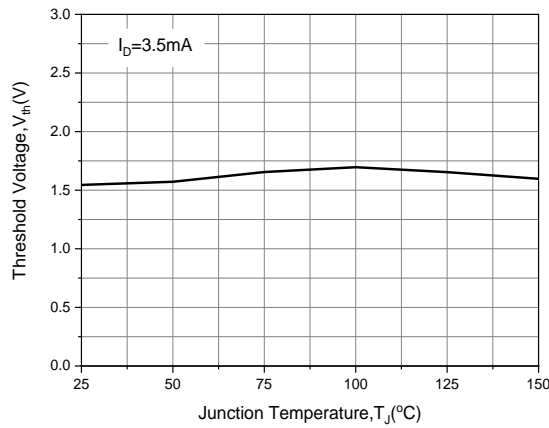


Figure 9. Threshold Voltage vs. Temperature

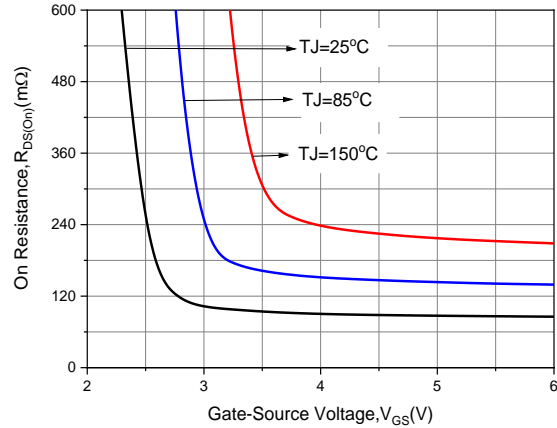


Figure 10. On-resistance vs. Gate Voltage @5A

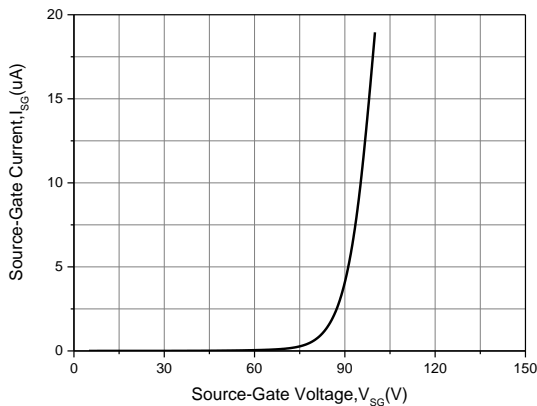


Figure 11. Reverse Gate Voltage

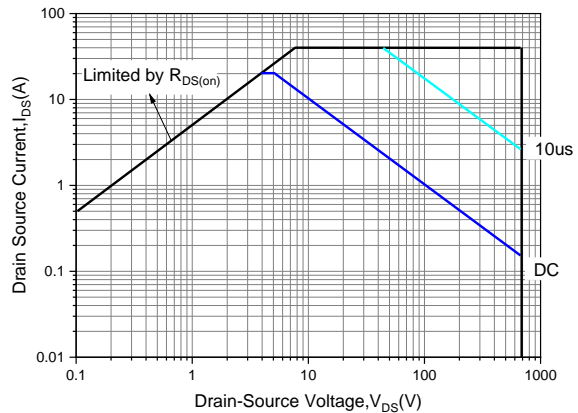


Figure 12. Safe Operating Area

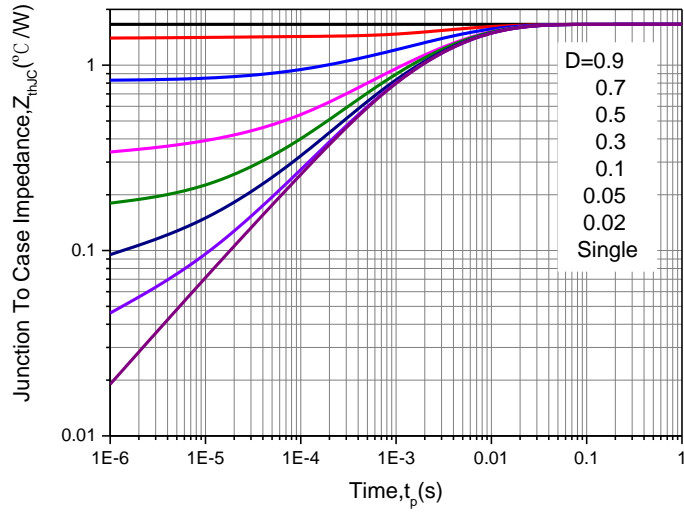
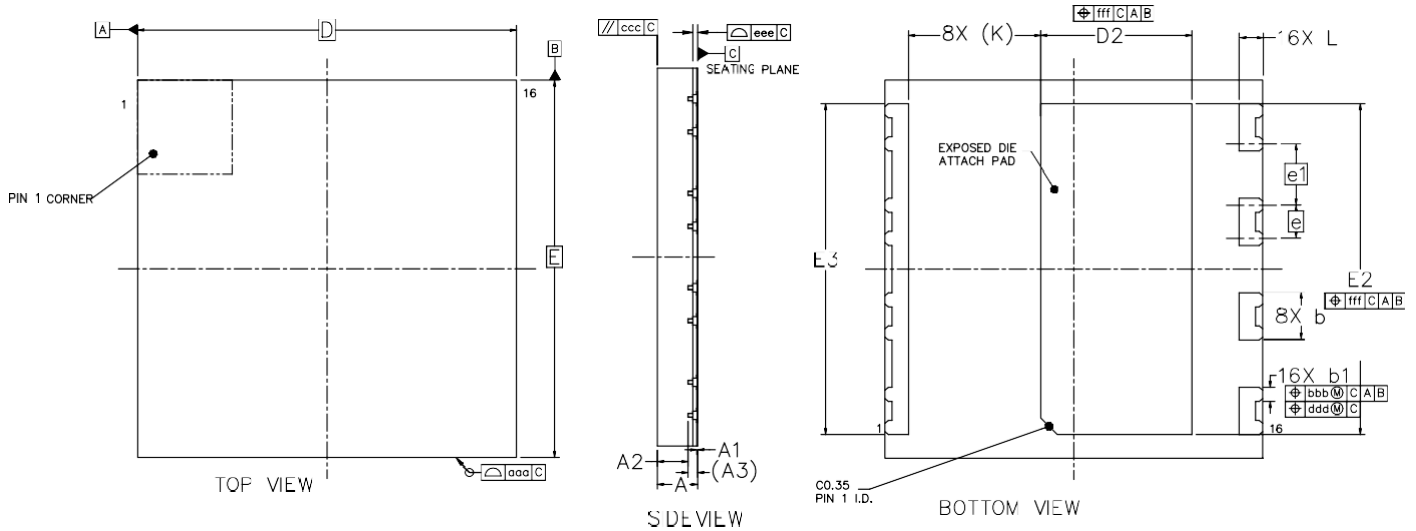


Figure 13. Transient Thermal Impedance (Junction-Case)

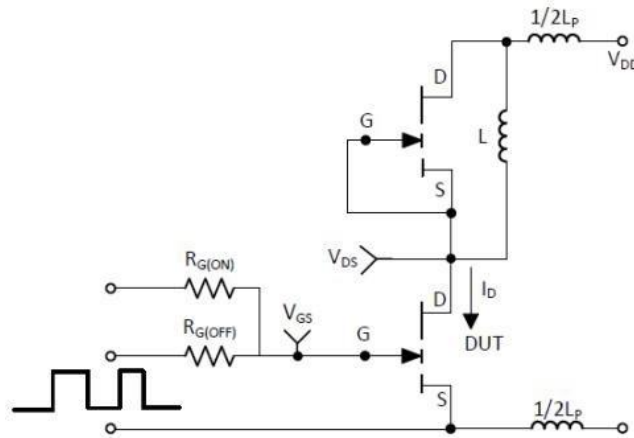
### Package Dimensions



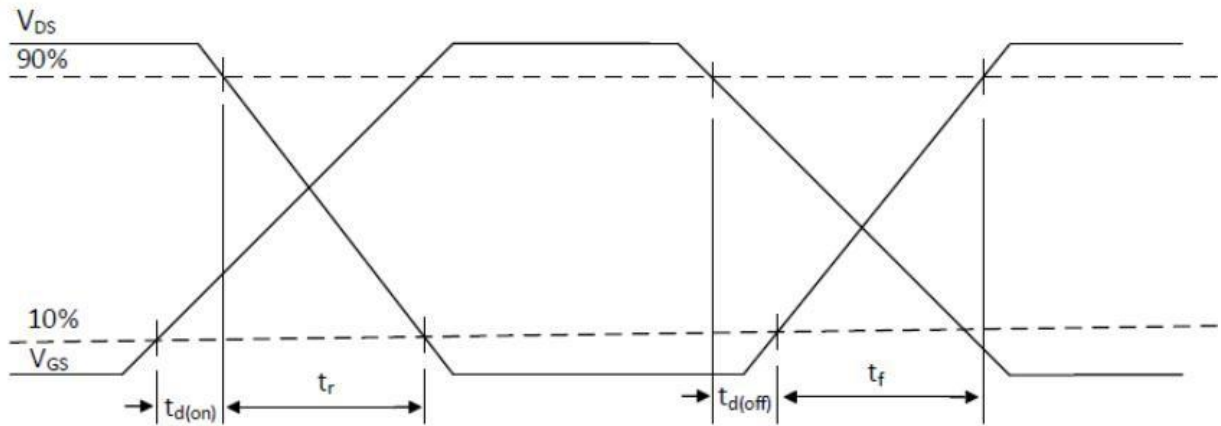
	SYMBOL	MIN	NOM	MAX	
TOTAL THICKNESS	A	0.80	0.85	0.90	
STAND OFF	A1	0	0.02	0.05	
MOLD THICKNESS	A2	---	0.647	---	
L/F THICKNESS	A3		0.203		
LEAD WIDTH	b	0.90	1.00	1.10	
	b1	0.25	0.30	0.35	
BODY SIZE	X	D	8 BSC		
	Y	E	8 BSC		
LEAD PITCH	e	0.7 BSC			
	e1	1.3 BSC			
EP SIZE	X	D2	3.10	3.20	3.30
	Y	E2	6.90	7.00	7.10
	Y	E3	6.90	7.00	7.10
LEAD LENGTH	L	0.40	0.50	0.60	
LEAD TIP TO EXPOSED PAD EDGE	K	2.8 REF			
PACKAGE EDGE TOLERANCE	aaa	0.1			
MOLD FLATNESS	ccc	0.1			
COPLANARITY	eee	0.08			
LEAD OFFSET	bbb	0.1			
	ddd	0.05			
EXPOSED PAD OFFSET	fff	0.1			



Testing Conditions

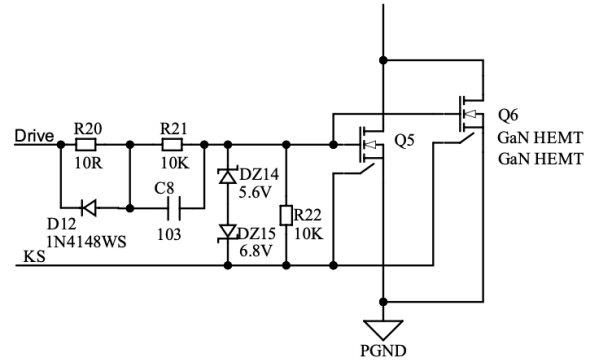
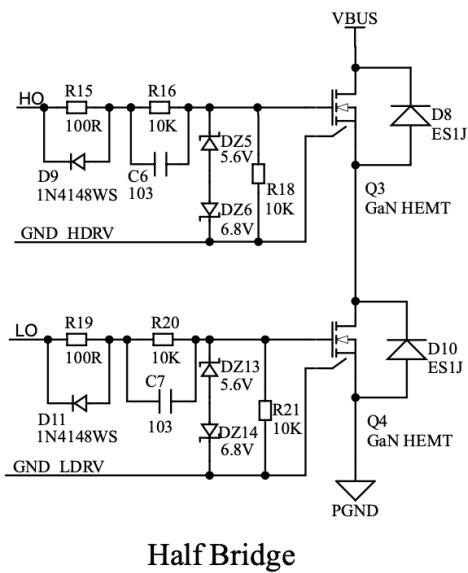


Switching Test Circuit

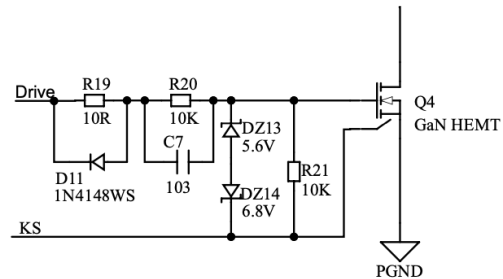


Switching Time Waveform

### Gate Driving Examples



**Two Devices in Parallel**



**Single Device**

## Revision History

Document revision	Date	Description of changes
2.7	2023.10.27	Target datasheet
2.8	2023.12.26	Updated ordinate in Figure7
2.9	2024.3.28	Add Vth @150°C
3.0	2024.4.8	Add Dynamic Rdson
3.1	2025.3.6	Revise Vth



X3G6509B8  
700V 82mΩ E-Mode GaN HEMT

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## Important Notice

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### Questions?

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