Datasheet

X3USN0103X0D2A

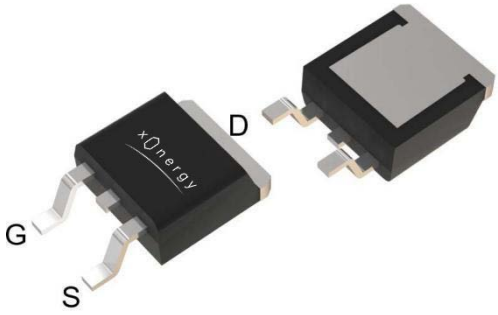
Contents

X3USN0103X0D2A

100V N-Channel Advanced Power MOSFET

Features

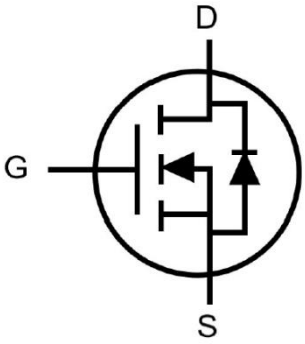
V_{DS}	$R_{DS(on)}$@V_{GS}=10V	I_D
100V	2.2mΩ	180A



- Excellent FoM
- Low $R_{DS(on)}$ to minimize conduction losses
- 100% ΔVDS、UIS & R_g Tested

Applications

- Hard Switching and High Speed Circuit
- Synchronous Rectification in SMPS
- DC/DC in Telecoms and Industrial



HF Halogen-Free

Pb-Free RoHS

Type	Package	Qty
X3USN0103X0D2A	TO-263	800

Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage		100	V
V_{GS}	Gate-Source Voltage		±20	V
I_S	Diode Continuous Forward Current (Wire bond limited)	T_C = 25°C	180	A
I_D	Continuous Drain Current @VGS=10V(Wire bond limited)	T_C = 25°C	180	A
	Continuous Drain Current @VGS=10V (Silicon limited)	T_C = 25°C	246	A
		T_C = 100°C	174	A
I_{DM}	Pulse Drain Current Tested ①	T_C=25°C	861	A
EAS	Maximum Avalanche Energy, Single Pulsed ②		1170	mJ
P_D	Maximum Power Dissipation ③	T_C=25°C	300	W
P_{DSM}	Maximum Power Dissipation ④	T_A=25°C	3.6	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	0.39	0.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	29	42	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current (T_J=25℃)	V_{DS}=100V, V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current (T_J=125℃)	V_{DS}=100V, V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V, V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.5	3	3.5	V
$R_{DS(on)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=50A	--	2.2	3.0	mΩ
		(T_J= 100 ℃)	--	3.4	--	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V_{DS}=50V,V_{GS}=0V, f=1 MHz	--	7765	--	pF
Coss	Output Capacitance		--	1295	--	pF
Crss	Reverse Transfer Capacitance		--	27	--	pF
Rg	Gate Resistance	f=1MHz	--	3.7	--	Ω
Qg	Total Gate Charge	V_{DS}=50V,I_D=20A, V_{GS}=10V	--	82	--	nC
Qgs	Gate-Source Charge		--	21	--	nC
Qgd	Gate-Drain Charge		--	27	--	nC
Switching Characteristics						
Td(on)	Turn-On Delay Time	V_{DD}=50V, I_D=20A, R_G=3Ω, V_{GS}=10V	--	22.8	--	ns
Tr	Turn-On Rise Time		--	17	--	ns
Td(off)	Turn-Off Delay Time		--	68.4	--	ns
Tf	Turn-Off Fall Time		--	15.2	--	ns
Source- Drain Diode Characteristics@ T_J= 25°C (unless otherwise stated)						
V_{SD}	Forward on Voltage	I_{SD}=50A, V_{GS}=0V	--	0.88	1	V
Trr	Reverse Recovery Time	V_{DD}=50V I_{SD}=20A, V_{GS}=0V di/dt=143A/μs	--	62	--	ns
Qrr	Reverse Tecovery Charge		--	208	--	nC

NOTE:
① This current is calculated on single pulse with 10us Pulse & Duty Cycle =10%
② This maximum value is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 68A, V_{GS} =10V； 100% FT tested at L = 0.5mH, I_{AS} = 33A.
③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.
④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.
⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.
⑥ The value of RθJA is measured with the device in a still air environment with TA =25°C.

Characteristics Diagrams

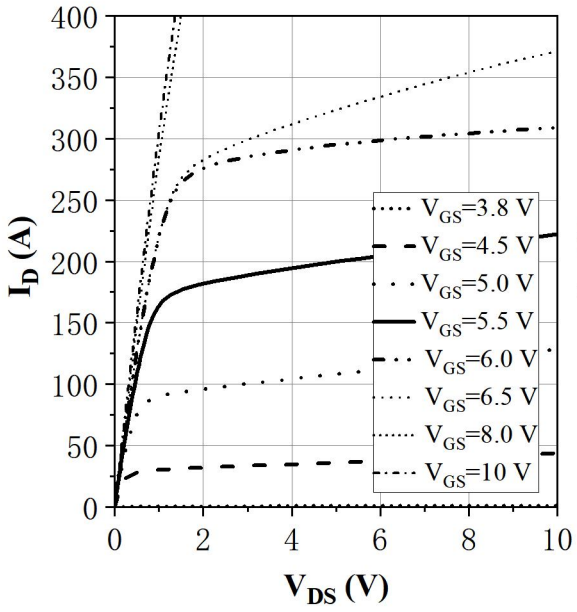


Fig 1. Output Characteristics

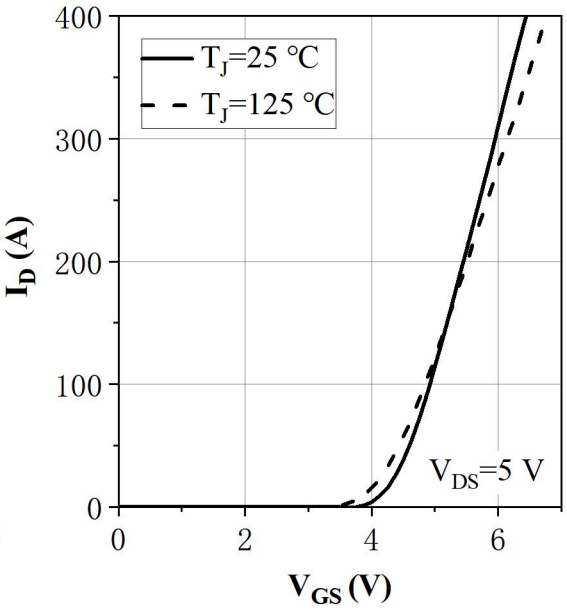


Fig 2. Transfer Characteristics

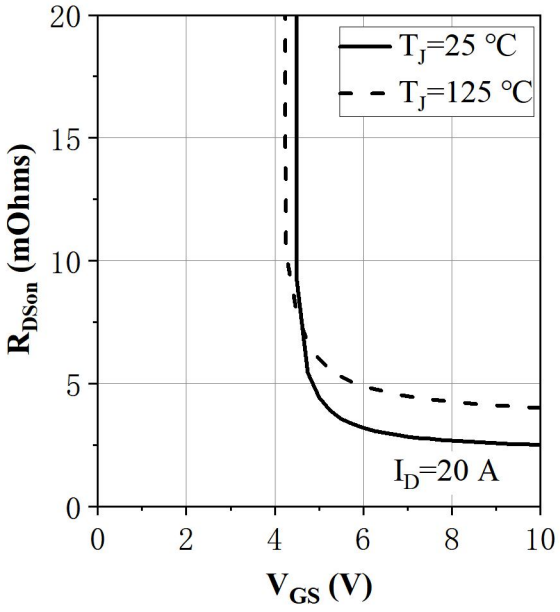


Fig 3. On-Resistance vs. Gate-Source Voltage

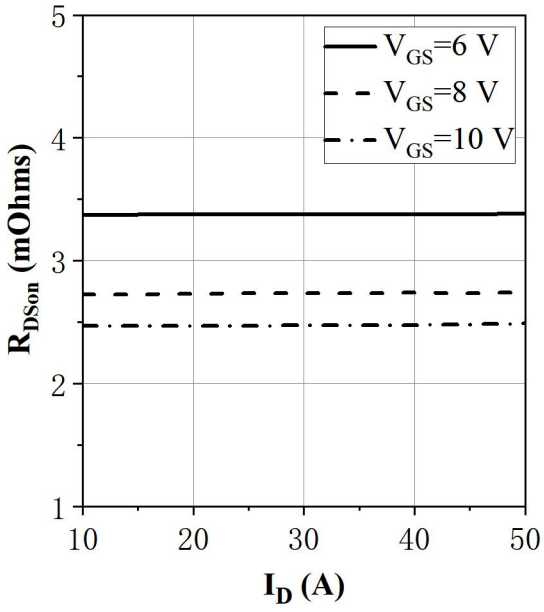


Fig 4. On-Resistance vs. Drain Current

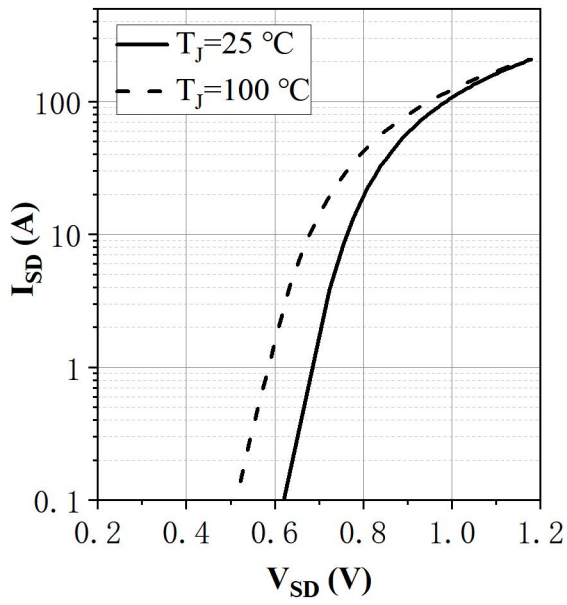


Fig 5. Source-Drain Diode Forward Voltage

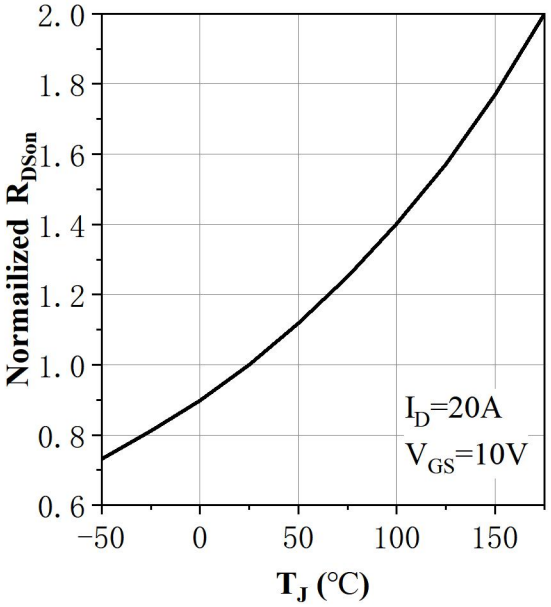


Fig 6. On-Resistance vs. Junction Temperature

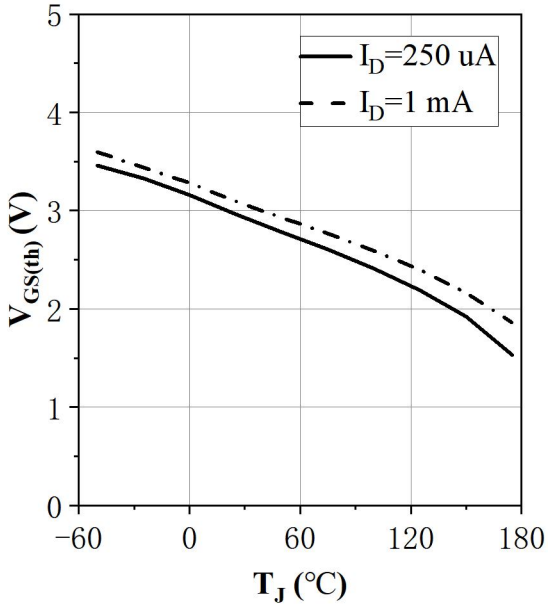


Fig 7. Gate Threshold Variation vs. Junction Temperature

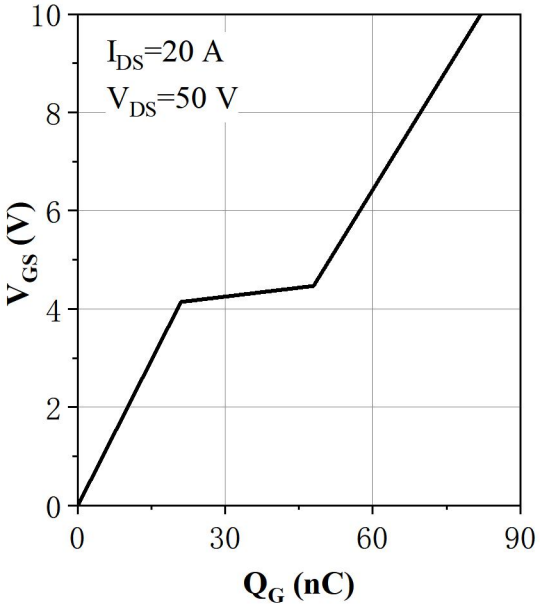


Fig 8. Gate Charge Characteristics

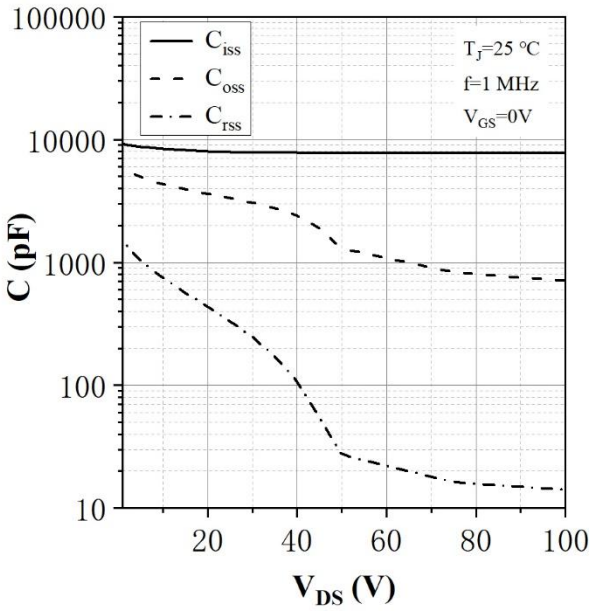


Fig 9. Capacitance Characteristics

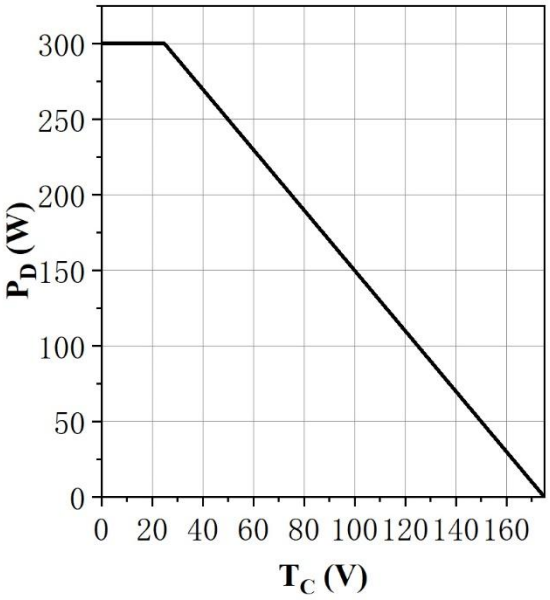


Fig 10. Power Derating

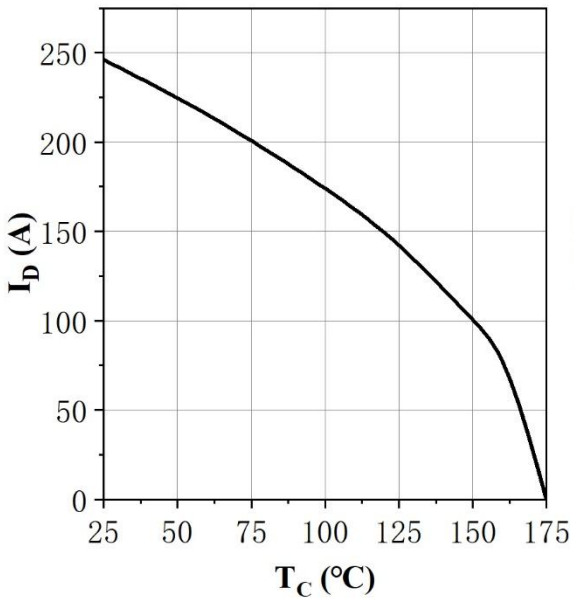


Fig 11. Current Derating

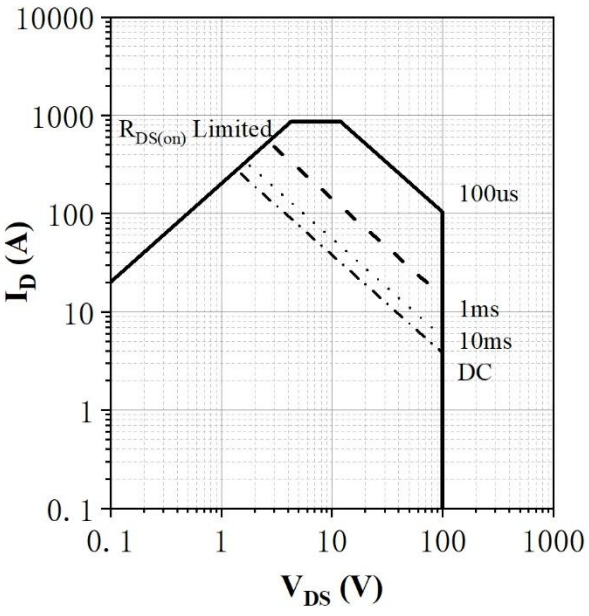


Fig 12. Safe Operating Area

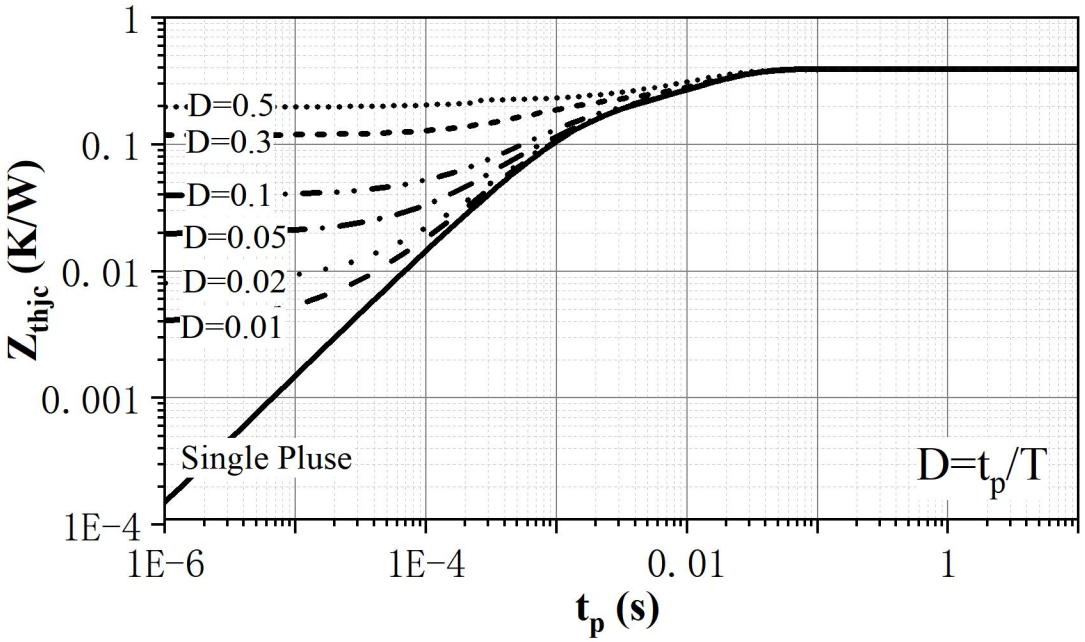
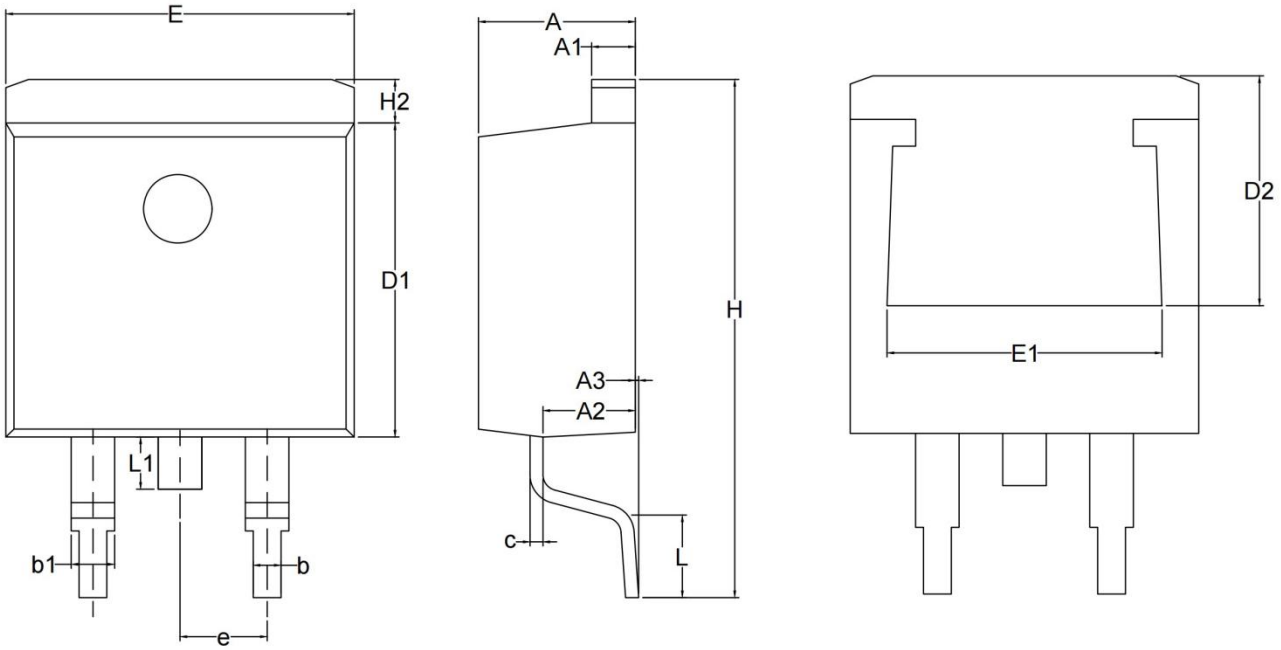


Fig 13. Normalized Maxinum Transient Thermal Impedance

Package Dimensions



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.37	4.57	4.77
A1	1.22	1.27	1.42
A2	2.49	2.69	2.89
A3	0.00	0.13	0.25
b	0.70	0.81	0.96
b1	1.17	1.27	1.47
c	0.30	0.38	0.53
D1	8.50	8.70	8.90
D2	6.60	--	--
E	9.86	10.16	10.36
E1	7.06	--	--
e	2.54 BSC		
H	14.70	15.10	15.50
H2	1.07	1.27	1.47
L	2.00	2.30	2.60
L1	1.40	1.55	1.70

Notes:

1. Refer to JEDEC TO-263 variation AB
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.

Revision History

Document revision	Date	Description of changes
1.0	2025.6.25	Target datasheet

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