SOLUTION BRIEF

Arm Neoverse Platform Optimization with Chronos Digital SerDes

CHRONOS

ARM IP

+ Neoverse

OVERVIEW & GOAL

The demand of datacenter workloads and internet traffic are growing exponentially with new applications such as generative AI or 6th generation mobile infrastructure pushing PPA limits on silicon systems and requiring new custom solutions to keep up with these challenging design constraints.

The traditional one-size-fits-all approach to computing is not the answer. The industry requires dynamic and adaptable processing to efficiently satisfy the variety of workloads and applications being run today.

Arm Neoverse addresses infrastructure needs today and into the future by providing the flexibility to implement cores that fit performance, power,

APPLICATION AREA

- 5G
- Artificial Intelligence
- Connectivity
- Server and Infrastructure

and cost requirements while delivering maximum efficiency. Specialized cores match individual workloads, a hierarchical comprehensive fabric supports data traffic, and scalable vector extensions are sized for AI.

Chronos Digital SerDes follows the same custom-tuneable philosophy and allows further optimization within the Arm Neoverse platform ecosystem.

CHALLENGE

ML algorithms require significant memory access, with reduced data reuse, as they are typically implemented as neural networks, with millions (sometimes billions) of parameters stored in memory and used during matrices computation.

To satisfy this need, latest computing SoCs keep growing in size to fit more cores and more memory, reaching or sometimes exceeding the reticle limit. This means more data travelling long distance across the die between memory controllers and processing units, escalating the need for a new generation of low-latency and high-throughput links that are also PVT insensitive. This allows for long distance data transport with minimal footprint.

This challenge is not new to the industry. A few decades ago, system engineers faced the very same issue, trying to efficiently connect different silicon chips within the same or across different boards. Their solution led to the development of many custom mixed-signal SerDes.

SOLUTION AND BENEFITS

Chronos Digital SerDes enables the automated deployment of high-throughput efficient on-chip connectivity with best-in-class latency, low power, and small bus-width footprint without any analog signalling or DLL/PLL requirements.

Chronos Digital SerDes is a tuneable soft IP, and is fully compatible with AMBA interconnect technology (CHI, AXI, ACE, etc.). It directly integrates within the Arm Neoverse platform and is used to connect high-performing latency sensitive links (such as the one between memory controllers and computing units) to eliminate register slicing and remove system bottleneck. It can also be used to minimize routing congestion in medium to lower-speed links (i.e. AXI links connecting controls and peripherals) to recover precious die area.

The Arm Neoverse platform, with standard AMBA interfaces, and integrated software environment allowed us to quickly develop a best-in-class networking solution as a reference design for a key customer, enabling short design cycle and easy integration at system level.

FURTHER RESOURCES

– chronostech.com