WHITE PAPER

Chronos Design- Innovation without Retraining

By M. T. Moreira, Chronos Tech

Introduction:

Integrated circuits (ICs) are widely spread in contemporary consumer products and are now ubiquitous and part of our daily lives. Initially, these circuits were all full-custom, and were meticulously handcrafted, component by component. However, as silicon technologies evolved, integration levels soared from thousands to billions of devices in a single chip. This was the beginning of the Very Large Scale Integration (VLSI) era. Figure 1 shows how transistor count grew over the last decades.

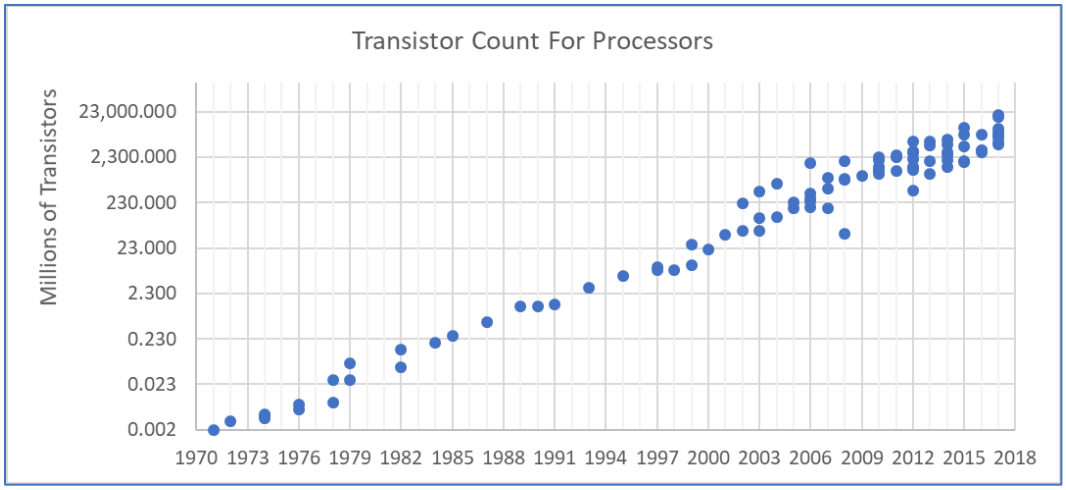

Figure 1 – Transistor count for processors against dates of introduction. Data counts with products from different vendors, including Apple, AMD, IBM, Intel, Motorola and Qualcomm.

With such evolution, full-custom design proved to be an unsustainable paradigm and semi-custom design methodologies took over. Moreover, as complexity grew, and new business opportunities were created, the semiconductor market was segmented in foundries, custom IC design houses, intellectual property (IP) providers, electronic design automation (EDA) tool vendors, etc.

This new ecosystem required the development of standard models and design flows that allowed designers to more easily deliver foundry compatible masks for specific applications. As a result, hardware description languages (HDLs) and the standard-cell design methodology were created and quickly spread among VLSI designers.

Using HDLs, designers can specify the behavior of an integrated circuit in a precise and technology independent manner, allowing the reuse of code and speeding up design time by decoupling design specification from implementation. Complementary, standard-cell methodologies allowed the automated mapping of these specifications into pre-designed and pre-verified IP blocks at the gate level by using EDA tools for synthesis, place and route, timing and power analysis and sign-off, to name a few. Figure 2 shows a generic VLSI design flow following such model. Note that each stage here can be divided into several substages, depending on the design, technology or management preferences.

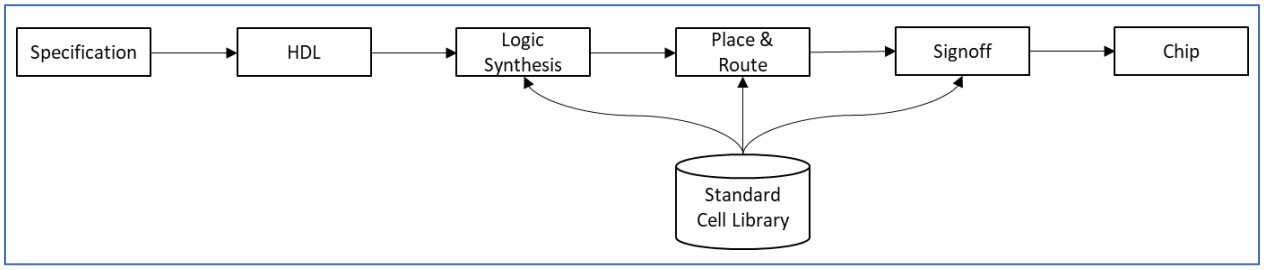

Figure 2 – Generic VLSI design flow.

This allowed substantial improvements in implementation time, from frontend to backend and is one of the reasons why semi-custom cell-based design is often cited as one of the key components in the success of the semiconductor industry.

Chronos solution:

Chronos technology targets IP integration in modern VLSI designs and was methodically planned to be compatible with industry standard methodologies, libraries, tools and flows. Our frontend environment decouples the specification of Chronos blocks and the target technology, allowing the designer to explore the design space of the application using Chronos Xplorer, our proprietary GUI. This way, one can access the trade offs between the different optimization areas enabled by Chronos technology.

The deployment of Chronos in a target technology starts with an automated process called “Chronification”, which generates an IP wrapper using standard HDL that can be seamlessly integrated in a VLSI design. Through this process, along with the HDL, several models are created for defining timing constraints, formal verification, functional and delay annotated simulation and performing optimizations during implementation.

For synthesis and place and route, Chronos technology relies on a standard-cell library that matches with traditional models for modeling electric characteristics and physical views. For timing analysis, which is a crucial step during these tasks, the technology employs a flop-based flow that enables standard static timing analysis (STA) tools to collect performance metrics of the circuit in the target technology. By doing so, designers can analyze and optimize Chronos blocks using standard implementation frameworks available from different vendors.

For example, Figure 3 shows a perspective of how Chronos technology can be used in a generic VLSI flow. Therefore, there is no need for interfering on established and proven design flows and methodologies or retraining teams of engineers.

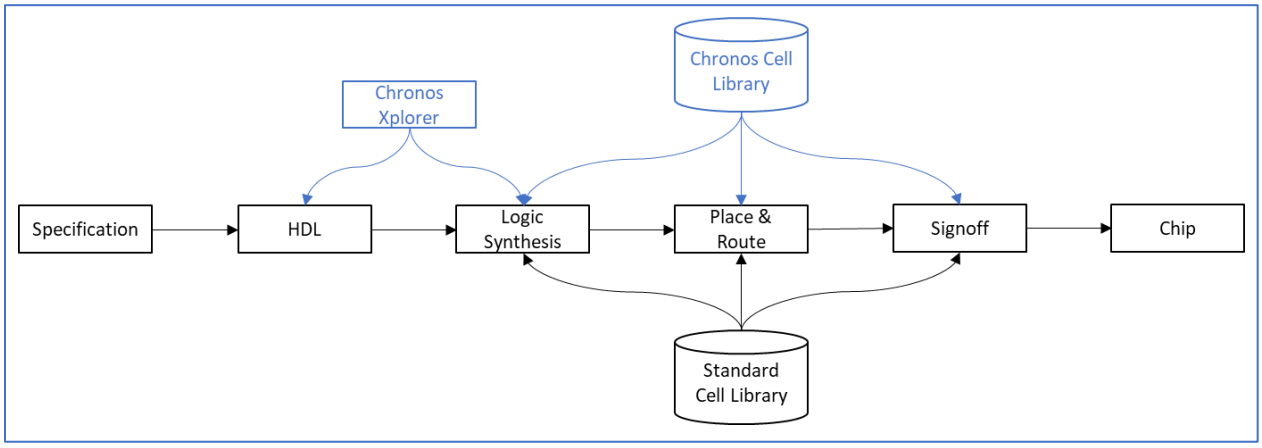

Figure 3 – Chronos technology in a generic VLSI design flow.

Finally, the foundations of our technology rely upon traditional methodologies that are industry proven and on formal methods that are scientifically proven. Our unique characteristics allow this disruptive technology to be integrated in modern VLSI circuits without jeopardizing traditional methodologies and inferring risks to design activities.