WHITE PAPER

Chronos Routability- Reducing Interconnect Overheads

By M. Pryor, Chronos Tech

Introduction:

Examining the scale of integration in modern System-on-Chip (SoC) designs highlights the importance of efficiently connecting IP's. The impact of sub-optimal implementation will increase design costs thru inflated design time and die area. Fundamental to the many physical tradeoffs a design team will consider during the floorplanning stage, is how many connections exist on an IP, and how far their counterparts reside. This is a primary factor in how much area overhead must be accommodated to route these data busses; either placed in channels that frame each IP, or routed through an adjacent block with density concessions. The expense has been accepted as the necessary result of ambitious integration, with little that can be done practically to alleviate its cost. Chronos technology creates new options to compress these data busses, route them in fewer wires, and optimize the value of each design.

Routing Interconnects:

The digital core of an IC is most efficiently used when densely packed with circuits such as standard cell logic and memory. To ease the effort to constrain and complete portions of the design in parallel, modularity is inserted with physical design partitioning. The result is many digital blocks within the chip, each packed with logic as tightly as possible while still able to route and close timing. But how about the portions of interconnect between blocks? Are they taking up more area than needed, or disturbing other critical design elements?

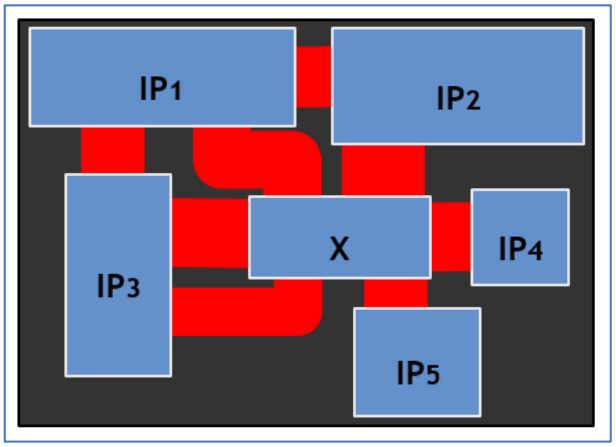

Figure 1: Hierarchical SoC floorplan

Often these channels remain sparsely populated with cells, under-utilized regions with buffering and pipelining. To mask these unsightly areas where silicon is left on the table, abutted IP design becomes attractive, but brings along its own drawbacks in lower IP utilization and delayed hierarchical closure. With either technique, the top-level interconnect is typically more constrained by routing demands than standard cell utilization. The repeater and register slice area are significant, but often pale in comparison to the area of thousands of nets that must cross the die from IP to IP. In addition, the pipeline flops burden the design with an impact to clock tree distribution with strict route isolation requirements.

To compound this floorplanning challenge, recent trends in fabrication technology have seen the decrease in transistor area outpace the reduction in signal routing width and spacing requirements. The semiconductor industry has been unable to find methods to pack wires together as tightly as needed to match transistor scaling, resulting in routing as a critical limitation to die utilization, especially in top level channels. Very few practical solutions exist to overcome this dilemma in the synchronous domain.

Chronos Solution:

Chronos technology presents a unique solution to minimize this overhead, enabled by delay insensitive channels and clockless temporal compression. By converting protocol to the asynchronous domain, data can be made to communicate robustly through fewer wires enabling channel widths to be reduced. In many cases this compression can exceed 50%. Another enormous benefit in a Chronos channel comes from removing the clock from the pipeline. When the clock net is removed, so are the related challenging and costly wide spacing rules and distribution requirements. This can greatly simplify timing closure of the IP by minimizing fanout and insertion delay of the clock network, and removing sensitive clock ECOs likely needed in pipeline networks.

Figure 2: Minimize the impact of cross-die data bussing

The internal speed of an IP no longer must dictate the speed of its data bus pipeline. Often there is much room to give within a technology to accelerate signals across a die, and Chronos takes advantage of that to reduce routing overhead, ease closure, and minimize die area.