WHITE PAPER

Chronos Verification – Asynchronous Verification Demystified

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Introduction:

Verification of IP is a critical undertaking in System on Chip (SoC) design. The focus must be kept on ensuring with high confidence that the RTL and resulting logic gates in silicon will function as expected, without system hang or other serious anomalies. Underestimating this task can lead to significant or even fatal silicon issues. Thus, it is of the utmost importance that pre-silicon and post-silicon verification tools, with their coverage metrics and FPGA validation, verify as much functional behavior as possible with software interactions.

Functionality:

There are several industry standard methods to verify functionality: Assertion-based Verification (ABV) and FPGA validation. ABV is a methodology in which design and verification engineers use assertions to capture specific design intent and, either through simulation, formal verification, or emulation of these assertions, verify that the design correctly implements that intent.

For digital simulation there are several verification metrics to determine quality of tests and correct functional behavior: code coverage (using block or line coverage and toggle coverage for structural RTL), functional coverage (using cover-groups for data coverage and assertions for mostly control related functionality).

Formal Verification

An industry standard Logic Equivalency Checker (LEC) is used to formally verify the source code RTL and the synthesized gates. A comparison of a reference design RTL against one with Chronos gasket around each IP showed zero non-equivalencies, formally proving the two circuit representations have the same behavior.

Digital Simulation

For digital simulation, verification tools such as Cadence Incisive are used, with Incisive Metric Center for reporting detailed metrics of the simulation outputs. The digital simulation setup consists of a testbench with a randomized data input pattern, and parameter setting for compression ratio. Industry standard assertions, such as the Verification IP (VIP) from ARM is used: ARM AXI Protocol Checker. See Figure 1 below that illustrates a testbench used to verify a Chronos Link.

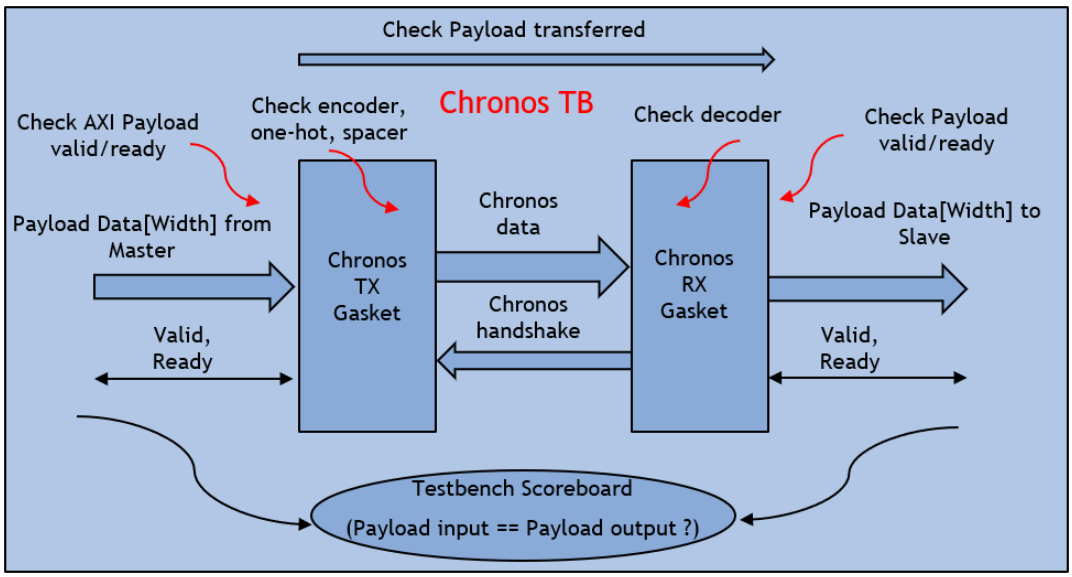

Figure 1: Testbench to Verify Chronos Link

Assertions

To ensure correctness of the Chronos IP, various assertions were inserted in the control and data-paths of the AXI payload. Assertions were added to check handshake with payload from AXI Payload to Chronos IP link and from Chronos IP to AXI slave. The ARM AXI Protocol Checker is also instantiated at the AXI boundary to ensure proper functionality. In addition, assertions are instantiated to check data integrity from Chronos IP link input to Chronos IP link output. Lastly, assertions are built into the Chronos IP library to check data encoding and data decoding as well as data patterns like one hot and spacer symbol. Quality of verification are reported by coverage reports such as below: Figure 2 Incisive functional simulation report, Figure 3 Covergroup (to check one-hot coverage), Toggle Coverage (to check structural RTL input/output changes) and Functional Coverage Report (assertions to check encode/decode and one-hot).

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        0    389      0    super_tb_chr_r_bits_link.chr_link.tx_gen.CHR_GEN.CHR_R.tx_ch.chr_r_tx16[0].tx_16b.tx2.tx2.tx2.hb1.protocol_assertion_out.data_pins[3].data_sent
        0    389      0    super_tb_chr_r_bits_link.chr_link.tx_gen.CHR_GEN.CHR_R.tx_ch.chr_r_tx16[0].tx_16b.tx2.tx2.tx2.hb1.protocol_assertion_out.data_pins[3].spacer_sent
        0      1      0    super_tb_chr_r_bits_link.chr_link.tx_gen.CHR_GEN.CHR_R.tx_ch.chr_r_tx16[0].tx_16b.tx2.tx2.tx2.hb1.protocol_assertion_out.reset_condition
        0   1534      0    super_tb_chr_r_bits_link.chr_link.tx_gen.CHR_GEN.CHR_R.tx_ch.chr_r_tx16[0].tx_16b.tx2.tx2.tx2.hb1.protocol_assertion_out.spacer_ack
        0   1326      0    super_tb_chr_r_bits_link.verif.axi4_errm_data_in_stable
        0   1528      0    super_tb_chr_r_bits_link.verif.axi_payload_dldr
Total Assertions = 1622,  Failing Assertions = 0,  Unchecked Assertions = 0
Assertion summary at time 21947500 PS + 0
```

Figure 2 Incisive Functional Simulation Report

Overall Instance-Based Coverage

CoverGroup Average	CoverGroup Covered	name
100.00%	100.00% (8/8)	Instance Coverage

Overall Instance-Based Coverage

Toggle Average	Toggle Covered	Functional Average	Functional Covered
100.00%	100.00% (1012/1012/196)	100.00%	100.00% (330/330)

Figure 3 Covergroup Coverage, Toggle Coverage and Functional Coverage Report

FPGA Validation

Functional verification on hardware can be achieved using an FPGA, where the system is setup to remap certain specialized logic into an equivalent logic function using LUTs. Because of that, only functionality is verified with this method, and not the whole sets of benefit that come with Chronos technology such as routability improvements, area, power, etc.…

An SoC based on the widely available RISC-V CPU has been created and used as the foundation for the verification of the technology. The SoC is comprised of multiples IPs (Ethernet, GPIOs, RAMs, ROM, UART, X-bar, etc.) and uses AMBA-AXI as the main fabric.

Two independent FPGA bitstream have been generated: one with the original SoC and the second one with Chronos Technology applied to each interface. The same software has been used to validate the functionality over days of operations on both bitstreams.

DFT

To ensure post-silicon functionality, Design-For-Test (DFT) can be performed on the SoC die and package using an Automated Test Equipment (ATE) machine. The regular flip-flops in the Chronos IP and other logic are converted into scannable flip-flops. Clock gated flip-flops have clocks enabled during test mode. These techniques are necessary to ensure "controllability" of the logic on the SoC. The DFT controller in an SoC chip will control shifting optimized data patterns into the scan-chain flip-flops and then switch to normal functional mode to force fabricated nets in the SoC to toggle to 0 or to 1. It will then shift out the captured values in the flip-flops and multiplex various internal nets out of the SoC to ensure "observability".

Performance/Integrity Validation

One of the major limiting factors in the deployment of asynchronous technology in general has always been related to testability and performance measurement. Chronos Technology solves both the above problems with AccuGauge technology.

AccuGauge allows accurate silicon real-time performance measurement on a link-by-link basis utilizing Built-In-Self-Test logic structure for the Chronos link. This revolutionary new technology can be used for example to screen parts during wafer die test, to assess performance during electrical validation or during the natural aging of the chip and guarantee acceptable margin or, it can be used to make speed & power trade-off for DVFS optimizations. Additionally, stuck-at can also be revealed by the AccuGauge results.

The knowledge of the real time available margin for each link, makes this technology well suited to modern SoC where trade-off must be used to maximize the user experience.

Summary:

In summary, all aspects of verification are ensured by ABV methodology with functional assertions, VIP and local testbench runs with coverage reports and validated in FPGA. DFT can be performed to ensure high quality post-silicon. Furthermore, AccuGauge Technology allows one to exploit new and advance usage model to take full advantage of each unique silicon die.

