VLSI IMPLEMENTATIONS WITH INDUSTRY ORIENTATION AND RESEARCH FOCUSED IEEE ACADEMIC PROJECTS FOR

M.TECH STUDENTS

M.TECH PROJECT LIST

2019-20
2019 IEEE Projects

1. Advanced AES Algorithm Using Dynamic Key in the Internet of Things System
2. Lightweight Cryptography for Internet of Insecure Things.
3. AES Security Improvement using Hybrid Approach for S-box design
4. A Hardware Implementation of SHA3 Hash Processor using Cortex-M0
5. Encryption Algorithm Based on Neural Network
6. Performance Comparison between AES256-Blowfish and Blowfish-AES256 Combinations.
8. VLSI Architecture for Energy Detection Based Spectrum Sensing
9. FPGA Based Implementation of FIR Filter for FOFDM Waveform.
10. Design of Logically Obfuscated n-bit ALU for Enhanced Security
11. Design and Execution of Enhanced Carry Increment Adder using Han-Carlson and Kogge Stone adder Technique
12. Double fault tolerance full adder design using fault localization.
14. Design and Analysis of Majority Logic Based Approximate Adders and Multiplier.
15. Area Efficient architecture for high speed wide data adders in Xilinx FPGAs
17. Performance Analysis of Wallace Tree Multiplier with Kogge stone adder using 15:4 Compressors.
18. Modified Binary Multiplier Circuit based on Vedic Mathematics
19. Fast and Energy Efficient binary to BCD converter with complement based logic design for BCD multipliers

20. Design and Simulation of 4 Bit QCA BCD Full Adder.

21. Design and Analysis of Majority Logic Based Approximate Adders and Multiplier.

22. Area efficient architecture for high speed wide data adders in Xilinx FPGAs.


2018 IEEE Projects


25. A New High Throughput and Area Efficient SHA-3 Implementation


27. Flexible Architecture of Memory BISTs.

28. AES block cipher implementations with AMBA-AHB interface

29. Double MAC on a DSP: Boosting the Performance of Convolutional Neural Networks on FPGAs


31. Efficient Shift-Add implementation of FIR Filters using variable partition hybrid form structures.

32. FIR filters design based on FPGA.

34. New Majority Gate Based Parallel BCD Adder Designs for Quantum-dot Cellular Automata.

35. Design and Analysis of Approximate Redundant Binary Multipliers.

36. Towards Efficient Modular Adders based on Reversible Circuits.

37. A review paper on different multipliers based on their different performance parameters.

38. Reducing the Hardware Complexity of a Parallel Prefix Adder.

39. A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier Design.


41. Comparison of Various Adders and their VLSI Implementation.

42. Research and implementation of hardware algorithms for multiplying binary numbers.

2017 IEEE Projects

43. Implementation of AES algorithm using Verilog.

44. High Performance Vedic Approach for data security using elliptic curve cryptography on FPGA.

45. Efficient FPGA Implementation of the SHA-3 Hash Function

46. Design of Reconfigurable LFSR for VLSI IC Testing in ASIC and FPGA.

47. Exploiting Addition Schemes for the Improvement of Optimized Radix-2 and Radix-4 FFT Butterflies.

48. A SAD architecture for Variable Block size motion estimation in H.264 Video Coding.

49. Novel High speed Vedic Multiplier proposal incorporating Adder based on Quaternary Signed Digit number system.
50. Analysis of Vedic Multiplier using Various Adder Topologies.

51. Low-Latency, Low-Area, and Scalable Systolic-Like Modular Multipliers for G F(2^m) Based on Irreducible All-One Polynomials.

52. Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers

53. Fast Binary Counters based on symmetric stacking.

54. Design and Implementation of High Speed Modified Booth Multiplier using Hybrid Adder.

2016 IEEE Projects

55. Development of an Improved Power-Throughput Blowfish Algorithm on FPGA

56. Low Power and Pipelined Secure hashing Algorithm3(SHA-3)

57. Low Power BIST based Multiplier Design and Simulation using FPGA.

58. Various Arbitration Algorithm for On-Chip(AMBA) Shared Bus Multi-Processor SoC.


60. Design & Implementation of Area Efficient Low Power High Speed MAC Unit using FPGA.

61. Low-Power Split-Radix FFT Processors Using Radix-2 Butterfly Units.

62. Design and Implementation of a Power and Speed Efficient Carry Select Adder on FPGA.

63. A Novel Implementation of High Speed Modified Brent Kung Carry Select Adder.

64. Design and Implementation of Multipliers.
65. Low Power & High Performance Implementation of Multiplier Architectures.


67. Optimizing the Implementation of SEC–DAEC Codes in FPGAs.