

Overview

Axiom Connectivity Digital Return SFPs are designed for superior flexibility and adaptability. By integrating numerous technical innovations, this Digital Return SFP Series ensures prolonged support for evolving network architectures.

1. Features

- Up to 2.5Gb/s Optical Transceivers
- LC/UPC Receptacle (9/125um, SMF)
- Compliant with SFP (Small Form Factor Pluggable) MSA
- Digital Diagnostic Monitoring compliant
- Supports Serial ID functionality
- Class 1 Laser Safety products
- Single +3.3 V power supply with Hot-pluggable Interface
- ROHS compliant

2. Applications

- SONET/OC-48 : 2.488Gb/s
- CPRI LINE : 2.4576Gb/s
- Digital repeater and Base station

3. Regulatory Compliance

| Items | Standard | Performance |
|-------------------------------------|---|-------------------------------|
| Electrostatic Discharge (ESD) | IEC 61000-4-2 | Class 1 |
| Electromagnetic Interference (EMI) | FCC Part 15 Class B | Compliant with standards(FCC) |
| Electromagnetic Compatibility (EMC) | Directive 89/336/EEC | Compliant with standards(CE) |
| Laser Eye Safety | FDA 21CFR 1040.10 and 1040.11 EN (IEC) 60825-1,2 | Class I laser product. |
| RoHS | 2002/95/EC 4.1&4.2 2005/747/EC | Compliant with RoHS |

4. Absolute Maximum Ratings

| Parameters | Symbol | Ratings | Units | Conditions |
|----------------------|------------------|-----------|-------|------------|
| Storage Temperature | T _{stg} | -40 ~ +95 | °C | Ambient |
| Power Supply Voltage | V _{CC} | < +4.0 | V | - |
| Ambient Humidity | H _{op} | 5 ~ 95 | % | w/o dew |

5. Operating conditions

| Parameters | Symbol | Values | | | | Conditions |
|------------------------------|-----------------|--------|-------|--------|-------------------|--------------------|
| | | Min. | Typ. | Max. | Units | |
| Power supply voltage | V _{CC} | +3.135 | +3.30 | +3.465 | V | - |
| Power supply current | I _{CC} | - | - | 550 | mA | - |
| Power Supply Noise Rejection | PSNR | - | - | 100 | mV _{p-p} | from 100Hz to 1MHz |
| Operating Temperature | T _C | - | - | +92 | °C | with Airflow |
| | T _A | -40 | - | - | | |

6. Optical Characteristics

| Parameters | Symbol | Values | | | | Conditions | |
|--------------------------------|---|---|------|---------------------|-------|--|-------------------------|
| | | Min. | Typ. | Max. | Units | | |
| Transmitter | | | | | | | |
| Optical Transmit Power | P _{avg} | -2 | - | +7 | dBm | - | |
| Transmitter Disable(Off) Power | P _{off} | - | - | -35 | dBm | @Tx_Disable is High | |
| Peak Wavelength | λ _p | λ _c -6.5 | - | λ _c +6.5 | nm | CWDM, DFB-LD, Note 1 | |
| Side Mode Suppression Ratio | SMSR | - | - | 30 | dB | - | |
| Spectral Width | Δλ | - | - | 1 | nm | @-20 dB | |
| Extinction Ratio | ER | 7 | - | - | dB | @2.4576Gb/s, PRBS 2 ⁷ -1 | |
| Eye pattern Mask | IEEE802.3/2008 section4/Figure53.8 or FC-PI-4 | | | | | | |
| Receiver | | | | | | | |
| Optical Sensitivity | S | - | - | -26 | dBm | PRBS 2 ⁷ -1,BER1x10 ⁻¹² , Source ER:7[dB] | |
| Maximum Input Power | P _{MAX} | 2 | - | - | dBm | | |
| Operating Wavelength | λ _o | 1260 | - | 1620 | nm | - | |
| Rx_LOS (Loss of signal) | Assert | P _A | -36 | - | - | dBm | Squelch function enable |
| | De-assert | P _D | - | - | -26 | dBm | - |
| | Hysteresis | P _A -P _D | 0 | - | 5 | dB | - |
| RSSI Calibration | R _{CAL} | Internal Calibrated (The host side can be read by an external way) | | | | | |

Note 1) The transmitter center wavelength
 λ_c (1271,1291,1311,1331,1351,1411,1431,1451,1471,1491,1511,1531,1551,1571,1591,1611nm)

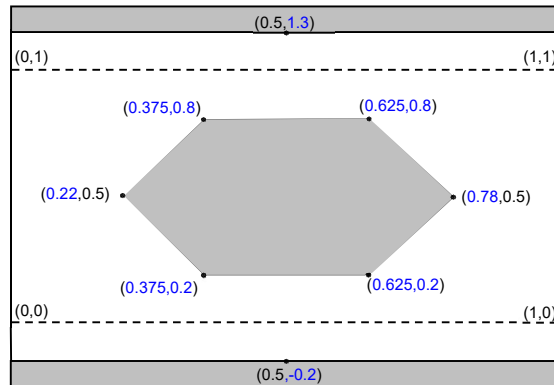


Figure 1. Mask of eye diagram for optical output (filtered)

7. Electrical Characteristics

| Parameters | | Symbol | Values | | | | Conditions |
|-------------------------------|---------------|-----------------|--------|------|--------------|-------|---|
| | | | Min. | Typ. | Max. | Units | |
| Transmitter | | | | | | | |
| Data Rate | | DR_T | - | 2.5 | - | Gb/s | - |
| Differential Input Voltage | | V_{INpp} | 150 | - | 1000 | mV | - |
| Differential Input Impedance | | Z_{IN} | 75 | 100 | 125 | ohm | - |
| Tx_Disable | Input_Low | V_{IL} | 0 | - | 0.8 | V | LVTTL, Normal at Low, High is Shutdown(P_{off}) |
| | Input_High | V_{IH} | 2.0 | - | $V_{cc}+0.3$ | V | |
| | Assert Time | t_{OFF} | - | - | 10 | us | High |
| | Negate Time | t_{ON} | - | - | 1 | ms | Low |
| Tx fault reset | | t_{reset} | 10 | - | - | us | High |
| Time to Initialize | | t_{start_up} | - | - | 300 | ms | - |
| Tx_Fault | Output_Low | V_{FOL} | 0 | - | 0.4 | V | LVTTL, Low is Normal |
| | Output_High | V_{FOH} | 2.0 | - | V_{cc} | V | |
| Receiver | | | | | | | |
| Data Rate | | DR_R | - | 2.5 | - | Gb/s | - |
| Differential Output Voltage | | V_{out} | 370 | - | 1005 | mV | - |
| Differential Output Impedance | | Z_{out} | 90 | 100 | 110 | ohm | - |
| Rx_LOS (Loss of signal) | Output_Low | V_{LOSL} | 0 | - | 0.8 | V | LVTTL, Low is normal |
| | Output_High | V_{LOSH} | 2.0 | - | V_{cc} | V | |
| | Assert time | t_{LOS-ON} | - | - | 100 | us | Low >> High |
| | Deassert time | $t_{LOS-OFF}$ | - | - | 100 | us | High >> Low |
| RS(Rate Select) | | V_{IL} | 0 | - | 0.8 | V | Not used |
| | | V_{IH} | 2.0 | - | $V_{cc}+0.3$ | V | |

8. Recommended Circuit Schematic

- Tx_Disable : Transmitter Disable, logic high, 4.7k to 10kohm pull up to Vcc on SFP
- Tx_Fault : Transmitter Fault, logic high, 4.7k to 10kohm pull up to Vcc on Host
- Rx_LOS : Receiver Loss of Signal, logic high, 4.7k to 10kohm pull up to Vcc on Host

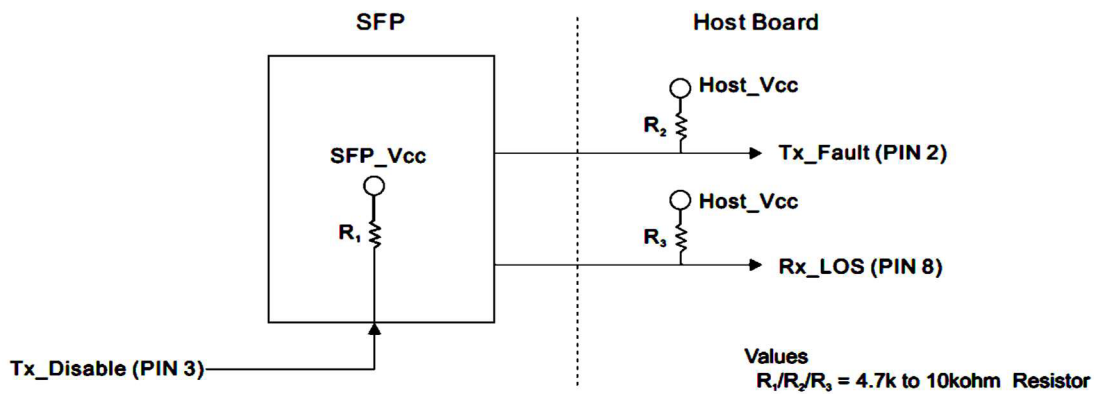


Figure 2 . Signal Definitions

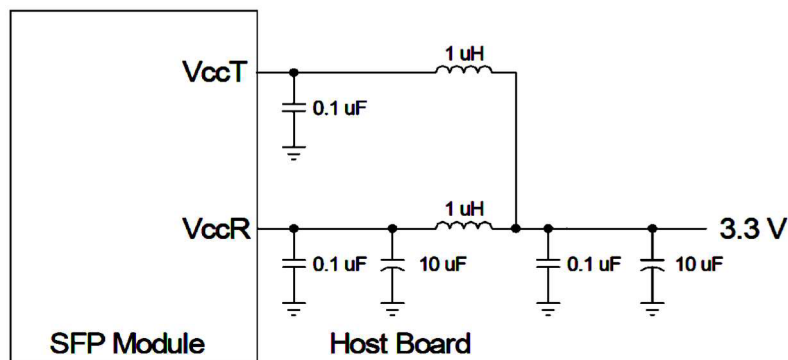


Figure 3 . Power Coupling

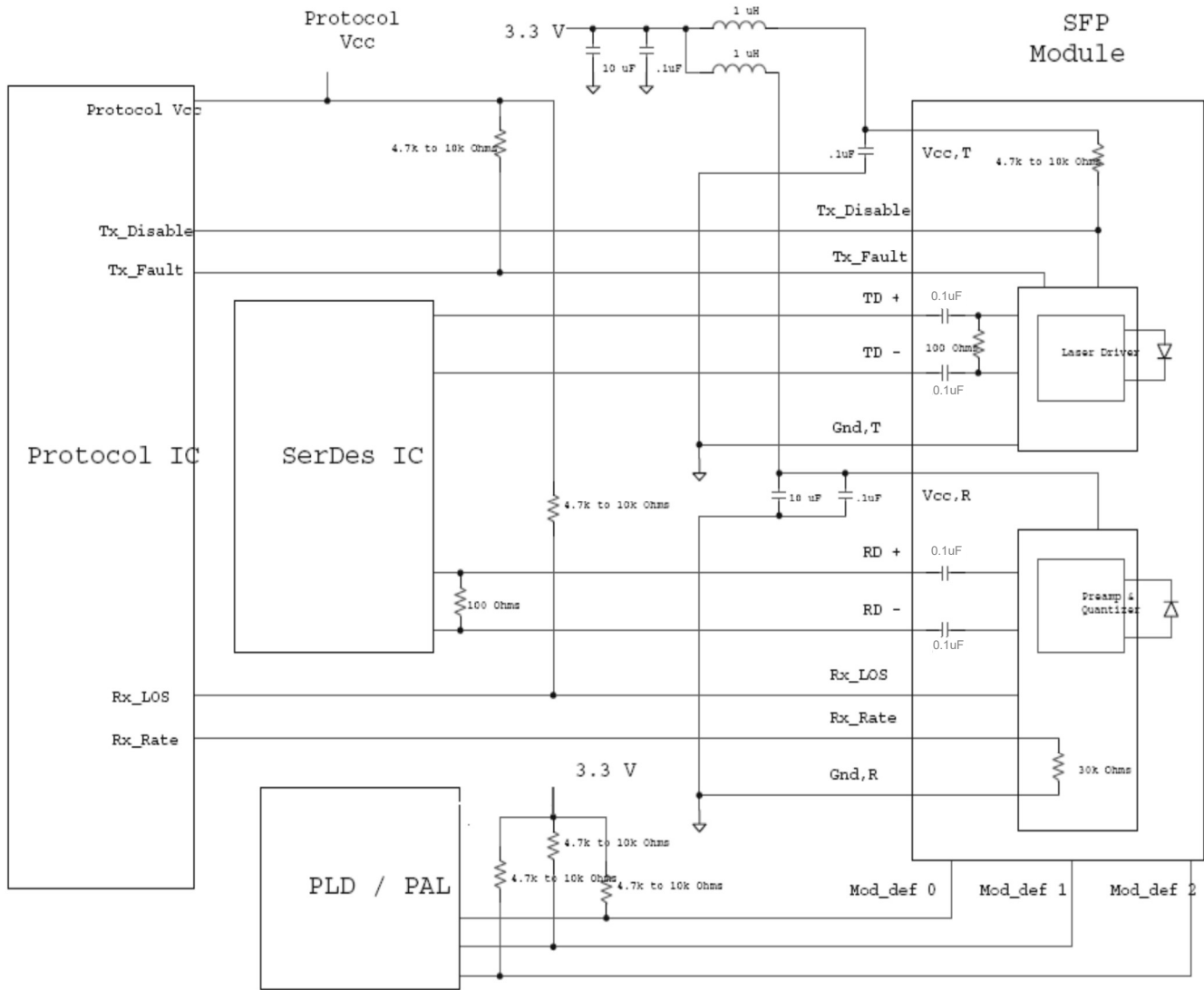


Figure 4 . Example SFP Host Board Schematic

9. Pin Information

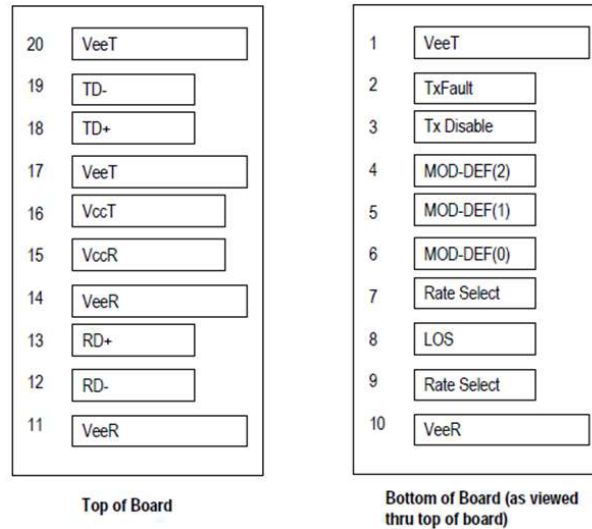


Figure 5 . 20-pin Connector

| Pin No. | Symbol | Descriptions | Sequence |
|---------|--------------|---|----------|
| Pin 1 | TGND(VeeT) | Ground | 1 |
| Pin 2 | Tx_Fault | Status Out | 3 |
| Pin 3 | Tx_Disable | Control In | 3 |
| Pin 4 | MOD_DEF(2) | Input/Output(SDA, I ² C data) | 3 |
| Pin 5 | MOD_DEF(1) | Input/Output(SCL, I ² C clock) | 3 |
| Pin 6 | MOD_DEF(0) | Indicates that the module is present, Grounded internally | 3 |
| Pin 7 | Rate Select1 | Rate Select In, Not used(Internally pull-down) | 3 |
| Pin 8 | RX_LOS | Status Out | 3 |
| Pin 9 | Rate Select2 | Rate Select In, Not used(Internally pull-down) | 3 |
| Pin10 | RGND(VeeR) | Ground | 1 |
| Pin 11 | RGND(VeeR) | Ground | 1 |
| Pin 12 | Rx_Data bar | Data Out Negative | 3 |
| Pin 13 | Rx_Data | Data Out Positive | 3 |
| Pin 14 | RGND(VeeR) | Ground | 1 |
| Pin 15 | Rx_Vcc(VccR) | Power | 2 |
| Pin 16 | Tx_Vcc(VccT) | Power | 2 |
| Pin 17 | TGND(VeeT) | Ground | 1 |
| Pin 18 | Tx_Data | Data In Positive | 3 |
| Pin 19 | Tx_Data bar | Data In Negative | 3 |
| Pin 20 | TGND(VeeT) | Ground | 1 |

10. 2-Wire Serial-Port Operation

The 2-wire serial-port interface supports a bi-directional data transmission protocol with device addressing. Connections to the bus are made through MOD_DEF2 and MOD_DEF1. Timing diagrams for the 2-wire serial port can be found in Figures 6. Within the bus specifications, a standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The Module works in both modes.

- **The following bus protocol has been defined:**

Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

- **Bus not busy:** Both data and clock lines remain high.
- **Start data transfer:** A change in the state of the data line from high to low while the clock is high defines a START condition.
- **Stop data transfer:** A change in the state of the data line from low to high while the clock line is high defines the STOP condition.
- **Data valid:** The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line can be changed during the low period of the clock signal. There is one clock pulse per bit of data. Figures 6 detail how data transfer is accomplished on the 2-wire bus.
- **Clock and Data Transitions:** The MOD_DEF2 pin is normally pulled high with an external resistor or device. Data on the MOD_DEF2 pin may only change during MOD_DEF1 -low time periods. Data changes during MOD_DEF1 -high periods will indicate a START or STOP condition depending on the conditions discussed below.
- **START Condition:** A high-to-low transition of MOD_DEF2 with MOD_DEF1 high is a START condition that must precede any other command. See the timing diagrams in Figures 6 for further details.
- **STOP Condition:** A low-to-high transition of MOD_DEF2 with MOD_DEF1 high is a STOP condition. After a read or write sequence, the stop command places the condition into a low-power mode.
- **Acknowledge:** All address and data bytes are transmitted through a serial protocol. The DDM Controller pulls the MOD_DEF2 line low during the ninth clock pulse to acknowledge that it has received each word.

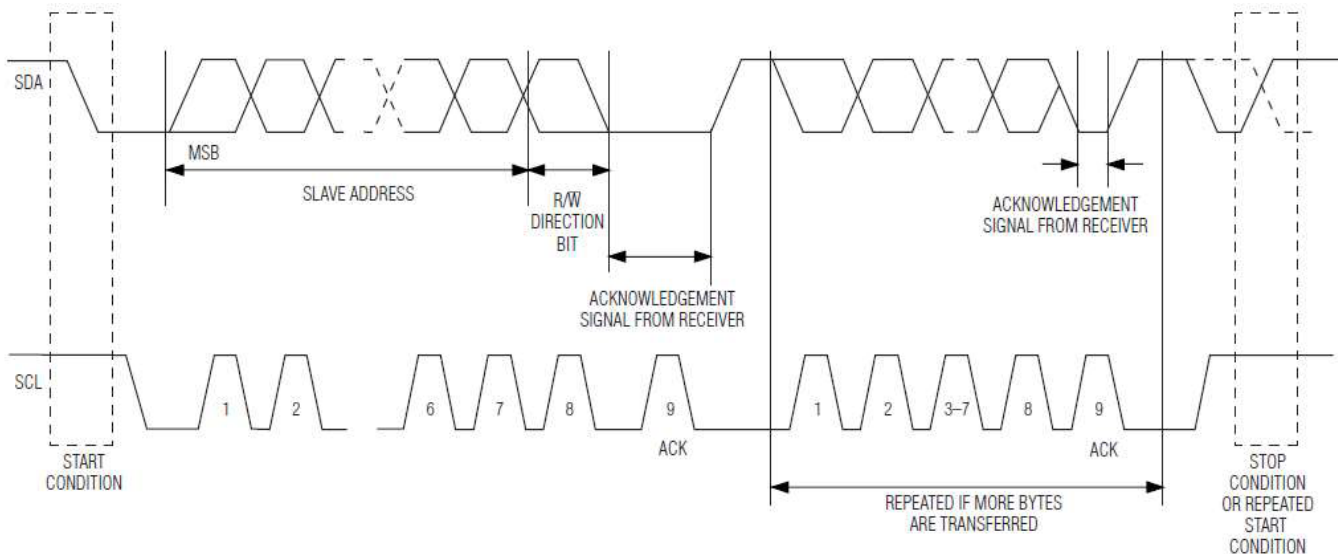


Figure 6 . 2-Wire Data Transfer Protocol

11. Package Description & Outline Diagram

* Unit: [mm]

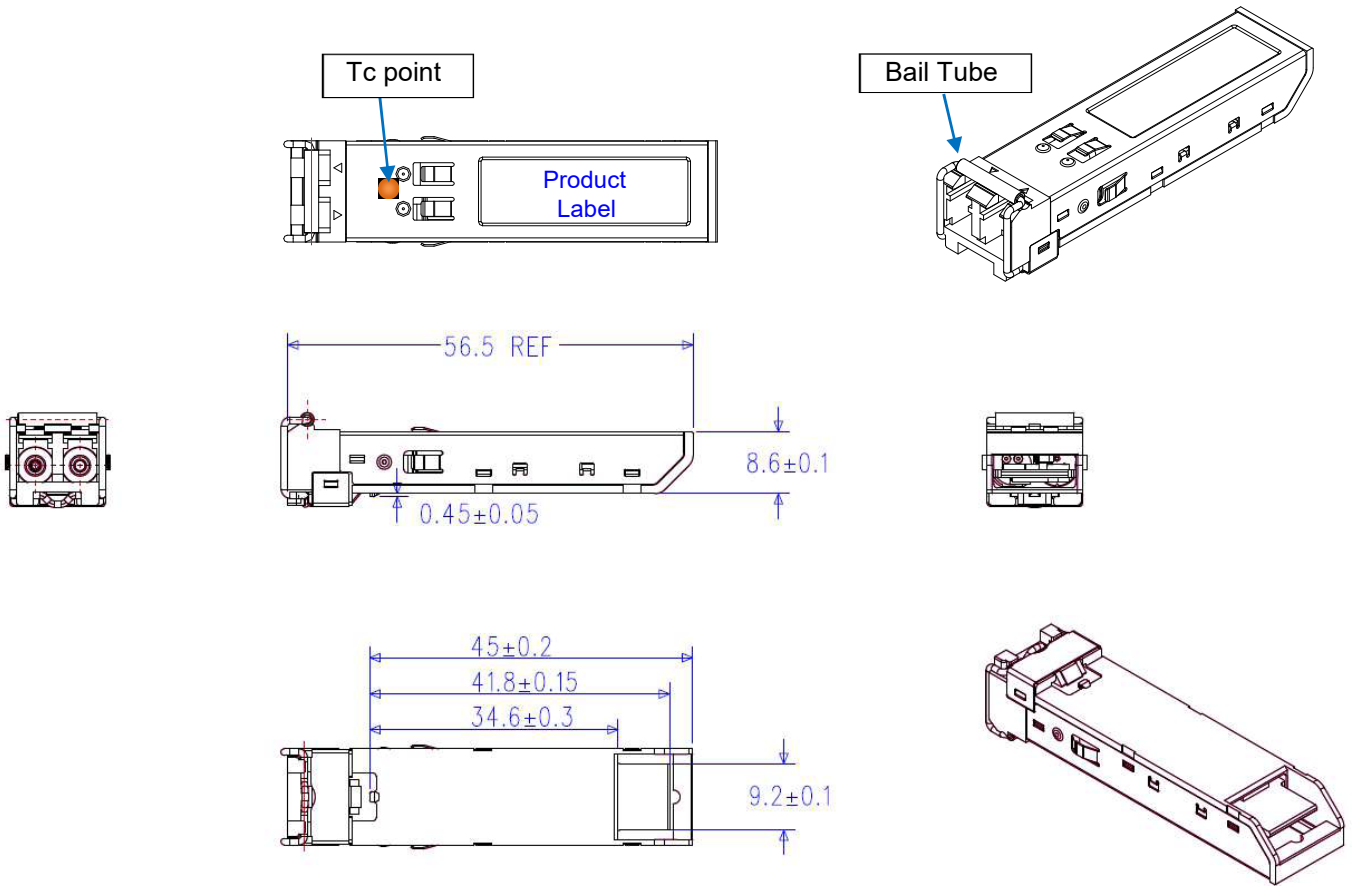


Figure 7 . Package outline diagram and example

12. Ordering Information

| Part No | Wavelength [nm] |
|---------------------|-----------------|
| AC-B-DR2TC40-U27-yy | 1271 |
| AC-B-DR2TC40-U29-yy | 1291 |
| AC-B-DR2TC40-U31-yy | 1311 |
| AC-B-DR2TC40-U33-yy | 1331 |
| AC-B-DR2TC40-U35-yy | 1351 |
| AC-B-DR2TC40-U37-yy | 1371 |
| AC-B-DR2TC40-U39-yy | 1391 |
| AC-B-DR2TC40-U41-yy | 1411 |
| AC-B-DR2TC40-U43-yy | 1431 |
| AC-B-DR2TC40-U45-yy | 1451 |
| AC-B-DR2TC40-U47-yy | 1471 |
| AC-B-DR2TC40-U49-yy | 1491 |
| AC-B-DR2TC40-U51-yy | 1511 |
| AC-B-DR2TC40-U53-yy | 1531 |
| AC-B-DR2TC40-U55-yy | 1551 |
| AC-B-DR2TC40-U57-yy | 1571 |
| AC-B-DR2TC40-U59-yy | 1591 |
| AC-B-DR2TC40-U61-yy | 1611 |