Overview

Axiom Connectivity Digital Return SFPs are designed for superior flexibility and adaptability. By integrating numerous technical innovations, this Digital Return SFP Series ensures prolonged support for evolving network architectures.

1. Features

- Up to 2.5Gb/s
- Un Cooled DFB-LD
- SFP LC/UPC Receptacle(9/125um, SMF)
- Compliant with SFP(Small Form Factor Pluggable) MSA
- Digital Diagnostic Monitoring compliant
- Supports Serial ID functionality
- Class 1 Laser Safety products
- Single +3.3 V power supply with Hot-pluggable Interface
- ROHS compliant

2. Applications

- Digital repeater and Base station
- CPRI/OBSAI Line
- Fiber Channel

3. Regulatory Compliance

Items	**Standard**	Performance
Electrostatic Discharge (ESD)	IEC 61000-4-2	Class 1
Electromagnetic Interference (EMI)	FCC Part 15 Class B	Compliant with standards(FCC)
Electromagnetic Compatibility (EMC)	Directive 89/336/EEC	Compliant with standards(CE)
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN (IEC) 60825-1,2	Class I laser product.
RoHS	Directive 2011/65/EU	Compliant with RoHS

4. Absolute Maximum Ratings

Parameters	Symbol	**Ratings**	Units	Conditions
Storage Temperature	T_{stg}	-40 ~ +85	°C	-
Power Supply Voltage	V_{CC}	< +4.0	V	-
Ambient Humidity	H_{op}	5 ~ 95	%	w/o dew

5. Operating conditions

Parameters	Symbol	Values				Conditions
		Min.	Typ.	Max.	Units	
Power supply voltage	V_{CC}	+3.135	+3.30	+3.465	V	-
Power supply current	I_{CC}	-	-	500	mA	-
Power Supply Noise Rejection	PSNR	-	-	100	mV_{p-p}	from 10Hz to 10MHz
Operating Temperature	Ta	-40				Case, with Airflow
	T_C	-	-	+85	°C	

6. Optical Characteristics

Parameters	Symbol	Values				Conditions
		Min.	Typ.	Max.	Units	
Transmitter						
Optical Transmit Power	P_f	0	-	+5.0	dBm	-
Transmitter Disable(Off) Power	P_{off}	-	-	-35	dBm	@Tx_Disable is High
Peak Wavelength	λ_p	λ_c -6.5	1491 1511	λ_c +6.5	nm	DFB -LD,
Side Mode Suppression Ratio	SMSR	30	-	-	dB	-
Spectral Width	Δλ	-	-	1.0	nm	@ -20 dB
Extinction Ratio	ER	7.0	-	-	dB	@2.5Gb/s, PRBS 2^{23} -1
Eye pattern Mask	02xGbEthernet					

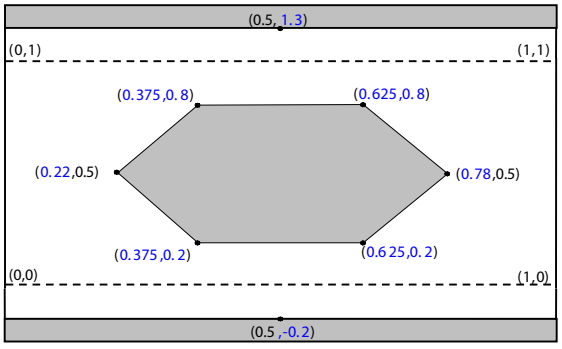

Figure 1. *Mask of eye diagram for optical output (filtered)*

7. Electrical Characteristics

Parameters		Symbol	Values				Conditions
			Min.	Typ.	Max.	Units	
Transmitter							
Data Rate		DR_T	-	2.5	-	Gb/s	
Differential Input Voltage		V_{INpp}	180	-	800	mV	-
Differential Input Impedance		Z_{IN}	90	100	110	ohm	-
Tx_Disable	Input_Low	V_{IL}	0	-	0.8	V	LVTTL,Normal at Low, High is Shutdown(P_{off})
	Input_High	V_{IH}	2.0	-	3.465	V	
	Assert Time	t_{OFF}	-	-	10	us	High
	Negate Time	t_{ON}	-	-	1	ms	Low
Tx fault reset		t_{reset}	10	-	-	Us	High
Time to Initialize		t_{start_up}	-	-	300	ms	-
Tx_Fault	Output_Low	V_{FOL}	0	-	0.8	V	LVTTL, Low is Normal
	Output_High	V_{FOH}	2.0	-	Vcc+0.3	V	

8. Recommended Circuit Schematic

- Tx_Disable : Transmitter Disable, logic high, 4.7k to 10kohm pull up to Vcc on SFP
- Tx_Fault : Transmitter Fault, logic high, 4.7k to 10kohm pull up to Vcc on Host

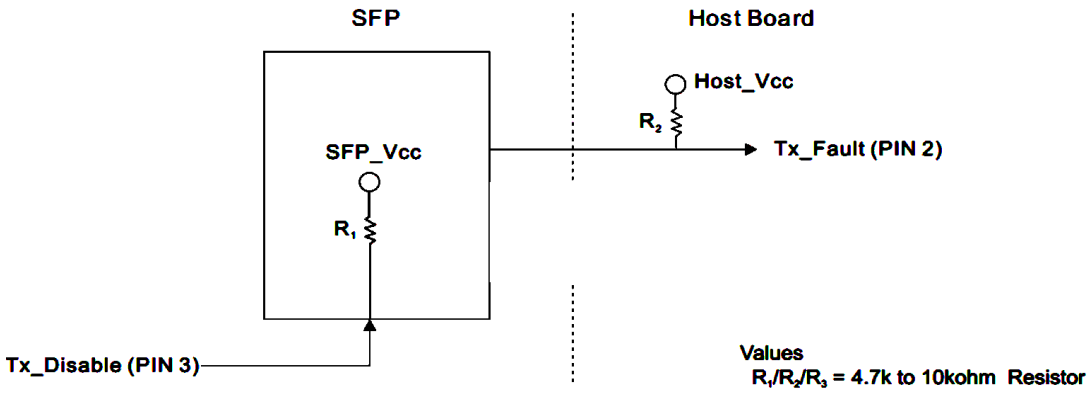

***Figure 2**. Signal Definitions*

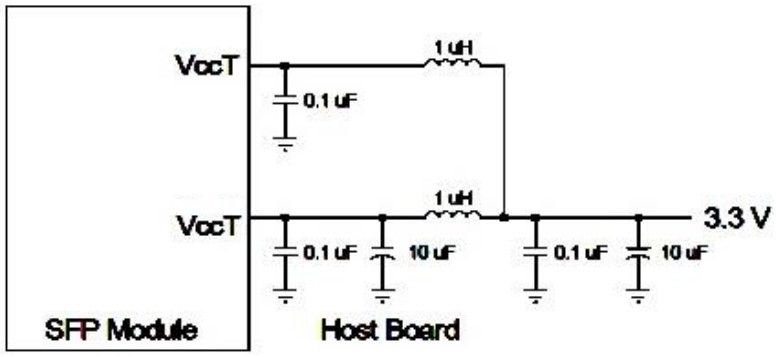

***Figure 3.** Power Coupling*

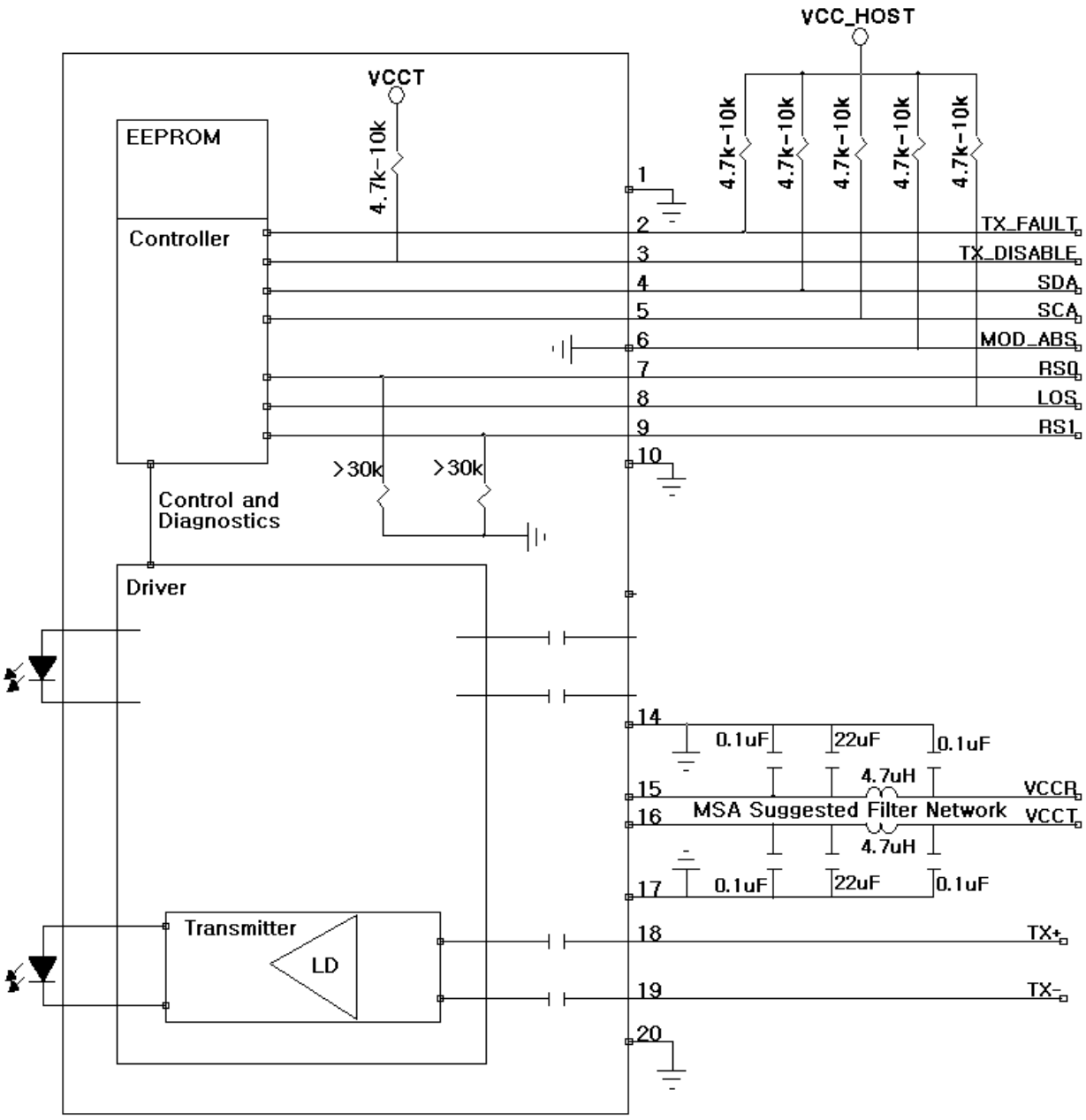

Figure 4. Example SFP Host Board Schematic

9. Pin Information

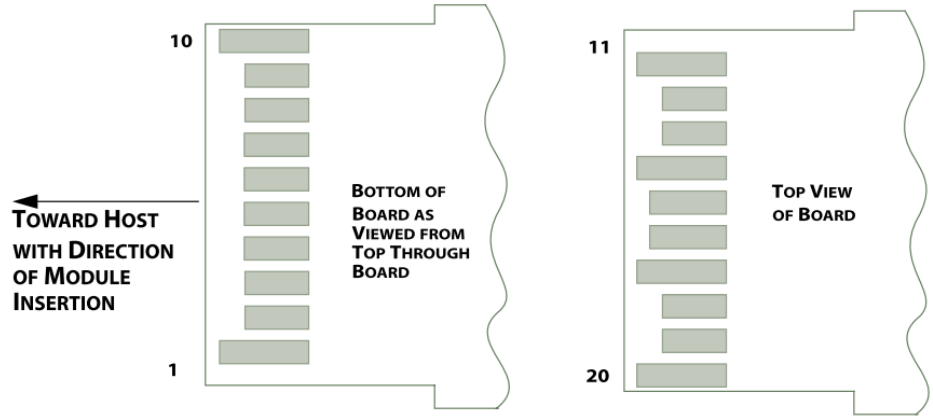

Figure 5-1. SFP+ Transceiver Electrical Pad Layout

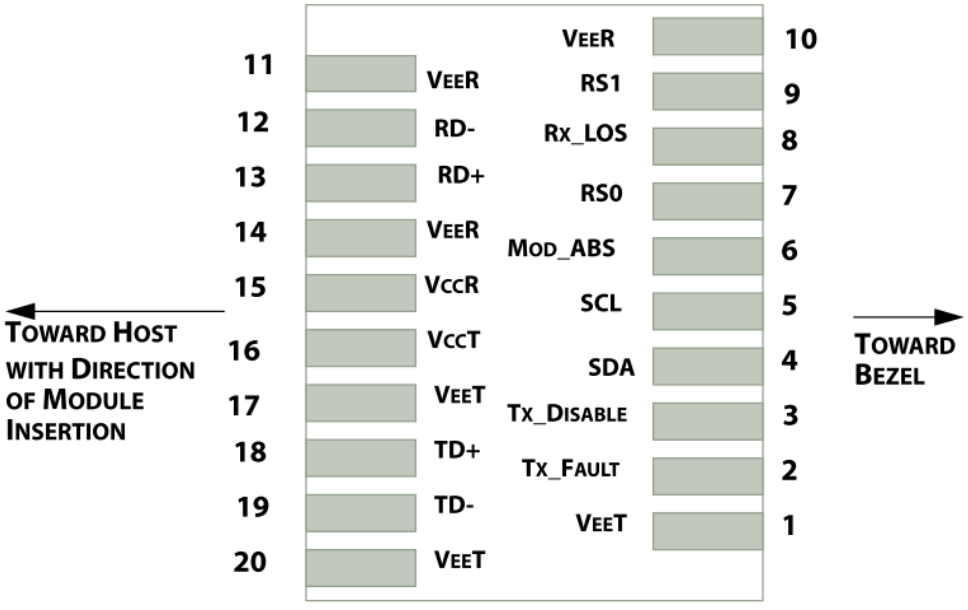

Figure 5-2. 20-pin Host PCB SFP+ pad assignment top view

Pin No.	Symbol	Descriptions	**Sequence**
Pin 1	TGND (VeeT)	Ground	1
Pin 2	Tx_Fault	Status Out	3
Pin 3	Tx_Disable	Control In	3
Pin 4	MOD_DEF(2)	Input/Output(SDA, I ^{2}C data)	3
Pin 5	MOD_DEF(1)	Input/Output(SCL, I ^{2}C clock)	3
Pin 6	MOD_DEF(0)	Indicates that the module is present , Grounded internally	3
Pin 7	Rate Select	Rate Select In, Not used (Internally N.C)	3
Pin 8	RX_LOS	Status Out	3
Pin 9	RGND (VeeR)	Ground	3
Pin10	RGND (VeeR)	Ground	1
Pin 11	RGND (VeeR)	Ground	1
Pin 12	Rx_Data bar	Data Out Negative	3
Pin 13	Rx_Data	Data Out Positive	3
Pin 14	RGND (VeeR)	Ground	1
Pin 15	Rx_Vcc (VccR)	Power	2
Pin 16	Tx_Vcc (VccT)	Power	2
Pin 17	TGND (VeeT)	Ground	1
Pin 18	Tx_Data	Data In Positive	3
Pin 19	Tx_Data bar	Data In Negative	3
Pin 20	TGND(VeeT)	Ground	1

10. 2-Wire Interface Electrical Specifications

Parameters	Symbol	Min.	**Max.**	Units	Notes
Host 2 -Wire Vcc	Vcch	3.14	3.46	V	Note 1
SCL and SDA	V_{OL}	0.0	0.8	V	R_P pulled to VccT/R, Note 2
	V_{OH}	Vcch -0.5	Vcch+0.3	V	
SCL and SDA	V_{IL}	-0.3	VccT*0.3	V	Note 3
	V_{IH}	VccT*0.7	VccT+0.5	V	
Input Current on the SCL and SDA Contacts	I_I	-10	10	µA	-
Capacitance on SCL and SDA contacts	C_i	-	14	pF	Note 4
Total bus capacitance for SCL and SDA	C_b[5]	-	100	pF	At 400kHz, 3.0k Ω Rp, max At 100kHz, 8.0k Ω Rp, max
		-	290	pF	At 400kHz, 1.1k Ω Rp, max At 100kHz, 2.75k Ω Rp, max

Notes:

1. *The Host 2-wire Vcc is the voltage used for resistive pull ups for the 2 wire interface*
2. *Rp is the pull up resistor. Active bus termination may be used by the host in place of a pull up resistor. Pull ups can be connected to any one of several power supplies, however the host board design shall ensure that no module contact has voltage exceeding module VccT/R + 0.5 V nor requires the module to sink more than 3.0mA current.*
3. *These voltages are measured on the other side of the connector to the device under test.*
4. *Ci is the capacitance looking into the module SCL and SDA contacts.0*
5. *Cb is the total bus capacitance on the SCL or SDA bus.*

11. 2-Wire Timing Specifications

Parameters	Symbol	Min.	**Max.**	Units	Notes
Clock Frequency	f_{SCL}	0	400	kHz	Note 1
Clock Pulse Width Low	t_{LOW}	1.3	-	µs	-
Clock Pulse Width High	t_{HIGH}	0.6	-	µs	-
Stop to Start Time	t_{BUF}	20	-	µs	Note 2
Start Hold Time	$t_{HD,STA}$	0.6	-	µs	-
Start Set -up Time	$t_{SU,STA}$	0.6	-	µs	-
Data In Hold Time	$t_{HD,DAT}$	0	-	µs	-
Data In Set -up Time	$t_{SU,DAT}$	0.1	-	µs	-
Input Rise Time (100kHz)	$t_{R,100}$	-	1000	ns	Note 3
Input Rise Time (400kHz)	$t_{R,400}$	-	300	ns	Note 3
Input Fall Time (100kHz)	$t_{F,100}$	-	300	ns	Note 4
Input Fall Time (400kHz)	$t_{F,400}$	-	300	ns	Note 4
Stop Set -up Time	$t_{SU,STO}$	0.6	-	µs	-
Serial Interface Clock Holdoff "Clock Stretching "	t_clock_hold	-	500	µs	Note 5

Notes:

1. *Module shall operate with f_{SCL} up to 100 kHz without requiring clock stretching. The module may clock stretch with f_{SCL} greater than 100 kHz and up to 400 kHz.*
2. *Between STOP and START and between ACK and Re-START.*
3. *From (V_{IL},MAX - 0.15) to (V_{IH},MIN + 0.15)*
4. *From (V_{IH},MIN + 0.15) to (V_{IL},MAX - 0.15)*
5. *Maximum time the module may hold the SCL line low before continuing with a read or write operation.*

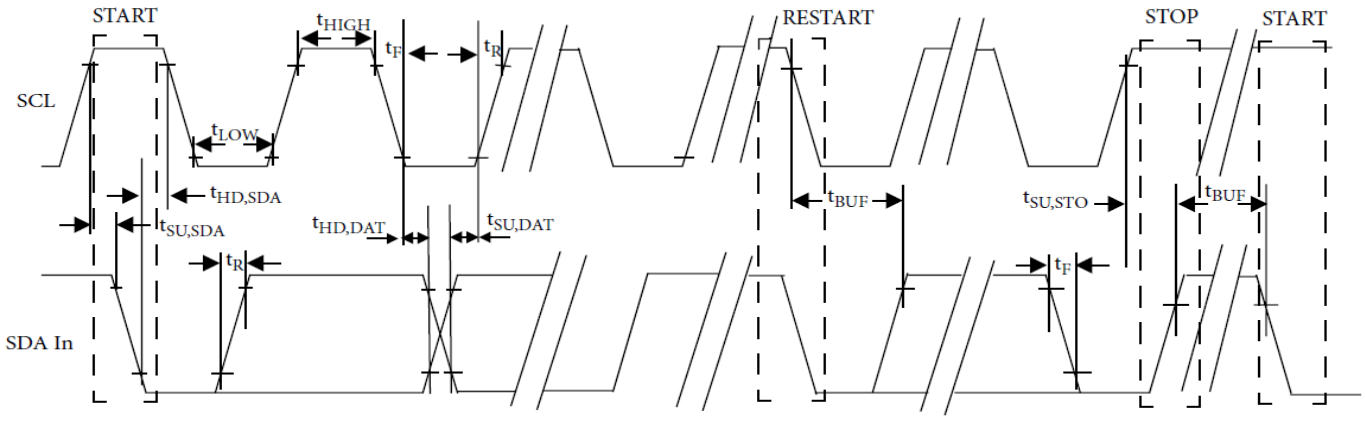

Figure 4. 2-Wire Bus Timing Diagram

12. Package Description & Outline Diagram

* Unit: [mm]

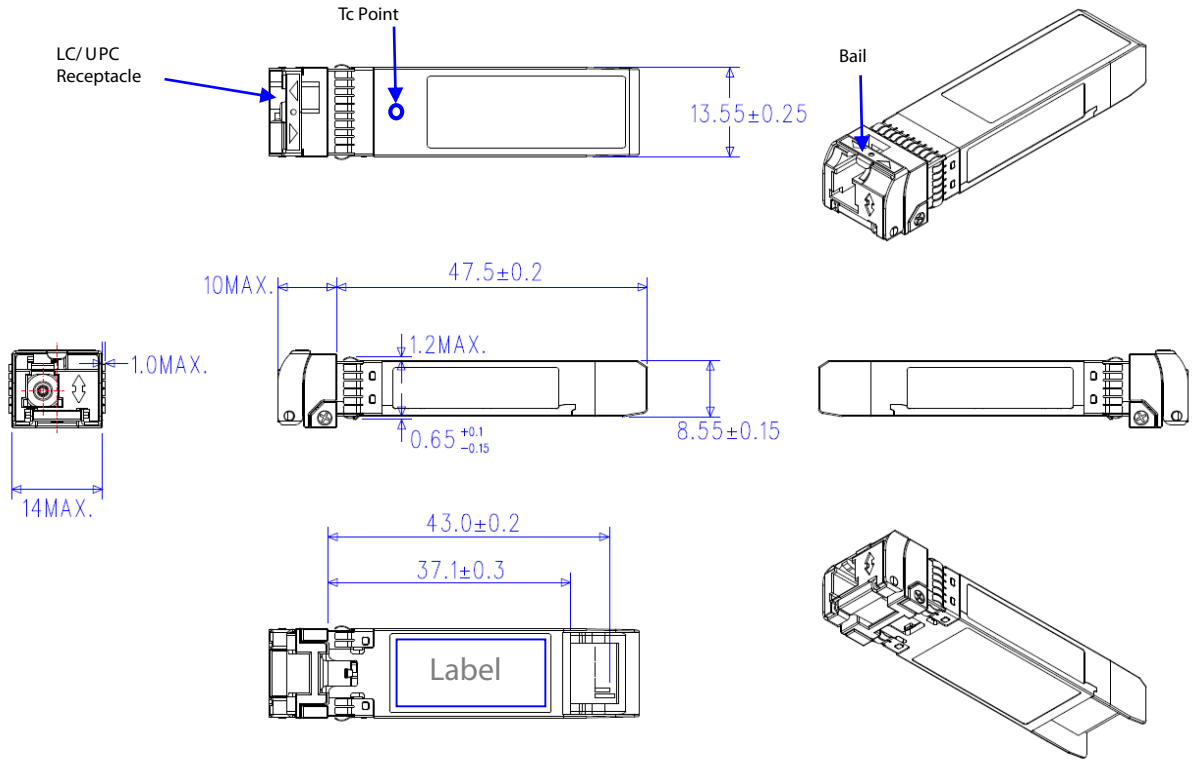

Figure 5. Package outline diagram and example

*** Part number information**

Part No	Wavelength [nm]
AC-B-DR2XC80-I27-yy	1271
AC-B-DR2XC80-I29-yy	1291
AC-B-DR2XC80-I31-yy	1311
AC-B-DR2XC80-I33-yy	1331
AC-B-DR2XC80-I35-yy	1351
AC-B-DR2XC80-I37-yy	1371
AC-B-DR2XC80-I39-yy	1391
AC-B-DR2XC80-I41-yy	1411
AC-B-DR2XC80-I43-yy	1431
AC-B-DR2XC80-I45-yy	1451
AC-B-DR2XC80-I47-yy	1471
AC-B-DR2XC80-I49-yy	1491
AC-B-DR2XC80-I51-yy	1511
AC-B-DR2XC80-I53-yy	1531
AC-B-DR2XC80-I55-yy	1551
AC-B-DR2XC80-I57-yy	1571
AC-B-DR2XC80-I59-yy	1591
AC-B-DR2XC80-I61-yy	1611