

## Overview

Axiom Connectivity Digital Return SFPs are designed for superior flexibility and adaptability. By integrating numerous technical innovations, this Digital Return SFP Series ensures prolonged support for evolving network architectures.

### 1. Features

- Up to 2.5Gb/s
- Un Cooled DFB-LD
- SFP LC/UPC Receptacle (9/125um, SMF)
- Compliant with SFP (Small Form Factor Pluggable) MSA
- Digital Diagnostic Monitoring compliant
- Supports Serial ID functionality
- Class 1 Laser Safety products
- Single +3.3 V power supply with Hot-pluggable Interface
- ROHS compliant

### 2. Applications

- Digital repeater and Base station
- CPRI/OBSAI Line
- Fiber Channel

### 3. Regulatory Compliance

Items	Standard	Performance
<b>Electrostatic Discharge (ESD)</b>	IEC 61000-4-2	Class 1
<b>Electromagnetic Interference (EMI)</b>	FCC Part 15 Class B	Compliant with standards(FCC)
<b>Electromagnetic Compatibility (EMC)</b>	Directive 89/336/EEC	Compliant with standards(CE)
<b>Laser Eye Safety</b>	FDA 21CFR 1040.10 and 1040.11 EN (IEC) 60825-1,2	Class I laser product.
<b>RoHS</b>	Directive 2011/65/EU	Compliant with RoHS

### 4. Absolute Maximum Ratings

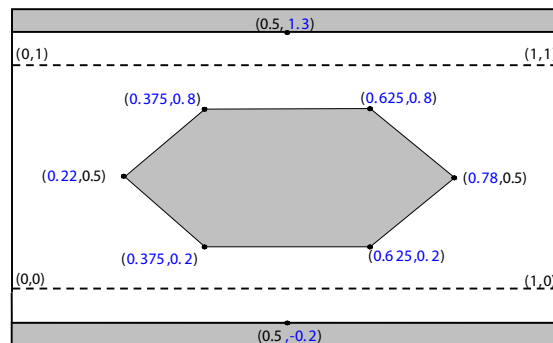
Parameters	Symbol	Ratings	Units	Conditions
Storage Temperature	T <sub>stg</sub>	-40 ~ +85	°C	-
Power Supply Voltage	V <sub>CC</sub>	< +4.0	V	-
Ambient Humidity	H <sub>op</sub>	5 ~ 95	%	w/o dew

**5. Operating conditions**

Parameters	Symbol	Values				Conditions
		Min.	Typ.	Max.	Units	
Power supply voltage	V <sub>CC</sub>	+3.135	+3.30	+3.465	V	-
Power supply current	I <sub>CC</sub>	-	-	500	mA	-
Power Supply Noise Rejection	PSNR	-	-	100	mV <sub>p-p</sub>	from 10Hz to 10MHz
Operating Temperature	T <sub>a</sub>	-40				Case, with Airflow
	T <sub>C</sub>	-	-	+85	°C	

**6. Optical Characteristics**

Parameters	Symbol	Values				Conditions
		Min.	Typ.	Max.	Units	
<b>Transmitter</b>						
Optical Transmit Power	P <sub>f</sub>	0	-	+5.0	dBm	-
Transmitter Disable(Off) Power	P <sub>off</sub>	-	-	-35	dBm	@Tx_Disable is High
Peak Wavelength	λ <sub>p</sub>	λ <sub>c</sub> -6.5	1311	λ <sub>c</sub> +6.5	nm	DFB -LD,
Side Mode Suppression Ratio	SMSR	30	-	-	dB	-
Spectral Width	Δλ	-	-	1.0	nm	@ -20 dB
Extinction Ratio	ER	7.0	-	-	dB	@2.5Gb/s, PRBS 2 <sup>23</sup> -1
Eye pattern Mask	02xGbEthernet					


**Figure 1. Mask of eye diagram for optical output (filtered)**

**7. Electrical Characteristics**

Parameters	Symbol	Values				Conditions	
		Min.	Typ.	Max.	Units		
<b>Transmitter</b>							
Data Rate	DR <sub>T</sub>	-	2.5	-	Gb/s		
Differential Input Voltage	V <sub>INpp</sub>	180	-	800	mV	-	
Differential Input Impedance	Z <sub>IN</sub>	90	100	110	ohm	-	
Tx_Disable	Input_Low	V <sub>IL</sub>	0	-	0.8	V	LVTTTL, Normal at Low, High is Shutdown(P <sub>off</sub> )
	Input_High	V <sub>IH</sub>	2.0	-	3.465	V	
	Assert Time	t <sub>OFF</sub>	-	-	10	us	High
	Negate Time	t <sub>ON</sub>	-	-	1	ms	Low
Tx fault reset	t <sub>reset</sub>	10	-	-	Us	High	
Time to Initialize	t <sub>start_up</sub>	-	-	300	ms	-	
Tx_Fault	Output_Low	V <sub>FOL</sub>	0	-	0.8	V	LVTTTL, Low is Normal
	Output_High	V <sub>FOH</sub>	2.0	-	V <sub>CC</sub> +0.3	V	

### 8. Recommended Circuit Schematic

- Tx\_Disable : Transmitter Disable, logic high, 4.7k to 10kohm pull up to Vcc on SFP
- Tx\_Fault : Transmitter Fault, logic high, 4.7k to 10kohm pull up to Vcc on Host

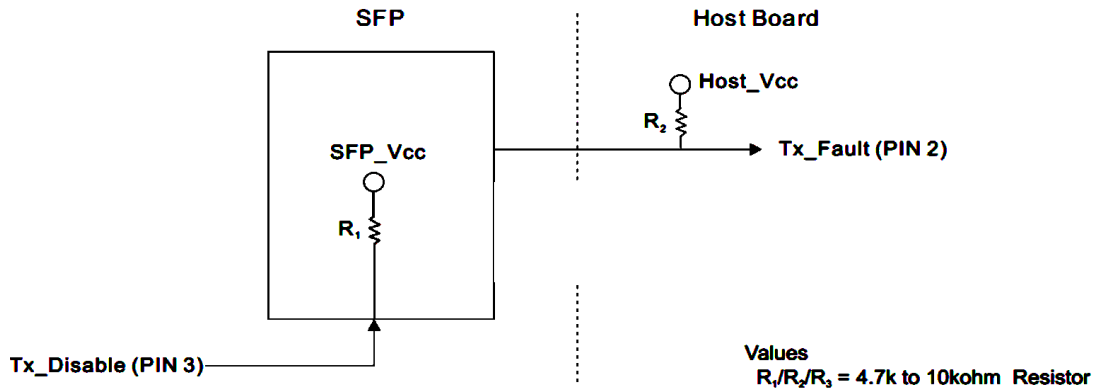


Figure 2. Signal Definitions

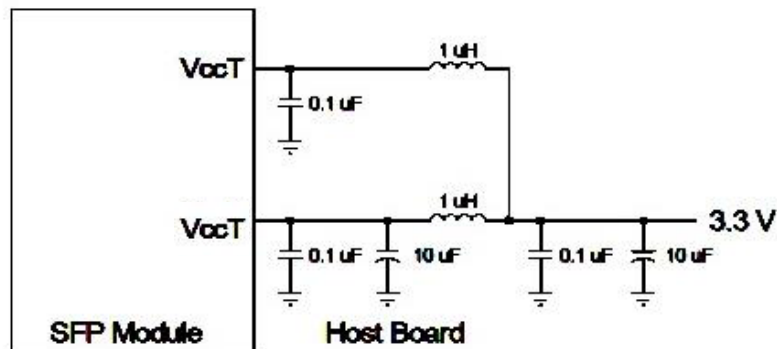
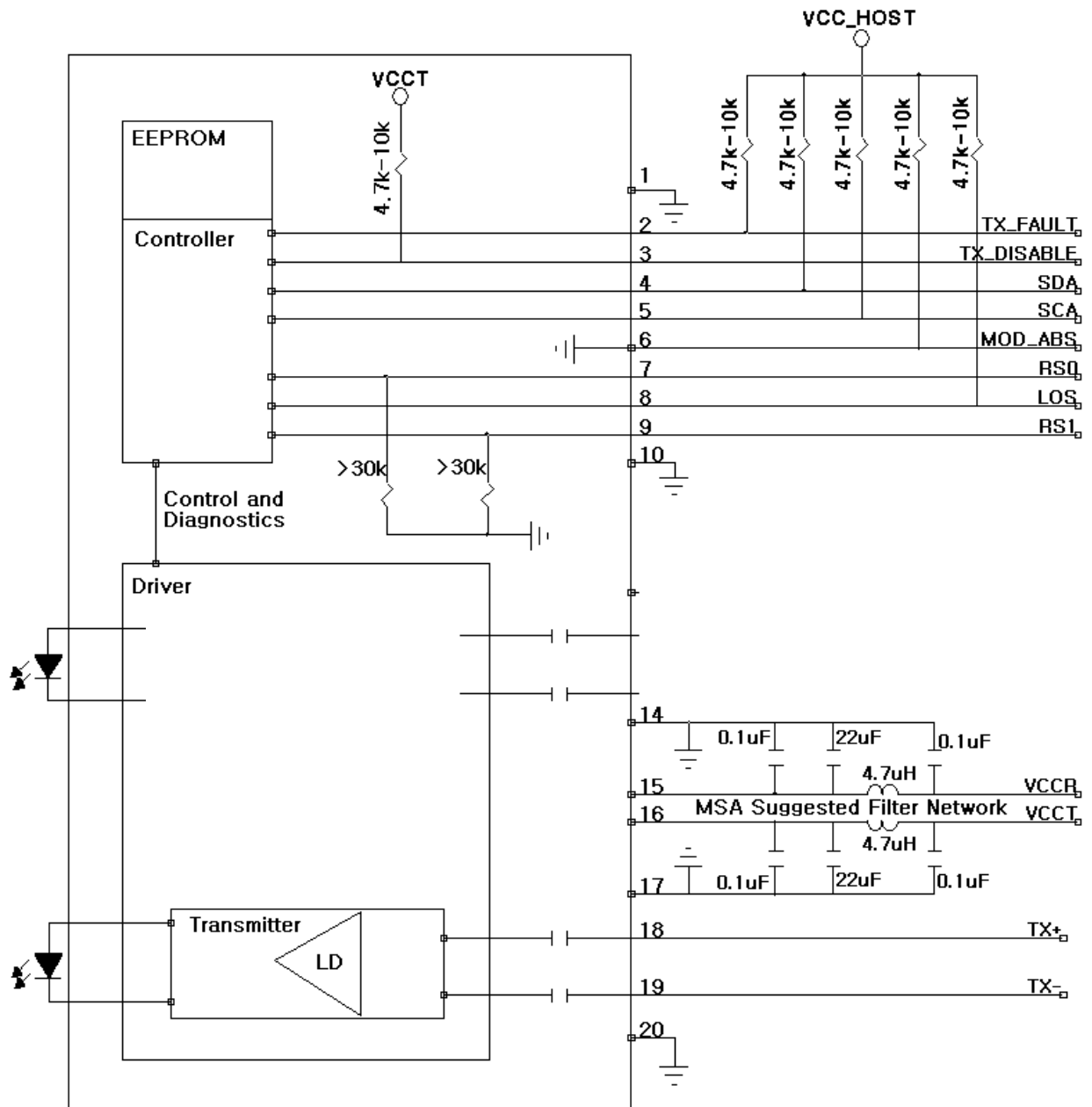
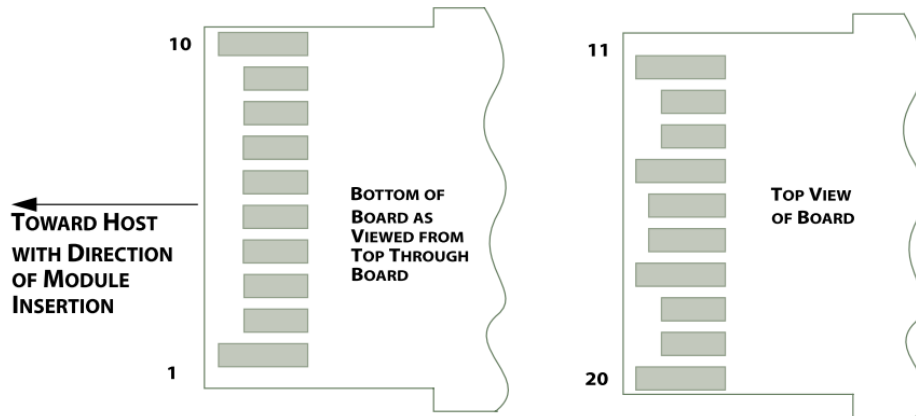


Figure 3. Power Coupling

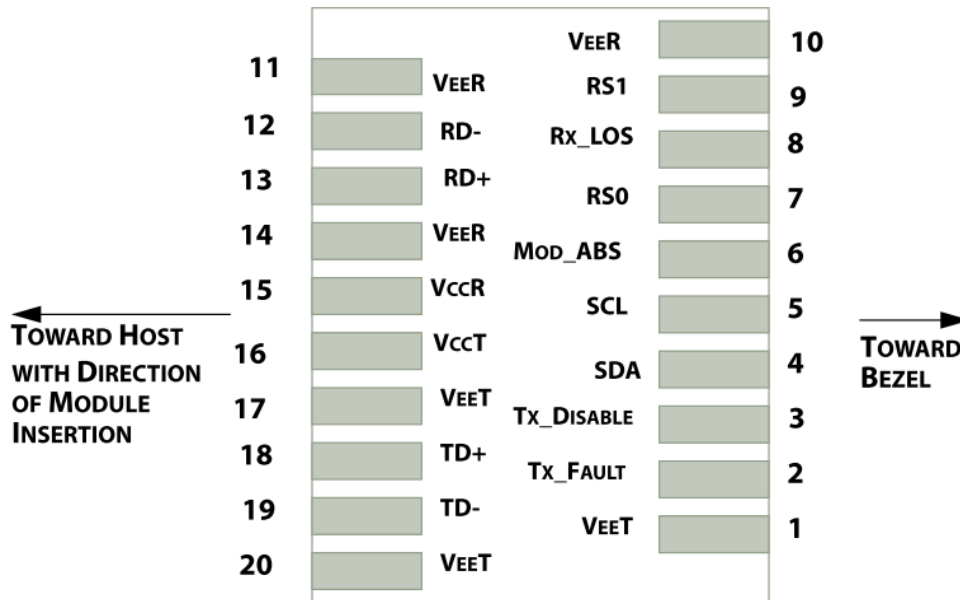


**Figure 4.** Example SFP Host Board Schematic

**9. Pin Information**



**Figure 5-1.** SFP+ Transceiver Electrical Pad Layout



**Figure 5-2.** 20-pin Host PCB SFP+ pad assignment top view

Pin No.	Symbol	Descriptions	Sequence
Pin 1	TGND (VeeT)	Ground	1
Pin 2	Tx_Fault	Status Out	3
Pin 3	Tx_Disable	Control In	3
Pin 4	MOD_DEF(2)	Input/Output(SDA, I <sup>2</sup> C data)	3
Pin 5	MOD_DEF(1)	Input/Output(SCL, I <sup>2</sup> C clock)	3
Pin 6	MOD_DEF(0)	Indicates that the module is present , Grounded internally	3
Pin 7	Rate Select	Rate Select In, Not used (Internally N.C)	3
Pin 8	RX_LOS	Status Out	3
Pin 9	RGND (VeeR)	Ground	3
Pin10	RGND (VeeR)	Ground	1
Pin 11	RGND (VeeR)	Ground	1
Pin 12	Rx_Data bar	Data Out Negative	3
Pin 13	Rx_Data	Data Out Positive	3
Pin 14	RGND (VeeR)	Ground	1
Pin 15	Rx_Vcc (VccR)	Power	2
Pin 16	Tx_Vcc (VccT)	Power	2
Pin 17	TGND (VeeT)	Ground	1
Pin 18	Tx_Data	Data In Positive	3
Pin 19	Tx_Data bar	Data In Negative	3
Pin 20	TGND(VeeT)	Ground	1

**10. 2-Wire Interface Electrical Specifications**

Parameters	Symbol	Min.	Max.	Units	Notes
Host 2 -Wire Vcc	Vcch	3.14	3.46	V	Note 1
SCL and SDA	V <sub>OL</sub>	0.0	0.8	V	R <sub>p</sub> pulled to VccT/R, Note 2
	V <sub>OH</sub>	Vcch -0.5	Vcch+0.3	V	
SCL and SDA	V <sub>IL</sub>	-0.3	VccT*0.3	V	Note 3
	V <sub>IH</sub>	VccT*0.7	VccT+0.5	V	
Input Current on the SCL and SDA Contacts	I <sub>I</sub>	-10	10	μA	-
Capacitance on SCL and SDA contacts	C <sub>i</sub>	-	14	pF	Note 4
Total bus capacitance for SCL and SDA	C <sub>b</sub> <sup>[5]</sup>	-	100	pF	At 400kHz, 3.0k Ω R <sub>p</sub> , max
		-	290	pF	At 100kHz, 8.0k Ω R <sub>p</sub> , max At 400kHz, 1.1k Ω R <sub>p</sub> , max At 100kHz, 2.75k Ω R <sub>p</sub> , max

**Notes:**

1. The Host 2-wire Vcc is the voltage used for resistive pull ups for the 2 wire interface
2. R<sub>p</sub> is the pull up resistor. Active bus termination may be used by the host in place of a pull up resistor. Pull ups can be connected to any one of several power supplies, however the host board design shall ensure that no module contact has voltage exceeding module VccT/R + 0.5 V nor requires the module to sink more than 3.0mA current.
3. These voltages are measured on the other side of the connector to the device under test.
4. C<sub>i</sub> is the capacitance looking into the module SCL and SDA contacts.0
5. C<sub>b</sub> is the total bus capacitance on the SCL or SDA bus.



### 11. 2-Wire Timing Specifications

Parameters	Symbol	Min.	Max.	Units	Notes
Clock Frequency	$f_{SCL}$	0	400	kHz	Note 1
Clock Pulse Width Low	$t_{LOW}$	1.3	-	$\mu s$	-
Clock Pulse Width High	$t_{HIGH}$	0.6	-	$\mu s$	-
Stop to Start Time	$t_{BUF}$	20	-	$\mu s$	Note 2
Start Hold Time	$t_{HD,STA}$	0.6	-	$\mu s$	-
Start Set -up Time	$t_{SU,STA}$	0.6	-	$\mu s$	-
Data In Hold Time	$t_{HD,DAT}$	0	-	$\mu s$	-
Data In Set -up Time	$t_{SU,DAT}$	0.1	-	$\mu s$	-
Input Rise Time (100kHz)	$t_{R,100}$	-	1000	ns	Note 3
Input Rise Time (400kHz)	$t_{R,400}$	-	300	ns	Note 3
Input Fall Time (100kHz)	$t_{F,100}$	-	300	ns	Note 4
Input Fall Time (400kHz)	$t_{F,400}$	-	300	ns	Note 4
Stop Set -up Time	$t_{SU,STO}$	0.6	-	$\mu s$	-
Serial Interface Clock Holdoff "Clock Stretching "	$t_{clock\_hold}$	-	500	$\mu s$	Note 5

**Notes:**

1. Module shall operate with  $f_{SCL}$  up to 100 kHz without requiring clock stretching. The module may clock stretch with  $f_{SCL}$  greater than 100 kHz and up to 400 kHz.
2. Between STOP and START and between ACK and Re-START.
3. From  $(V_{IL,MAX} - 0.15)$  to  $(V_{IH,MIN} + 0.15)$
4. From  $(V_{IH,MIN} + 0.15)$  to  $(V_{IL,MAX} - 0.15)$
5. Maximum time the module may hold the SCL line low before continuing with a read or write operation.

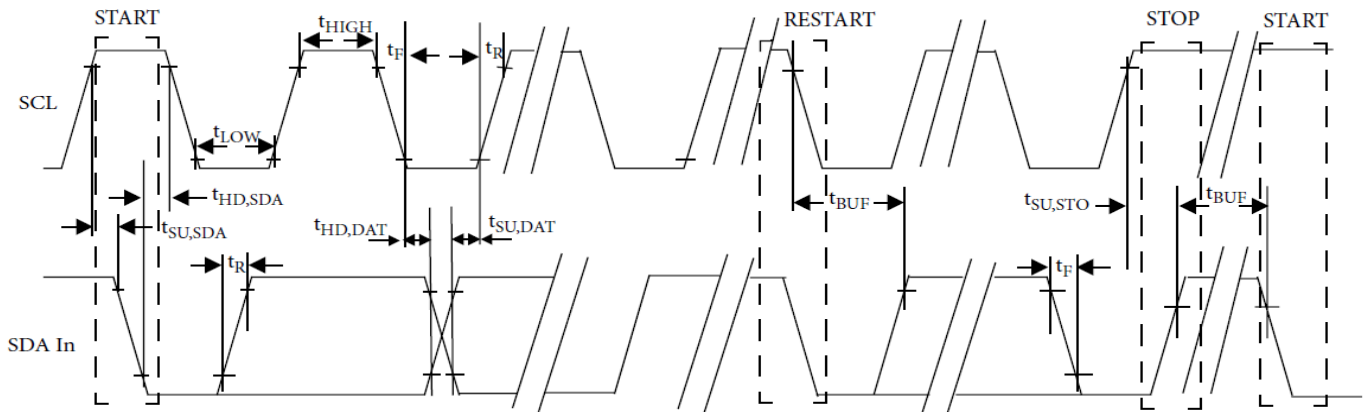


Figure 4. 2-Wire Bus Timing Diagram

**12. Package Description & Outline Diagram**

\* Unit: [mm]

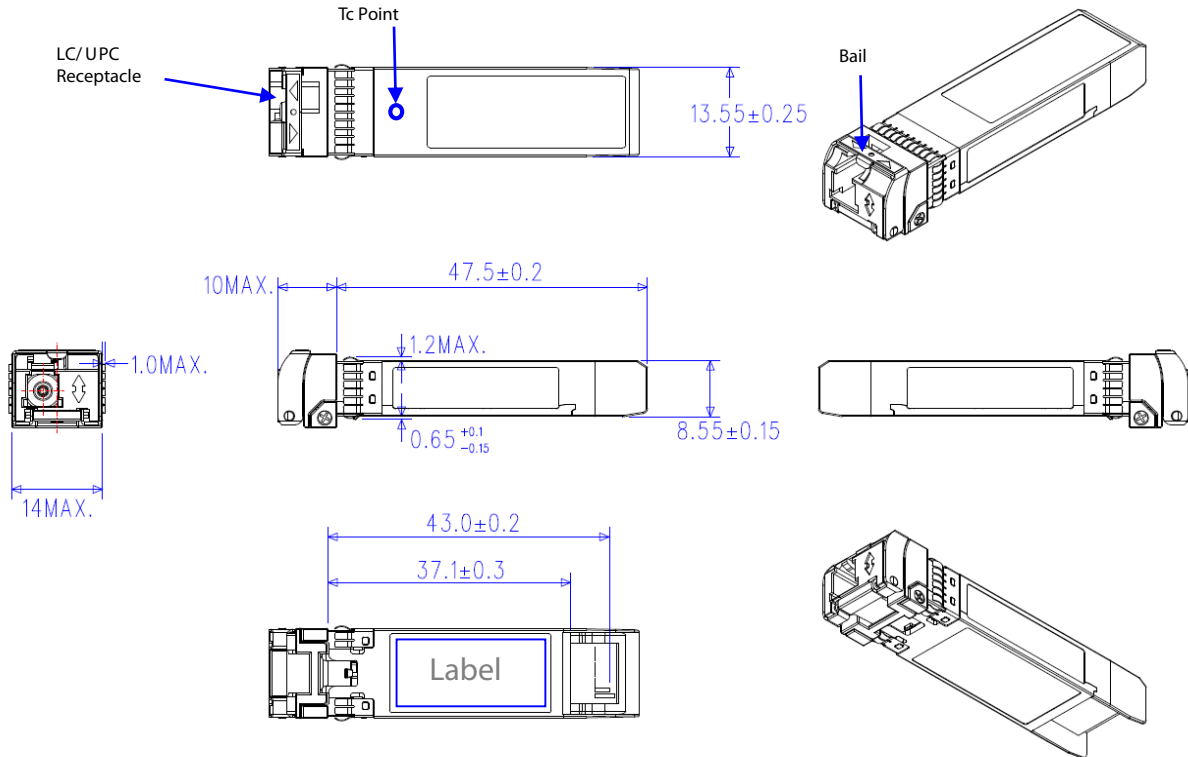


Figure 5. Package outline diagram and example

**\* Part number information**

Part Number	Description
AC-B-DR2XN20-I31-XX	2.5G DIGITAL RETURN SFP SMF, LC, 20KM, 1310NM, DOM IND TEMP TX ONLY