Overview

Axiom Connectivity Digital Return SFPs are designed for superior flexibility and adaptability. By integrating numerous technical innovations, this Digital Return SFP Series ensures prolonged support for evolving network architectures.

1. Features

- Up to 4.25Gb/s Optical Transceiver
- High-density SFP Transmitters
- Embedded Thermo-electric Cooling System
- Cooled transmitter with TEC, Tx (DFB-LD) / Rx (APD)
- LC/UPC Receptacle (9/125um, SMF)
- Compliant with SFP (Small Form Factor Pluggable) MSA
- Compliant with CWDM SFP MSA
- Digital Diagnostic Monitoring compliant
- Supports Serial ID functionality
- Class 1 Laser Safety products
- Single +3.3 V power supply with Hot-pluggable Interface
- Operating case Temperature: -40°C ~ 92°C
- ROHS compliant

2. Applications

- CPRI/OBSAI application : 1.2288, 2.4576, 3.072Gb/s
- Fiber Channel application : 1.0625, 2.125, 4.25Gb/s
- Digital repeater and Base station

3. Regulatory Compliance

Items	**Standard**	Performance
Electrostatic Discharge (ESD)	IEC 61000-4-2	Class 1
Electromagnetic Interference (EMI)	FCC Part 15 Class B	Compliant with standards(FCC)
Electromagnetic Compatibility (EMC)	Directive 89/336/EEC	Compliant with standards(CE)
Laser Eye Safety	FDA 21 CFR 1040.10 and 1040.11 EN (IEC) 60825-1,2	Class 1 laser product.
RoHS	Directive 2011/65/EU	Compliant with RoHS

4. Absolute Maximum Ratings

Parameters	Symbol	**Ratings**	Units	Conditions
Storage Temperature	T_{stg}	-40 ~ + 85	°C	Ambient
Power Supply Voltage	V_{CC}	< +4.0	V	-
Ambient Humidity	H_{op}	5 ~ 95	%	w/o dew
Optical Damage Threshold of Receiver	Pdamage	-1	dBm	-

5. Operating conditions

Parameters	Symbol	Values				Conditions
		Min.	Typ.	Max.	Units	
Power supply voltage	V_{CC}	+3.135	+3.30	+3.465	V	-
Power supply current	I_{CC}	-	-	500	mA	Cooled type
Power Supply Noise Rejection	PSNR	-	-	100	mV_{p-p}	from 100Hz to 1MHz
Operating Temperature	T_C	-40	-	+92	°C	Case, with Airflow

6. Optical Characteristics

Parameters		Symbol	Values				Conditions
			Min.	Typ.	Max.	Units	
Transmitter							
Optical Transmit Power		P_f	+2.0	-	+6.0	dBm	-
Transmitter Disable(Off) Power		P_{off}	-	-	-30	dBm	@Tx_Disable is High
Peak Center Wavelength	1491nm	λ_p	1484.5	1491	1497.5	pm	CWDM, DFB-LD
	1511nm		1504.5	1511	1517.5		
Spectral Width		Δλ	-	-	0.3	nm	@ -20 dB, 4.25Gb/s, PRBS 2^7 -1
Side Mode Suppression Ratio		SMSR	35	-	-	dB	-
RIN 12OMA		RIN	-	-	-120	dB/Hz	-
Extinction Ratio		ER	4.0	-	-	dB	@ 4.25 Gb/s, PRBS 2^7-1
Eye pattern Mask		FC-PI-4					
Receiver							
Optical Sensitivity		S	-	-	-23.0	dBm	PRBS 2^7-1,BER1x10^{-12} Source ER= 4.0 [dB]
Optical Overload		OL	-8.0	-	-	dBm	
Operating Wavelength		λ_O	1290	-	1610	nm	-
Rx_LOS (Loss of signal)	Assert	P_A	-35.0	-	-	dBm	Squelch function enable
	De-assert	P_D	-	-	-23.0	dBm	-
	Hysteresis	P_A-P_D	0.5	2	5	dB	-
Receiver Reflectance		-	-	-	-27	dB	@ λ_O
RSSI Calibration		R_{CAL}	Internal Calibration (The host side can be read by an external way)				-

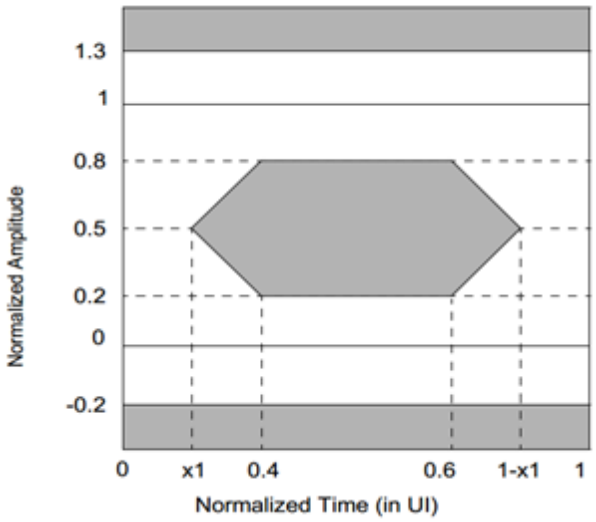

Figure 1. *Mask of eye diagram for optical output (filtered)*

7. Electrical Characteristics

Parameters		Symbol	Values				Conditions
			Min.	Typ.	Max.	Units	
Transmitter							
Data Rate		DR_T	1.062	-	4.250	Gb/s	-
Differential Input Voltage		V_{INpp}	150	-	1000	mV	-
Differential Input Impedance		Z_{IN}	90	100	110	ohm	-
Tx_Disable	Input_Low	V_{IL}	0	-	0.8	V	LVTTL,Normal at Low, High is Shutdown(P_{off})
	Input_High	V_{IH}	2.0	-	Vcc	V	
	Assert Time	t_{OFF}	-	-	10	us	High
	Negate Time	t_{ON}	-	-	1	ms	Low
Tx Disable to reset		t_{reset}	10	-	-	us	High
Time to Initialize_Cooled, Including reset of Tx_Fault		t_{Init_cooled}	-	-	90	sec	Cooled version, for wavelength stabilization at worst case(Low & High temperature)
Tx_Fault	Output_Low	V_{FOL}	0	-	0.8	V	LVTTL, Low is Normal
	Output_High	V_{FOH}	2.0	-	Vcc+0.3	V	
Receiver							
Data Rate		DR_R	1.062	-	4.250	Gb/s	-
Differential Output Voltage		V_{out}	370	-	1005	mV	-
Differential Output Impedance		Z_{out}	90	100	110	ohm	-
Rx_LOS (Loss of signal)	Output_Low	V_{LOSL}	0	-	0.8	V	LVTTL, Low is normal
	Output_High	V_{LOSH}	2	-	Vcc+0.3	V	
	Assert time	$t_{LOS\ -ON}$	-	-	100	us	Low *>>High*
	Deassert time	$t_{LOS\ -OFF}$	-	-	100	us	High *>>Low*

8. Recommended Circuit Schematic

Tx_Disable : Transmitter Disable, logic high, 4.7k to 10kohm pull up to Vcc on SFP
Tx_Fault : Transmitter Fault, logic high, 4.7k to 10kohm pull up to Vcc on Host
Rx_LOS : Receiver Loss of Signal, logic high, 4.7k to 10kohm pull up to Vcc on Host

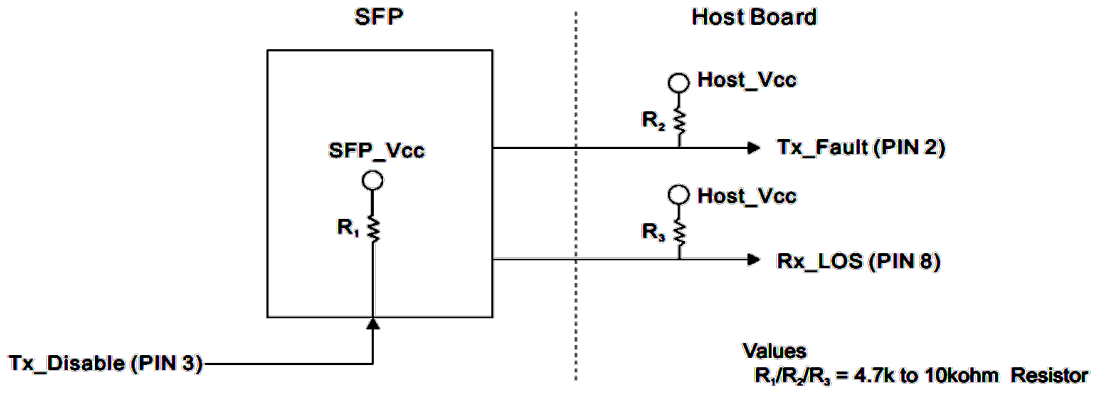

***Figure 2**. Signal Definitions*

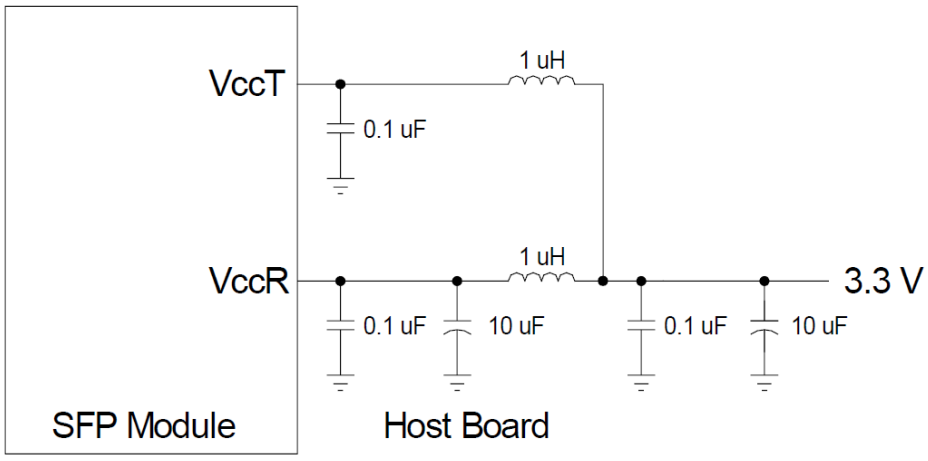

Figure 3. *Recommended Host Board Supply Filtering Network*

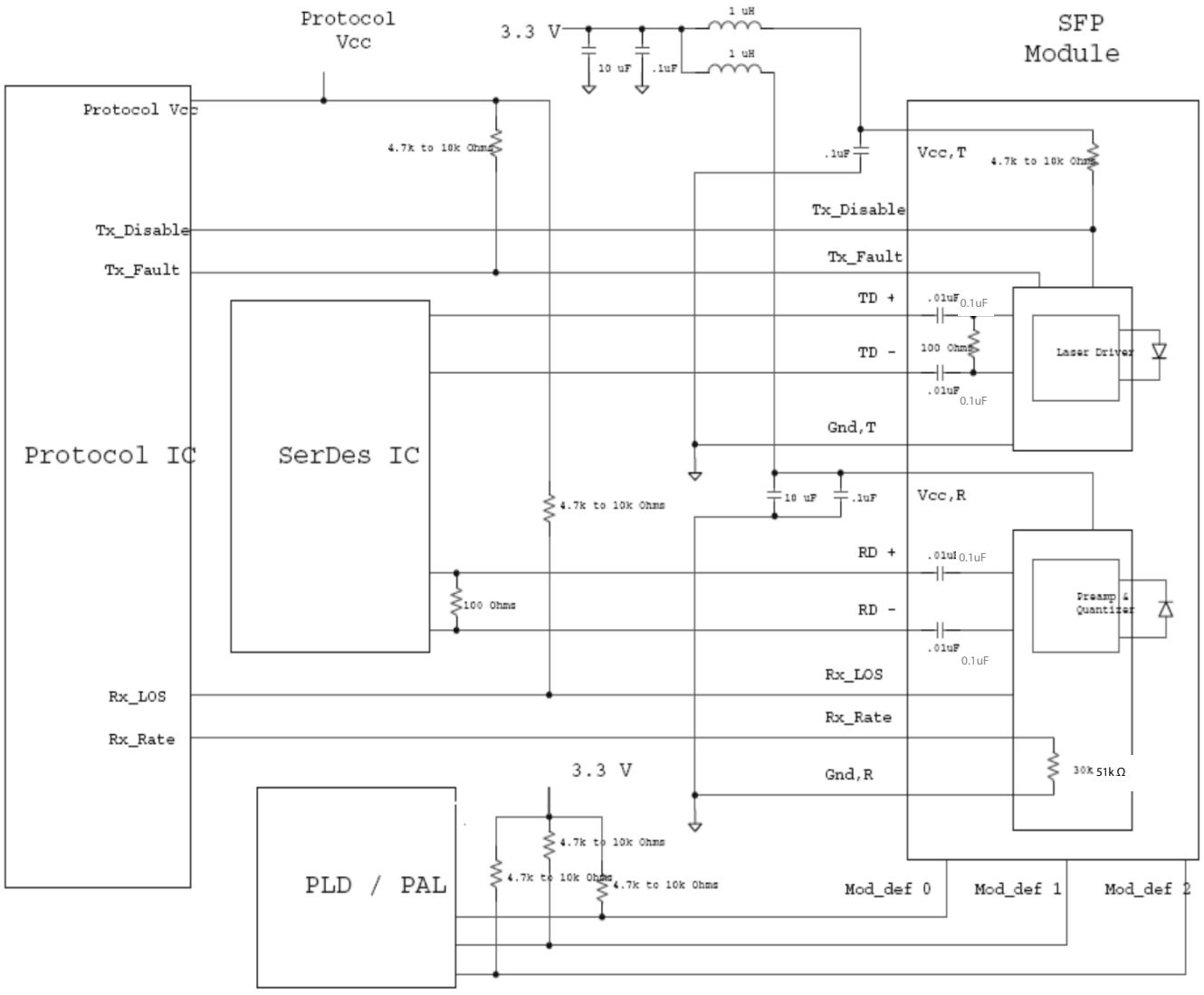

Figure 4. Example SFP Host Board Schematic

9. Pin Information

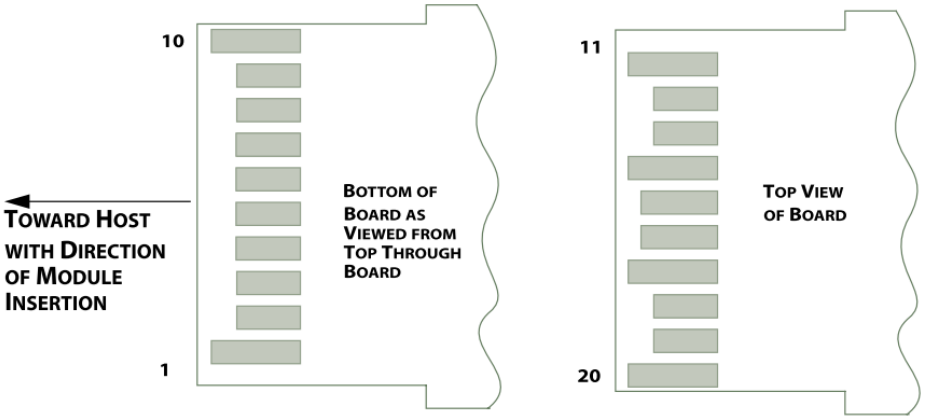

Figure 5-1. SFP+ Transceiver Electrical Pad Layout

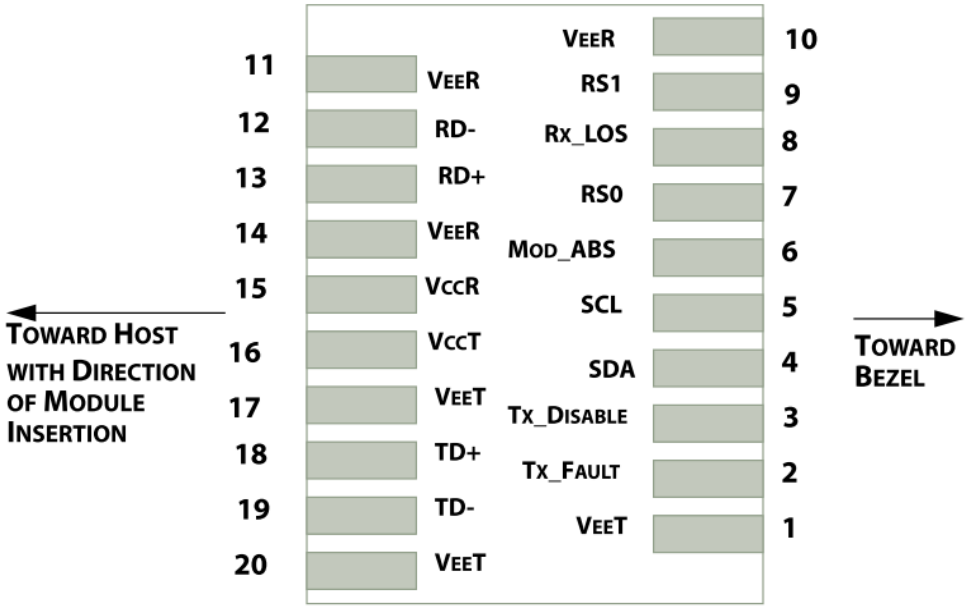

Figure 5-2. 20-pin Host PCB SFP+ pad assignment top view

Pin No.	Symbol	Descriptions	Sequence	Notes
1	VeeT	Transmitter Signal Ground	1st	-
2	Tx_Fault	Transmitter Fault (LVTTL -O) – High indicates a fault condition	3rd	Note 1
3	Tx_Disable	Transmitter Disable (LVTTL -I) – High or open disables the transmitter	3rd	Note 2
4	SDA	Two Wire Serial Interface Data Line (LVCMOS – I/O) (same as MOD -DEF2 in INF -8074)	3rd	Note 3
5	SCL	Two Wire Serial Interface Clock Line (LVCMOS – I/O) (same as MOD -DEF1 in INF -8074)	3rd	Note 3
6	MOD -ABS	Module Absent, (controlled by module)	3rd	Note 4
7	RS0	Receiver Rate Select 0 - not used (Internally pull-down, 51kohm)	3rd	-
8	RX_LOS	Receiver Loss of Signal Indication (LVTTL -O)	3rd	Note 1
9	RS1	Transmitter Rate Select 1 - not used (Internally pull-down, 51kohm)	3rd	-
10	VeeR	Receiver Signal Ground	1st	-
11	VeeR	Receiver Signal Ground	1st	-
12	RD -	Receiver Data Output, Inverted (CML -O)	3rd	-
13	RD+	Receiver Data Output, Non-Inverted (CML -O)	3rd	-
14	VeeR	Receiver Signal Ground	1st	-
15	VccR	Receiver Power + 3.3 V	2nd	-
16	VccT	Transmitter Power + 3.3 V	2nd	-
17	VeeT	Transmitter Signal Ground	1st	-
18	TD+	Transmitter Data Input, Non-Inverted Data (CML -I)	3rd	-
19	TD -	Transmitter Data Input, Inverted (CML -I)	3rd	-
20	VeeT	Transmitter Signal Ground	1st	-

Notes:

1. This is an open drain output that on the host board requires a 4.7kΩ to 10kΩ pull *-up resistor to Vcc_Host.*
2. This input is internally biased high with a 4.7kΩ to 10kΩ pull *-up resistor to VccT.*
3. *Two-Wire Serial interface clock and data lines require an external pull-up resistor dependent on the capacitance load.*
4. *They must be pulled up with a 4.7kΩ to 10 kΩ resistor on the host board. MOD-ABS is grounded by the module to indicate the module is present*

10. 2-Wire Serial-Port Operation

The 2-wire serial-port interface supports a bi-directional data transmission protocol with device addressing. Connections to the bus are made through SDA and SCL. Timing diagrams for the 2-wire serial port can be found in Figure 6. Within the bus specifications, a standard mode (100 kHz clock rate) and a fast mode (400kHz clock rate) are defined.

• The following bus protocol has been defined:

Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

- **Bus not busy:** Both data and clock lines remain high.
- **Start data transfer:** A change in the state of the data line from high to low while the clock is high defines a START condition.
- **Stop data transfer:** A change in the state of the data line from low to high while the clock line is high defines the STOP condition.
- **Data valid:** The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line can be changed during the low period of the clock signal. There is one clock pulse per bit of data. Figure 6 detail how data transfer is accomplished on the 2-wire bus.
- **Clock and Data Transitions:** The SDA pin is normally pulled high with an external resistor or device. Data on the SDA pin may only change during SCL low time periods. Data changes during SCL -high periods will indicate a START or STOP condition depending on the conditions discussed below.
- **START Condition:** A high-to-low transition of SDA with SCL high is a START condition that must precede any other command. See the timing diagrams in Figure 6 for further details.
- **STOP Condition:** A low-to-high transition of SDA with SCL high is a STOP condition. After a read or write sequence, the stop command places the condition into a low-power mode.
- **Acknowledge:** All address and data bytes are transmitted through a serial protocol. The DDM controller pulls the SDA line low during the ninth clock pulse to acknowledge that it has received each word.

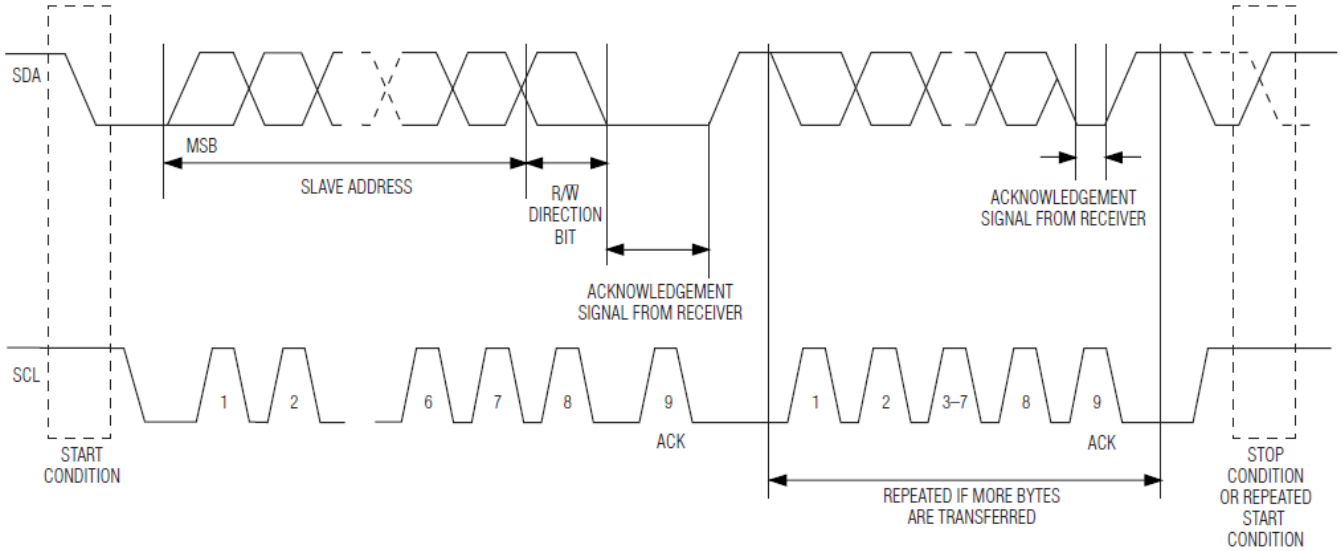

Figure 6. 2-Wire Data Transfer Protocol

11. Package Description & Outline Diagram

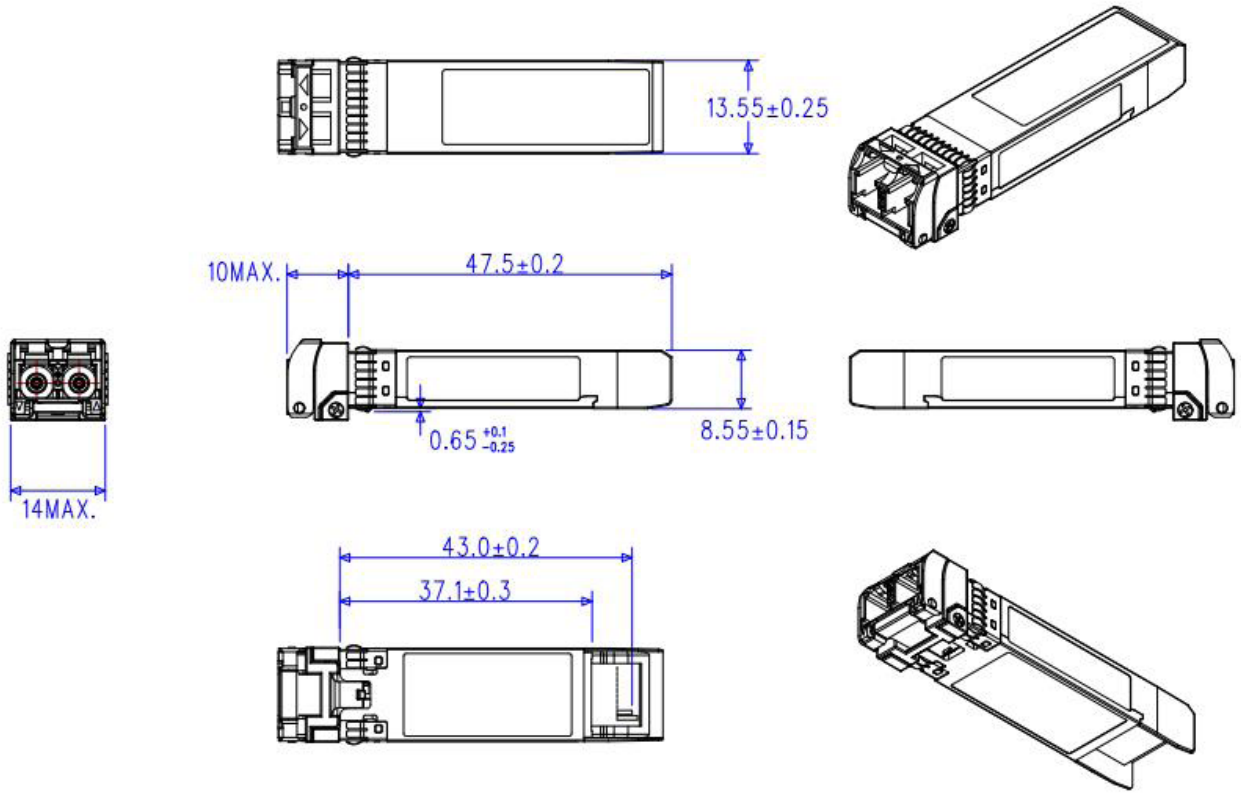

Figure 7. Package outline diagram

*** Part number information**

Part No	Wavelength [nm]
AC-B-DR4TC40-U27-yy	1271
AC-B-DR4TC40-U29-yy	1291
AC-B-DR4TC40-U31-yy	1311
AC-B-DR4TC40-U33-yy	1331
AC-B-DR4TC40-U35-yy	1351
AC-B-DR4TC40-U37-yy	1371
AC-B-DR4TC40-U39-yy	1391
AC-B-DR4TC40-U41-yy	1411
AC-B-DR4TC40-U43-yy	1431
AC-B-DR4TC40-U45-yy	1451
AC-B-DR4TC40-U47-yy	1471
AC-B-DR4TC40-U49-yy	1491
AC-B-DR4TC40-U51-yy	1511
AC-B-DR4TC40-U53-yy	1531
AC-B-DR4TC40-U55-yy	1551
AC-B-DR4TC40-U57-yy	1571
AC-B-DR4TC40-U59-yy	1591
AC-B-DR4TC40-U61-yy	1611