Overview

Axiom Connectivity Digital Return SFPs are designed for superior flexibility and adaptability. By integrating numerous technical innovations, this Digital Return SFP Series ensures prolonged support for evolving network architectures.

1. Features

- Up to 4.9152Gb/s Optical Transmitters
- High-density SFP Transmitters
- Embedded Thermo-electric Cooling System
- 100GHz ITU Grid, C-Band Tx(DFB-LD)
- LC/UPC Receptacle (9/125um, SMF)
- Compliant with SFP+(Small Form Factor Pluggable Plus) MSA
- Compliant with DWDM SFP MSA
- Digital Diagnostic Monitoring compliant
- Supports Serial ID functionality
- Class 1 Laser Safety products
- Single +3.3 V power supply with Hot-pluggable Interface
- Operating case temperature : -40℃ ~ 92℃
- ROHS compliant

2. Applications

- CPRI/OBSAI application
- Fibre Channel application
- Digital repeater and Base station

3. Regulatory Compliance

Items	**Standard**	Performance
Electrostatic Discharge (ESD)	IEC 61000-4-2	Class 1
Electromagnetic Interference (EMI)	FCC Part 15 Class B	Compliant with standards(FCC)
Electromagnetic Compatibility (EMC)	Directive 89/336/EEC	Compliant with standards(CE)
Laser Eye Safety	FDA 21 CFR 1040.10 and 1040.11 EN (IEC) 60825-1,2	Class 1 laser product.
RoHS	Directive 2011/65/EU	Compliant with RoHS

4. Absolute Maximum Ratings

Parameters	Symbol	**Ratings**	Units	Conditions
Storage Temperature	T_{stg}	-40 ~ + 92	℃	Ambient
Power Supply Voltage	V_{CC}	< +4.0	V	-
Ambient Humidity	H_{op}	5 ~ 95	%	w/o dew

5. Operating conditions

Parameters	Symbol	Values				Conditions
		Min.	Typ.	**Max.**	Units	
Power supply voltage	V_{CC}	+3.135	+3.30	+3.465	V	-
Power supply current	I_{CC}	-	-	500	mA	Cooled type
Power Supply Noise Rejection	PSNR	-	-	100	mV_{p-p}	from 100Hz to 1MHz
Operating Temperature	T_C	-40	-	+92		Case, with Airflow

6. Optical Characteristics

Parameters		Symbol	Values				Conditions
			Min.	Typ.	Max.	Units	
Transmitter							
Optical Transmit Power		P_f	+3.0	-	+7.0	dBm	-
Transmitter Disable(Off) Power		P_{off}	-	-	-30	dBm	@Tx_Disable is High
Channel Spacing		λ	100			GHz	Corresponds to approximately 0.8 nm
Peak Center Wavelength	End of Life	λ_p	λ_p -100	λ_p	λ_p +100	pm	λ_p = 100 GHz ITU Grid
	BOL Offset		λ_p -25	λ_p	λ_p +25		
Spectral Width		Δλ	-	-	0.3	nm	@ -20 dB, 4.9152G b/s, PRBS 2^7 -1,
Side Mode Suppression Ratio		SMSR	35	-	-	dB	-
Optical Rise/Fall Time		t_f/t_r	-	-	90	ps	Unfiltered, 80% -20%
RIN $_{12}$OMA		RIN	-	-	-120	dB/Hz	-
Dispersion Penalty		DP	-	-	3.0	dB	1600ps/nm, BER 1x10^{-12}
Total Jitter (peak to peak)		Tjpp	-	-	59.8	ps	-
Extinction Ratio		ER	4.0	-	-	dB	@ 4.9152G b/s, PRBS 2^7 -1
Eye pattern Mask		Compliant with FC-PI-4					

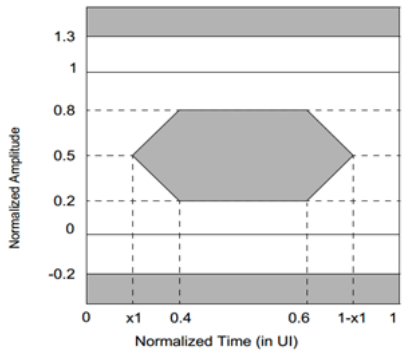

Figure 1. *Mask of eye diagram for optical output (filtered)*

7. Electrical Characteristics

Parameters		Symbol	Values				Conditions
			Min.	Typ.	Max.	Units	
Transmitter							
Data Rate		DR_T	1.0625	-	4.9152	Gb/s	-
Differential Input Voltage		V_{INpp}	190	-	700	mV	-
Differential Input Impedance		Z_{IN}	90	100	110	ohm	-
Tx_Disable	Input_Low	V_{IL}	0	-	0.8	V	LVTTL,Normal at Low, High is Shutdown(P_{off})
	Input_High	V_{IH}	2.0	-	Vcc	V	
	Assert Time	t_{OFF}	-	-	10	us	High
	Negate Time	t_{ON}	-	-	1	ms	Low
Tx Disable to reset		t_{reset}	10	-	-	us	High
Time to Initialize_Cooled, Including reset of Tx_Fault		t_{Init_cooled}	-	-	90	sec	Cooled version, for wavelength stabilization at worst case(Low & High temperature)
Tx_Fault	Output_Low	V_{FOL}	0	-	0.8	V	LVTTL, Low is Normal
	Output_High	V_{FOH}	2.0	-	Vcc+0.3	V	

8. Recommended Circuit Schematic

Tx_Disable : Transmitter Disable, logic high, 4.7k to 10kohm pull up to Vcc on SFP
Tx_Fault : Transmitter Fault, logic high, 4.7k to 10kohm pull up to Vcc on Host
Rx_LOS : Receiver Loss of Signal, logic high, 4.7k to 10kohm pull up to Vcc on Host

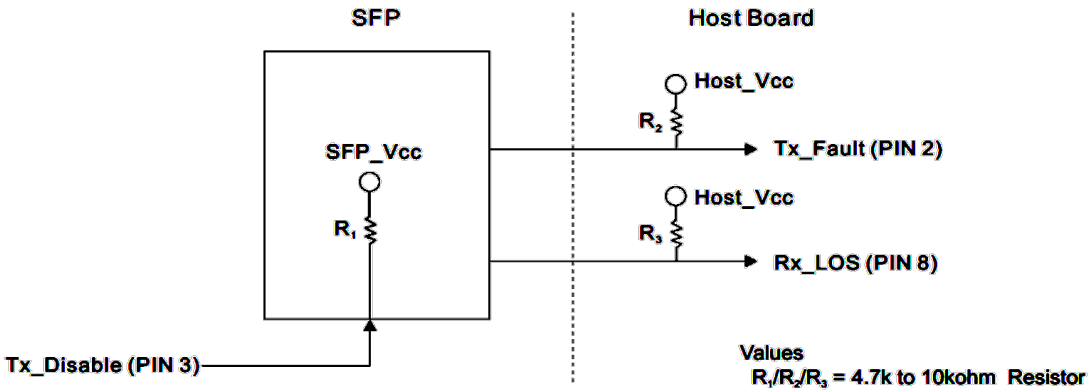

***Figure 2**. Signal Definitions*

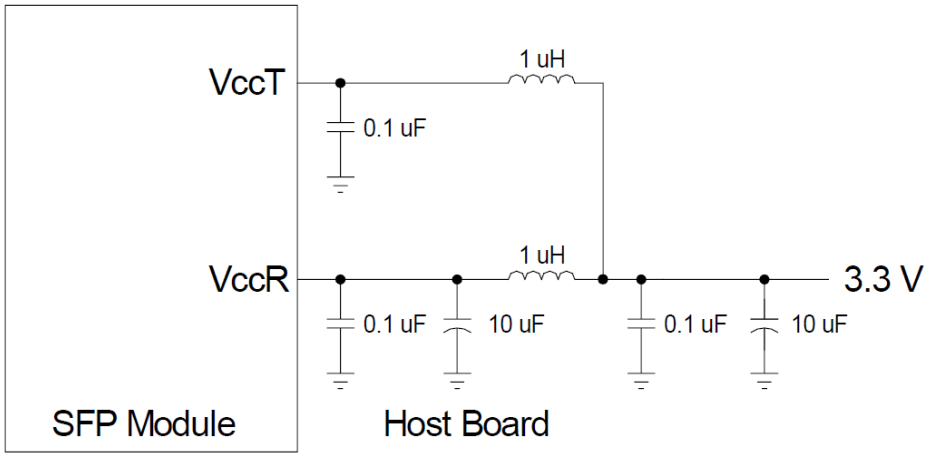

Figure 3. *Recommended Host Board Supply Filtering Network*

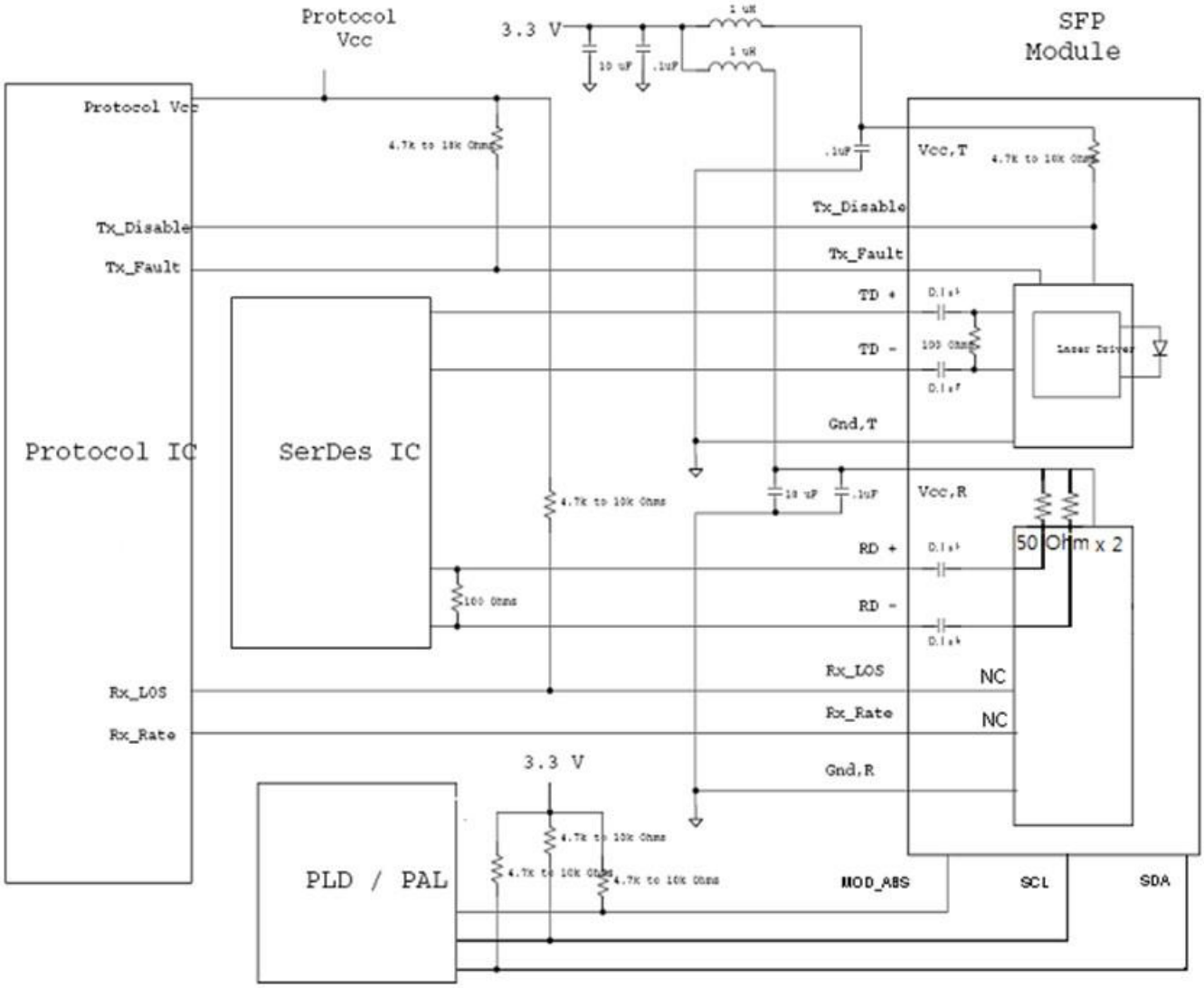

Figure 4. Example SFP Host Board Schematic

9. Pin Information

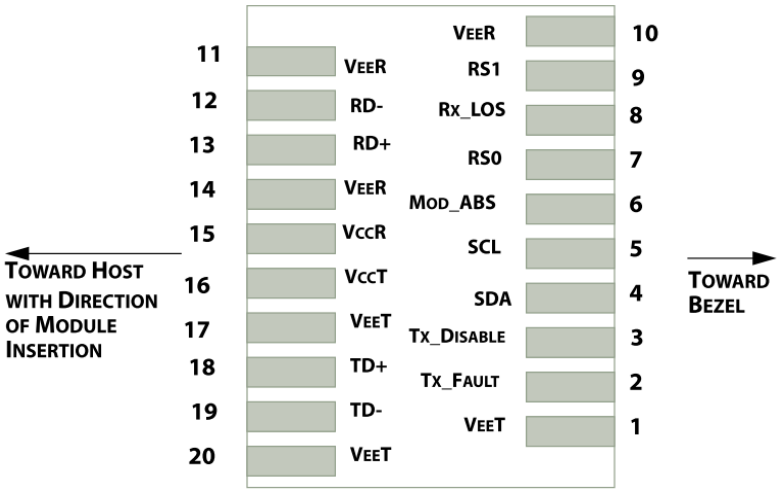

Figure 5. 20 -pin Connector

Pin No.	Symbol	Descriptions	Sequence
Pin 1	TGND (VeeT)	Ground	1
Pin 2	Tx_Fault	Status Out	3
Pin 3	Tx_Disable	Control In	3
Pin 4	MOD_DEF(2)	Input/Output(SDA, I ^{2}C data)	3
Pin 5	MOD_DEF(1)	Input/Output(SCL, I ^{2}C clock)	3
Pin 6	MOD_DEF(0)	Indicates that the module is present , Grounded internally	3
Pin 7	RS 0	Rate Select 0 In(N.C)	3
Pin 8	RX_LOS	Status Out (N.C)	3
Pin 9	RS 1	Rate Select 1 In(N.C)	3
Pin10	RGND (VeeR)	Ground	1
Pin 11	RGND (VeeR)	Ground	1
Pin 12	Rx_Data bar	Data Out Negative (N.C)	3
Pin 13	Rx_Data	Data Out Positive (N.C)	3
Pin 14	RGND (VeeR)	Ground	1
Pin 15	Rx_Vcc (VccR)	Power	2
Pin 16	Tx_Vcc (VccT)	Power	2
Pin 17	TGND (VeeT)	Ground	1
Pin 18	Tx_Data	Data In Positive	3
Pin 19	Tx_Data bar	Data In Negative	3
Pin 20	TGND (VeeT)	Ground	1

10. 2-Wire Serial-Port Operation

The 2-wire serial-port interface supports a bi-directional data transmission protocol with device addressing. Connections to the bus are made through MOD_DEF2 and MOD_DEF1. Timing diagrams for the 2-wire serial port can be found in Figure 6. Within the bus specifications, a standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined.

• **The following bus protocol has been defined:**
Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

- **Bus not busy:** Both data and clock lines remain high.
- **Start data transfer:** A change in the state of the data line from high to low while the clock is high defines a START condi tion.
- **Stop data transfer:** A change in the state of the data line from low to high while the clock line is high defines the STOP condition.
- **Data valid:** The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line can be changed during the low period of the clock signal. There is one clock pulse per bit of data. Figure 6 detail how data transfer is accomplished on the 2-wire bus.
- **Clock and Data Transitions:** The MOD_DEF2 pin is normally pulled high with an external resistor or device. Data on the MOD_DEF2 pin may only change during MOD_DEF1 -low time periods. Data changes during MOD_DEF1 -high periods will indicate a START or STOP condition depending on the conditions discussed below.
- **START Condition:** A high-to-low transition of MOD_DEF2 with MOD_DEF1 high is a START condition that must precede any other command. See the timing diagrams in Figure 6 for further details.
- **STOP Condition:** A low-to-high transition of MOD_DEF2 with MOD_DEF1 high is a STOP condition. After a read or write sequence, the stop command places the condition into a low-power mode.
- **Acknowledge:** All address and data bytes are transmitted through a serial protocol. The MCU pulls the MOD_DEF2 line low during the ninth clock pulse to acknowledge that it has received each word.

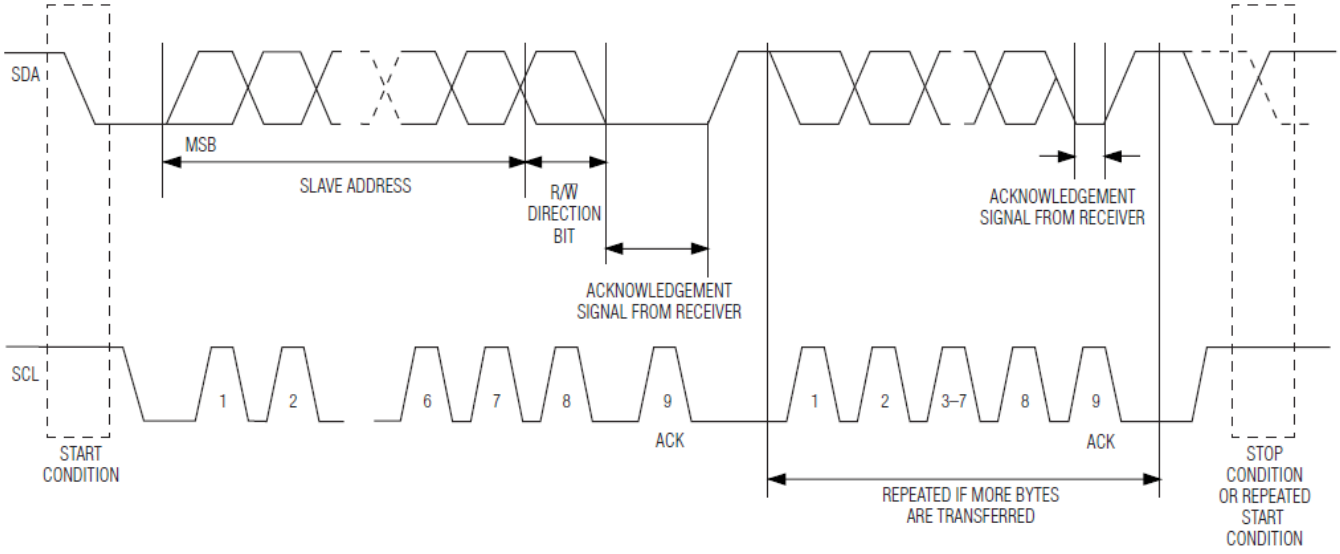

Figure 6. 2-Wire Data Transfer Protocol

11. Package Description & Outline Diagram

* Unit: [mm]

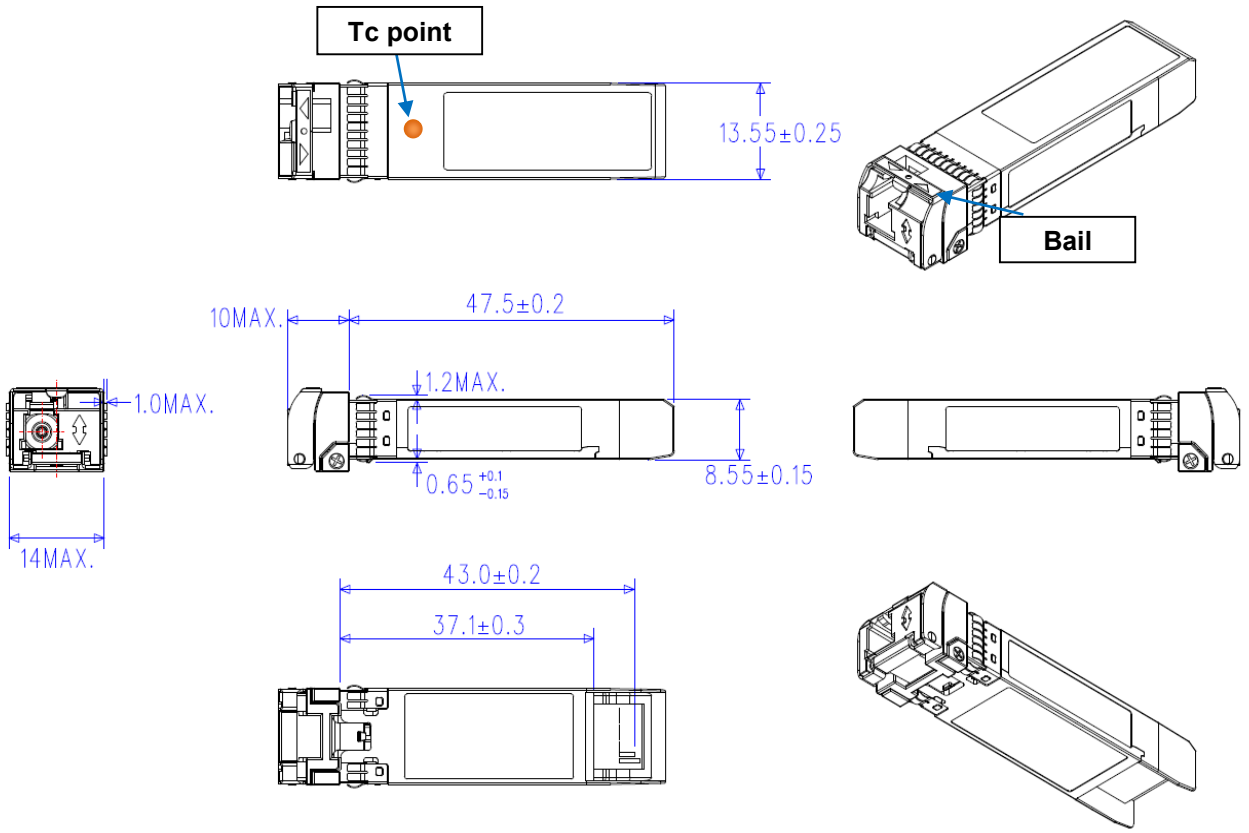

Figure 7. Package outline diagram and example

*** Part number information(ITU-T G.694.1 100GHz Spacing)**

ITU-T CH No.	Part No	Frequency [THz]	Wavelength [nm]	ITU-T CH No.	Part No	Frequency [THz]	Wavelength [nm]
1	AC-B-DR5XD80-U01-yy	190.1	1557.03	32	AC-B-DR5XD80-U32-yy	193.2	1551.72
2	AC-B-DR5XD80-U02-yy	190.2	1576.20	33	AC-B-DR5XD80-U33-yy	193.3	1550.92
3	AC-B-DR5XD80-U03-yy	190.3	1575.37	34	AC-B-DR5XD80-U34-yy	193.4	1550.12
4	AC-B-DR5XD80-U04-yy	190.4	1574.54	35	AC-B-DR5XD80-U35-yy	193.5	1549.32
5	AC-B-DR5XD80-U05-yy	190.5	1573.71	36	AC-B-DR5XD80-U36-yy	193.6	1548.51
6	AC-B-DR5XD80-U06-yy	190.6	1572.89	37	AC-B-DR5XD80-U37-yy	193.7	1547.72
7	AC-B-DR5XD80-U07-yy	190.7	1572.06	38	AC-B-DR5XD80-U38-yy	193.8	1546.92
8	AC-B-DR5XD80-U08-yy	190.8	1571.24	39	AC-B-DR5XD80-U39-yy	193.9	1546.12
9	AC-B-DR5XD80-U09-yy	190.9	1570.42	40	AC-B-DR5XD80-U40-yy	194.0	1545.32
10	AC-B-DR5XD80-U10-yy	191.0	1569.59	41	AC-B-DR5XD80-U41-yy	194.1	1544.53
11	AC-B-DR5XD80-U11-yy	191.1	1568.77	42	AC-B-DR5XD80-U42-yy	194.2	1543.73
12	AC-B-DR5XD80-U12-yy	191.2	1567.95	43	AC-B-DR5XD80-U43-yy	194.3	1542.94
13	AC-B-DR5XD80-U13-yy	191.3	1567.13	44	AC-B-DR5XD80-U44-yy	194.4	1542.14
14	AC-B-DR5XD80-U14-yy	191.4	1566.31	45	AC-B-DR5XD80-U45-yy	194.5	1541.35
15	AC-B-DR5XD80-U15-yy	191.5	1565.50	46	AC-B-DR5XD80-U46-yy	194.6	1540.56
16	AC-B-DR5XD80-U16-yy	191.6	1564.68	47	AC-B-DR5XD80-U47-yy	194.7	1539.77
17	AC-B-DR5XD80-U17-yy	191.7	1563.86	48	AC-B-DR5XD80-U48-yy	194.8	1538.98
18	AC-B-DR5XD80-U18-yy	191.8	1563.05	49	AC-B-DR5XD80-U49-yy	194.9	1538.19
19	AC-B-DR5XD80-U19-yy	191.9	1562.23	50	AC-B-DR5XD80-U50-yy	195.0	1537.40
20	AC-B-DR5XD80-U20-yy	192.0	1561.42	51	AC-B-DR5XD80-U51-yy	195.1	1536.61
21	AC-B-DR5XD80-U21-yy	192.1	1560.61	52	AC-B-DR5XD80-U52-yy	195.2	1535.82
22	AC-B-DR5XD80-U22-yy	192.2	1559.79	53	AC-B-DR5XD80-U53-yy	195.3	1535.04
23	AC-B-DR5XD80-U23-yy	192.3	1558.98	54	AC-B-DR5XD80-U54-yy	195.4	1534.25
24	AC-B-DR5XD80-U24-yy	192.4	1558.17	55	AC-B-DR5XD80-U55-yy	195.5	1533.47
25	AC-B-DR5XD80-U25-yy	192.5	1557.36	56	AC-B-DR5XD80-U56-yy	195.6	1532.68
26	AC-B-DR5XD80-U26-yy	192.6	1556.55	57	AC-B-DR5XD80-U57-yy	195.7	1531.90
27	AC-B-DR5XD80-U27-yy	192.7	1555.75	58	AC-B-DR5XD80-U58-yy	195.8	1531.12
28	AC-B-DR5XD80-U28-yy	192.8	1554.94	59	AC-B-DR5XD80-U59-yy	195.9	1530.33
29	AC-B-DR5XD80-U29-yy	192.9	1554.13	60	AC-B-DR5XD80-U60-yy	196.0	1529.55
30	AC-B-DR5XD80-U30-yy	193.0	1553.33	61	AC-B-DR5XD80-U61-yy	196.1	1528.77
31	AC-B-DR5XD80-U31-yy	193.1	1552.52				