

# 100Gb/s CFP2 LR4 Optical Transceiver

## Product Features

- Hot Pluggable CFP2 MSA package
- IEEE 802.3ba 100GBASE-LR4 compliant
- ITU-T 411-9D1F compliant
- CFP-MSA-CFP2-HW-Specification compliant
- Up to 10km for G.652 SMF
- Receiver: up to 4 x 28Gb/s PIN ROSA
- Transmitter: up to 4 x 28Gb/s WDM TOSA
- (1295.56,1300.05,1304.58,1309.14nm)
- 4 x 28G Electrical Serial Interface (CEI-28G-VSR)
- MDIO management interface with Digital Diagnostic
- +3.3V power supply
- Power consumption less than 9W
- Compact size: 107.5 x 41.5 x 12.4 mm
- Operating case temperature: 0 to +70 °C
- Duplex LC Receptacle
- ROHS-6 compliant

## Applications

- 100GE Routers and Switches
- 100G DWDM/OTN
- 100G Network Security
- And Monitoring

This 100G CFP2 LR4 optical Transceiver integrates receiver and transmitter path on one module. In the transmit side, four lanes of serial data streams are recovered, retimed, and passed to four laser drivers. The laser drivers control four EMLs (Electric-absorption Modulated Lasers) with center wavelength of 1296 nm, 1300nm, 1305nm and 1309 nm. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector. In the receive side, the four lanes of optical data streams are optically de-multiplexed by the integrated optical de-multiplexer. Each data stream is recovered by a PIN photo-detector and trans-impedance amplifier, retimed. This module features a hot-pluggable electrical interface, low power consumption and MDIO management interface.

## Ordering Information

Part Number	Description
AC-E-CFP2LR4-xx	CFP2 100G LR4 10km optical transceiver with full real-time digital diagnostic monitoring

## Regulatory Compliance

Feature	Standard	Performance
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN 55022:2010, Class B	Compatible with standards
Electromagnetic susceptibility (EMS)	EN 55024:2010	Compatible with standards
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1,2	Compatible with Class I laser product

**Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Min.	Max	Unit
Storage temperature ( case )	T <sub>stg</sub>	—	-40	+85	°C
Relative humidity	RH	-	5	85	%
Damage Threshold for Receiver	P <sub>max</sub>	—	—	+10.0	dBm
Power Supply	V <sub>cc</sub> 3.3V	—	-0.3	+3.6	V
	V <sub>cc</sub> 5.0V	—	—	—	V
Input 3.3V LVCMOS signal level	V <sub>i</sub>	—	-0.3	V <sub>cc</sub> +0.3	V
Input 1.2V LVCMOS signal level	V <sub>i</sub>		-0.3	1.6	V
ESD Sensitivity on module and all host pins	HBM	Human Body model R=1.5K, C=100pF	—	2000	V

**Recommended operating conditions**

100Gb/s CFP2 recommended working conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	T <sub>c</sub>	0	—	+70	°C
Supply voltage	V <sub>cc</sub> 3.3V	+3.14	+3.3	+3.47	V
Supply Current	I <sub>cc</sub> 3.3V	—	—	2.56	A
Power dissipation	P	—	—	9	W
Low Power dissipation	P <sub>Low</sub>			2	W
In-rush Current	I <sub>inrush</sub>			200	mA/us
Turn-off rush Current	I <sub>turnoff</sub>	-200			mA/us
Link Distance	L	2M	—	10km	G.652 SMF

**Low Speed Electrical Characteristics**

100Gb/s CFP2 3.3V LVCMOS Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V <sub>CC</sub>		3.2	3.3	3.4	V
Input High Voltage	V <sub>IH</sub>		2		V <sub>CC</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>		-0.3		0.8	V
Input Leakage Current	I <sub>IN</sub>		-10		+10	mA
Output High Voltage (I <sub>OH</sub> = -100uA)	V <sub>OH</sub>		V <sub>CC</sub> -0.2		V <sub>CC</sub> +0.3	V
Output Low Voltage (I <sub>OL</sub> = 100uA)	V <sub>OL</sub>		-0.3		0.2	V
Minimum Pulse Width of Control Pin Signal	t <sub>CNTL</sub>		100			us

100Gb/s CFP2 1.2V LVCMOS Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input High Voltage	V <sub>IH</sub>		0.84		1.5	V
Input Low Voltage	V <sub>IL</sub>		-0.3		0.36	V
Input Leakage Current	I <sub>IN</sub>		-100		+100	uA
Output High Voltage	V <sub>OH</sub>		1.0		1.5	V
Output Low Voltage	V <sub>OL</sub>		-0.3		0.2	V
Output High Current	I <sub>OH</sub>				-4	mA
Output Low Current	I <sub>OL</sub>		+4			mA
Input capacitance	C <sub>i</sub>				10	pF

## 100Gb/s CFP2 Timing Parameters for CFP2 Hardware Signal Pins

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert				1	ms
Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert				10	s
Receiver Loss of Signal Assert Time	t_loss_assert				100	us
Receiver Loss of Signal De-Assert Time	t_loss_deassert				100	us
Global Alarm Assert Delay Time	GLB_ALRMn_assert				150	ms
Global Alarm De-Assert Delay Time	GLB_ALRMn_deassert				150	ms
Management Interface Clock Period	t_prd		250			ns
Host MDIO t_setup	t_setup		10			ns
Host MDIO t_hold	t_hold		10			ns
CFP2 MDIO t_delay	t_delay		0		175	ns
Initialization time from Reset	t_initialize				2.5	s
Transmitter Disabled (TX_DIS asserted)	t_deassert				100	us
Transmitter Enabled (TX_DIS de-asserted)	t_assert				2	ms

## 100Gb/s CFP2 MDIO and MDC Timing Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Management Interface Clock Frequency	F_MDC		0.1		4	MHz

Management Interface Clock Period	t_prd		250		10000	ns
Host MDIO t_setup	t_setup		10			ns
Host MDIO t_hold	t_hold		10			ns
CFP2 MDIO t_delay <sup>1</sup>	t_delay		0		175	ns
MDC high and low time	twidth		40		60	%
			160			ns
MDIO/MDC termination in CFP2	Zt		100			kOhm

### High Speed Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Transmitter (CEI-28G-VSR input interface)</b>						
Signal Rate Per Lane		100GE		25.7812		Gb/s
Signal Rate Per Lane		OTU4		27.9525		Gb/s
Signal Rate Tolerance		100GE	-100		100	ppm
Signal Rate Tolerance		OTU4	-20		20	ppm
Input Differential Voltage	Vdiff	Emphasis off			1200	mVppd
Differential Input Resistance	Rdin		85	100	115	Ω
Input Impedance Mismatch	Rm				5	%
Sinusoidal Jitter, Maximum					5	Upp
Sinusoidal Jitter, High Frequency					0.05	Upp
<b>Receiver (CEI-28G-VSR output interface)</b>						
Signal Rate Per Lane		100GE		25.7812		Gb/s
Signal Rate Per Lane		OTU4		27.9525		Gb/s

Signal Rate Tolerance		100GE	-100		100	ppm
Signal Rate Tolerance		OTU4	-20		20	ppm
Output Differential Voltage	Vdiff	Equalization off	600	750	900	mVppd
Differential Resistance	Rdo		85	100	115	Ω
Differential Termination Resistance Mismatch	Rdm				5	%
Output Rise and Fall Time	T <sub>tr</sub> , T <sub>tf</sub>	20% to 80%			15	ps
Common Mode Noise(RMS)	Ncm				12	mV
Uncorrelated Unbounded Gaussian Jitter				0.1	0.15	Upp
Uncorrelated Bounded High Probability Jitter				0.18	0.28	Upp
Total Jitter	T <sub>j</sub>			0.28	0.43	Upp

**Optical Characteristics(100G Ethernet)**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Transmitter</b>						
Channel data rate				25.7812		Gbps
Aggregate data rate				103.125		Gbps
Data rate variation			-100		+100	ppm
Lane Center Wavelength	λ <sub>CT0</sub>		1294.53	1295.56	1296.59	nm
	λ <sub>CT1</sub>		1299.02	1300.05	1301.09	nm
	λ <sub>CT2</sub>		1303.54	1304.58	1305.63	nm
	λ <sub>CT3</sub>		1308.09	1309.14	1310.19	nm
Total Average Launch Power	P <sub>out</sub>		—	—	10.5	dBm

Average Launch Power per Lane	Peach		-4.3	—	4.5	dBm
Optical Modulation Amplitude per Lane	OMA		-1.3	—	4.5	dBm
Difference in Launch power between any two lanes(OMA)			—	—	5.0	dB
Launch power in OMA minus TDP, per lane	Pomatdp		-2.3	—	—	dBm
Average Launch Power of TX_DIS Transmitter per lane	Poff	TX_DIS=H	—	—	-30	dBm
Extinction Ratio	ER		4	5.5	—	dB
SMSR	SMSR		30	—	—	dB
Dispersion Penalty	DP	10km SMF	—	—	2.2	dB
Relative Intensity Noise	RIN	Mod off	—	—	-130	dB/Hz
Optical Return Loss Tolerance	TRL		—	—	20	dB
Transmitter reflectance	Tef		—	—	-12	dB
Optical Eye Mask {X1, X2, X3, Y1, Y2, Y3} <sup>1</sup>	EM		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			
<b>Receiver</b>						
Channel data rate				25.7812		Gbps
Data rate variation			-100		+100	ppm
Lane Center Wavelength	$\lambda_{CR0}$		1294.53	1295.56	1296.59	nm
	$\lambda_{CR1}$		1299.02	1300.05	1301.09	nm
	$\lambda_{CR2}$		1303.54	1304.58	1305.63	nm
	$\lambda_{CR3}$		1308.09	1309.14	1310.19	nm
Damage threshold	P <sub>DT</sub>		—	5.5	—	dBm
Average receiver power per lane	Rpow		-10.6	—	4.5	dBm

Receive power OMA per lane	Rovl		—	—	4.5	dBm
Difference in receive power between any two lanes(OMA)			—	—	5.5	dB
Receiver Sensitivity(OMA) per lane	Psen		—	—	-8.6	dBm
Stressed Receiver Sensitivity per Lane	Psen_str		—	—	-6.8	dBm
Receiver Reflectance	Ref		—	—	-26	dB
Conditions of stressed receiver sensitivity test						
Vertical eye closure penalty per Lane			—	—	1.8	dB
Stressed eye jitter per Lane			—	—	0.3	UI
Rx-Lane LOS Assert			—	—	-12	dBm
Rx-Lane LOS Deassert			-13.6	—	—	dBm
Rx-Lane LOS Hysteresis			0.5	—	—	dB

### Optical Characteristics(OTU4)

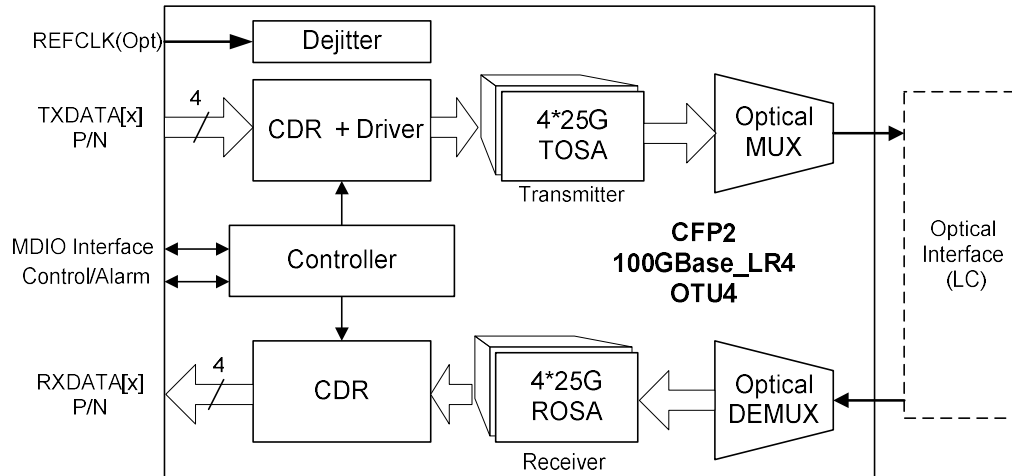
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Transmitter</b>						
Channel data rate				27.9525		Gbps
Aggregate data rate				111.809		Gbps
Data rate variation			-20		+20	ppm
Lane Center Wavelength	$\lambda_{CT0}$		1294.53	1295.56	1296.59	nm
	$\lambda_{CT1}$		1299.02	1300.05	1301.09	nm
	$\lambda_{CT2}$		1303.54	1304.58	1305.63	nm
	$\lambda_{CT3}$		1308.09	1309.14	1310.19	nm
Total Average Launch Power	Pout		—	—	8.9	dBm



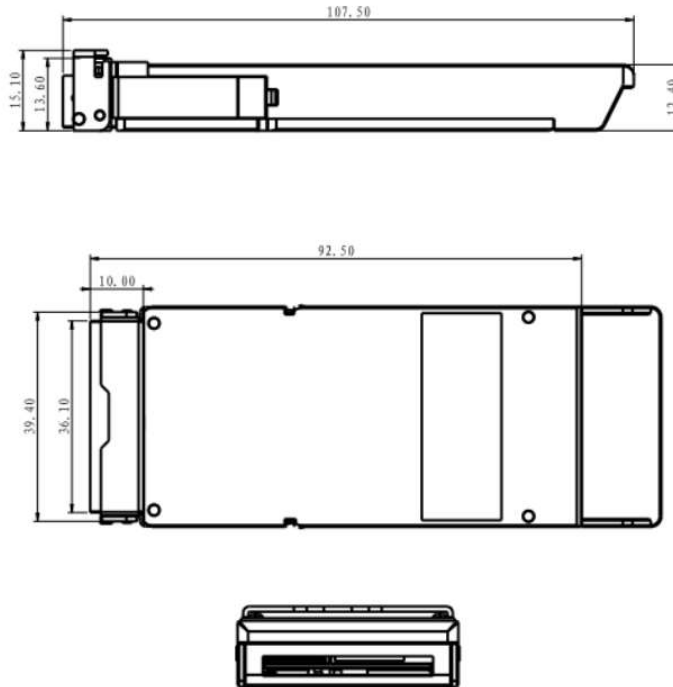
Average Launch Power per Lane	Peach		-2.5	—	2.9	dBm
Optical Modulation Amplitude per Lane	OMA		-1.2	—	4.5	dBm
Difference in Launch power between any two lanes(OMA)			—	—	5.0	dB
Average Launch Power of TX_DIS Transmitter per lane	Poff	TX_DIS=H	—	—	-30	dBm
Extinction Ratio	ER		7	—	—	dB
SMSR	SMSR		30			dB
Relative Intensity Noise	RIN	Mod off	—	—	-130	dB/Hz
Optical Return Loss Tolerance	T <sub>RL</sub>		—	—	20	dB
Transmitter reflectance	Tef		—	—	-26	dB
Optical Eye Mask {X1, X2, X3, Y1, Y2, Y3} <sup>1</sup>	EM	Test Points 20000	NRZ 25G RATIO {x1:0.25,x2:0.4,x3:0.45, y1:0.25,y2:0.28,y3:0.4}			
<b>Receiver</b>						
Channel data rate				27.9525		Gbps
Data rate variation			-20		+20	ppm
Lane Center Wavelength	λ <sub>CR0</sub>		1294.53	1295.56	1296.59	nm
	λ <sub>CR1</sub>		1299.02	1300.05	1301.09	nm
	λ <sub>CR2</sub>		1303.54	1304.58	1305.63	nm
	λ <sub>CR3</sub>		1308.09	1309.14	1310.19	nm
Damage threshold	P <sub>DT</sub>		—	5.5	—	dBm
Average receiver power per lane	Rpow		-8.8	—	2.9	dBm
Average total input power					8.9	dBm

Channel power difference					5.5	dB
Optical path penalty					1.5	dB
Receiver Sensitivity per lane <sup>2</sup>	Psen		—	—	-10.3	dBm
Receiver Reflectance	Ref		—	—	-26	dB
Rx-Lane LOS Assert			-13.6	—	—	dBm
Rx-Lane LOS Deassert			—	—	-12	dBm
Rx-Lane LOS Hysteresis			0.5	—	—	dB

**Function Diagram**

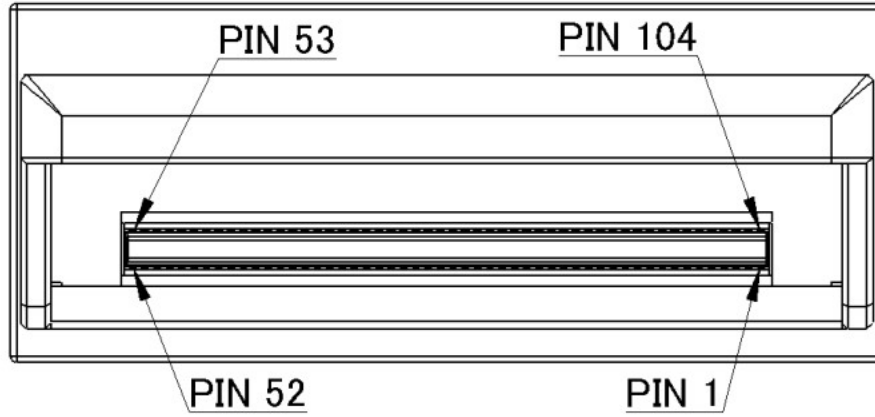


**Mechanical Dimension**

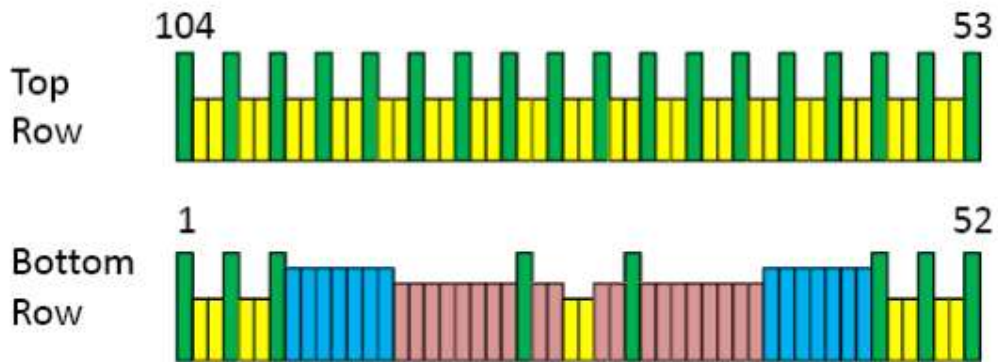


(unit mm)

**Pin Assignment and Description**



CFP2 Connector Pin Map Orientation



CFP2 Pin Map Connector

Bottom (Nx25G)		Top (4x25G)		Top (8x25G)	
1	GND	104	GND		GND
2	(TX_MCLKn)	103	N.C.		TX1n
3	(TX_MCLKp)	102	N.C.		TX7p
4	GND	101	GND		GND
5	N.C.	100	TX3n		TX6n
6	N.C.	99	TX3p		TX6p
7	3.3V_GND	98	GND		GND
8	3.3V_GND	97	TX2n		TX5n
9	3.3V	96	TX2p		TX5p
10	3.3V	95	GND		GND
11	3.3V	94	N.C.		TX4n
12	3.3V	93	N.C.		TX4p
13	3.3V_GND	92	GND		GND
14	3.3V_GND	91	N.C.		TX3n
15	VND_IO_A	90	N.C.		TX3p
16	VND_IO_B	89	GND		GND
17	PRG_CNTRL1	88	TX1n		TX2n
18	PRG_CNTRL2	87	TX1p		TX2p
19	PRG_CNTRL3	86	GND		GND
20	PRG_ALARM1	85	TX0n		TX1n
21	PRG_ALARM2	84	TX0p		TX1p
22	PRG_ALARM3	83	GND		GND
23	GND	82	N.C.		TX0n
24	TX_DIS	81	N.C.		TX0p
25	RX_LOS	80	GND		GND
26	MOD_LOPWR	79	(REFCLKn)	(REFCLKn)	
27	MOD_ABS	78	(REFCLKp)	(REFCLKp)	
28	MOD_RSTn	77	GND		GND
29	GLB_ALRMn	76	N.C.		RX7n
30	GND	75	N.C.		RX7p
31	MDIO	74	GND		GND
32	MDIO	73	RX3n		RX6n
33	PRTADR0	72	RX3p		RX6p
34	PRTADR1	71	GND		GND
35	PRTADR2	70	RX2n		RX5n
36	VND_IO_C	69	RX2p		RX5p
37	VND_IO_D	68	GND		GND
38	VND_IO_E	67	N.C.		RX4n
39	3.3V_GND	66	N.C.		RX4p
40	3.3V_GND	65	GND		GND
41	3.3V	64	N.C.		RX3n
42	3.3V	63	N.C.		RX3p
43	3.3V	62	GND		GND
44	3.3V	61	RX1n		RX2n
45	3.3V_GND	60	RX1p		RX2p
46	3.3V_GND	59	GND		GND
47	N.C.	58	RX0n		RX1n
48	N.C.	57	RX0p		RX1p
49	GND	56	GND		GND
50	(RX_MCLKn)	55	N.C.		RX0n
51	(RX_MCLKp)	54	N.C.		RX0p
52	GND	53	GND		GND

REFCLK  
(Optional)

### Pin Assignment

PIN	Name	I/O	Logic	Description
1	GND			
2	(TX_MCLKn)	O	CML	Not Support
3	(TX_MCLKp)	O	CML	Not Support
4	GND			
5	N.C.			No Connect
6	N.C.			No Connect
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V_GND			
9	3.3V			3.3V Module Supply Voltage
10	3.3V			3.3V Module Supply Voltage

11	3.3V			3.3V Module Supply Voltage
12	3.3V			3.3V Module Supply Voltage
13	3.3V_GND			
14	3.3V_GND			
15	VND_IO_A	I/O		Module Vendor I/O. Must No Connect at host board
16	VND_IO_B	I/O		Module Vendor I/O. Must No Connect at host board
17	PRG_CNTL1	I	LVC MOS w/ PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used 4.75kohm pull up in the module
18	PRG_CNTL2	I	LVC MOS w/ PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤3W, "01": ≤6W, "10": ≤9W, "11" or NC: ≤12W = not used 4.75kohm pull up in the module
19	PRG_CNTL3	I	LVC MOS w/ PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤3W, "01": ≤6W, "10": ≤9W, "11" or NC: ≤12W = not used 4.75kohm pull up in the module
20	PRG_ALRM1	O	LVC MOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up
21	PRG_ALRM2	O	LVC MOS	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready.
22	PRG_ALRM3	O	LVC MOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
23	GND			
24	TX_DIS	I	LVC MOS w/ PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled

25	RX_LOS	O	LVC MOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	MOD_LOPWR	I	LVC MOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled 4.75kohm pull up in the module
27	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVC MOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, 4.75kohm pull down in the module
29	GLB_ALRMn	O	LVC MOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	GND			
31	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
32	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			

40	3.3V_GND			
41	3.3V			3.3V Module Supply Voltage
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			
46	3.3V_GND			
47	N.C			No Connect
48	N.C			No Connect
49	GND			
50	(RX_MCLKn)	O	CML	Not Support
51	(RX_MCLKp)	O	CML	Not Support
52	GND			