Overview

Axiom Connectivity Digital Return SFPs are designed for superior flexibility and adaptability. By integrating numerous technical innovations, this Digital Return SFP Series ensures prolonged support for evolving network architectures.

1. Features

- Cooled CWDM EML transmitter with TEC
- Supports 9.8304 to 10.3125Gb/s bit rates
- PIN TIA Receiver
- Maximum link length of 40Km
- LC/UPC Duplex optical connector interface
- Power Consumption < 2.0W, Depending on Temperature
- Single 3.3V power supply
- Compliant to SFP+ MSA (SFF-8431 for electrical interface and SFF-8432 for mechanical interface)
- Hot-pluggable SFP+ footprint
- Digital Diagnostic Monitoring compliant
- RoHS-6 compliant

2. Applications

- 10GBASE 10G Ethernet
- Remote PHY

3. Regulatory Compliance

Items	**Standard**	Performance
Electrostatic Discharge (ESD)	IEC 61000-4-2	Class 1
Electromagnetic Interference (EMI)	FCC Part 15 Class B	Compliant with standards(FCC)
Electromagnetic Compatibility (EMC)	Directive 89/336/EEC	Compliant with standards(CE)
Laser Eye Safety	FDA 21 CFR 1040.10 and 1040.11 EN (IEC) 60825-1,2	Class 1 laser product.
RoHS	Directive 2011/65/EU	Compliant with RoHS

4. Absolute Maximum Ratings

Parameters	Symbol	Ratings	Units	Notes
Storage Temperature	Tst	-40 ~ 85	°C	-
Relative Humidity	RH	0 ~ 85	%	Non condensation
Transmitter differential input voltage	Vp	2.5	V	-
Power Supply Voltage	VccT, VccR	-0.5 ~ 4.0	V	-

5. Operating conditions

Parameters	Symbol	Min.	Max.	Units	Notes
Case operating temperature	TC	-40	85	°C	with Airflows
Module Supply Voltage	VccT, VccR	+3.135	+3.465	V	-
Total Power Consumption	PC	-	2.0	W	-
Power Supply Noise Tolerance	PSNT	-	66	mVpp	10 Hz to 10 MHz

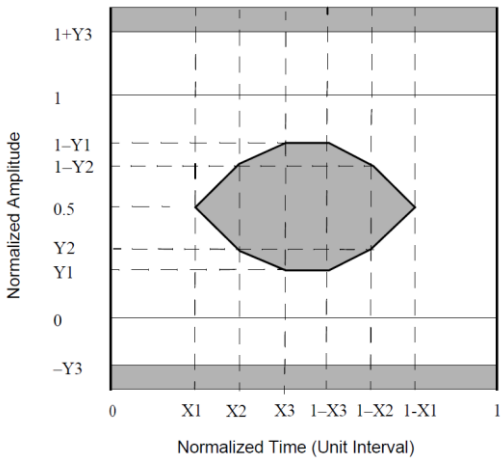

Figure 1. Transmitter optical Eye Mask Definition

Notes:

SFP+ module compliance points are defined as the following, SFF8431/Chapter3.3.2/Figure14:

- *B': SFP+ module transmitter input at the input of the Module Compliance Board.*
- *C': SFP+ module receiver output at the output of the Module Compliance Board.*

6. Optical Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Units	Notes
Transmitter						
Peak Wavelength	λ_p	1471, 1491, 1511, 1531, 1551, 1571, 1591, 1611			nm	@ λp ± 6.5nm
Center wavelength spacing	-	20			nm	-
Spectral Width@-20dB	$\Delta\lambda_{-20dB}$	-	-	0.30	nm	At -20dB
Side Mode Suppression Ratio	SMSR	30.0	-	-	dB	-
Average Optical Power	P_{ave}	+1.0	-	+5.0	dBm	-
Extinction Ratio	ER	8.2	-	-	dB	@10.3Gb/s, PRBS 2^{31} -1
Transmitter and dispersion penalty	DP	-	-	2.0	dB	-
Laser Off Power	P_{off}	-	-	-30.0	dBm	-
Relative intensity noise	$RIN_{12}OMA$	-	-	-128.0	dB/Hz	-
Transmitter Output Eye Mask	IEEE 802.3-2012 Clause 52.9.7					Figure 2 @ page3
Receiver						
Operating Wavelength	λ_o	1260	-	1620	nm	-
Receiver sensitivity (Average)	S	-	-	-15.0	dBm	Note 1
Receiver power(Pave) Overload	OL	-6.0	-	-	dBm	Note 1
Sensitivity(OMA)	S_{OMA}	-	-	-13.3	dBm	Note 1
Receiver Reflectance	R_R	-	-	-27.0	dB	@ λ_o
Loss of signal-Asserted	LOS_A	-29.0	-	-	dBm	Note 2
Loss of signal-De-asserted	LOS_D	-	-	-15.0	dBm	Note 2
Loss of signal Hysteresis	LOS_{D-A}	0.5	2.5	5.0	dB	-

Notes:

1. *Measured with at 10.3125Gb/s, Source ER>8.2dB, PRBS 2^{31} -1, BER<10^{-12}*
2. *Loss of Signal (LOS) detection responds only to OMA and the indicator will respond unpredictably with the application of un-modulated optical*

7. Low Speed Signal Electrical Characteristics

Parameters	Symbol	Min.	Max.	Units	Notes
Tx_Fault, Rx_LOS	V_{OL}	-0.3	0.4	V	At 0.7mA
	I_{OH}	-50	37.5	µA	Note 1
Tx_Disable, RS0, RS1	V_{IL}	-0.3	0.8	V	Note 2
	V_{IH}	2.0	VccT + 0.3	V	Note 2

Notes:

1. Measured with a 4.7kΩ load pull up to Vcc_Host
2. Tx Disable has an internal 4.7kΩ to 10kΩ pull up to VccT

8. Low Speed Signals Timing Specifications

Parameters	Symbol	Min.	Max.	Units	Notes
Tx Disable assert time	t_off	-	100	µs	Note 1
Tx Disable negate time	t_on	-	2	ms	Note 2
Time to initialize. Cold and warm start time	t_start_up	-	90	s	Note 3, Cooled type
Rx LOS assert delay	t_los_on	-	100	µs	Note 4
Rx LOS negate delay	t_los_off	-	100	µs	Note 5
Tx Fault Assert	Tx_fault_on	-	1	ms	Note 6
Tx Fault Reset	t_reset	10	-	µs	Note 7

Notes:

1. *Rising edge of Tx_Disable to fall of output signal below 10% of nominal*
2. *Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery*
3. *Time from power on or falling edge of Tx_Disable to when the modulated optical output rises above 90% of nominal and the Two-Wire interface is available*
4. *From occurrence of loss of signal to assertion of Rx_LOS*
5. *From occurrence of presence of signal to negation of Rx_LOS*
6. *From occurrence of fault to assertion of Tx_Fault*
7. *Time Tx_Disable must be held high to reset Tx_Fault*

9. High Speed Signal Electrical Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Units	Notes
Module Transmitter Input Electrical Specifications at B '						
Tx Input Differential Voltage	V_I	190	-	700	mV	Note 1
Differential Input Resistance	R_I	95	100	105	ohm	-
Differential Input S-parameter (Note 2)	SDD11	-	-	Note 3	dB	0.01to 4.1 GHz
		-	-	Note 4	dB	4.1 to 11.1 GHz
Reflected Differential to Common Mode Conversion	SCD11	-	-	-10	dB	0.01 to 11.1GHz
Module Receiver Output Electriacl Specifications at C '						
Rx Output Differential Voltage	V_o	300	-	850	mV	Note 1
Termination Mismatch at 1 MHz	ΔZM	-	-	5	%	-
Single Ended Output Voltage Tolerance	-	-0.3	-	4.0	V	-
Output AC Common Mode Voltage	-	-	-	7.5	mV	RMS, Note 5
Differential Output S-parameter	SDD22	-	-	Note 6	dB	0.01 to 4.1 GHz
		-	-	Note 7	dB	4.1 to 11.1 GHz
Common Mode Output Reflection Coefficient	SCC22	-	-	Note 8	dB	0.01 to 2.5 GHz
		-	-	-3	dB	2.5 to 11.1 GHz
Rx Output Rise and Fall Time	tr, tf	28	-	-	ps	20% to 80%
Rx Output Total Jitter	T_J	-	-	0.70	Ulp-p	-
Rx Output Deterministic Jitter	D_J	-	-	0.42	Ulp-p	-

Notes:

1. *Voltage swing for 1G operation is equivalent to voltage swing in 10G operation (SFF-8431 Rev 3.0).*
2. *Measured at B" with Host Compliance Board and Module Compliance Board pair.*
3. *Reflection Coefficient given by equation SDD11 (dB) < -12 + 2 × SQRT (f), with f in GHz.*
4. *Reflection Coefficient given by equation SDD11 (dB) < -6.3 + 13 × log10 (f/5.5), with f in GHz.*
5. *The RMS value is measured by calculating the standard deviation of the histogram for one UI of the common mode signal.*
6. *Reflection Coefficient given by equation SDD22 (dB) < -12 + 2 × SQRT (f), with f in GHz.*
7. *Reflection Coefficient given by equation SDD22 (dB) < -6.3 + 13 × log10 (f/5.5), with f in GHz.*
8. *Reflection Coefficient given by equation SCC22 (dB) < -7 + 1.6 × f, with f in GHz.*

10. Pin Information

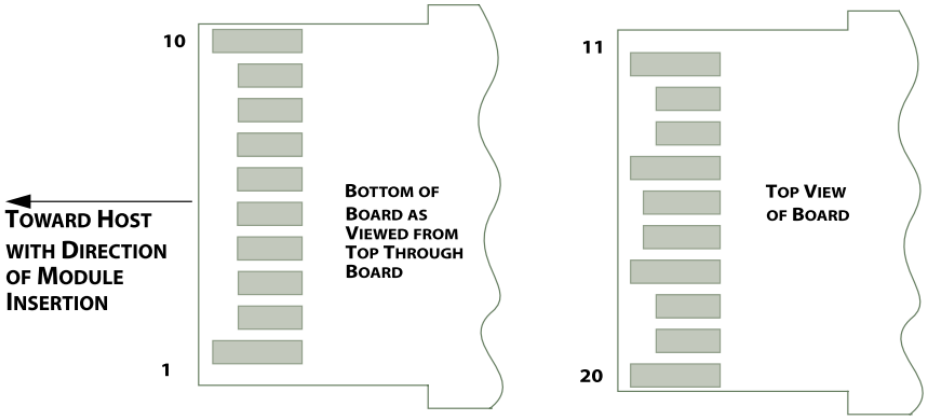

Figure 2-1. SFP+ Transceiver Electrical Pad Layout

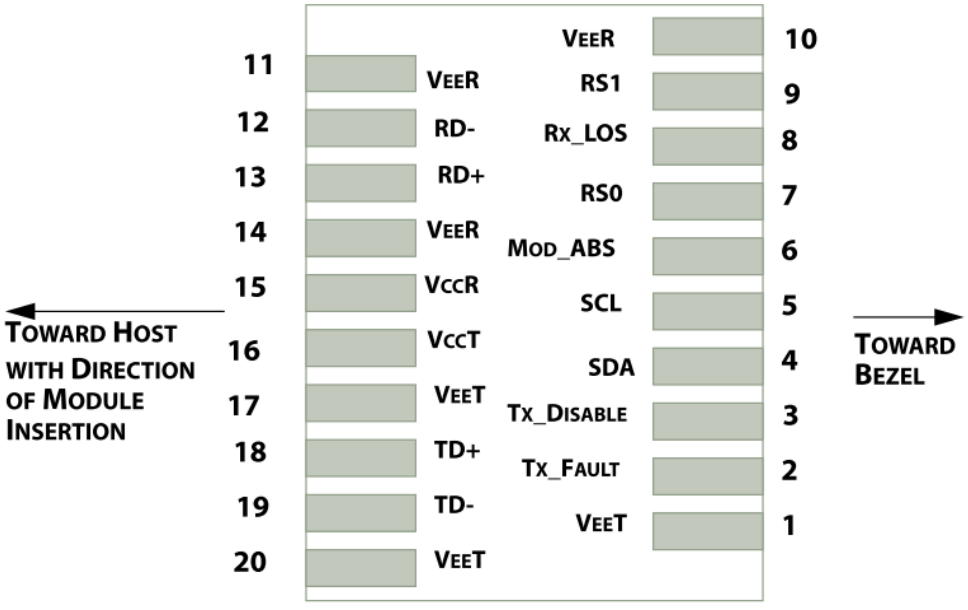

Figure 2-2. 20-pin Host PCB SFP+ pad assignment top view

Pin No.	Symbol	Descriptions	Sequence	Notes
1	VeeT	Transmitter Signal Ground	1st	-
2	Tx_Fault	Transmitter Fault (LVTTL-O) – High indicates a fault condition	3rd	Note 1
3	Tx_Disable	Transmitter Disable (LVTTL-I) – High or open disables the transmitter	3rd	Note 2
4	SDA	Two Wire Serial Interface Data Line (LVCMOS – I/O) (same as MOD-DEF2 in INF-8074)	3rd	Note 3
5	SCL	Two Wire Serial Interface Clock Line (LVCMOS – I/O) (same as MOD-DEF1 in INF-8074)	3rd	Note 3
6	MOD-ABS	Module Absent, (controlled by module)	3rd	Note 4
7	RS0	Receiver Rate Select 0 - not used(Internally pull-down, 51kohm)	3rd	-
8	RX_LOS	Receiver Loss of Signal Indication (LVTTL-O)	3rd	Note 1
9	RS1	Transmitter Rate Select 1 - not used(Internally pull-down, 51kohm)	3rd	-
10	VeeR	Receiver Signal Ground	1st	-
11	VeeR	Receiver Signal Ground	1st	-
12	RD-	Receiver Data Output, Inverted (CML-O)	3rd	-
13	RD+	Receiver Data Output, Non-Inverted (CML-O)	3rd	-
14	VeeR	Receiver Signal Ground	1st	-
15	VccR	Receiver Power + 3.3 V	2nd	-
16	VccT	Transmitter Power + 3.3 V	2nd	-
17	VeeT	Transmitter Signal Ground	1st	-
18	TD+	Transmitter Data Input, Non-Inverted Data (CML-I)	3rd	-
19	TD-	Transmitter Data Input, Inverted (CML-I)	3rd	-
20	VeeT	Transmitter Signal Ground	1st	-

Notes:

1. *This is an open drain output that on the host board requires a 4.7kΩ to 10kΩ pull-up resistor to Vcc_Host.*
2. *This input is internally biased high with a 4.7kΩ to 10kΩ pull-up resistor to VccT.*
3. *Two-Wire Serial interface clock and data lines require an external pull-up resistor dependent on the capacitance load.*
4. *They must be pulled up with a 4.7kΩ to 10 kΩ resistor on the host board. MOD-ABS is grounded by the module to indicate the module is present*

11. Recommended application schematic

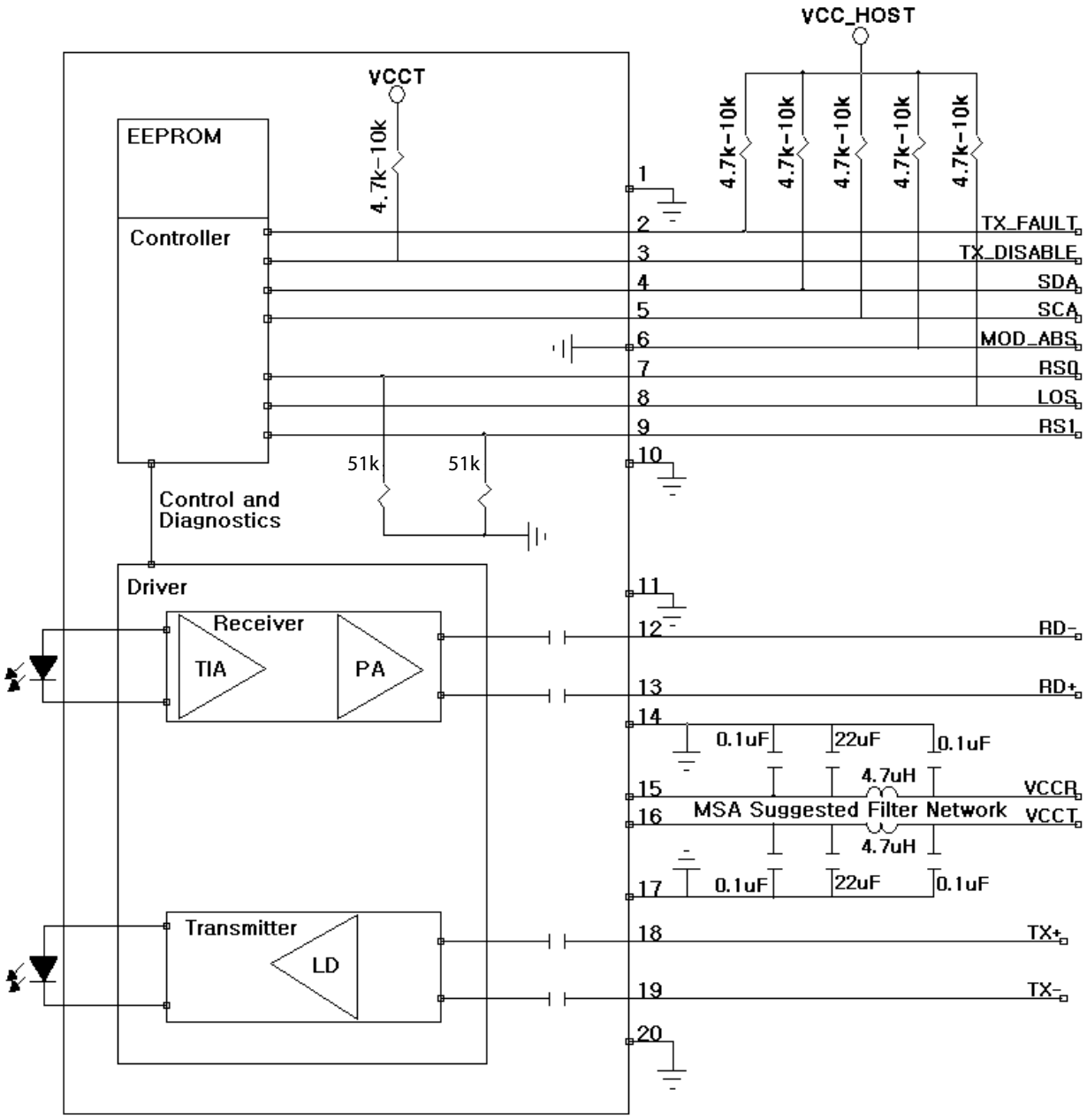

Figure 3. Recommended application schematic

Notes:

1. *Tx_Disable : Transmitter Disable, logic high, open drain compatible, 4.7k to 10kohm pull up to Vcc on module*
2. *Tx_Fault : Transmitter Fault, logic high, open drain compatible, 4.7k to 10kohm pull up to Vcc on Host*
3. *Rx_LOS : Receiver Loss of Signal, logic high, open drain compatible, 4.7k to 10kohm pull up to Vcc on Host*

12. 2-Wire Interface Electrical Specifications

Parameters	Symbol	Min.	Max.	Units	Notes
Host 2-Wire Vcc	Vcch	3.14	3.46	V	Note 1
SCL and SDA	V_{OL}	0.0	0.8	V	R_P pulled to VccT/R, Note 2
	V_{OH}	Vcch-0.5	Vcch+0.3	V	
SCL and SDA	V_{IL}	-0.3	VccT*0.3	V	Note 3
	V_{IH}	VccT*0.7	VccT+0.5	V	
Input Current on the SCL and SDA Contacts	I_I	-10	10	µA	-
Capacitance on SCL and SDA contacts	C_i	-	14	pF	Note 4
Total bus capacitance for SCL and SDA	C_b[5]	-	100	pF	At 400kHz, 3.0kΩ Rp, max At 100kHz, 8.0kΩ Rp, max
		-	290	pF	At 400kHz, 1.1kΩ Rp, max At 100kHz, 2.75kΩ Rp, max

Notes:

1. *The Host 2-wire Vcc is the voltage used for resistive pull ups for the 2 wire interface*
2. *Rp is the pull up resistor. Active bus termination may be used by the host in place of a pull up resistor. Pull ups can be connected to any one of several power supplies, however the host board design shall ensure that no module contact has voltage exceeding module VccT/R + 0.5 V nor requires the module to sink more than 3.0mA current.*
3. *These voltages are measured on the other side of the connector to the device under test.*
4. *Ci is the capacitance looking into the module SCL and SDA contacts.0*
5. *Cb is the total bus capacitance on the SCL or SDA bus.*

13. 2-Wire Timing Specifications

Parameters	Symbol	Min.	Max.	Units	Notes
Clock Frequency	f_{SCL}	0	400	kHz	Note 1
Clock Pulse Width Low	t_{LOW}	1.3	-	µs	-
Clock Pulse Width High	t_{HIGH}	0.6	-	µs	-
Stop to Start Time	t_{BUF}	20	-	µs	Note 2
Start Hold Time	$t_{HD,STA}$	0.6	-	µs	-
Start Set-up Time	$t_{SU,STA}$	0.6	-	µs	-
Data In Hold Time	$t_{HD,DAT}$	0	-	µs	-
Data In Set-up Time	$t_{SU,DAT}$	0.1	-	µs	-
Input Rise Time (100kHz)	$t_{R,100}$	-	1000	ns	Note 3
Input Rise Time (400kHz)	$t_{R,400}$	-	300	ns	Note 3
Input Fall Time (100kHz)	$t_{F,100}$	-	300	ns	Note 4
Input Fall Time (400kHz)	$t_{F,400}$	-	300	ns	Note 4
Stop Set-up Time	$t_{SU,STO}$	0.6	-	µs	-
Serial Interface Clock Holdoff "Clock Stretching"	t_clock_hold	-	500	µs	Note 5

Notes:

1. *Module shall operate with f_{SCL} up to 100 kHz without requiring clock stretching. The module may clock stretch with f_{SCL} greater than 100 kHz and up to 400 kHz.*
2. *Between STOP and START and between ACK and Re-START.*
3. *From (V_{IL},MAX - 0.15) to (V_{IH},MIN + 0.15)*
4. *From (V_{IH},MIN + 0.15) to (V_{IL},MAX - 0.15)*
5. *Maximum time the module may hold the SCL line low before continuing with a read or write operation.*

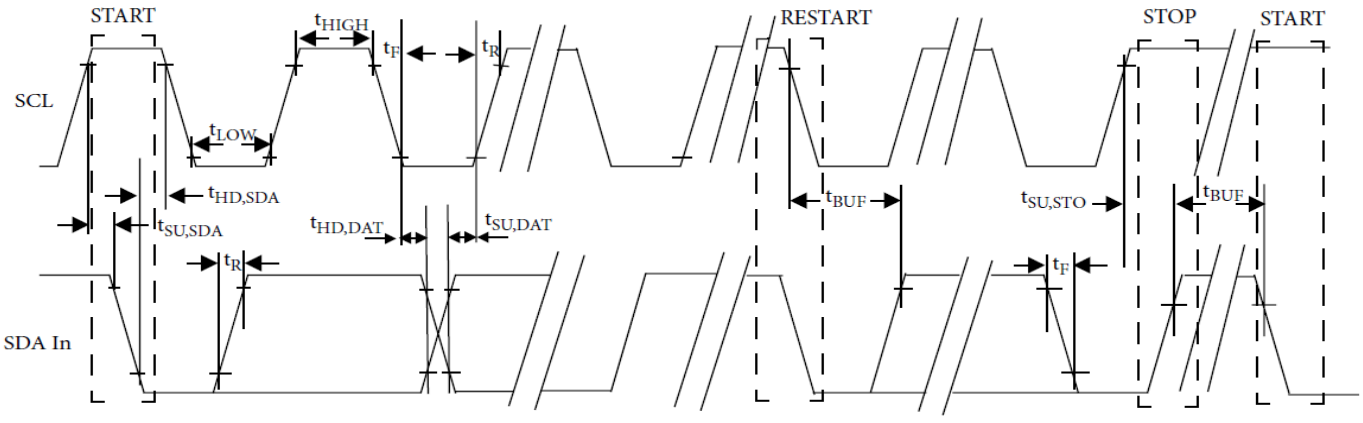

Figure 4. 2-Wire Bus Timing Diagram

14. Package Description & Outline Diagram

* Unit: [mm]

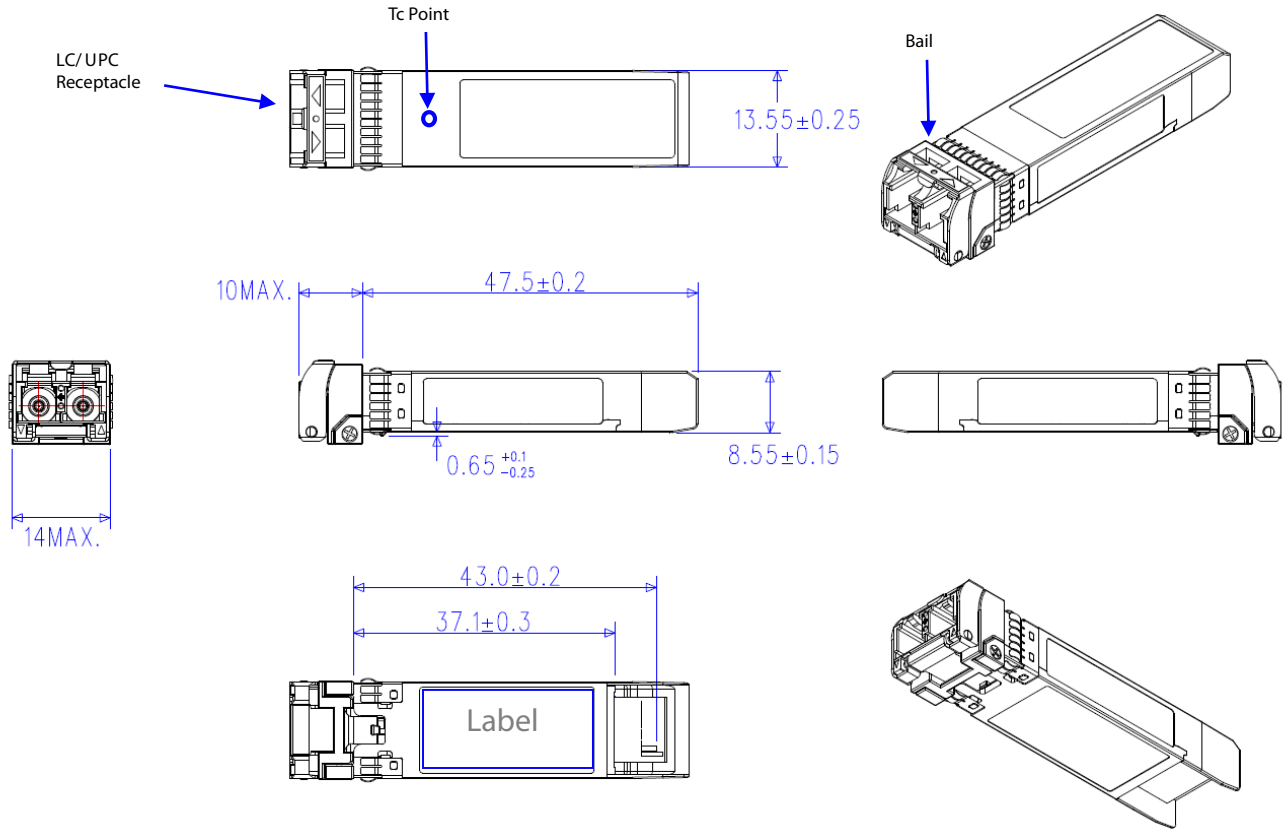

Figure 5. Package outline diagram and example

*** Part number information**

Part No	Wavelength [nm]
AC-E-DR10TC40-I27-yy	1271
AC-E-DR10TC40-I29-yy	1291
AC-E-DR10TC40-I31-yy	1311
AC-E-DR10TC40-I33-yy	1331
AC-E-DR10TC40-I35-yy	1351
AC-E-DR10TC40-I37-yy	1371
AC-E-DR10TC40-I39-yy	1391
AC-E-DR10TC40-I41-yy	1411
AC-E-DR10TC40-I43-yy	1431
AC-E-DR10TC40-I45-yy	1451
AC-E-DR10TC40-I47-yy	1471
AC-E-DR10TC40-I49-yy	1491
AC-E-DR10TC40-I51-yy	1511
AC-E-DR10TC40-I53-yy	1531
AC-E-DR10TC40-I55-yy	1551
AC-E-DR10TC40-I57-yy	1571
AC-E-DR10TC40-I59-yy	1591
AC-E-DR10TC40-I61-yy	1611