64Mbit ADMUX CellularRAM Data Sheet

CSA6416SB-FI-A1

Version: 1

Table of Contents

1. Feature

Fully compliant to CellularRAM 1.5 Specification

Single device supports asynchronous and burst operations

VCC, VCCQ voltages:

- 1.7V–1.95V VCC
- 1.7V–1.95V VCCQ

Random access time: 70ns

Burst mode READ and WRITE access:

- 4, 8, 16, or 32 words, or continuous burst
- Burst wrap sequential

Max clock rate: 133 MHz (^{t}CLK = 7.5ns)

Burst initial latency: 37.5ns (5 clocks) at 133 MHz

^{t}ACLK: 5.5ns at 133 MHz

Low power consumption:

- Asynchronous READ: <25mA
- Initial access, burst READ: (39ns [4 clocks] at 109 MHz)<35mA

Continuous burst READ: <30mA

Low-power features

On-chip temperature compensated refresh (TCR)

Partial array refresh (PAR)

Frequency:

- 83Mhz, 109Mhz, 133Mhz

Timing: 70ns access

2. Description

CellularRAM™ products are high-speed, CMOS pseudo-static random-access memory developed for low-power, portable applications. This CSA6416SB-FI-A1 64Mb device has a DRAM core organized as 4 Meg x 16 bits. This device includes an industry-standard burst mode Flash interface that dramatically increases read/write bandwidth compared with other low-power SRAM or Pseudo SRAM offerings.

To operate seamlessly on a burst Flash bus, CellularRAM products incorporate a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device READ/WRITE performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array.

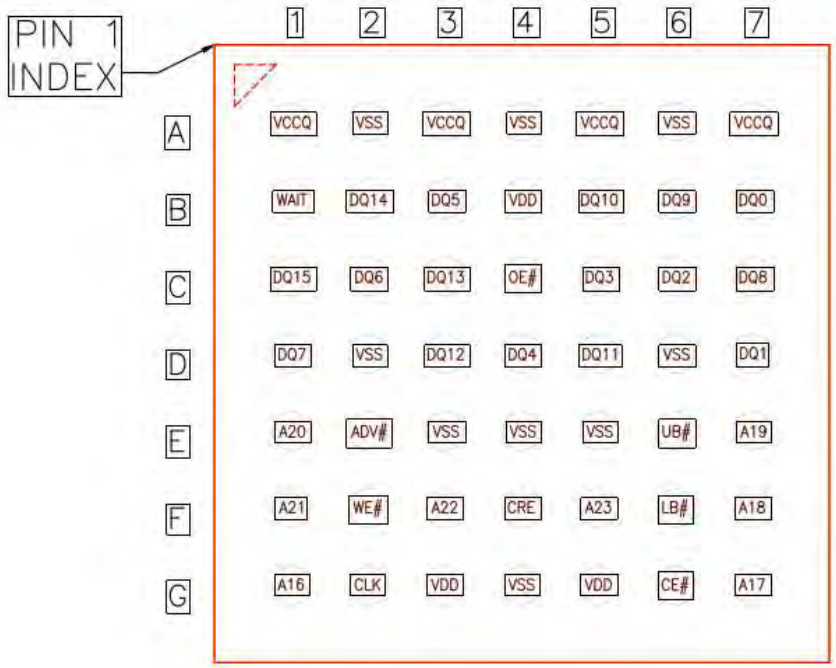
These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three mechanisms to minimize standby current. Partial array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data. Temperature compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature—the refresh rate decreases at lower temperatures to minimize current consumption during standby. The system configurable refresh mechanisms are accessed through the RCR.

This CellularRAM device is compliant with the industry standard CellularRAM 1.5 feature set established by the CellularRAM Workgroup. It includes support for both variable and fixed latency, with three output-device drive-strength settings, additional wrap options, and a device ID register (DIDR)

3. Package Information

Ball Assignment for 49b MINIBGA (general diagram for 64Mb to 256Mb)



Top View Through Package

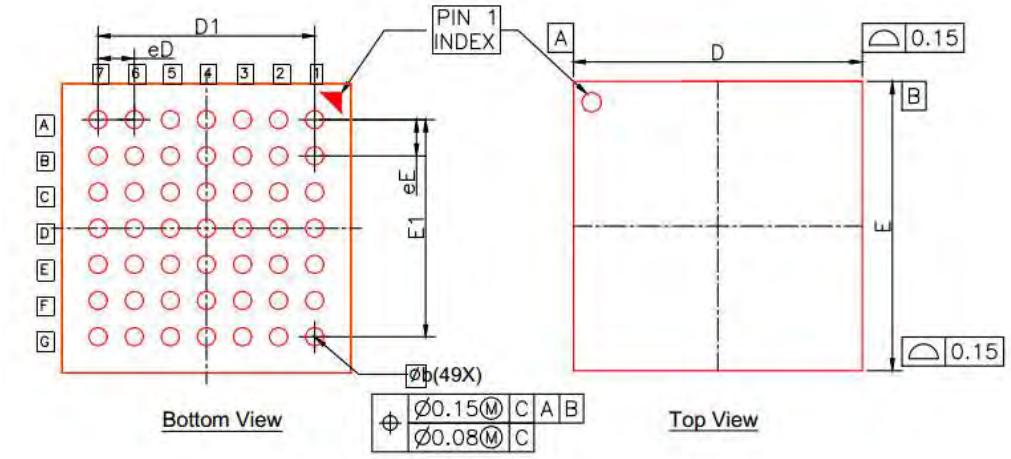
(4x4x0.8mm)(P0.5)(B0.25)

For 64Mb, Pin of 3F “A22” is defined as NC, and pin of 5F “A23” is defined as NC.

Special note: CSA6416SB-FI-A1, pin of 5F “A23” is defined as “VDD” or always pull “high”

3.1 Package Outline Drawing

- 49b FBGA, 4x4x0.8max, 0.5mm pitch, 0.25mm size

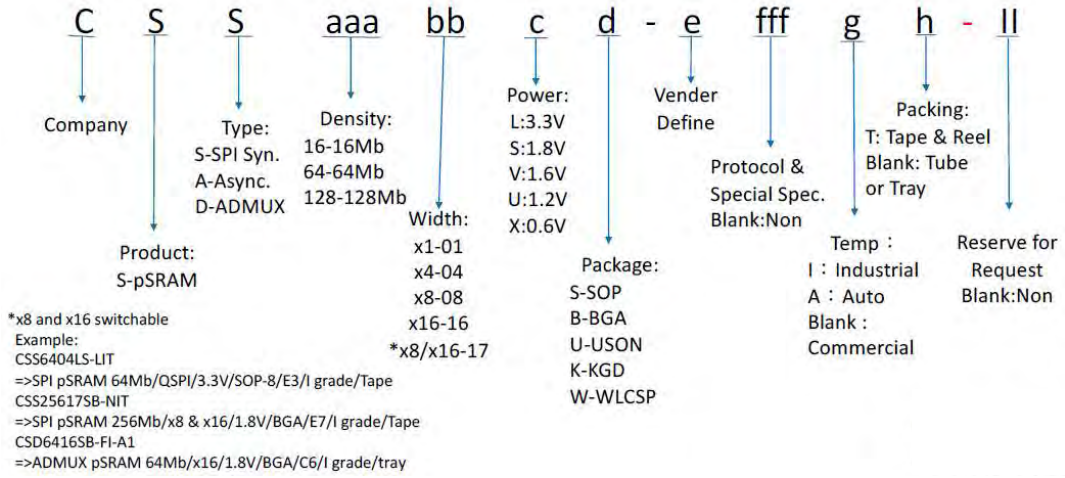


Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.60	0.70	0.80
A1	0.13	0.18	0.23
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D1		3.00 BSC	
E1		3.00 BSC	
eD		0.50 BSC	
eE		0.50 BSC	

NOTE:
1. SCALE 1:3
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. THE PATTERN OF PIN1 FIDUCIAL IS FOR REFERANCE ONLY

4. Ordering Information

Product Naming Rule:



4.1 Part Number:

Part Number	Density	Amax	Temperature	Note
CSA6416SB-FI-A1	64Mb	A21	-25°C to +85°C	49B

5. Package Ball Signal Table

Table 1 Signals Table

Symbol	Type	Description	Comments
VDD	Power	Core supply 1.8V	
VDDQ/VCCQ	Power	IO supply 1.8V	
VSS	Ground	Core supply ground	
VSSQ	Ground	IO supply ground	
A/DQ[15:0]	IO	Address/DQ bus [15:0]	
A[max:16]	Input	Address [max:16] 64M: max = 21	
LB#	Input	Lower byte select, active low. In Advanced PSRAM write, it's data-mask for lower byte, active high. DML=1 means "do not write".	
UB#	Input	Upper byte select, active low. In Advanced PSRAM write, it's data-mask for upper byte, active high. DMH=1 means "do not write".	
CE#	Input	Chip select, active low.	
WE#	Input	Write enable, active low.	
ADV#	Input	Address-Data-Valid, active low. When ADV# is low, A/DQ is used to input address.	
CLK	Input	Clock.	
OE#	Input	Output enable, active low.	
WAIT	Output	Wait signal indicating the cycle's data is valid.	
CRE	Input	Control register select	Optional

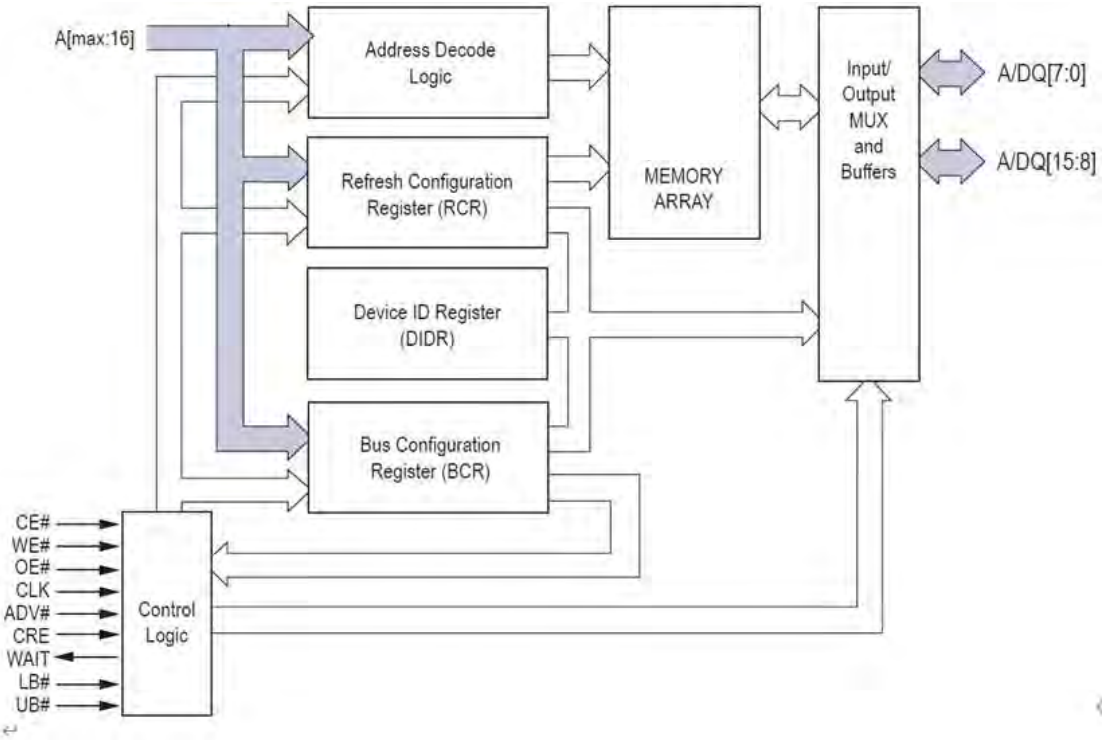
Table 2: Bus Operations

Asynchronous Mode BCR[15] = 1	Power	CLK[1]	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT[2]	A/DQ[15:0][3]	Notes
Read	Active	L		L	L	H	L	L	Low-Z	Data out	4
Write	Active	L		L	X	L	L	L	High-Z	Data in	4
Standby	Standby	L	X	H	X	X	L	X	High-Z	High-Z	5, 6
No operation	Idle	L	X	L	X	X	L	X	Low-Z	X	4, 6
Configuration register write	Active	L		L	H	L	H	X	Low-Z	High-Z	
Configuration register read	Active	L		L	L	H	H	L	Low-Z	Config. reg. out	
Burst mode BCR[15] = 0	**Power**	**CLK[1]**	**ADV#**	**CE#**	**OE#**	**WE#**	**CRE**	**LB#/ UB#**	**WAIT[2]**	**A/DQ[15:0][3]**	**Notes**
Async read	Active	H or L		L	L	H	L	L	Low-Z	Data out	4, 7
Async write	Active	H or L		L	X	L	L	L	High-Z	Data in	4
Standby	Standby	H or L	X	H	X	X	L	X	High-Z	High-Z	5, 6
No operation	Idle	H or L	X	L	X	X	L	X	Low-Z	X	4, 6
Initial burst read	Active		L	L	X	H	L	L	Low-Z	Address	4, 8
Initial burst write	Active		L	L	H	L	L	X	Low-Z	Address	4, 8
Burst continue	Active		H	L	X	X	X	L	Low-Z	Data in or Data out	4, 8
Burst suspend	Active	X	X	L	H	X	X	X	Low-Z	High-Z	4, 8
Configuration register write	Active		L	L	H	L	H	X	Low-Z	High-Z	8, 9
Configuration register read	Active		L	L	L	H	H	L	Low-Z	Config. reg. out	8, 9

Notes:

1. CLK must be static (HIGH or LOW) during async read and async write modes; and to achieve standby power during standby mode. CLK must be static (HIGH or LOW) during burst suspend.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. VIN = VCCQ or 0V; all device inputs must be static (unswitched) in order to achieve standby current.
7. When the BCR is configured for sync mode, sync READ and WRITE, and async WRITE are supported by all vendors. Cascadeteq devices also support asynchronous READ.
8. Burst mode operation is initialized through the bus configuration register (BCR[15]).
9. Initial cycle. Following cycles are the same as BURST CONTINUE. CE# must stay LOW for the equivalent of a single word burst (as indicated by WAIT).

6. Function Diagram

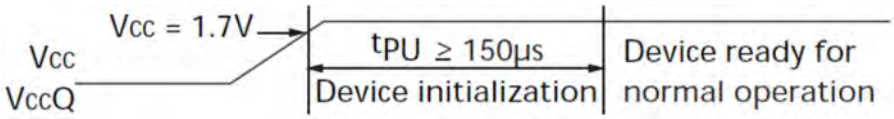


7. Powerup Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings. (See Figure 14 and Figure 18) VCC and VCCQ must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150µs to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

7.1 Powerup Initialization Timing

Figure 1



8. Bus Operating Mode

CellularRAM products incorporate a burst mode interface found on Flash products targeting low power, wireless applications. This bus interface supports asynchronous and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the BCR.

8.1 Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry standard SRAM control bus (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 2) are initiated by bringing CE#, ADV#, and LB#/UB# LOW while keeping OE# and WE# HIGH, and driving the address onto the A/DQ bus. ADV# is taken HIGH to capture the address, and OE# is taken LOW. Valid data will be driven out of the I/Os after the specified access time has elapsed.

WRITE operations (Figure 3) occur when CE#, ADV#, WE#, and LB#/UB# are driven LOW with the address on the A/DQ bus. ADV# is taken HIGH to capture the address, then the WRITE data is driven onto the bus. During asynchronous WRITE operations, the OE# level is a "Don't Care," and WE# will override OE#; however, OE# must be HIGH while the address is driven onto the A/DQ bus. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first).

During asynchronous operation, the CLK input must be held static (HIGH or LOW). WAIT will be driven while the device is enabled and its state should be ignored. WE# LOW time must be limited to ^{t}CEM.

Figure 2 READ Operation (ADV# LOW)

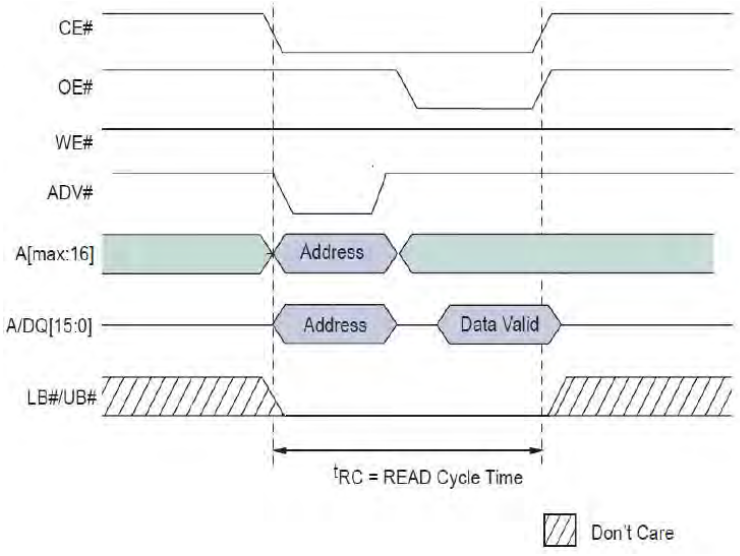
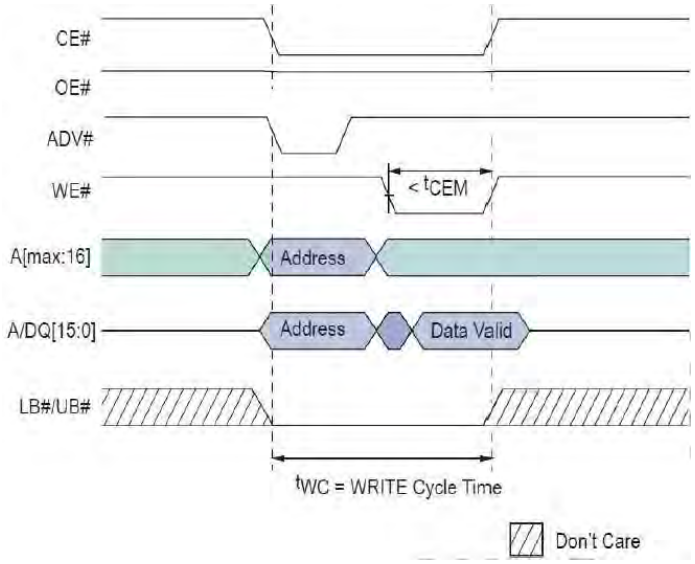


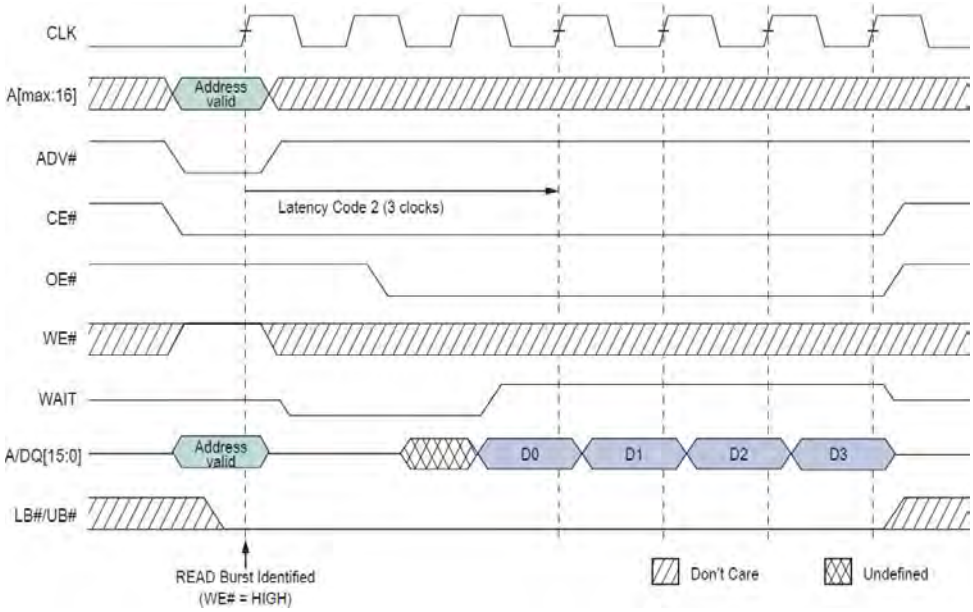
Figure 3 WRITE Operation



8.2 Burst Mode Operation

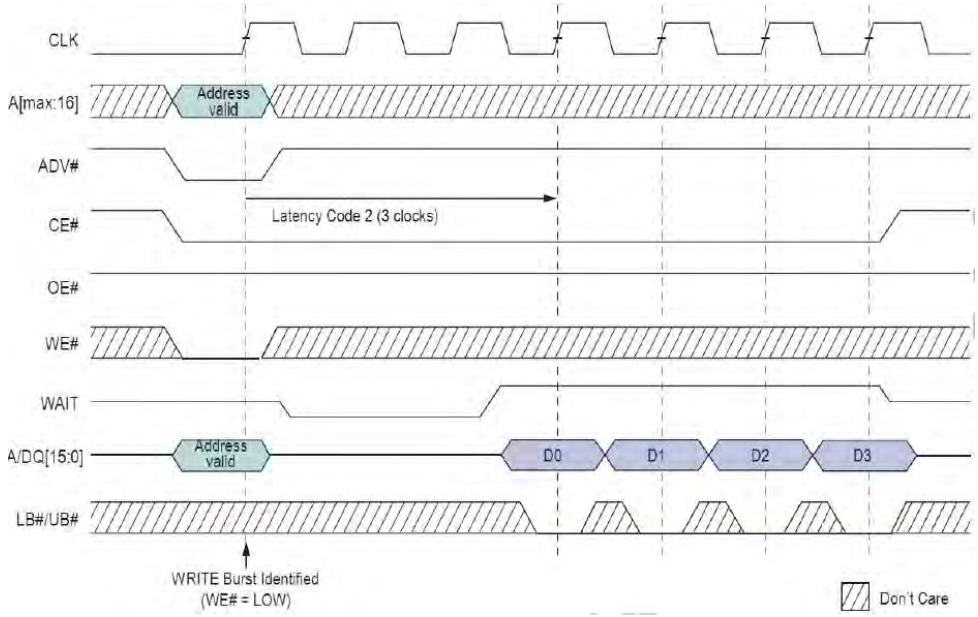
Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to access is latched on the rising edge of the next clock that ADV# is LOW. During this first clock rising edge, WE# indicates whether the operation is going to be a READ (WE# = HIGH, Figure 4) or WRITE (WE# = LOW, Figure 5)

Figure 4 Burst Mode READ (4-word burst)



Note:
Non-default BCR settings for burst mode READ (4-word burst): Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay. Diagram in Figure 4 is representative of variable latency with no refresh collision or fixed-latency access.

Figure 5 Burst Mode-WRITE (4-word burst)



Note:
Non-default BCR settings for burst mode WRITE (4-word burst): Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

The size of a burst can be specified in the BCR either as a fixed length or continuous. Fixed-length bursts consist of four, eight, sixteen, or thirty-two words. Continuous bursts have the ability to start at a specified address and burst to the end of the row.

The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and CellularRAM device. The initial latency for READ operations can be configured as fixed or variable (WRITE operations always use fixed latency). Variable latency allows the CellularRAM to be configured for minimum latency at high clock frequencies, but the controller must monitor WAIT to detect any conflict with refresh cycles.

Fixed latency outputs the first data word after the worst-case access delay, including allowance for refresh collisions. The initial latency time and clock speed determine the latency count setting.

Fixed latency is used when the controller cannot monitor WAIT. Fixed latency also provides improved performance at lower clock frequencies.

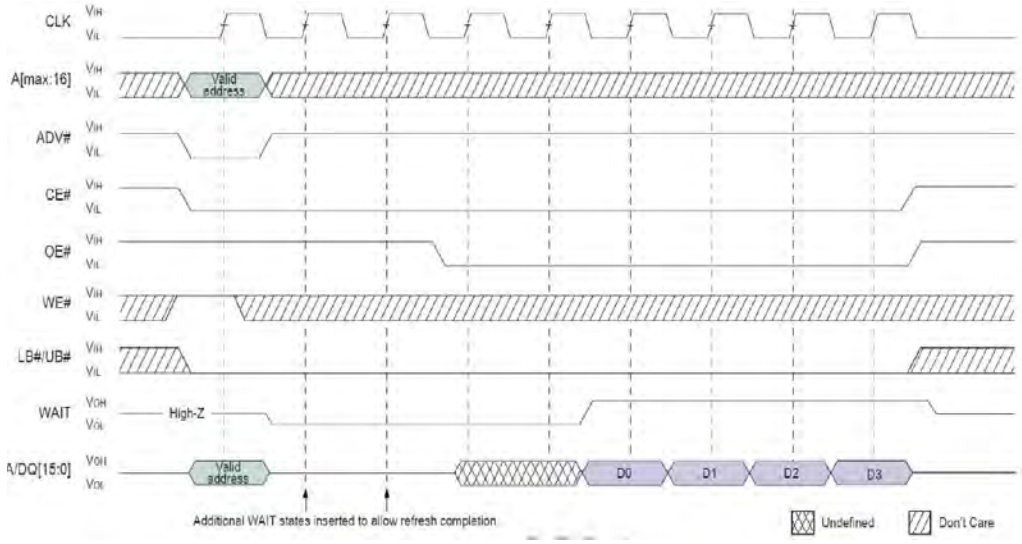
The WAIT output asserts when a burst is initiated, and de-asserts to indicate when data is to be transferred into (or out of) the memory. WAIT will again be asserted at the boundary of the row, unless wrapping within the burst length.

To access other devices on the same bus without the timing penalty of the initial latency for a new burst, burst mode can be suspended. Bursts are suspended by stopping CLK. CLK can be stopped HIGH or LOW. If another device will use the data bus while the burst is suspended, OE# should be taken HIGH to disable the CellularRAM outputs; otherwise,

OE# can remain LOW. Note that the WAIT output will continue to be active, and as a result no other devices should directly share the WAIT connection to the controller. To continue the burst sequence, OE# is taken LOW, then CLK is restarted after valid data is available on the bus.

The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than tCEM. If a burst suspension will cause CE# to remain LOW for longer than tCEM, CE# should be taken HIGH and the burst restarted with a new CE# LOW/ADV# LOW cycle.

Figure 6 Refresh Collision During Variable-Latency READ Operation



Note
Non-default BCR settings for refresh collision during variable-latency READ operation: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

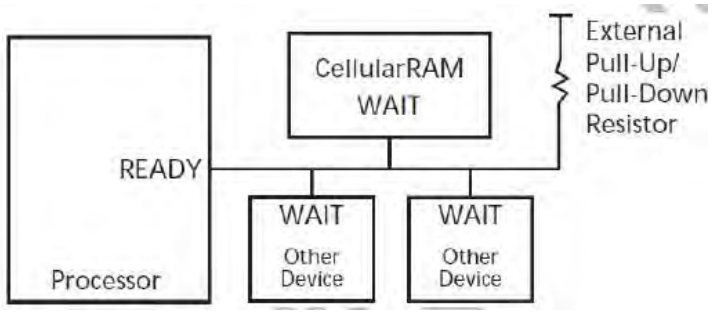
8.3 Mixed-Mode Operation

The device supports a combination of synchronous READ and asynchronous WRITE operations when the BCR is configured for synchronous operation. (Cascadeteq devices also support asynchronous READ.) The asynchronous WRITE operations require that the clock (CLK) remain static (HIGH or LOW) during the entire sequence. The ADV# signal latches the target address. CE# can remain LOW when transitioning between mixed-mode operations with fixed latency enabled; how- ever, the CE# LOW time must not exceed tCEM. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers. See Figure 36 for the “Asynchronous WRITE Followed by Burst READ” timing diagram.

8.4 WAIT Operation

The WAIT output on a CellularRAM device is typically connected to a shared, system-level WAIT signal. (See below Figure 7) The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

Figure 7 Wired or WAIT Configuration



When a READ or WRITE operation has been initiated, WAIT goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the CellularRAM device.

When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.

During a burst cycle, CE# must remain asserted until the first data is valid. Bringing CE# HIGH during this initial latency may cause data corruption.

When using variable initial access latency (BCR[14] = 0), the WAIT output performs an arbitration role for READ operations launched while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed. (See Figure 6) When the refresh operation has completed, the READ operation will continue normally.

WAIT will be asserted but should be ignored during asynchronous READ and WRITE operations.

By using fixed initial latency (BCR[14] = 1), this CellularRAM device can be used in burst mode without monitoring the WAIT signal. However, WAIT can still be used to determine when valid data is available at the start of the burst and at the end of the row. If WAIT is not monitored, the controller must stop burst accesses at row boundaries on its own.

8.5 Row Boundary Crossing

CellularRAM 1.5 supports the Row Boundary Crossing (RBC) operation for both READ and WRITE bursts. Row Boundary Crossing is available for both Fixed Latency and Variable

Latency operations. Refresh may not be allowed during a Row Boundary Crossing, so tCEM must be observed.

The RBC operation is entered if the burst continues past the last column address of the row. For the Wrap-On (BCR[3]=0) setting, RBC is not accessible. Note that Cascadeteq CellularRAM has a Row Length of 256 bits, thus, the End of Row occurs at A[7:0] = FFh. The Row Length of the Cel- lularRAM can be obtained from a READ operation of the Device ID Register (DIDR[15]).

If the RAM is set to Wrap-Off (BCR[3] = 1) or Continuous Burst and a Row Boundary Crossing is not desired, care must be taken to properly terminate any burst at End of Row by deasserting CE#.

8.6 Row Boundary Crossing Latency

Row Boundary Crossing is facilitated by the WAIT pin, which asserts at the last data word of the current row, and then de-asserts when the first valid data of the new row is available (see Figure 29 and Figure 34). The assertion and de-assertion of WAIT relative to these data packets is controlled by the WAIT Configuration (BCR[8]).

The actual latency to cross the row boundary is a function of the initial latency type; variable latency (default) vs. fixed latency (IL = BCR[14]), latency count (LC = BCR[13:11]) and READ vs. WRITE burst, as shown in Table 3.

Table 3 Row Boundary Crossing Latency

Initial Latency	Burst Operation	NUMBER OF CYCLES WAIT IS ASSERTED (LC = BCR[13:11])
Variable	READ	LC+2
Variable	WRITE	LC+1
Fixed	READ	LC+1
Fixed	WRITE	LC+1

8.7 LB#/UB# Operation

The LB# enable and UB# enable signals support byte-wide data WRITEs. During WRITE operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first. LB# and UB# must be LOW during READ cycles.

When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

9. Low-Power Operation

9.1 Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is HIGH.

The device will enter a reduced power state upon completion of a READ or WRITE operation, or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

9.2 Temperature Compensated Refresh

Temperature compensated refresh (TCR) allows for adequate refresh at different temperatures. This CellularRAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The device continually adjusts the refresh rate to match that temperature.

9.3 Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map. (See Table 8) READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

10. Register

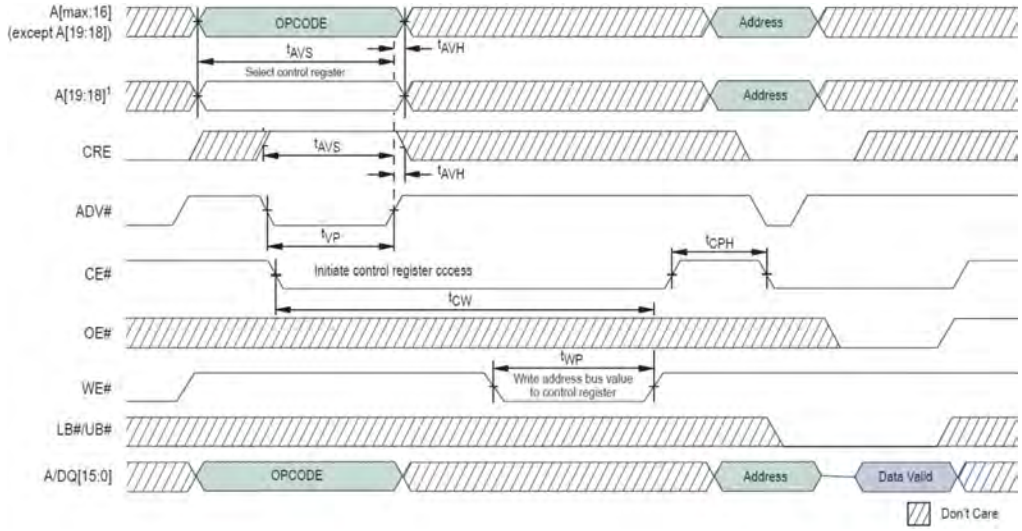
Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up, and can be updated any time the devices are operating in a standby state. A DIDR provides information on the device manufacturer, CellularRAM generation, and the specific device configuration. The DIDR is read-only.

10.1 Access Using CRE

The registers can be accessed using either a synchronous or an asynchronous operation when the control register enable (CRE) input is HIGH. (See Figures 8, 9, 10 and 11) When CRE is LOW, a READ or WRITE operation will access the memory array. The configuration register values are written via addresses A[max:0]. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are "Don't Care." The BCR is accessed when A[19:18] are 10b; the RCR is accessed when A[19:18] are 00b. The DIDR is read when A[19:18] are 01b. For reads, address inputs other than A[19:18] are "Don't Care," and register bits 15:0 are output on DQ[15:0]. Immediately after performing a configuration register READ or WRITE operation, reading the memory array is highly recommended.

In parts with "-Z" option, CRE pin is disabled internally and CRE access is not available.

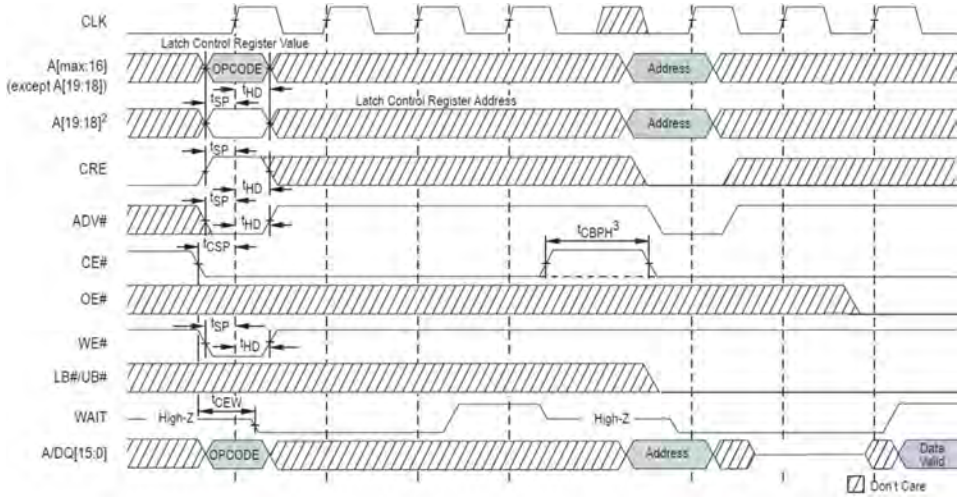
Figure 8 Configuration Register WRITE, Asynchronous Mode, Followed by READ ARRAY Operation



Note

A[19:18] = 00b to load RCR, and 10b to load BCR.

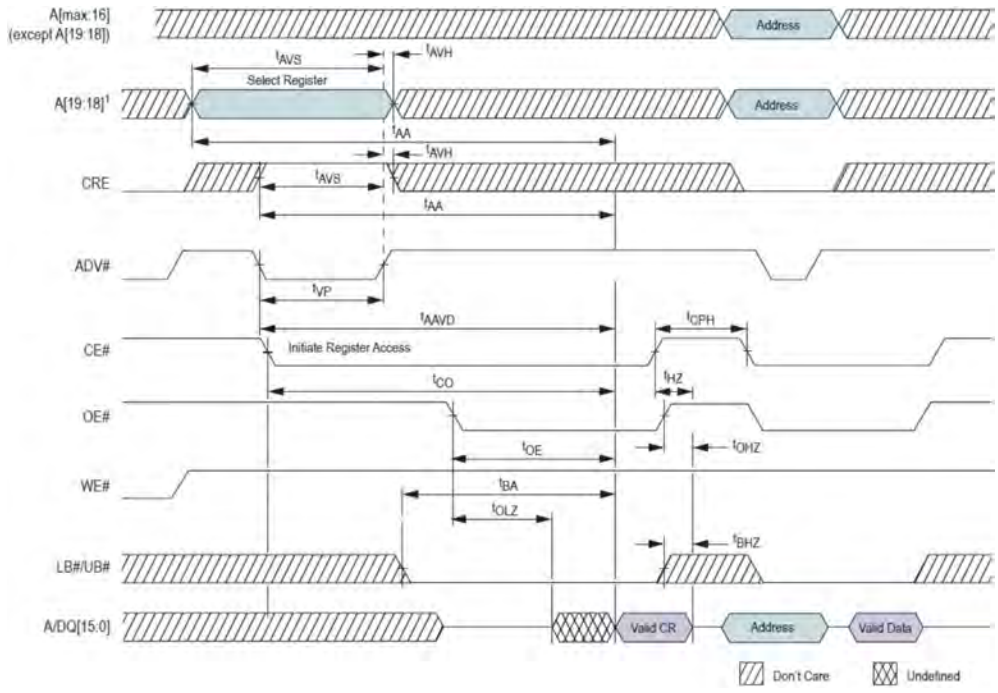
Figure 9 Configuration Register WRITE, Synchronous Mode Followed by READ ARRAY Operation



Note

1. Non-default BCR settings for synchronous mode configuration register WRITE followed by READ ARRAY operation: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. A[19:18] = 00b to load RCR, and 10b to load BCR.
3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

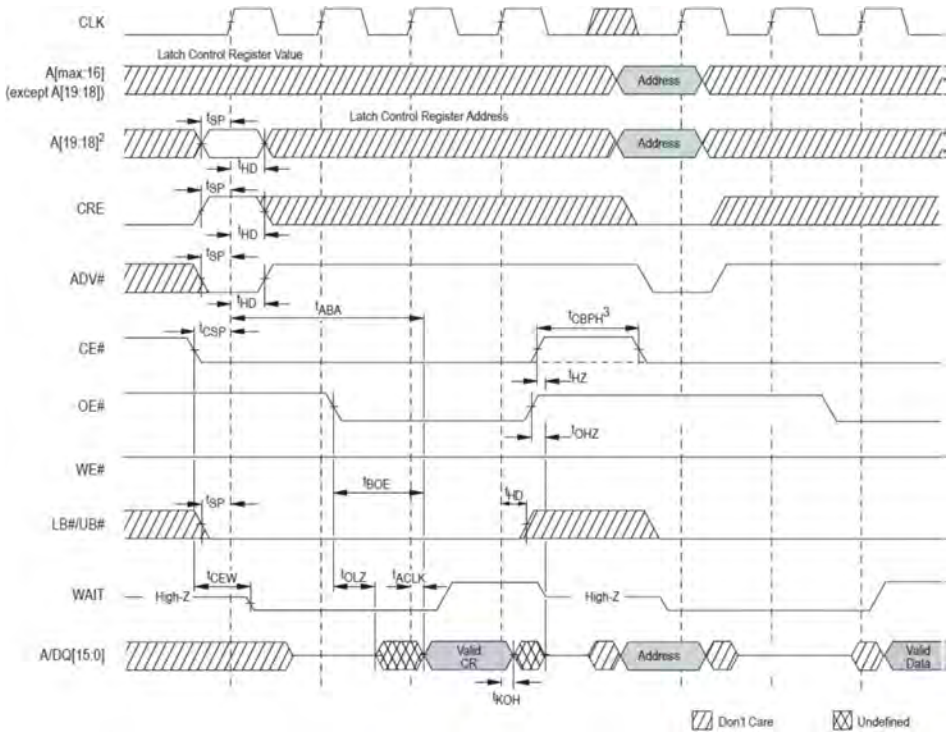
Figure 10 Register READ, Asynchronous Mode Followed by READ ARRAY Operation



Note:

A[19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.

Figure 11 Register READ, Synchronous Mode Followed by READ ARRAY Operation



Note
1. Non-default BCR settings for synchronous mode register READ followed by READ ARRAY operation: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. A[19:18] = 00b to read RCR, 10b to read BCR, and 01b to read DIDR.
3. CE# must remain LOW to complete a burst-of-one READ. WAIT must be monitored additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

10.2 Software Access

Software access of the registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be modified and all registers can be read using the software sequence.

The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations. (See Figure 12.) The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation. (See Figure 13) The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (FFFFFFh for 256Mb, 7FFFFFh for 128Mb, 3FFFFF for 64Mb, 1FFFFF for 32Mb, FFFFF for 16Mb); the contents of this address are not changed by using this sequence.

The data value presented during the third operation (WRITE) in the sequence defines whether the BCR, RCR, or the DIDR is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR; if the data is 0002h, the sequence will access the DIDR. During the fourth operation, DQ[15:0]

transfer data in to or out of bits 15–0 of the registers.

The use of the software sequence does not affect the ability to perform the standard (CRE-con- trolled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for CRE. If the software mechanism is used, CRE can simply be tied to VSS. The port line often used for CRE control purposes is no longer required.

Figure 12 Load Configuration Register

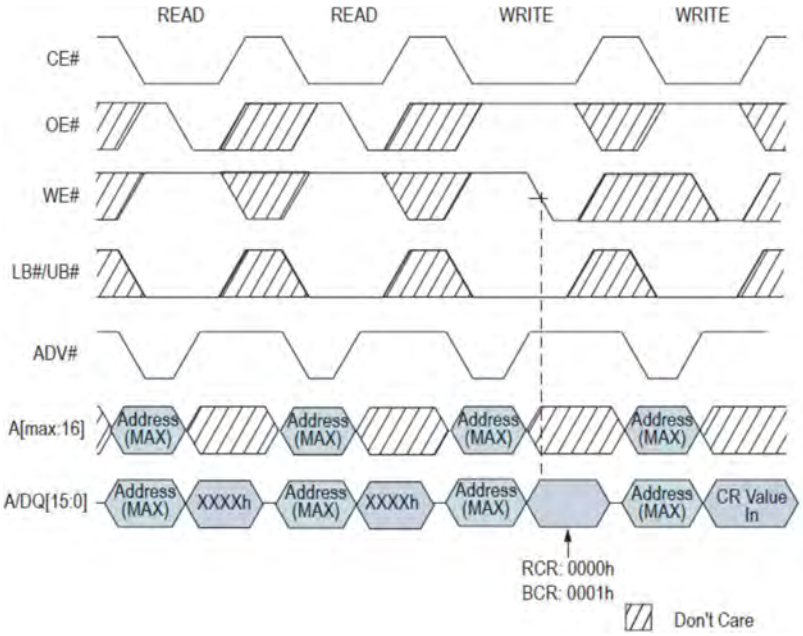
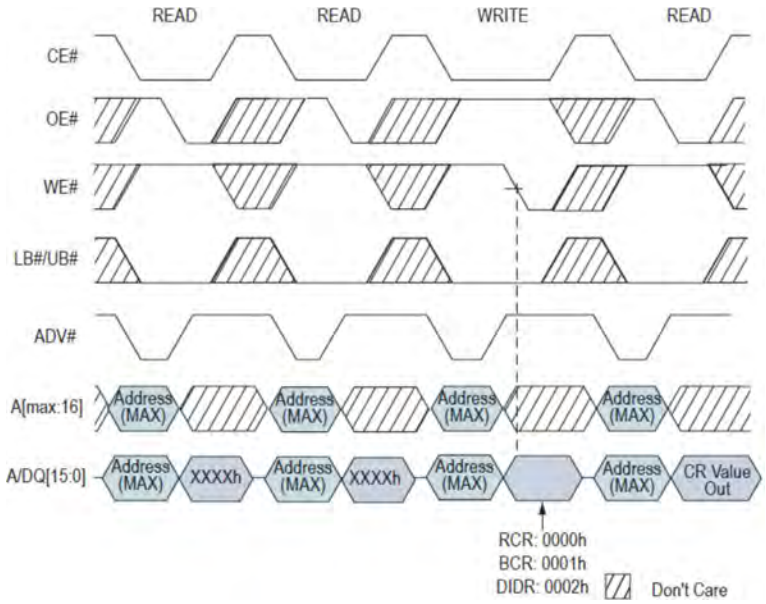


Figure 13 Read Configuration Register

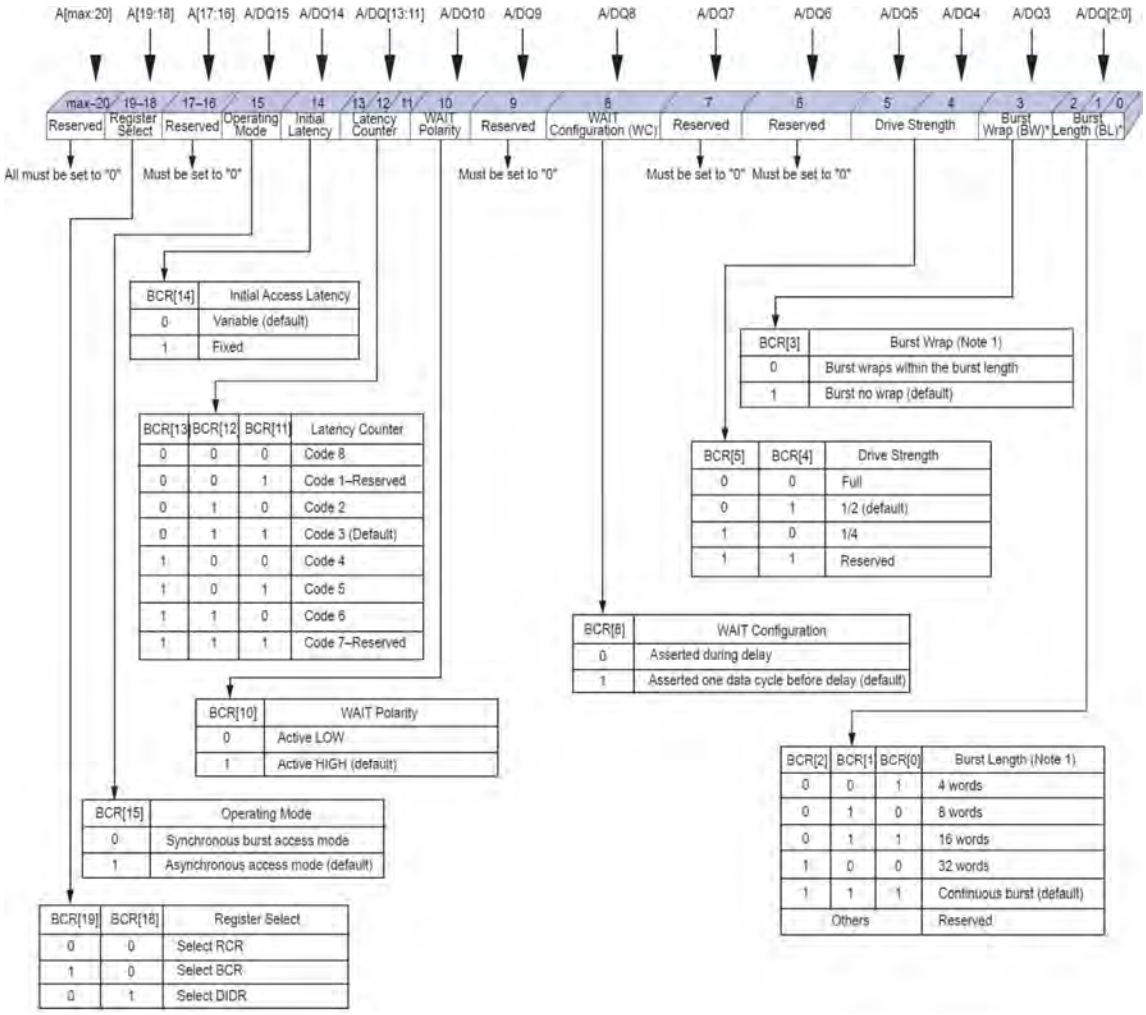


10.3 Bus Configuration Register

The BCR defines how the CellularRAM device interacts with the system memory bus. Figure 14 describes the control bits in the BCR. At power-up, the BCR is set to 9D1Fh.

The BCR is accessed with CRE HIGH and A[19:18] = 10b, or through the register access software sequence with DQ = 0001h on the third cycle.

Figure 14 Bus Configuration Register Definition



Note

1. Burst wrap and length apply to both READ and WRITE operations.
2. Reserved bits must be set to zero. Reserved bits not set to zero will affect device functionality. Writing 1 to reserved bits may be blocked in some devices.
3. Reserved bit BCR[8] can be used for Sort Reject Information of all Cascadeteq products. Please contact Cascadeteq to discussed on it in detailed.

BCR[8]	Normal	Failed Die ID
0		Fail die
1	Default	Pass die

Burst Length (BCR[2:0]) Default = Continuous Burst

Burst lengths define the number of words the device outputs during burst READ and WRITE operations. The device supports a burst length of 4, 8, 16, or 32 words. The device can also be set in continuous burst mode where data is accessed sequentially up to the end of the row.

Burst Wrap (BCR[3]) Default = No Wrap

The burst-wrap option determines if a 4-, 8-, 16-, or 32-word READ or WRITE burst wraps within the burst length, or steps through sequential addresses. If the wrap option is not enabled, the device accesses data from sequential addresses up to the end of the row.

Table 4 Sequence and Burst Length

Burst Wrap		Starting Address	4-Word Burst Length	8-Word Burst Length	16-Word Burst Length	32-Word Burst Length	Continuous Burst
BCR[3]	Wrap	(Decimal)	Linear	Linear	Linear	Linear	Linear
0	Yes	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-...-29-30-31	0-1-2-3-4-5-6-...
		1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-...-30-31-0	1-2-3-4-5-6-7-...
		2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-...-31-0-1	2-3-4-5-6-7-8-...
		3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-...-0-1-2	3-4-5-6-7-8-9-...
		4		4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-...-1-2-3	4-5-6-7-8-9-10-...
		5		5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7-...-2-3-4	5-6-7-8-9-10-11-...
		6		6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8-...-3-4-5	6-7-8-9-10-11-12-...
		7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-...-4-5-6	7-8-9-10-11-12-13-...
		...			...	...	...
		14			14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-...-11-12-13	14-15-16-17-18-19-20-...
		15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-...-12-13-14	15-16-17-18-19-20-21-...
		...				...	...
		30				30-31-0-...-27-28-29	30-31-32-33-34-...
		31				31-0-1-...-28-29-30	31-32-33-34-35-...
1	No	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-...-29-30-31	0-1-2-3-4-5-6-...
		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	1-2-3-...-30-31-32	1-2-3-4-5-6-7-...
		2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	2-3-4-...-31-32-33	2-3-4-5-6-7-8-...
		3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	3-4-5-...-32-33-34	3-4-5-6-7-8-9-...
		4		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19	4-5-6-...-33-34-35	4-5-6-7-8-9-10-...
		5		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12-13-...-15-16-17-18-19-20	5-6-7-...-34-35-36	5-6-7-8-9-10-11-...
		6		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13-14-...-16-17-18-19-20-21	6-7-8-...-35-36-37	6-7-8-9-10-11-12-...
		7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-...-17-18-19-20-21-22	7-8-9-...-36-37-38	7-8-9-10-11-12-13-...
		...			...	...	...
		14			14-15-16-17-18-19-...-23-24-25-26-27-28-29	14-15-16-...-43-44-45	14-15-16-17-18-19-20-...
		15			15-16-17-18-19-20-...-24-25-26-27-28-29-30	15-16-17-...-44-45-46	15-16-17-18-19-20-21-...
		...				...	...
		30				30-31-32-...-59-60-61	30-31-32-33-34-35-36-...
		31				31-32-33-...-60-61-62	31-32-33-34-35-36-37-...

Drive Strength (BCR[5:4]) Default = Outputs Use Half-Drive Strength

The output driver strength can be altered to full, one-half, or one-quarter strength to adjust for different data bus loading scenarios. The reduced-strength options are intended for stacked chip (Flash + CellularRAM) environments when there is a dedicated memory bus. The reduced-drive-strength option minimizes the noise generated on the data bus during READ operations. Full output drive strength should be selected when using a discrete CellularRAM device in a more heavily loaded data bus environment. Outputs are configured at half-drive strength during testing. See Table 5 for additional information.

Table 5 Drive Strength

BCR[5]	BCR[4]	Drive Strength	Impedance Typ (Ω)	Use Recommendation
0	0	Full	25–30	CL = 30pF to 50pF
0	1	1/2 (default)	50	CL = 15pF to 30pF 133 MHz at light load
1	0	1/4	100	CL = 15pF or lower
1	1	Reserved		

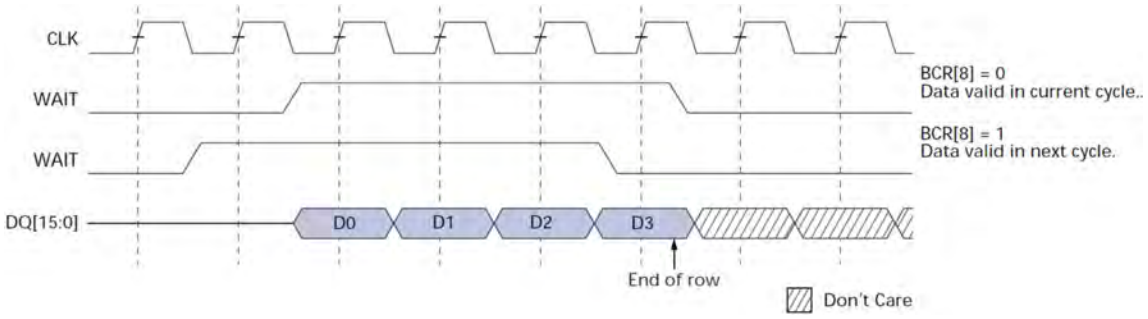
WAIT Configuration (BCR[8]) Default = WAIT Transitions One Clock Before Data Valid/Invalid

The WAIT configuration bit is used to determine when WAIT transitions between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller will use the WAIT signal to coordinate data transfer during synchronous READ and WRITE opera- tions. When BCR[8] = 0, data will be valid or invalid on the clock edge immediately after WAIT transitions to the de-asserted or asserted state, respectively. When BCR[8] = 1, the WAIT signal transitions one clock period prior to the data bus going valid or invalid. See Figure 15

WAIT Polarity (BCR[10]) Default = WAIT Active HIGH

The WAIT polarity bit indicates whether an asserted WAIT output should be HIGH or LOW. This bit will determine whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state.

Figure 15 WAIT Configuration During Burst Operation



Note
Signals shown are for WAIT active LOW, no wrap.

Latency Counter (BCR[13:11]) Default = Three Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a READ or WRITE operation and the first data value transferred. For allowable latency codes, see Tables 6 and 7, respectively, and Figures 16 and 17, respectively

Initial Access Latency (BRC[14]) Default = Variable

Variable initial access latency outputs data after the number of clocks set by the latency counter. However, WAIT must be monitored to detect delays caused by collisions with refresh operations.

Fixed initial access latency outputs the first data at a consistent time that allows for worst-case refresh collisions. The latency counter must be configured to match the initial latency and the clock frequency. It is not necessary to monitor WAIT with fixed initial latency. The burst begins after the number of clock cycles configured by the latency counter. (See Table 7 and Figure 17)

Table 6 Variable Latency Configuration Codes

BCR[13:11]	Latency Configuration Code	Latency[1]		Max Input CLK Frequency (MHz)		
		Normal	Refresh Collision	–7	–9	–12
010	2 (3 clocks)	2	4	66 (15ns)	66 (15ns)	66 (15ns)
011	3 (4 clocks)—default	3	6	109 (9.17ns)	109 (9.17ns)	83 (12ns)
100	4 (5 clocks)	4	8	133 (7.5ns)	—	—
Others	Reserved	—	—	—	—	—

Note
1. Latency is the number of clock cycles from the initiation of a burst operation until data appears. Data is transferred on the next clock cycle.
2. When running maximum frequency at LC=3, under some extreme low-voltage operating conditions, latency without refresh may be 1 cycle more than indicated in this table. Wait and data are always synchronized, and function is guaranteed.

Figure 16 Latency Counter (Variable Initial Latency, No Refresh Collision)

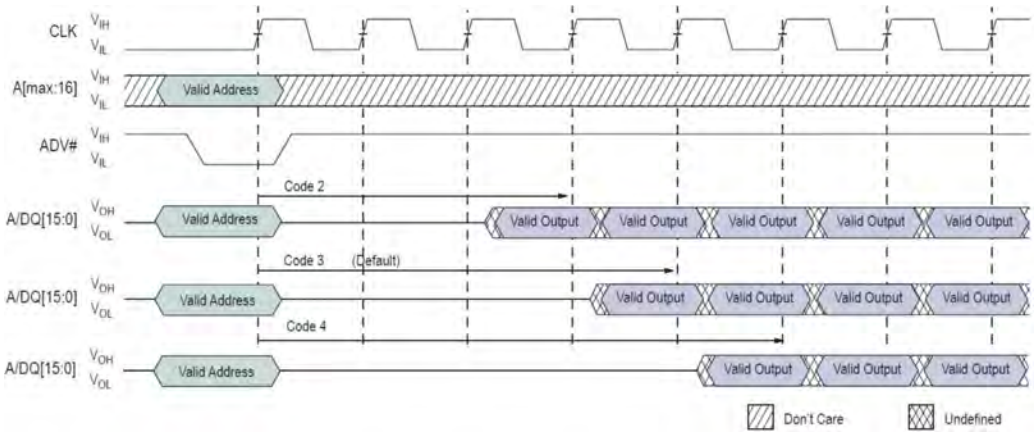
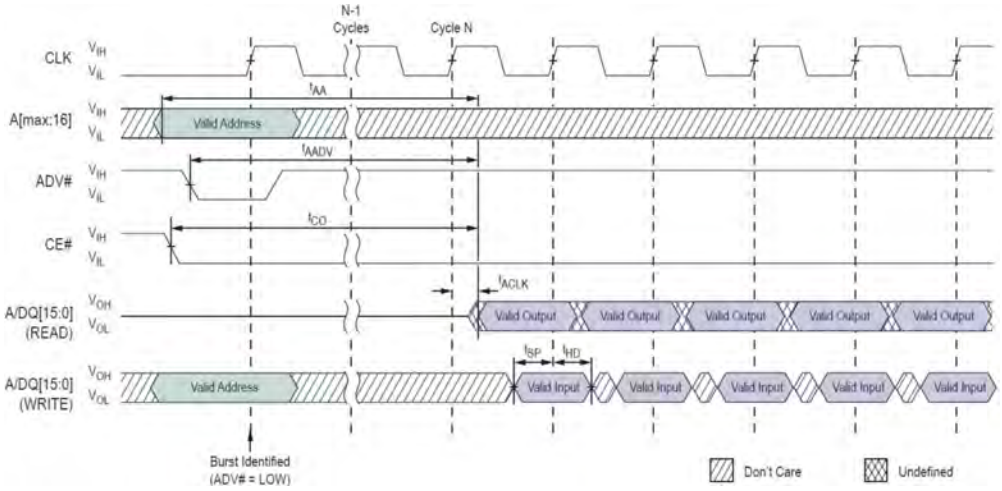


Table 7 Fixed Latency Configuration Codes

BCR[13:11]	Latency Configuration	Latency Count (N)	Max Input CLK Frequency (MHz)		
			–7	–9	–12
010	2 (3 clocks)	2	33 (30ns)	33 (30ns)	33 (30ns)
011	3 (4 clocks)—default	3	52 (19.2ns)	52 (19.2ns)	52 (19.2ns)
100	4 (5 clocks)	4	66 (15ns)	66 (15ns)	66 (15ns)
101	5 (6 clocks)	5	75 (13.3ns)	75 (13.3ns)	75 (13.3ns)
110	6 (7 clocks)	6	109 (9.17ns)	109 (9.17ns)	83 (12ns)
000	8 (9 clocks)	8	133 (7.5ns)	—	—
Others	Reserved	—	—	—	—

Figure 17 Latency Counter (Fixed Latency)



Operating Mode (BCR[15]) Default = Asynchronous Operation

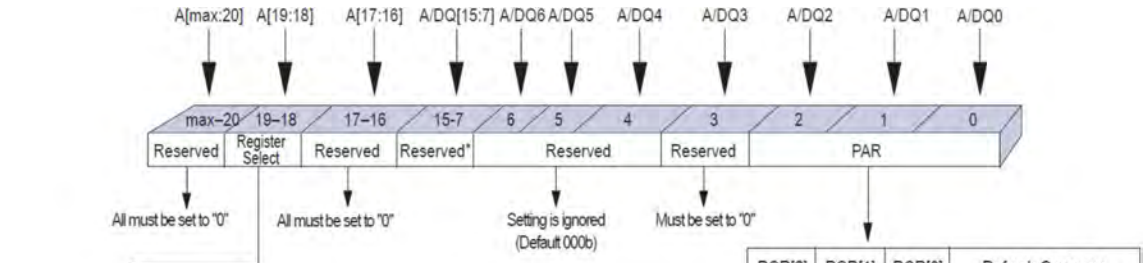
The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

10.4 Refresh Configuration Register

The refresh configuration register (RCR) defines how the CellularRAM device performs its trans- parent self-refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Figure 18 describes the control bits used in the RCR. At power-up, the RCR is set to 0000h.

The RCR is accessed with CRE HIGH and A[19:18] = 00b; or through the register access software sequence with DQ = 0000h on the third cycle. (See “Registers”)

Figure 18 Refresh Configuration Register Mapping



RCR[19]	RCR[18]	Register Select
0	0	Select RCR
1	0	Select BCR
0	1	Select DIDR

RCR[2]	RCR[1]	RCR[0]	Refresh Coverage
0	0	0	Full array (default)
0	0	1	Bottom 1/2 array
0	1	0	Bottom 1/4 array
0	1	1	Bottom 1/8 array
1	0	0	None of array
1	0	1	Top 1/2 array
1	1	0	Top 1/4 array
1	1	1	Top 1/8 array

Notes:
1. Reserved bits must be set to zero except RCR[15] & RCR[12] below. Reserved bits not set to zero will affect device functionality. Writing 1 to reserved bits may be blocked in some devices.
2. Reserved bit RCR[15] can be used for Sort Reject Information, **ADMUX only**. Please contact Cascadeteq for this function in detailed.

BCR [15]	Standard	Extended
0	Reserved	Pass die
1	Reserved	Fail die

Partial Array Refresh (RCR[2:0] Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map. (See Table 8 and Table 9)

Table 8 64Mb Address Patterns for PAR

RCR[2]	RCR[1]	RCR[0]	Active Section	Address Space	Size	Density
0	0	0	Full die	000000h–3FFFFFh	4 Meg x 16	64Mb
0	0	1	One-half of die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	1	0	One-quarter of die	000000h–0FFFFFh	1 Meg x 16	16Mb
0	1	1	One-eighth of die	000000h–07FFFFh	512K x 16	8Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	200000h–3FFFFFh	2 Meg x 16	32Mb
1	1	0	One-quarter of die	300000h–3FFFFFh	1 Meg x 16	16Mb
1	1	1	One-eighth of die	380000h–3FFFFFh	512K x 16	8Mb

10.5 Device Identification Register

The DIDR provides information on the device manufacturer, CellularRAM generation, and the specific device configuration. Table 9 describes the bit fields in the DIDR. This register is read-only.

The DIDR is accessed with CRE HIGH and A[19:18] = 01b, or through the register access software sequence with A/DQ = 0002h on the third cycle

Table 9 Device Identification Register Mapping

Bit Field	DIDR[15]		DIDR[14:11]		DIDR[10:8]		DIDR[7:5]		DIDR[4:0]	
Field name	Row length		Device version		Device density		CellularRAM generation		Vendor ID	
	Length	Bit Setting	Version	Bit Setting	Density	Bit Setting	Generation	Bit Setting	Vendor	Bit Setting
Options	512 words	0b	1st	0000b	64Mb	010b	CR 1.0	001b	AP Memory	01101b
	256 words	1b	2nd	0001b	128Mb	011b	CR 1.5	010b		
			...	...	32Mb	001b	CR 2.0	011b		
					256Mb	100b				
					512Mb	101b				
					16Mb	000b				

Note

The Row Length DIDR[15] of standard CR1.5 is zeo for 128 words and one for 256 words. However current Cascadeteq products are all 256 words only. In order to support the new product of row length =512 words Cascadeteq redefined the ZERO of this bit to 512 words in distinguish of existing products. Please contact Cascadeteq in detailed

Part Number Table for Row Length Specific

Part Number	DIDR [15]
CSA6416SB-FI-A1	0b

11. Electrical Characteristics

Table 10 Absolute Maximum Ratings

Parameter	Rating
Voltage to any ball except VCC, VCCQ relative to VSS	–0.3V to VCCQ + 0.3V
Voltage on VCC supply relative to VSS	–0.2V to +2.45V
Voltage on VCCQ supply relative to VSS	–0.2V to +2.45V
Storage temperature (plastic)	–55°C to +150°C
Operating temperature (case) Wireless	–30°C to +85°C
Soldering temperature and time 10s (solder ball only)	+260°C

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 11 Electrical Characteristics and Operating Conditions

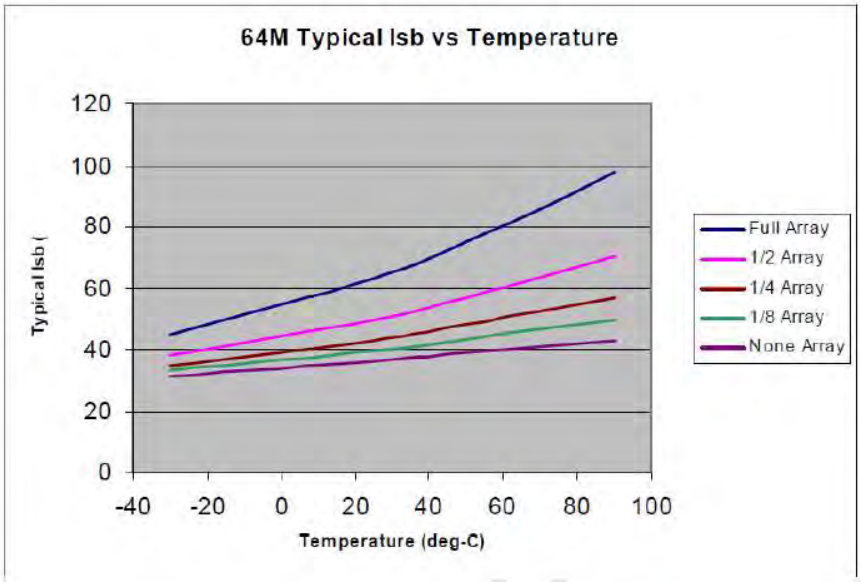
Temperature (–25ºC < TC < +85ºC)

Description	Conditions	Symbol		Min	Max	Unit	Notes
Supply voltage		VCC		1.7	1.95	V	
I/O supply voltage		VCCQ		1.7	1.95	V	
Input high voltage		VIH		VCCQ – 0.4	VCCQ + 0.2	V	1
Input low voltage		VIL		–0.20	0.4	V	2
Output high voltage	IOH = –0.2mA	VOH		0.80 VCCQ		V	3
Output low voltage	IOL = +0.2mA	VOL			0.20 VCCQ	V	3
Input leakage current	VIN = 0 to VCCQ	ILI			1	µA	
Output leakage current	OE# = VIH or chip disabled	ILO			1	µA	
Operating Current	**Conditions**	**Symbol**		**Typ**	**Max**	**Unit**	**Notes**
Asynchronous random READ/WRITE	VIN = VCCQ or 0V; chip enabled, IOUT = 0	ICC1	–70		25	mA	4,7
			–85		22		
Initial access, burst READ/WRITE		ICC2	133 MHz		40	mA	4,7
			109 MHz		35		
			83 MHz		30		
Continuous burst READ		ICC3R	133 MHz		35	mA	4,7
			109 MHz		30		
			83 MHz		25		
Continuous burst WRITE		ICC3W	133 MHz		40	mA	4,7
			109 MHz		35		
			83 MHz		30		
Standby current	VIN = VCCQ or 0V; CE# = VCCQ	ISB	256Mb 2-die device	50	500	µA	5, 6
			128Mb Standard		300		
			64Mb Standard		200		
			32Mb Standard		150		
			32Mb Reduced		120		
			16Mb Standard		120		
			16Mb Reduced		100		

Note

1. Input signals may overshoot to VCCQ + 1.0V for periods less than 2ns during transitions.
2. Input signals may undershoot to VSS – 1.0V for periods less than 2ns during transitions
3. BCR[5:4] = 01b (default setting of one-half drive strength).
4. This parameter is specified with the outputs disabled to avoid external loading effects.
The user must add the current required to drive output capacitance expected in the actual system.
5. ISB (max) values measured with PAR set to FULL ARRAY and at +85°C. In order to achieve low standby current, all inputs must be driven to either VCCQ or VSS. ISB might be slightly higher for up to 500ms after power-up, or when entering standby mode.
6. ISB (typ) is the average ISB at 25°C and VCC = VCCQ = 1.8V. This parameter is verified during characterization and is not 100% tested.
7. For 256M 2-die device Icc spec is 10mA above the single-die spec values shown in this table.

Figure 19 Typical Refresh Current vs. Temperature (ITCR)



Note
These Isb vs PAR curves are for illustration only. The actual Isb reduction in PAR may deviate from this Figure.

Table 12 Maximum Isb specifications under PAR settings

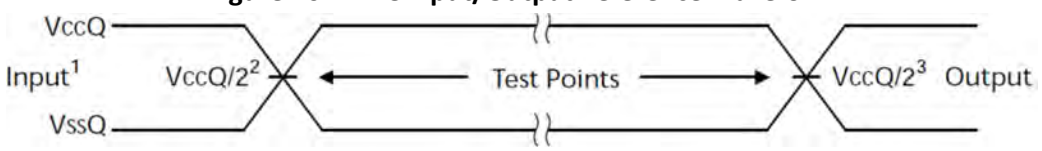
Density	Isb (Max) Full Array (µA)	Isb (Max) 1/2 Array (µA)	Isb (Max) 1/4 Array (µA)	Isb (Max) 1/8 Array (µA)	Isb (Max) None of Array (µA)
64Mb	200	170	150	140	130

Table 13 Capacitance

Description	Conditions	Symbol	Min	Max	Units	Notes
Input Capacitance	T_C = +25°C; f = 1 MHz; V_{IN} = 0V	C_{IN}	2.0	6	pF	1
Input/Output Capacitance (DQ)		C_{IO}	3.5	6	pF	1

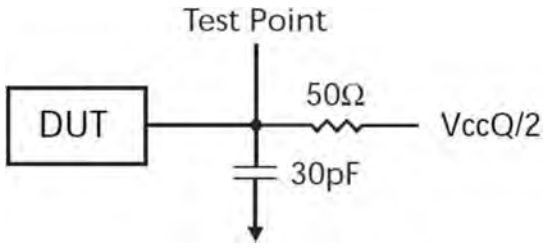
Note
These parameters are verified in device characterization and are not 100% tested

Figure 20 AC Input/Output Reference Waveform



Note
1. AC test inputs are driven at VCCQ for a logic 1 and VSSQ for a logic 0. Input rise and fall times (10% to 90%) <1.6ns.
2. Input timing begins at VCCQ /2.
3. Output timing ends at VCCQ /2.

Figure 21 AC Output Load Circuit



Note
All tests are performed with the outputs configured for default setting of half drive strength (BCR[5:4] = 01b).

12. Timing Requirements

Table 14 Asynchronous READ Cycle Timing Requirements

All tests performed with outputs configured for default setting of half drive strength, (BCR[5:4] = 01b).

Parameter	Symbol	-7/9		-12		Unit	Notes
		Min	Max	Min	Max		
Address access time	^{t}AA		70		70	ns	
ADV# access time	^{t}AADV		70		70	ns	
Address hold from ADV# HIGH	^{t}AVH	2		2		ns	
Address setup to ADV# HIGH	^{t}AVS	5		5		ns	
LB#/UB# access time	^{t}BA		70		70	ns	
LB#/UB# disable to DQ High-Z Output	^{t}BHZ		7		7	ns	1
OE# LOW to WAIT valid	^{t}OEW	1	7.5	1	7.5	ns	
Chip select access time	^{t}CO		70		70	ns	
CE# LOW to ADV# HIGH	^{t}CVS	7		7		ns	
Chip disable to DQ and WAIT High-Z output	^{t}HZ		7		7	ns	1
Output enable to valid output	^{t}OE		20		20	ns	
Output disable to DQ High-Z output	^{t}OHZ		7		7	ns	1
Output enable to Low-Z output	^{t}OLZ	3		3		ns	2
ADV# pulse width LOW	^{t}VP	5		5		ns	

Note
1. Low-Z to High-Z timings are tested with the circuit shown in Figure 21. The High-Z timings measure a 100mV transition from either VOH or VOL toward VCCQ/2.
2. High-Z to Low-Z timings are tested with the circuit shown in Figure 21. The Low-Z timings measure a 100mV transition away from the High-Z (VCCQ /2) level toward either VOH or VOL.

Table 15 Burst READ Cycle Timing Requirements

All tests performed with outputs configured for default setting of half drive strength, (BCR[5:4] = 01b).

Parameter	Symbol	–7		–9		–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address access time (fixed latency)	^{t}AA		70		70		70	ns	
ADV# access time (fixed latency)	^{t}AADV		70		70		70	ns	
Burst to READ access time (variable latency)	^{t}ABA		35.5		34.5		45	ns	
CLK to output delay	^{t}ACLK		5.5		7		9	ns	
Address hold from ADV# HIGH (fixed latency)	^{t}AVH	2		2		2		ns	
Burst OE# LOW to output delay	^{t}BOE		20		20		20	ns	
CE# HIGH between subsequent burst or mixed-mode operations	^{t}CBPH	max(15ns ,2n^{t}CLK)		max(15ns ,2n^{t}CLK)		max(15ns ,2n^{t}CLK)			1
Maximum CE# pulse width for 128Mb and lower	^{t}CEM		4		4		4	µs	1
Maximum CE# pulse width for 256Mb 1-die device	^{t}CEM		2		2		2	µs	1,4
Maximum CE# pulse width for 256Mb 2-die device	^{t}CEM		4		4		4	µs	1,4
CE# LOW to WAIT valid	^{t}CEW	1	7.5	1	7.5	1	7.5	ns	
CLK period	^{t}CLK	7.5		9.17		12.		ns	
Chip select access time (fixed latency)	^{t}CO		70		70		70	ns	
CE# setup time to active CLK edge	^{t}CSP	2.5		3		4		ns	
Hold time from active CLK edge	^{t}HD	1.5		2		2		ns	
Chip disable to DQ and WAIT High-Z output	^{t}HZ		7		7		7	ns	2
CLK rise or fall time	^{t}KHKL		1.2		1.6		1.8	ns	
CLK to WAIT valid	^{t}KHTL		5.5		7		9	ns	
Output HOLD from CLK	^{t}KOH	2		2		2		ns	
CLK HIGH or LOW time	^{t}KP	3		3		4		ns	
Output disable to DQ High-Z output	^{t}OHZ		7		7		7	ns	2
Output enable to Low-Z output	^{t}OLZ	3		3		3		ns	3
Setup time to active CLK edge	^{t}SP	2		3		3		ns	
ADV# pulse width LOW	^{t}VP	5		5		5		ns	

Note

1. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by both of the following two conditions for CE# HIGH: a) more than or equal to 2 CLK periods, and b) longer than 15ns.
2. Low-Z to High-Z timings are tested with the circuit shown in Figure 21. The High-Z timings measure a 100mV transition from either VOH or VOL toward VCCQ /2.
3. High-Z to Low-Z timings are tested with the circuit shown in Figure 21. The Low-Z timings measure a 100mV transition away from the High-Z (VCCQ /2) level toward either VOH or VOL.
4. tCEM of 2us applies to 256M single-die device. For a 256M device formed by 2-die stack of 128M devices, tCEM is 4us.

Table 16 Asynchronous WRITE Cycle Timing Requirements

Parameter	Symbol	–7/9		–12		Unit	Notes
		Min	Max	Min	Max		
Address and ADV# LOW setup time	tAS	0		0		ns	
Address HOLD from ADV# going HIGH	tAVH	2		2		ns	
Address setup to ADV# going HIGH	tAVS	5		5		ns	
Address valid to end of WRITE	tAW	70		70		ns	
LB#/UB# select to end of WRITE	tBW	70		70		ns	
CE# LOW to WAIT valid	tCEW	1	7.5	1	7.5	ns	
CE# HIGH between subsequent async operations	tCPH	5		5		ns	
CE# LOW to ADV# HIGH	tCVS	7		7		ns	
Chip enable to end of WRITE	tCW	70		70		ns	
Data HOLD from WRITE time	tDH	0		0		ns	
Data WRITE setup time	tDW	20		20		ns	
Chip disable to WAIT High-Z output	tHZ		7		7	ns	1
ADV# pulse width	tVP	5		5		ns	
ADV# setup to end of WRITE	tVS	70		70		ns	
WRITE to DQ High-Z output	tWHZ		7		7	ns	1
WRITE pulse width	tWP	45		45		ns	2
WRITE recovery time	tWR	0		0		ns	

Note

1. Low-Z to High-Z timings are tested with the circuit shown in Figure 21. The High-Z timings measure a 100mV transition from either VOH or VOL toward VCCQ/2.
2. WE# LOW time must be limited to tCEM.

Table 17 Burst WRITE Cycle Timing Requirements

Parameter	Symbol	–7		–9		–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address and ADV# LOW setup time	tAS	0		0		0		ns	1
Address HOLD from ADV# HIGH (fixed latency)	tAVH	2		2		2		ns	
CE# HIGH between subsequent burst or mixed-mode operations	tCBPH	5		5		6		ns	2
Maximum CE# pulse width for 128Mb and below	tCEM		4		4		4	µs	2
Maximum CE# pulse width for 256Mb 1-die device	tCEM		2		2		2	µs	2,4
Maximum CE# pulse width for 256Mb 2-die device	tCEM		4		4		4	µs	2,4
CE# LOW to WAIT valid	tCEW	1	7.5	1	7.5	1	7.5	ns	
Clock period	tCLK	7.5		9.17		12		ns	
CE# setup to CLK active edge	tCSP	2.5		3		4		ns	
Hold time from active CLK edge	tHD	1.5		2		2		ns	
Chip disable to WAIT High-Z output	tHZ		7		7		7	ns	3
CLK rise or fall time	tKHKL		1.2		1.6		1.8	ns	
Clock to WAIT valid	tKHTL		5.5		7		9	ns	
CLK HIGH or LOW time	tKP	3		3		4		ns	
Setup time to activate CLK edge	tSP	2		3		3		ns	
ADV# pulse width LOW	tVP	5		5		5		ns	

Note

1. tAS required if tCSP > 20ns.
2. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.
3. Low-Z to High-Z timings are tested with the circuit shown in Figure 21.
The High-Z timings measure a 100mV transition from either VOH or VOL toward VCCQ/2.
4. tCEM of 2us applies to 256M single-die device. For a 256M device formed by 2-die stack of 128M devices, tCEM is 4us.

13. Timing Diagrams

Figure 22 Initialization Period

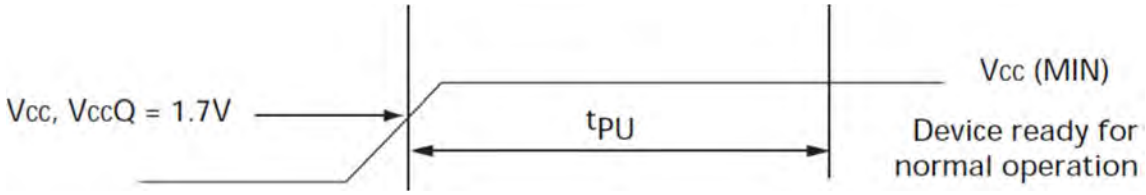


Figure 23 Asynchronous READ

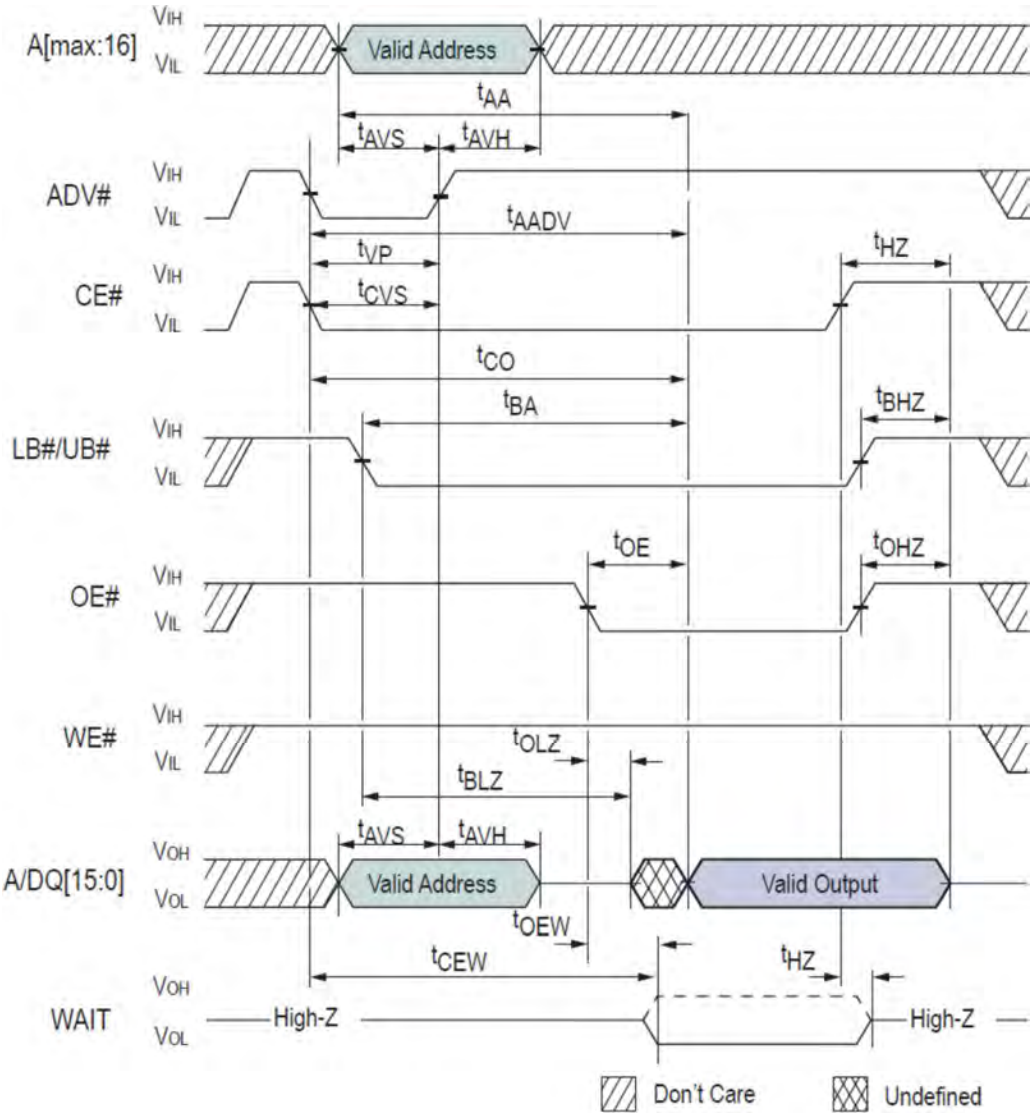
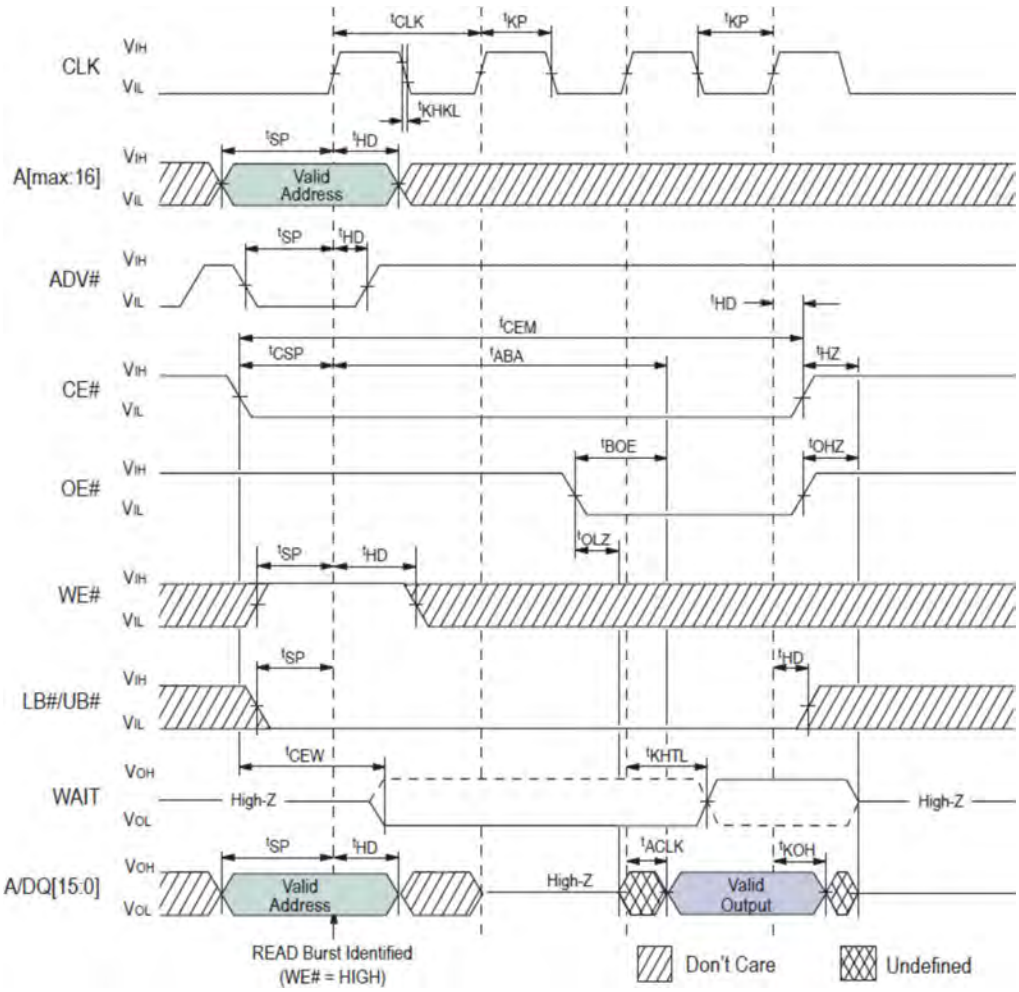
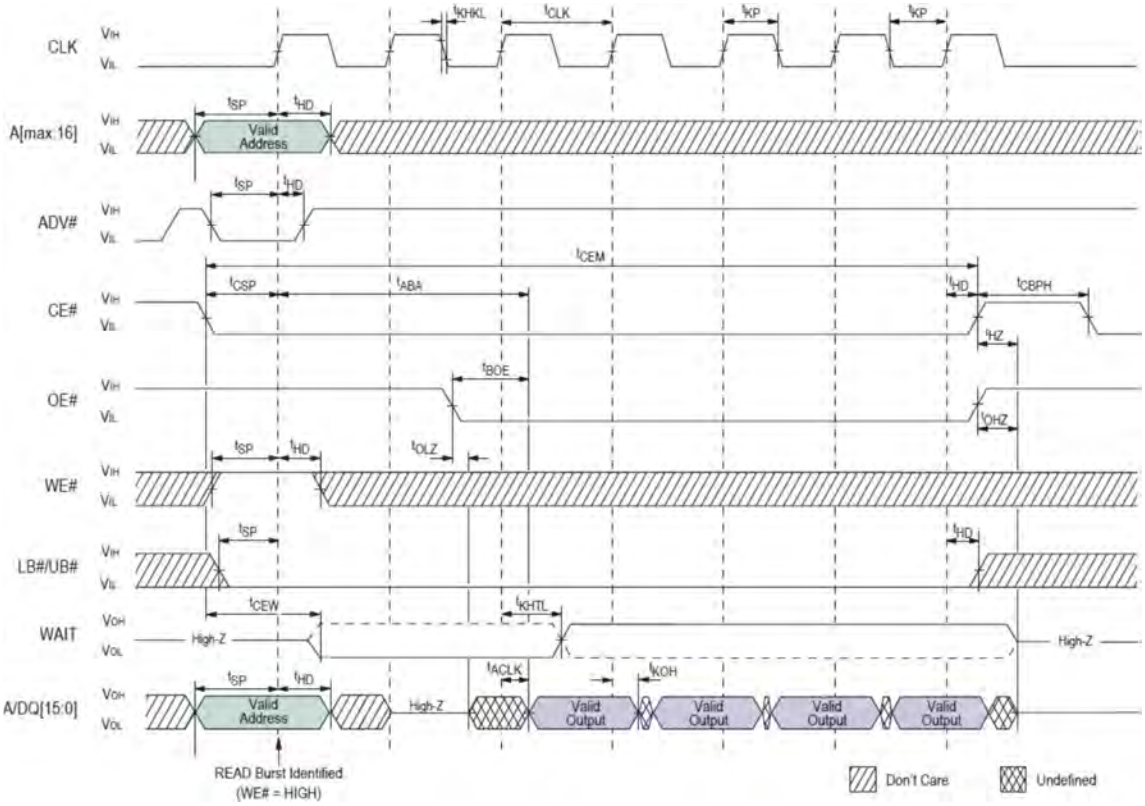


Figure 24 Single-Access Burst READ Operation—Variable Latency



Note:
Non-default BCR settings: Latency code 2 (3 clocks); WAIT active LOW; WAIT asserted during delay.

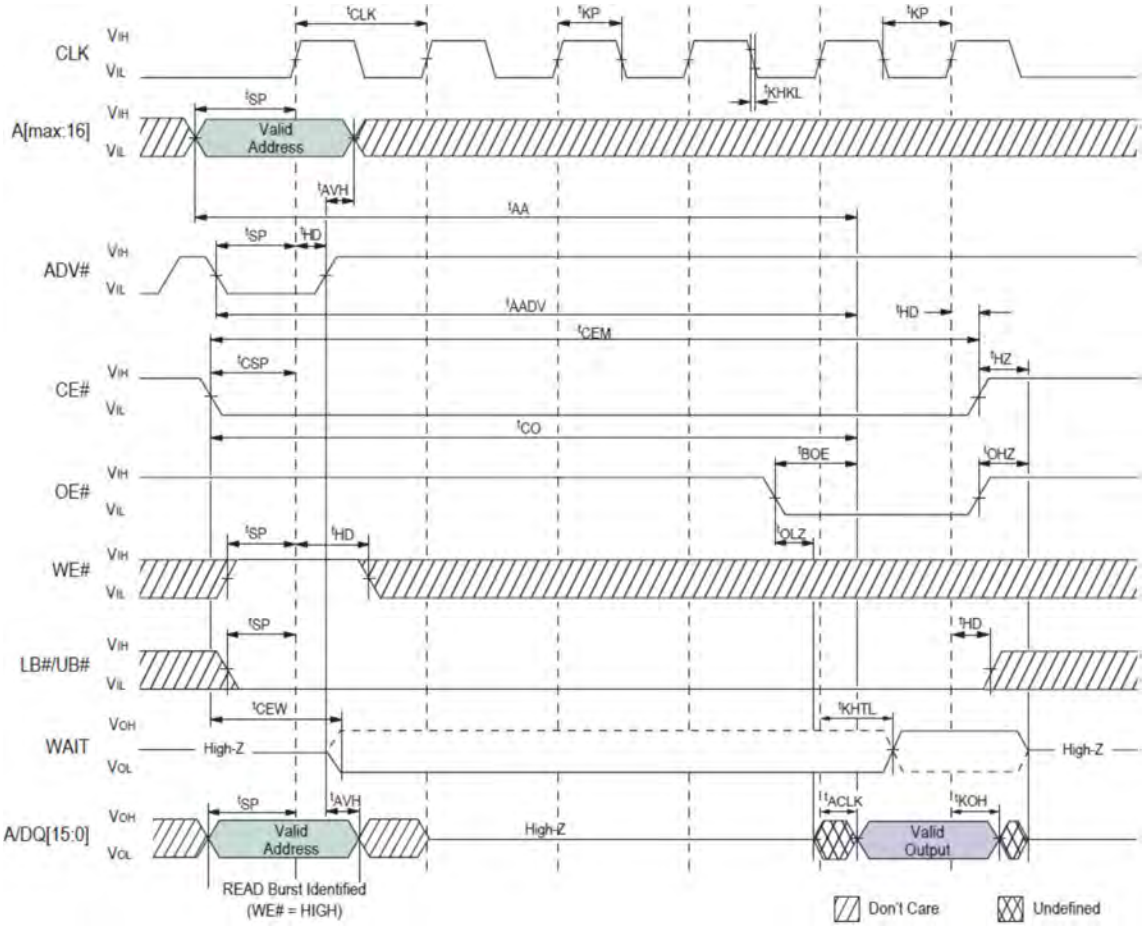
Figure 25 4-Word Burst READ Operation—Variable Latency



Note

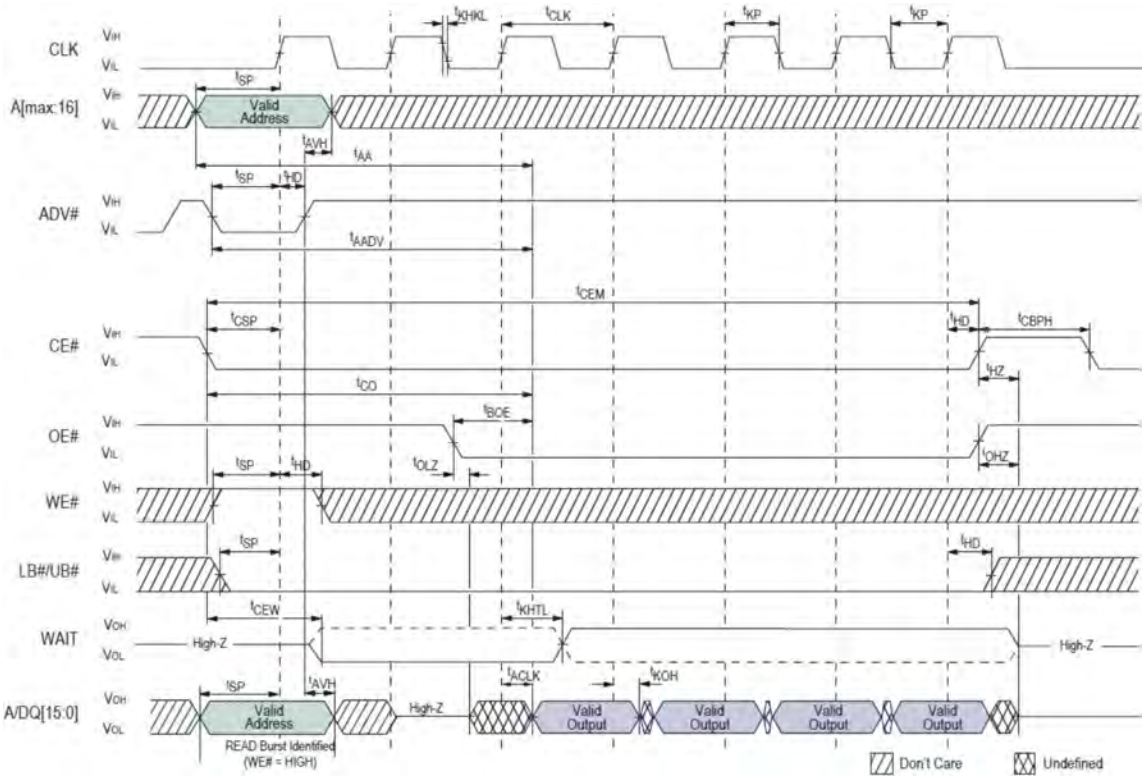
1. Non-default BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. WAIT will remain de-asserted if CE# remains LOW past the end of the defined burst length.
3. A/DQ[15:0] will output undefined data if CE# remains LOW past the end of the defined burst length.

Figure 26 Single-Access Burst READ Operation—Fixed Latency



Note
Non-default BCR settings: Fixed latency; latency code 4 (5 clocks); WAIT active LOW; WAIT asserted during delay.

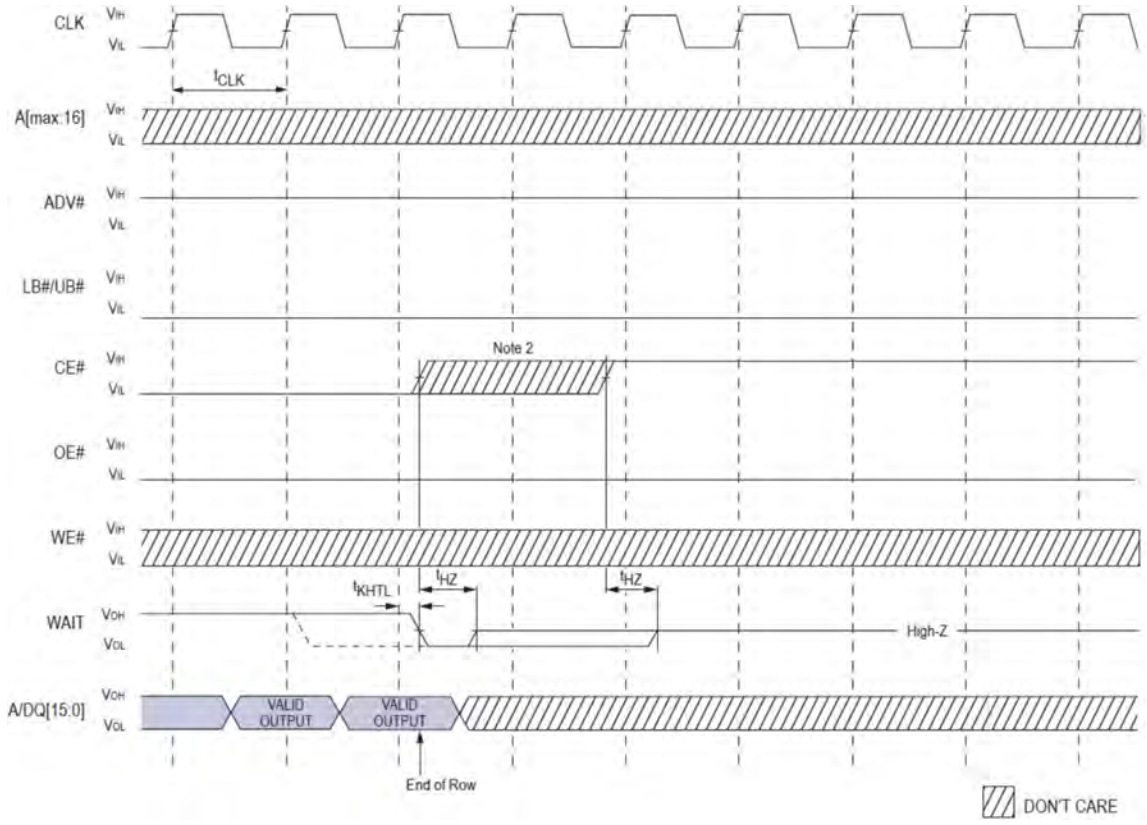
Figure 27 4-Word Burst READ Operation—Fixed Latency



Note

1. Non-default BCR settings: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. WAIT will remain de-asserted if CE# remains LOW past the end of the defined burst length.
3. A/DQ[15:0] will output undefined data if CE# remains LOW past the end of the defined burst length.

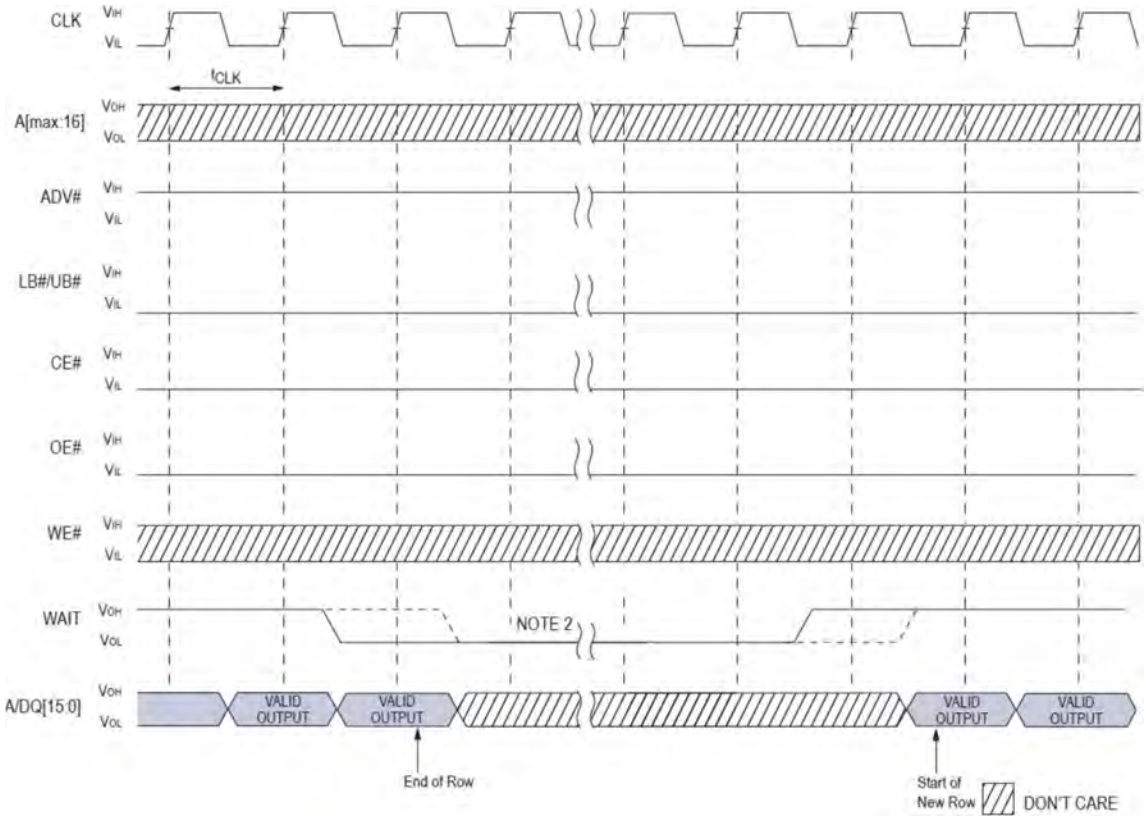
Figure 28 Burst READ at End-of-Row (Wrap Off)



Note

1. Non-default BCR settings for burst READ at end of row: fixed or variable latency; WAIT active LOW; WAIT asserted during delay.
2. For burst READs, CE# must go HIGH before the second CLK after the WAIT period begins (before the second CLK after WAIT asserts with BCR[8] = 0, or before the third CLK after WAIT asserts with BCR[8] = 1).

Figure 29 Burst Read Row Boundary Crossing



Note

1. Non-default BCR setting for burst READ at end of row: fixed or variable latency; WAIT active LOW; WAIT asserted 1 cycle advanced.
2. WAIT will be asserted for LC+2 cycles for variable latency, and LC+1 cycles for fixed latency.

Figure 30 Asynchronous WRITE

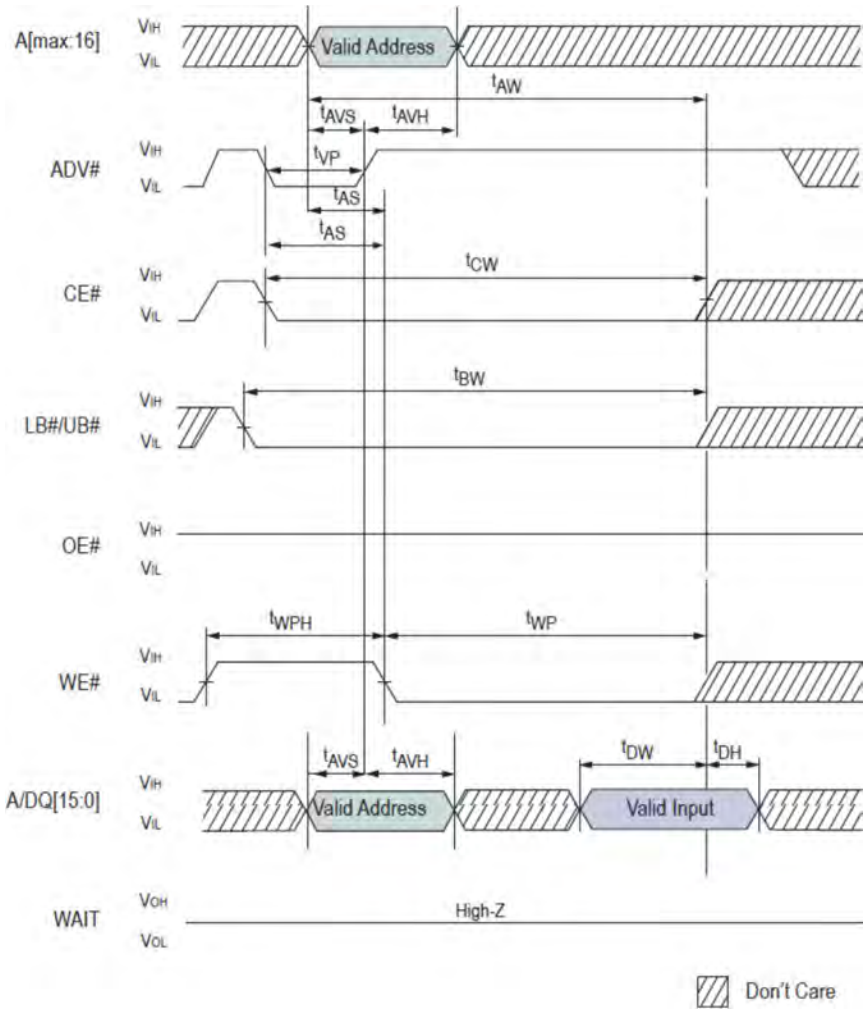
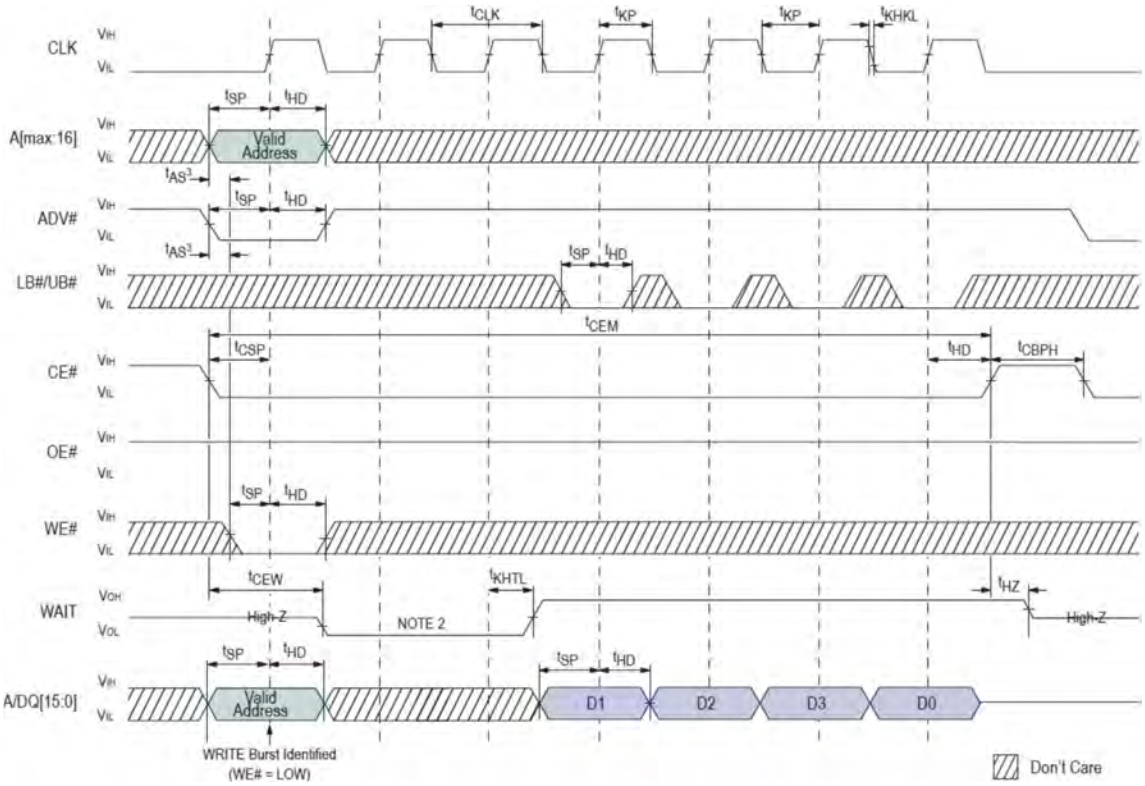


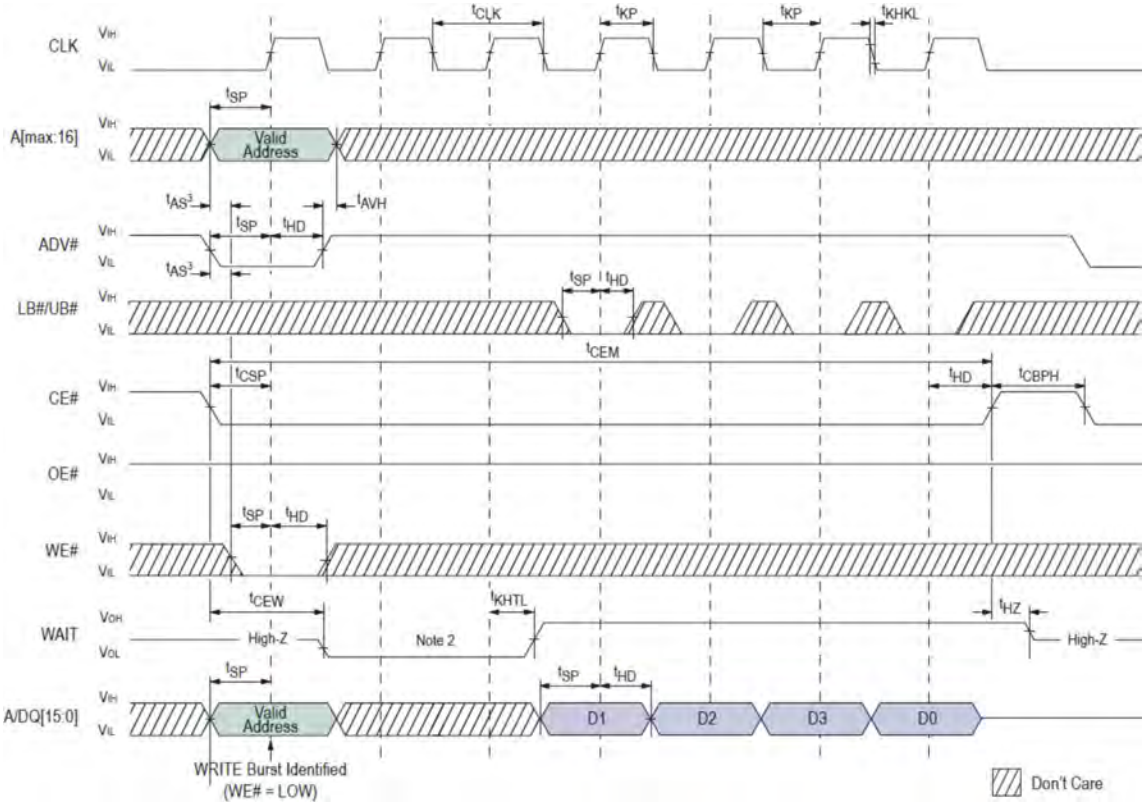
Figure 31 Burst WRITE Operation—Variable Latency Mode



Note

1. Non-default BCR settings for burst WRITE operation in variable latency mode: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay; burst length four; burst wrap enabled.
2. WAIT asserts for LC cycles for both fixed and variable latency. LC = Latency Code (BCR[13:11]).
3. tAS required if tCSP > 20ns.
4. CE# must go HIGH before any clock edge following the last word of a defined-length burst.

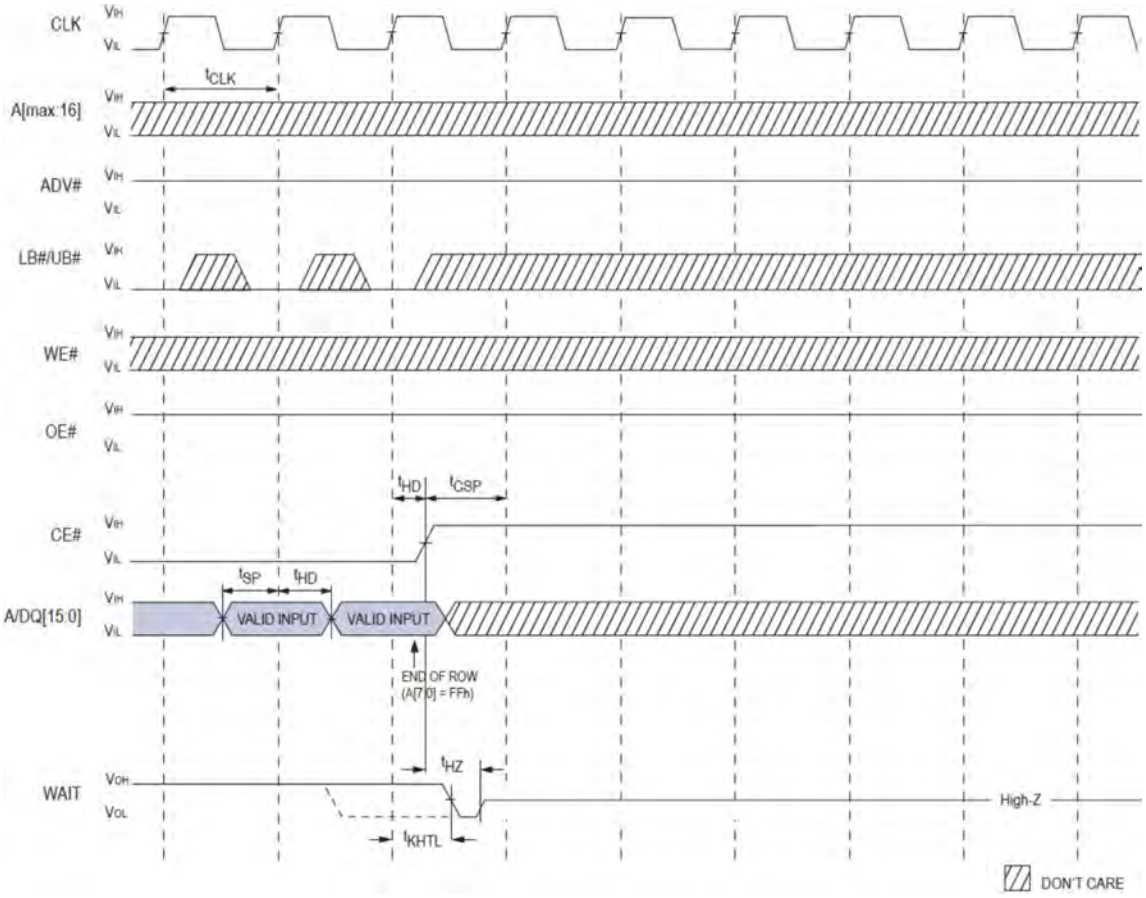
Figure 32 Burst WRITE Operation—Fixed Latency Mode



Note

1. Non-default BCR settings for burst WRITE operation in fixed latency mode: Fixed latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay; burst length four; burst wrap enabled.
2. WAIT asserts for LC cycles for both fixed and variable latency. LC = Latency Code (BCR[13:11]).
3. tAS required if tCSP > 20ns.
4. CE# must go HIGH before any clock edge following the last word of a defined-length burst.

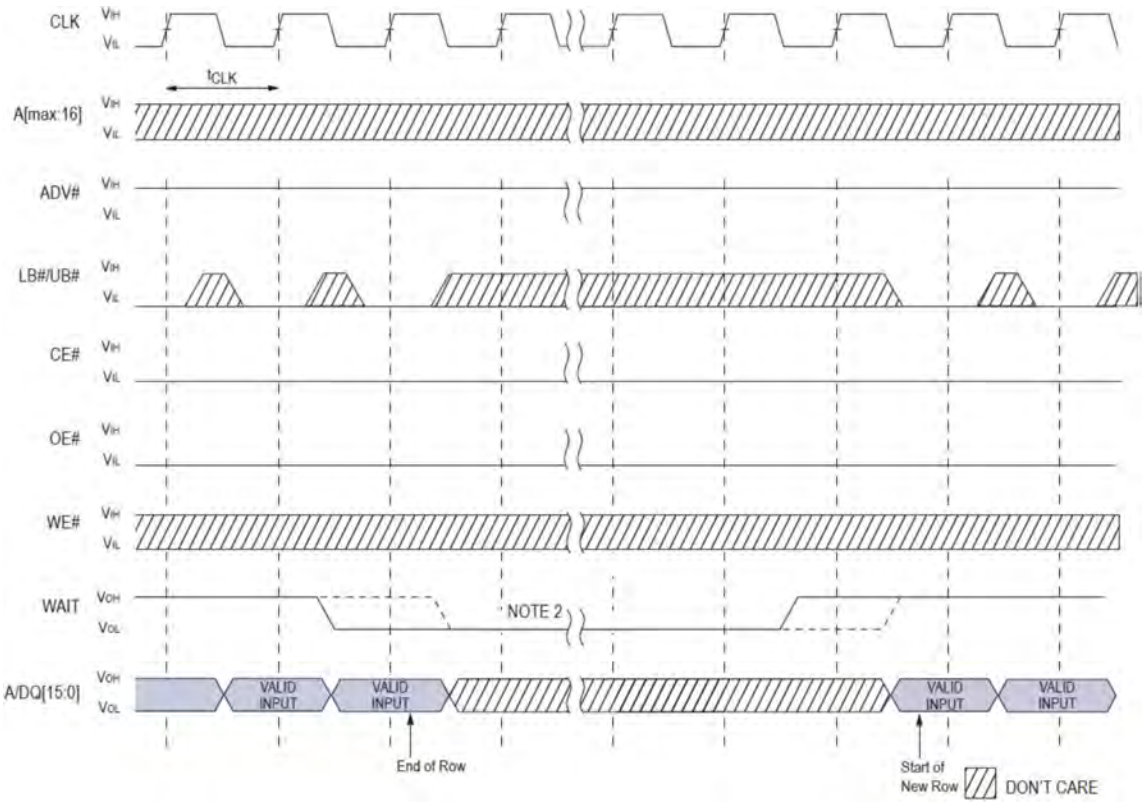
Figure 33 Burst WRITE at End of Row (Wrap Off)



Note

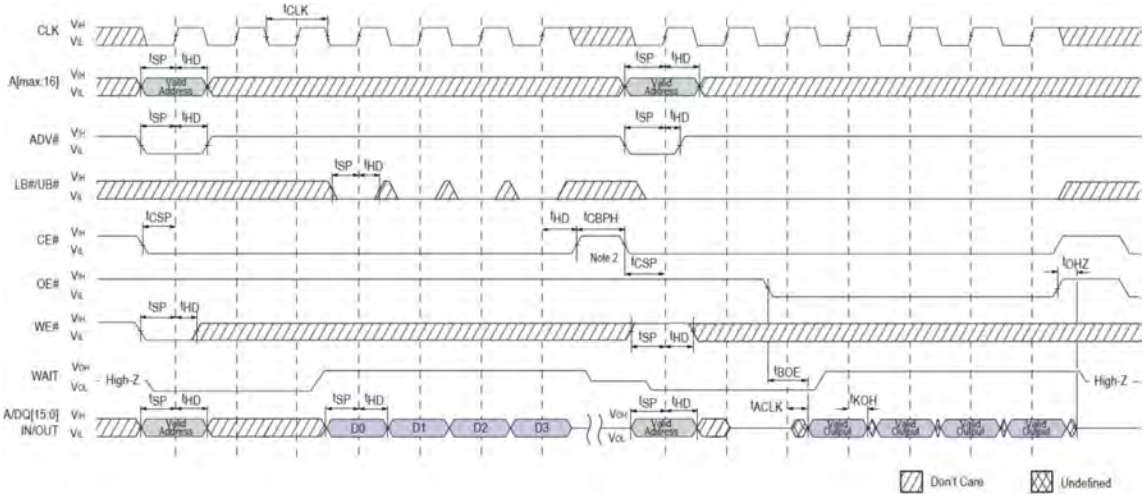
1. Non-default BCR settings for burst WRITE at end of row: fixed or variable latency; WAIT active LOW; WAIT asserted in the same cycle as data (dotted line indicating 1 cycle ahead).
2. For burst WRITE, to ensure successful write of last data word, CE# rising edge must meet tHD. Similarly, to block write of the next data word, CE# rising edge must meet tCSP.

Figure 34 Burst Write Row Boundary Crossing



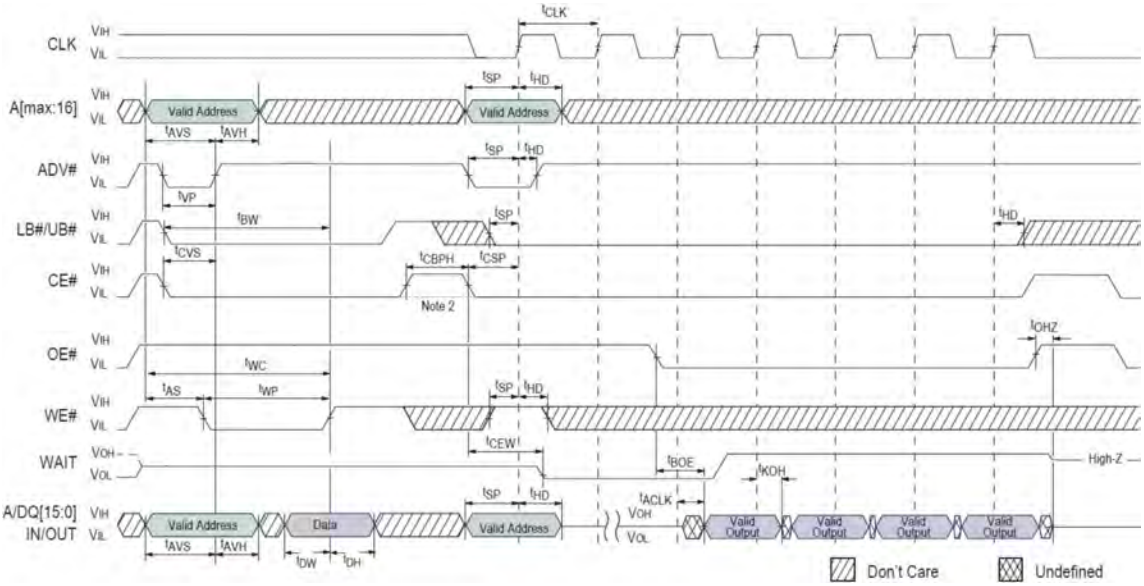
Note
1. Non-default BCR setting for burst READ at end of row: fixed or variable latency; WAIT active LOW; WAIT asserted 1 cycle advanced.
2. WAIT will be asserted for LC+1 cycles for both variable and fixed latency.

Figure 35 Burst WRITE Followed by Burst READ



Note
1. Non-default BCR settings for burst WRITE followed by burst READ: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

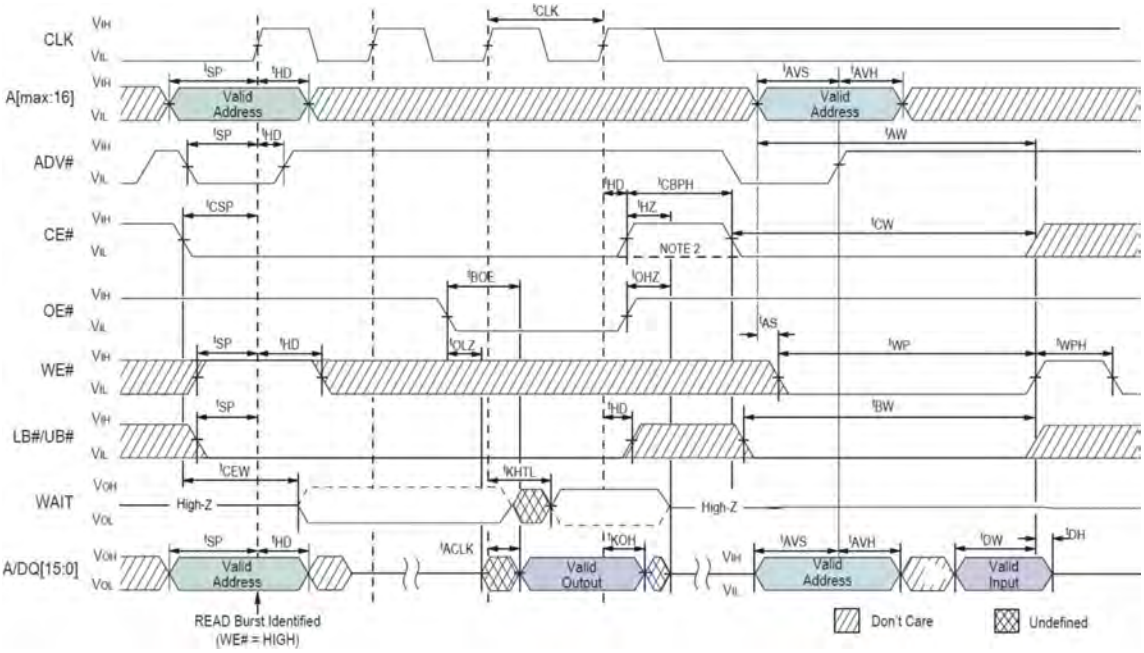
Figure 36 Asynchronous WRITE Followed by Burst READ



Note

1. Non-default BCR settings for asynchronous WRITE followed by burst READ: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning to fixed-latency burst READs. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

Figure 37 Burst READ Followed by Asynchronous WRITE



Note

1. Non-default BCR settings for burst READ followed by asynchronous WE#-controlled WRITE: Fixed or variable latency; latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, CE# must go HIGH. CE# can stay LOW when transitioning from fixed-latency burst READs; asynchronous operation begins at the falling edge of ADV#. A refresh opportunity must be provided every tCEM. A refresh opportunity is satisfied by either of the following two conditions: a) clocked CE# HIGH, or b) CE# HIGH for longer than 15ns.

14. Revision History

Vision	Who	Date	Description
1	William CHEN	Nov 16 2022	Initial branded release