



128Mbit Quad-SPI Pseudo-SRAM Data Sheet

CSS12804S

Version: 1



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The CSS12804S is general part number of 128Mb 1.8V Quad-SPI Pseudo-SRAM product family. The package type and detailed part number refers to 3. Package Information, 4 Ordering Information and 4.1 Part Number.

1. Feature and Specification

Interface:

SPI/QPI with SDR mode

Single Supply Voltage:

VDD=1.62 to 1.98V

Performance: clock update up to:

144MHz for Wrapped Burst operation

84MHz for Linear 2048 Burst operation

Organization:

128Mb, 16M x 8bits

Addressable Bit Range:

A[23:0]

Page Size:

2048 bytes

Refresh:

Self-managed

Operating Temperature Range (refer to 4.1 Part Number)

Tc = -40°C to +85°C (standard)

Tc = -40°C to +105°C (extended)

Maximum Standby Current

590µA @ 105°C

420µA @ 85°C

Typical Halfsleep™ Mode with data retained

30µA @ 25°C

Output Drive LVCMOS with programmable drive strengths of 50, 100 and 200Ω

Dedicated Wrapped Burst read and write commands

Linear 2048 Length Burst

is supported up to 84MHz and can cross page boundary as long as tCEM is met

Register Configurable Wrap Lengths of 16, 32, 64 and 2048

Software Reset

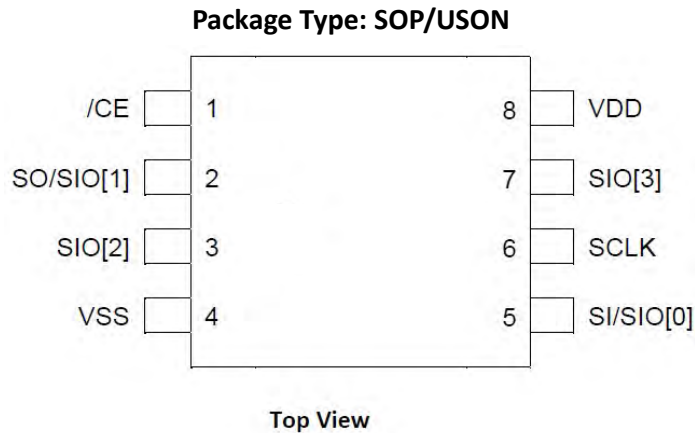
2. Description

The feature of the CSS12804S is a high speed, low pin count interface. It has 4 SDR I/O pins and operates in SPI(serial peripheral interface) or QPI (quad peripheral interface) mode with frequencies up to 144 MHz. The data input (A/DQ) to the memory relies on clock (CLK) to latch all instructions, addresses and data. It is most suitable for low-power and low cost applications like wearable or IoT devices. It incorporates a seamless self-managed refresh mechanism. Hence it does not require the support of DRAM refresh from system host. The self-refresh feature is a special design to maximize performance of memory read operation.

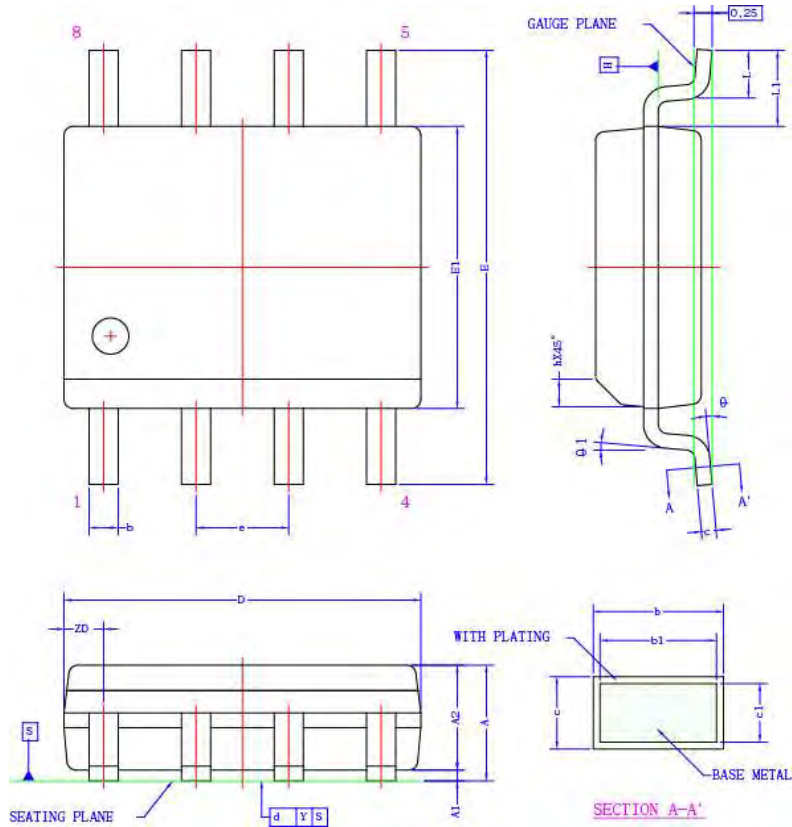
3. Package Information

The CSS12804SS is available in standard package including 8-lead SOP-8L(150)

The CSS12804SU is available in advanced package including 8-lead USON-8L(3x2mm)



3.1 Package Outline Drawing
3.1.1 SOP-8L (150) Drawing

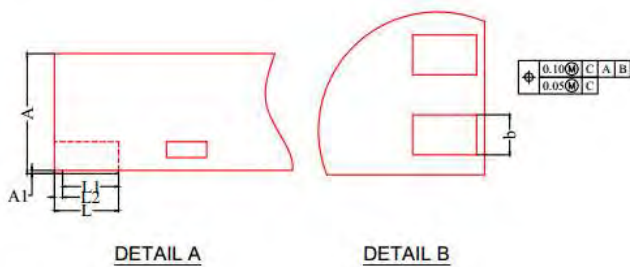
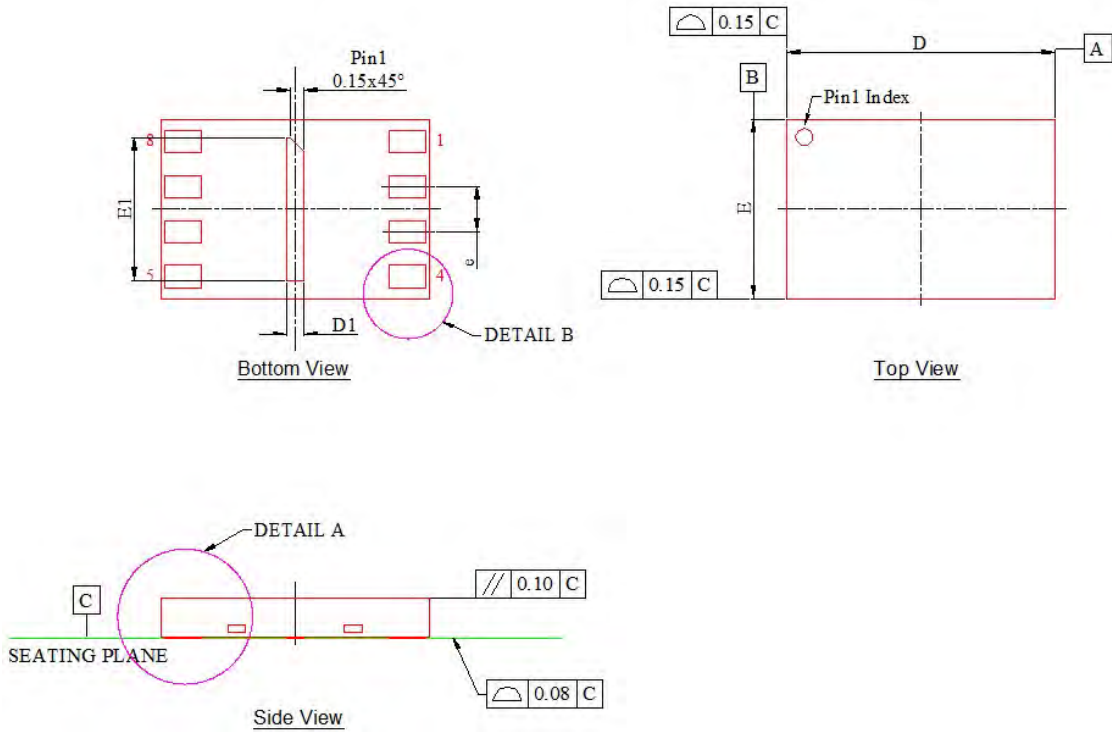


SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1,35	1,60	1,75	53	63	69
A1	0,10	0,15	0,25	4	6	10
A2	1,35	1,45	1,55	53	57	61
b	0,31	-	0,51	12	-	20
b1	0,28	0,40	0,48	11	16	19
c	0,17	-	0,25	7	-	10
c1	0,17	0,20	0,23	7	8	9
D	4,80	4,90	5,00	189	193	197
E	6,00 BSC			236 BSC		
E1	3,80	3,90	4,00	150	154	157
e	1,27 BSC			50 BSC		
L	0,40	0,66	1,27	16	26	50
L1	1,05 REF			41 REF		
ZD	0,55 REF			22 REF		
h	0,25	0,38	0,50	10	15	20
Y	-	-	0,10	-	-	4
θ	0°	-	8°	0°	-	8°
θ1	0°	-	-	0°	-	-

NOTE :

- REFER TO JEDEC STD: MS-012 AA.
- DIMENSION *D* DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION AND GATE BURRS SHALL NOT EXCEED 0,15mm PER SIDE.
DIMENSION *E1* DOES NOT INCLUDE INTERLEAD MOLD FLASH OR PROTRUSION. INTERLEAD MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0,25mm PER SIDE.
D AND *E1* DIMENSIONS ARE DETERMINED AT DATUM H.
- DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0,10mm TOTAL IN EXCESS OF THE *b* DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

3.1.2 USON-8L (3x2mm) Drawing



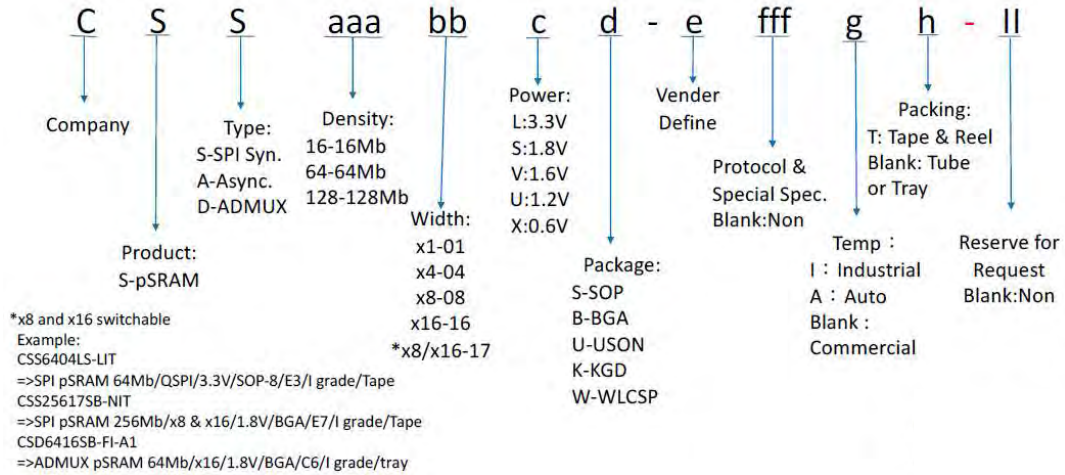
Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.40	0.45	0.50
A1	0.00	---	0.05
D	2.90	3.00	3.10
D1	0.10	0.20	0.30
E	1.90	2.00	2.10
E1	1.50	1.60	1.70
L	0.40	0.45	0.50
L1	0.30	---	---
L2	---	---	0.15
b	0.20	0.25	0.30
e	0.50 BSC		

NOTE:

- Scale 1:4
- ALL DIMENSIONS AND TOLERANCES TAKE REFERENCE TO JEDEC MO-229
- DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

4. Ordering Information

Product Naming Rule:



4.1 Part Number:

Part Number	Density	Temperature	Note
CSS12804SU-O	128Mb	0-70C	USON
CSS12804SU-OI	128Mb	-40~85C	USON
CSS12804SS-O	128Mb	0-70C	SOP8
CSS12804SS-OI	128Mb	-40~85C	SOP8
CSS12804SS-OJ	128Mb	-40~105C	SOP8

5. Package Ball Signal Table

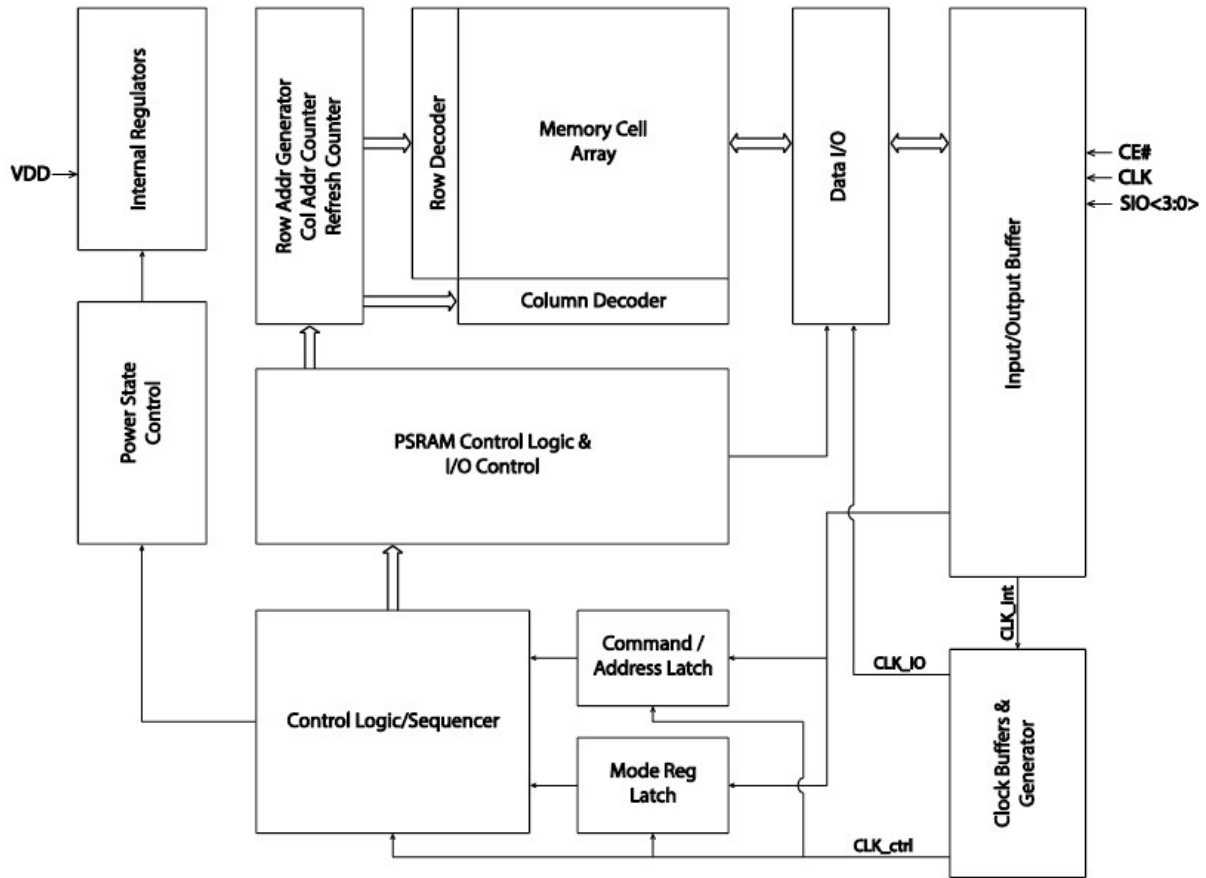
All signals are listed in below table 1

Table 1 Signals Table

Symbol	Type	SPI Mode Function		QPI Mode Function	Comments
VDD	Power	Core supply 1.8V			
VSS	Ground	Core supply ground			
CE#	Input	Chip select, active low. When CE#=1, chip is in standby			
CLK	Input	Clock Signal			
SI/SIO[0]	IO	Serial Input	IO[0]*	IO[0]	
SO/SIO[1]	IO	Serial Output	IO[1]*	IO[1]	
SIO[2]	IO	--	IO[2]*	IO[2]	
SIO[3]	IO	--	IO[3]*	IO[3]	

Note: * Quad SPI mode

6. Function Diagram

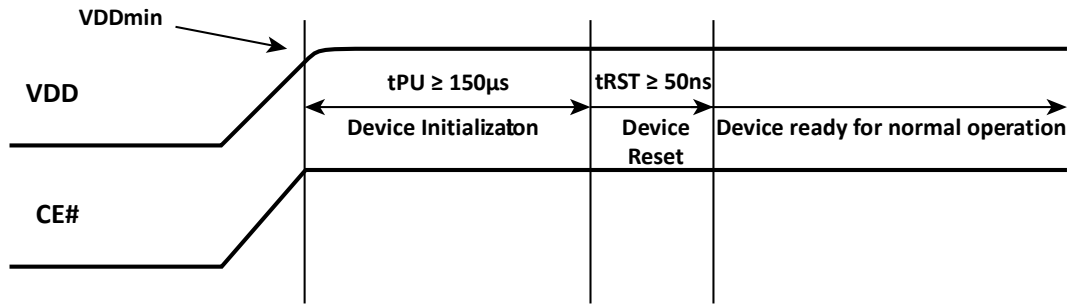


7. Powerup Initialization

This SPI/QPI products include an on-chip voltage sensor used to start the self-initialization process. When VDD reaches a stable level at or above minimum VDD, the device will require 150µs and user-issued RESET Operation to complete its self-initialization process. From the beginning of power ramp to the end of the 150µs period, CLK should remain LOW, CE# should remain HIGH (track VDD within 200mV) and SI/SO/SIO[3:0] should remain LOW.

After the Device Reset $t_{RST} \geq 50ns$ period the device is ready for normal operation.

Figure 1 Power-Up Initialization Timing



8. Interface Description

8.1 Address Space

SPI/QPI PSRAM device is byte-addressable. 128M device is addressed with A[23:0].

8.2 Page Length

Read and write operations are default page size of 2048 bytes.

8.3 Drive Strength

The device powers up in 50Ω.

8.4 Power-On Status

The device powers up in SPI Mode. It is required to have CE# high before beginning any operations.

8.5 Command/Address Latching Truth Table

The device recognizes the following commands specified by the various input methods

Table 2 True Table

Command	Code	SPI Mode (QE=0)					QPI Mode (QE=1)				
		Cmd	Addr	Wait Cycle	DIO	Max Freq.	Cmd	Addr	Wait Cycle	DIO	Max Freq.
Read	'h03	S	S	0	S	33	N/A				
Fast Read	'h0B	S	S	8	S	144/84*	Q	Q	4	Q	66
Fast Read Quad	'hEB	S	Q	6	Q	144/84*	Q	Q	6	Q	144/84*
Write	'h02	S	S	0	S	144/84*	Q	Q	0	Q	144/84*
Quad Write	'h38	S	Q	0	Q	144/84*	same as 'h02				
Wrapped Read	h8B	S	S	8	S	144	Q	Q	6	Q	144
Wrapped Write	h82	S	S	0	S	144	Q	Q	0	Q	144
Mode Register Read	hB5	S	S	8	S	144	Q	Q	6	Q	144
Mode Register Write	hB1	S	S	0	S	144	Q	Q	0	Q	144
Enter Quad Mode	'h35	S	-	-	-	144	N/A				
Exit Quad Mode	'hF5	N/A					Q	-	-	-	144
Reset Enable	'h66	S	-	-	-	144	Q	-	-	-	144
Reset	'h99	S	-	-	-	144	Q	-	-	-	144
Half Sleep Entry	'hC0	S	-	-	-	144	Q	-	-	-	144
Read ID	'h9F	S	S	0	S	33	N/A				

Remark: S = Serial IO, Q = Quad IO

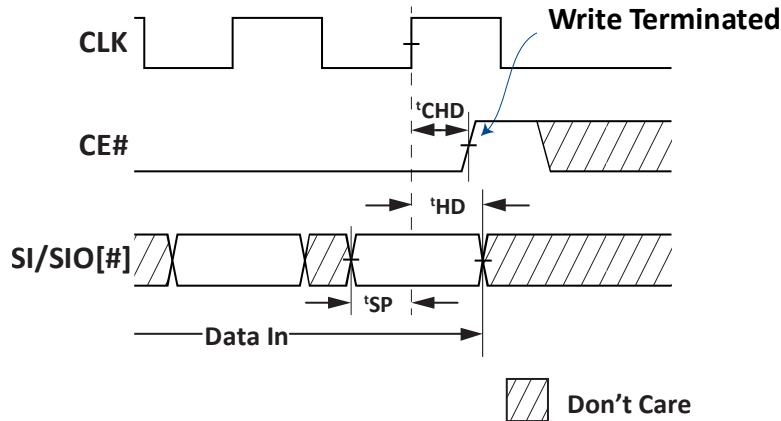
The device recognizes the following commands specified by the various input methods

Note *: Linear 2048 Length burst can be performed *crossing page boundary(RBX)* by non-Wrapped burst commands issued while setting of MRO[6:5]=11. Frequency limits are therefore: *Max Freq.* is up to 84MHz when *Linear 2048 Length*, and *Max Freq.* is 144MHz under Wrapped Burst Operation

8.6 Command Termination

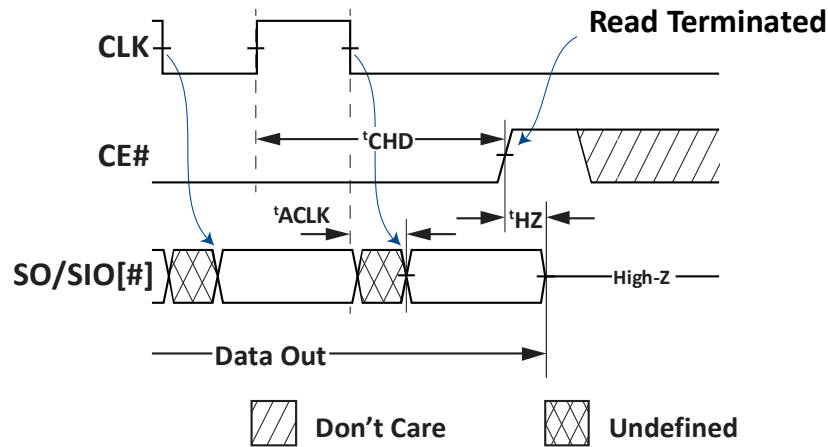
All Reads & Writes must be completed by raising CE# high immediately afterwards in order to terminate the active command and set the device into standby. Not doing so will block internal refresh operations and cause memory failure.

Figure 2 Write Command Termination



For a memory controller to correctly latch the last piece of data prior to read termination, it is recommended to provide a longer CE# hold time ($t'CHD > t'ACLK + t'CLK$) for a sufficient data window.

Figure 3 Read Command Termination



9. Mode Register Definition

Table 3 Mode Register Table

MR No.	MA[3:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	`h0	R/W	rsvd.	Wrap			rsvd.			DQ Zout

Table 4 Wrap Codes MR0[6:5]

Wrap Burst Settings		Page Boundary Crossing	
MR0[6:5]	Wrapped Length	Non-Wrap CMDs (`h03,`h0B,`hEB,`h02,`h38)	Wrap CMDs(`h8B,`h82)
00	16	Wrap 16, no cross page boundary	
01	32	Wrap 32, no cross page boundary	
10	64	Wrap 64, no cross page boundary	
11 (default)	2048 (page size)	Linear, can cross page boundary	Wrap 2048, no cross page boundary

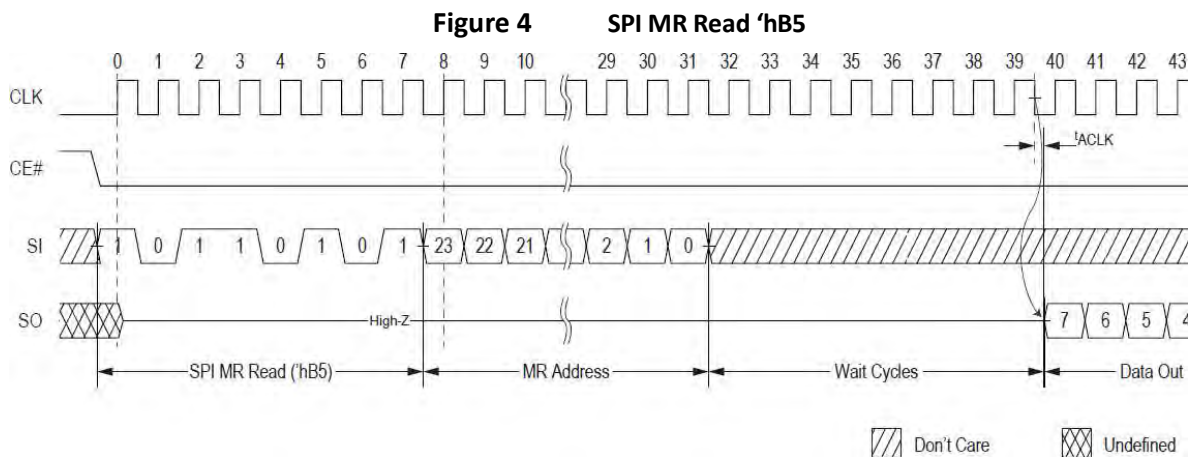
Table 5 DQ Output Drive Strength Codes MR0[1:0]

DQ Output Drive Strength	
MR0[1:0]	Impedance
00(default)	50Ω
01	100Ω
10	200Ω
others	reserved

10. Mode Register Operations

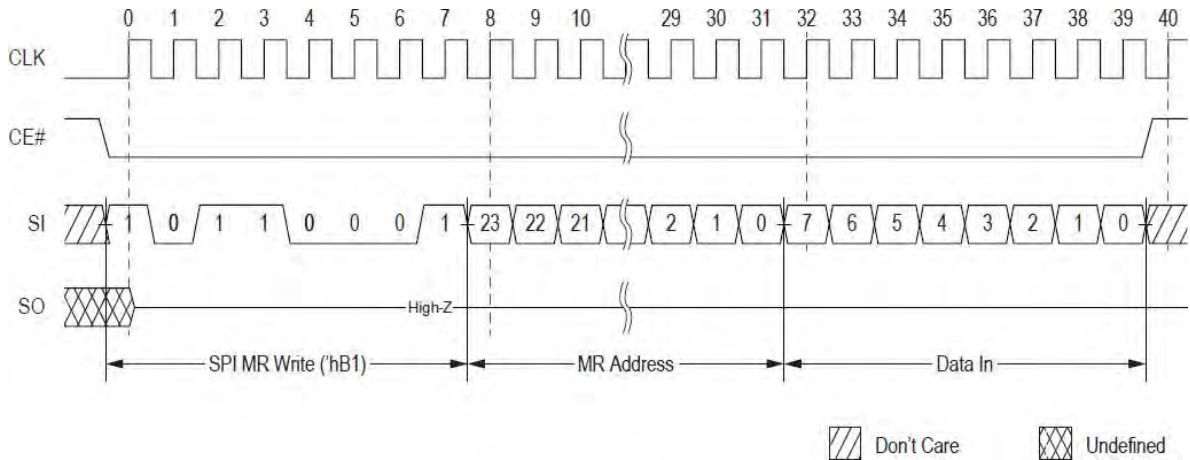
10.1 SPI MR Read Operation

For all reads, MR data will be available ^tACLK after the falling edge of CLK.



10.2 SPI MR Write Operation

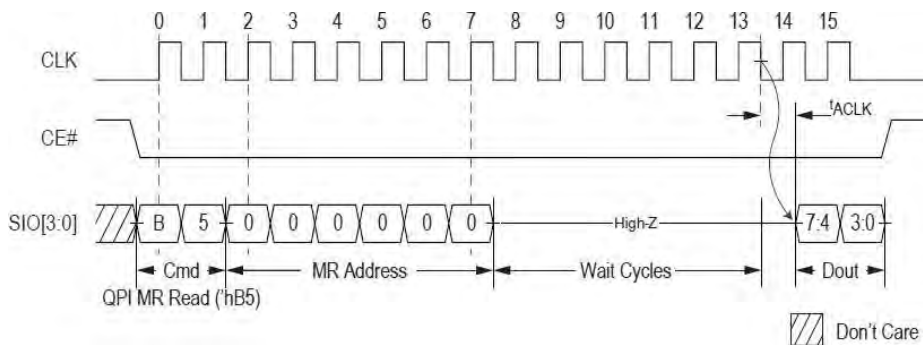
Figure 5 SPI MR Write 'hB1



10.3 QPI MR Read Operation

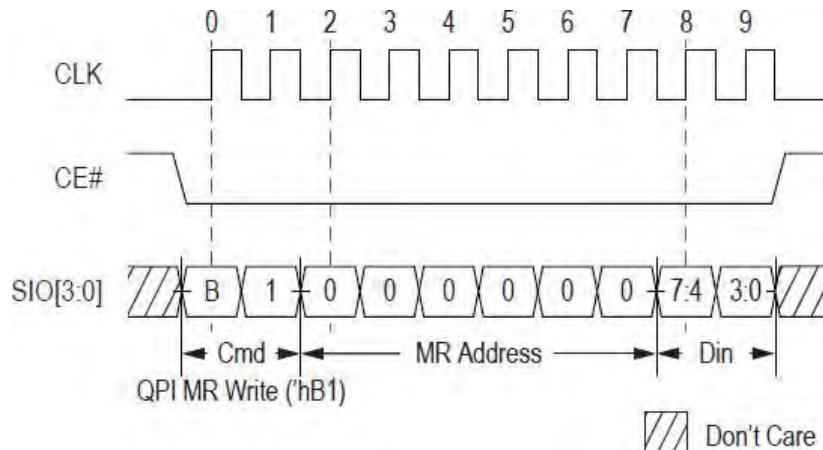
For all reads, MR data will be available ^tACLK after the falling edge of CLK.

Figure 6 QPI MR Read 'hB5



10.4 QPI MR Write Operation

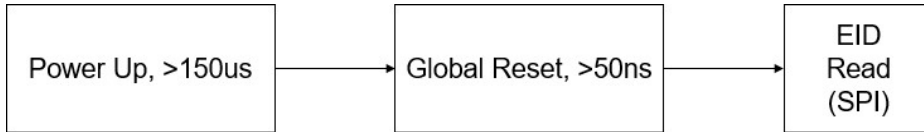
Figure 7 QPI MR Write 'hB1



11. Read ID

Read ID command provides information of vendor ID, known-good-die, device density, and manufacturing ID. Note that Read ID command can be used ONLY as Power up initialization after the device Reset $t_{RST} \geq 50ns$ right after Global Reset command.

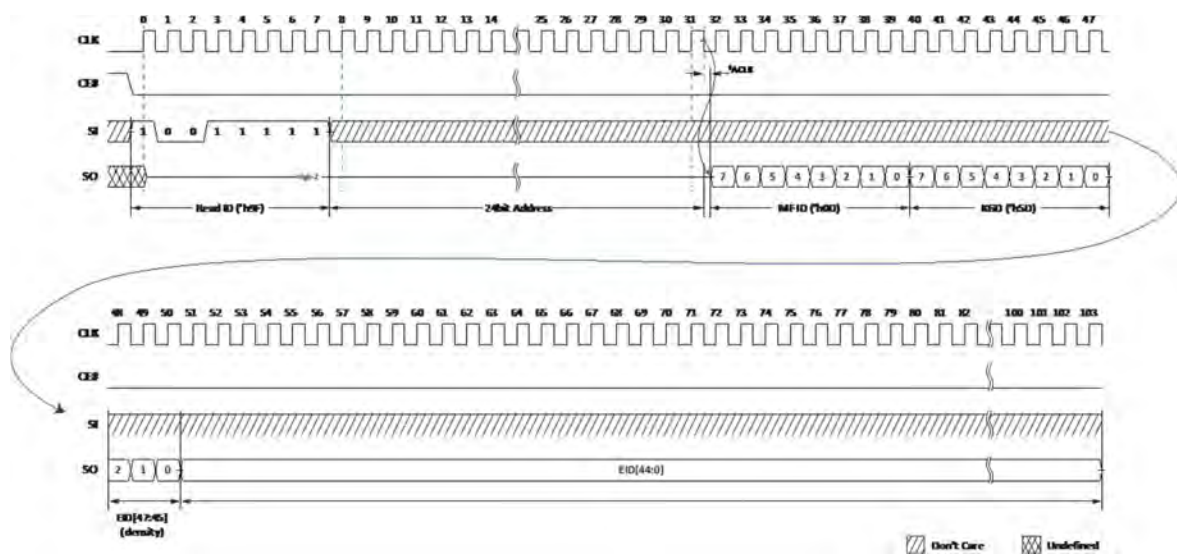
Figure 8 Pre-condition of EID Read



11.1 SPI Read ID Operation

This command is similar to Fast Read, but without the wait cycles and the device outputs EID value instead of data.

Figure 9 SPI Read ID 'h9F (available only in SPI mode)



12. Halfsleep™ Mode Operation

Halfsleep™ Mode is a feature which puts the device in an ultra-low power state, while the stored data is retained. Halfsleep™ Mode Entry can be entered by issuing a command 'hC0. CE# going high initiates the Halfsleep™ mode and must be maintained for the minimum duration of 't_{HS}. The Halfsleep™ Entry command sequences are shown below.

Figure 10 SPI Halfsleep™ Entry 'hC0.

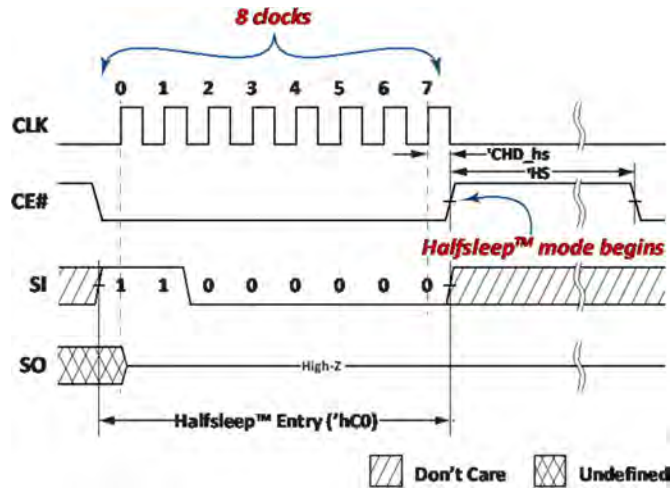
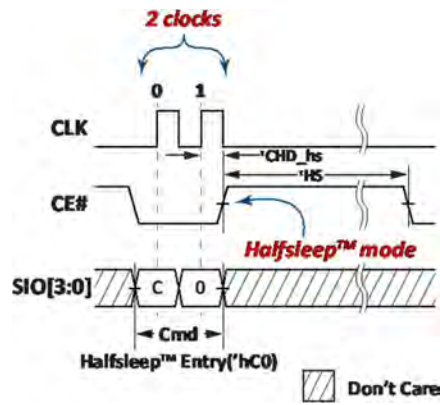
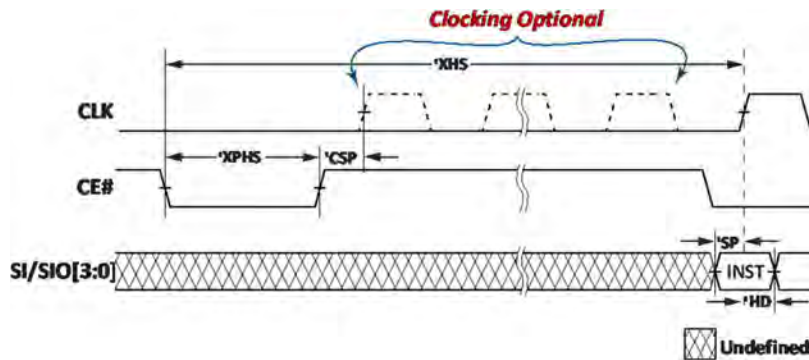


Figure 11 QPI Halfsleep™ Entry 'hC0



Halfsleep™ Exit is initiated by a low pulsed CE#. Afterwards, CE# can be held high with or without clock toggling until the first operation begins (observing minimum tXHS).

Figure 12 Halfsleep™ Exit



13. SPI Mode Operations

The device powers up into SPI mode by default but can also be switched into QPI mode.

13.1 SPI Read Operations

For all reads, data will be available t_{ACLK} after the falling edge of CLK.

SPI Reads can be done in four ways:

1. 'h03: Serial CMD, Serial Addr/IO, slow frequency, with wrap or linear bursting.
2. 'h0B: Serial CMD, Serial Addr/IO, fast frequency, with wrap or linear bursting.
3. 'hEB: Serial CMD, Quad Addr/IO, fast frequency, with wrap or linear bursting.
4. 'h8B: Serial CMD, Serial Addr/IO, fast frequency, with forced wrap (register configurable lengths).

Figure 13 SPI Read 'h03 (max freq 33MHz)

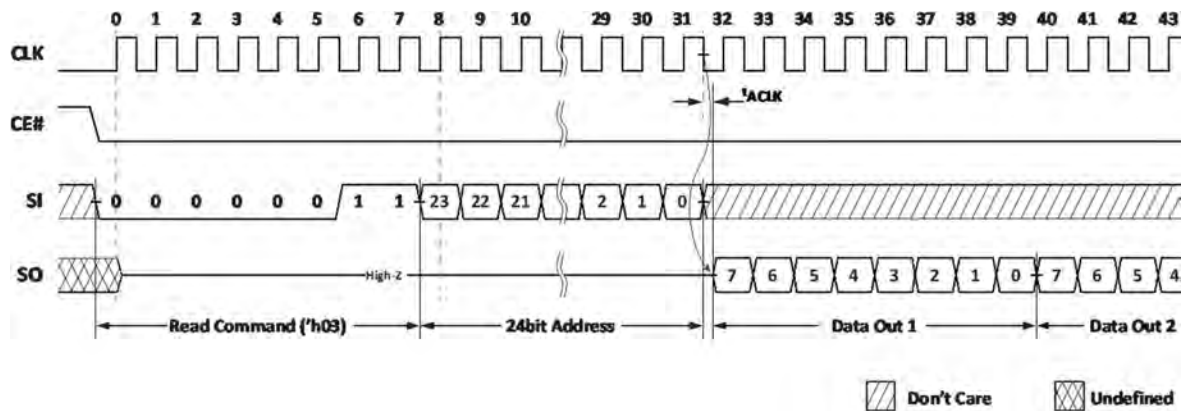


Figure 14 SPI Fast Read 'h0B (max freq 144/84 MHz)

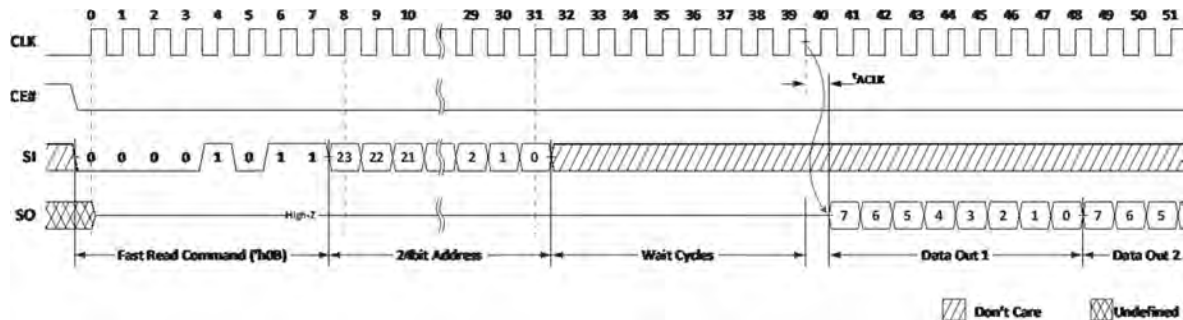
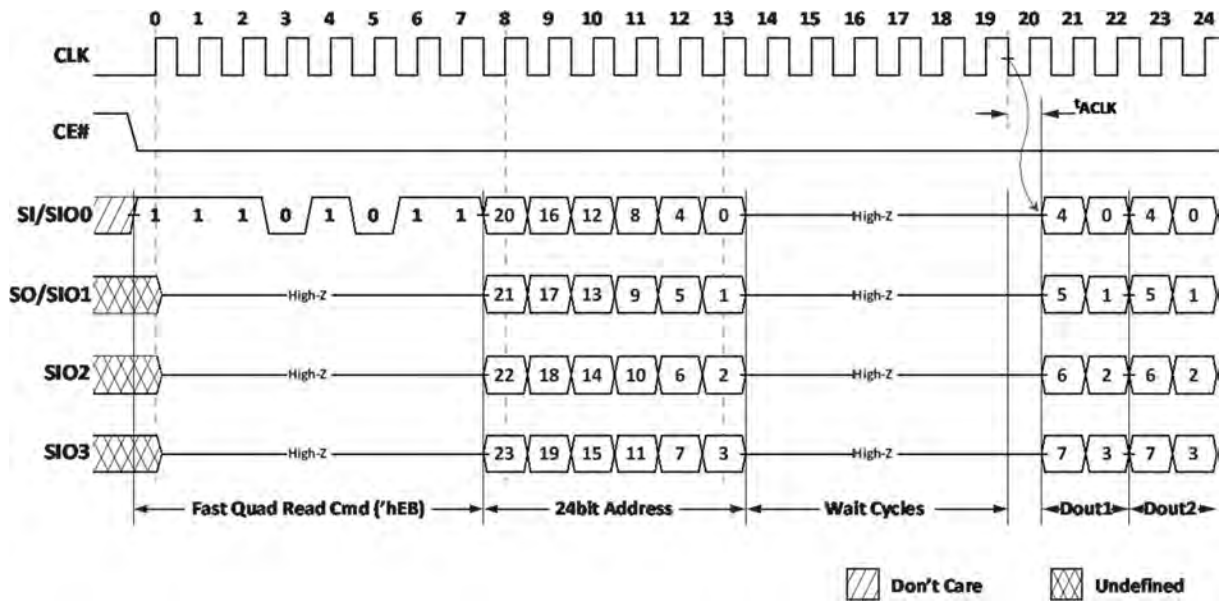


Figure 15 SPI Fast Quad Read 'hEB (max freq 144/84 MHz)



13.2 SPI Write Operation

Figure 16 SPI Write 'h02

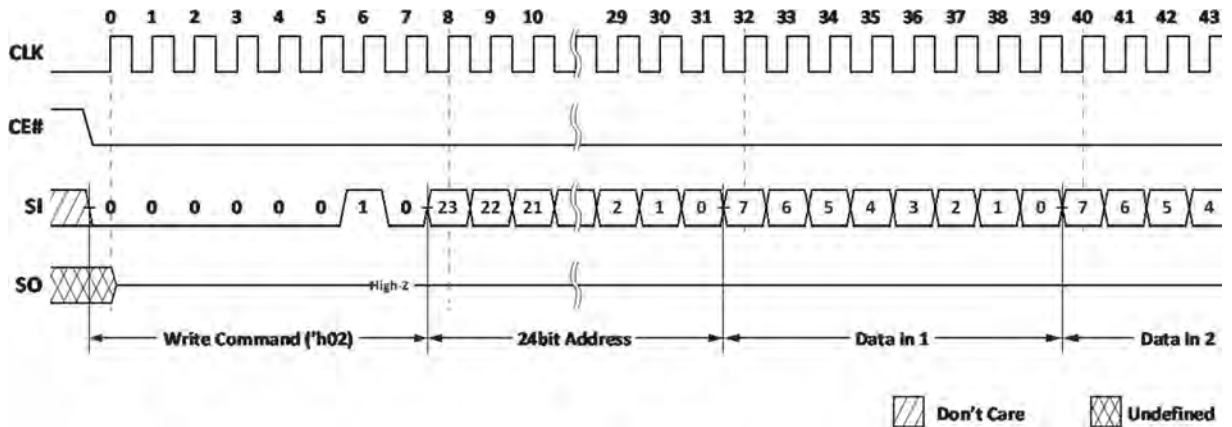
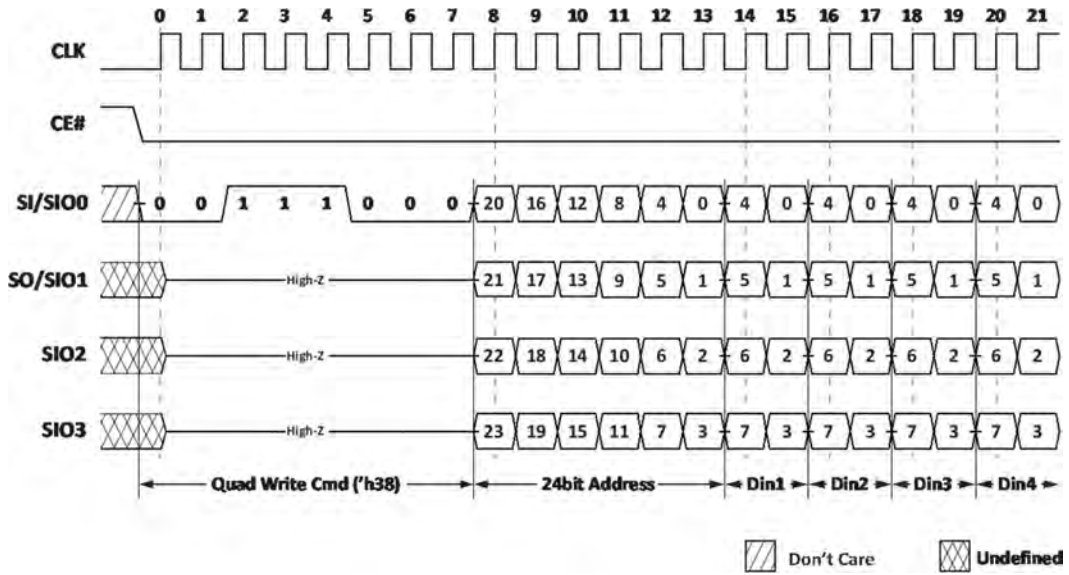


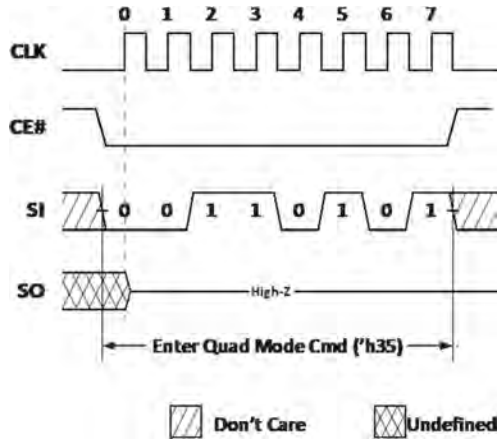
Figure 17 SPI Quad Write 'h38



13.3 SPI Quad Mode Enable Operation

This command switches the device into quad IO mode

Figure 18 Quad Mode Enable 'h35 (available only in SPI mode)



14. QPI Mode Operations

14.1 QPI Read Operations

For all reads, data will be available t_{ACLK} after the falling edge of CLK.

QPI Reads can be done in one of three ways:

1. 'h0B: Quad CMD, Addr & IO, slow frequency with wrap or linear bursting.
2. 'hEB: Quad CMD, Addr & IO, fast frequency with wrap or linear bursting.
3. 'h8B: Quad CMD, Addr & IO, fast frequency with forced wrap (register configurable lengths).

Figure 19 QPI Fast Read 'h0B (max freq 66 MHz)

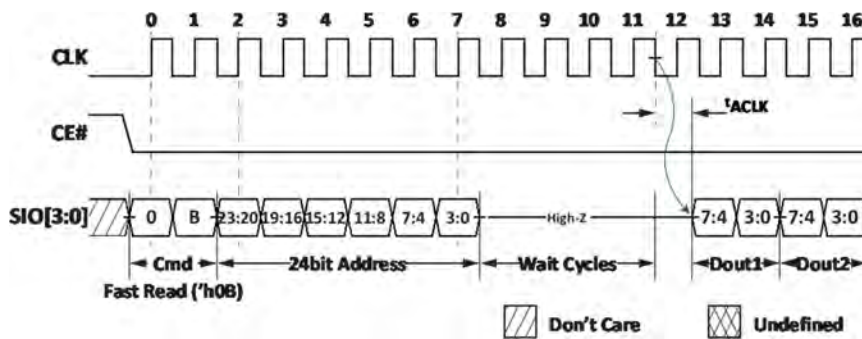
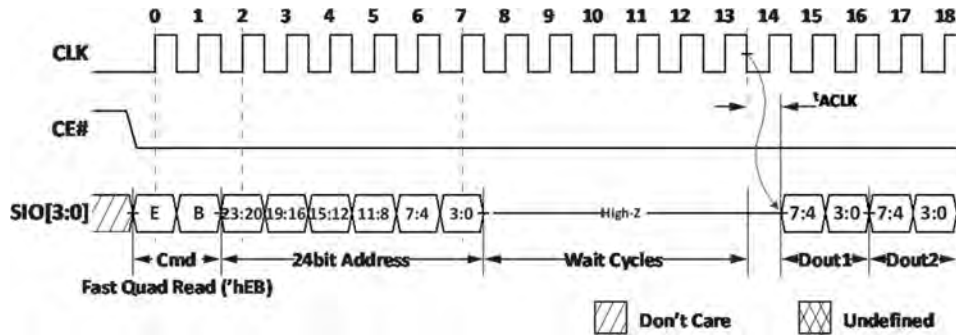


Figure 20 QPI Fast Quad Read 'hEB (max freq 144/84 MHz)

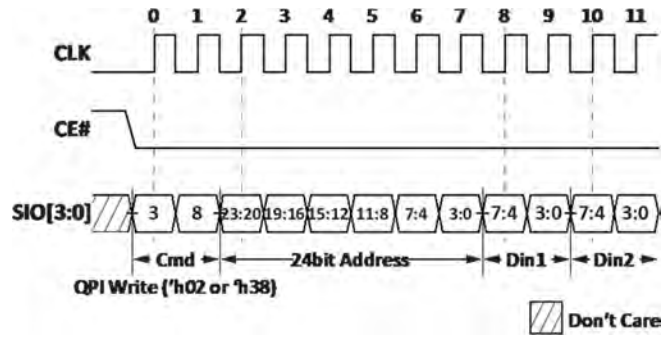


14.2 QPI Write Operation(s)

QPI write command can be done in one of two ways.

1. 'h02 or 'h38: Quad CMD, Addr & IO, with wrap or linear bursting.
2. 'h82: Quad CMD, Addr & IO, with forced wrap (register configurable lengths).

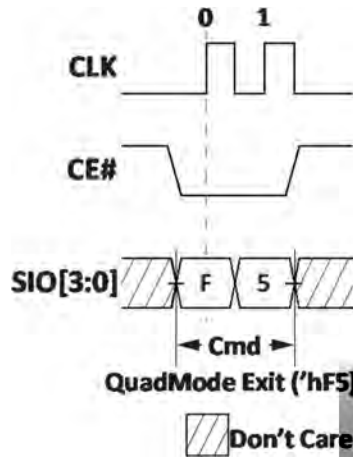
Figure 21 QPI Write



14.3 QPI Quad Mode Exit Operation

This command will switch the device back into serial IO mode.

Figure 22 Quad Mode Exit 'hF5 (only available in QPI mode)



15. Reset Operation

The Reset operation is used as a system (software) reset that puts the device in SPI standby mode which is also the default mode after power-up. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST)

Figure 23 SPI Reset

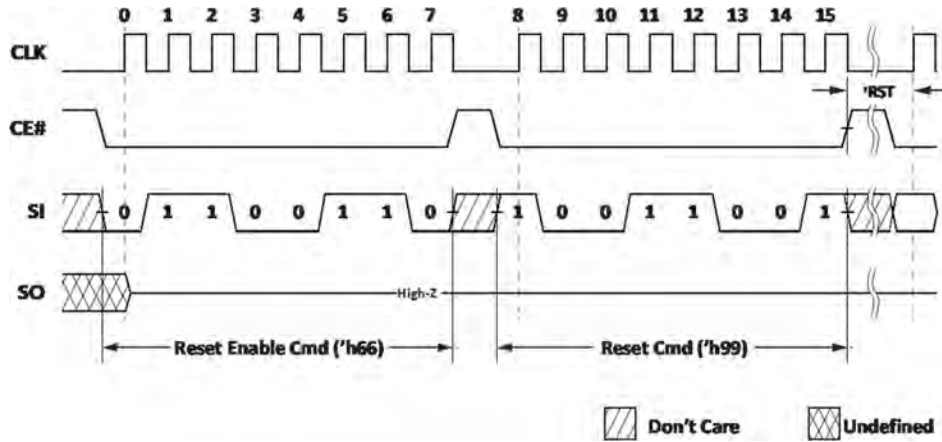
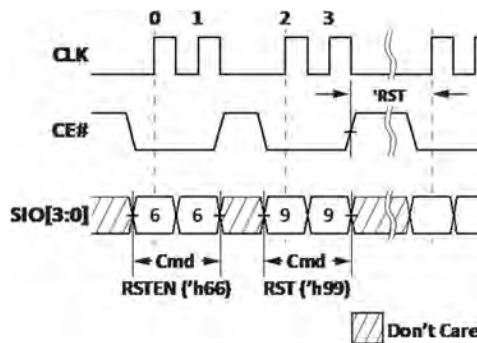


Figure 24 QPI Reset



Reset command has to immediately follow the Reset-Enable command in order for the reset operation to take effect. Any command other than the Reset command after the Reset-Enable command will cause the device to exit Reset-Enable state and abandon reset operation.

16. Input/Output Timing

Figure 25 Input Timing

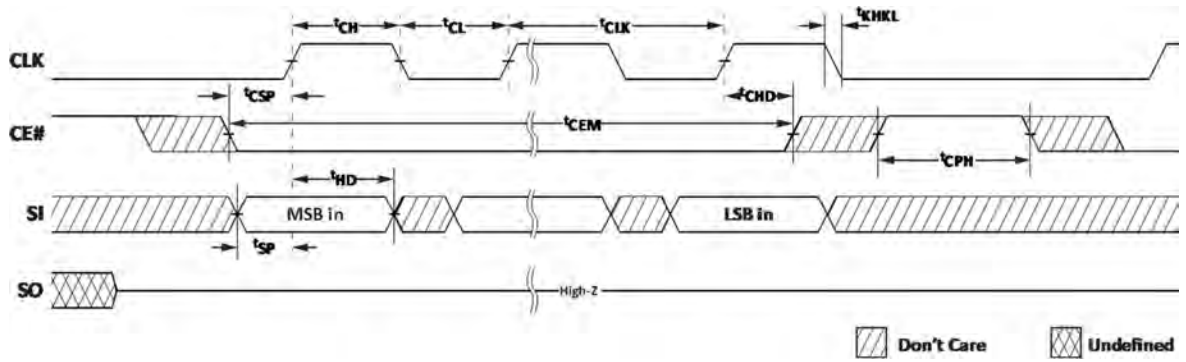
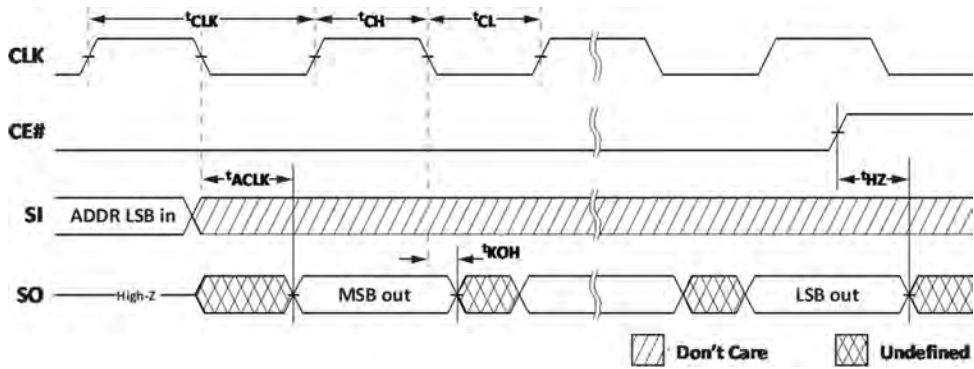


Figure 26 Output Timing



17. Electrical Specifications

17.1 Absolute Maximum Ratings

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage to any ball except V _{DD} relative to	V _T	-0.4 to V _{DD} +0.4	V	
Voltage on V _{DD} supply relative to V _{SS}	V _{DD}	-0.4 to +2.45	V	
Storage Temperature	T _{STG}	-55 to +150	°C	1

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

17.2 Pin Capacitance

Table 7 Pin Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	C _{IN}		6	pF	V _{IN} =0V
Output Pin Capacitance	C _{OUT}		8	pF	V _{OUT} =0V

Note: spec'd at 25°C.

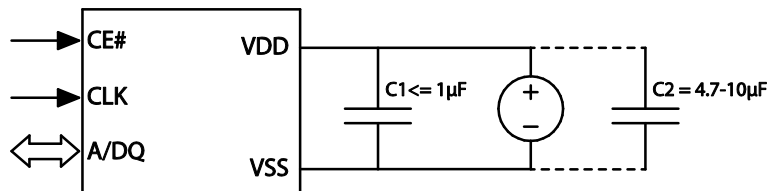
Table 8 Load Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Load Capacitance	C _L		15	pF	

Note: System C_L for the use of package

17.3 Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.



17.3.1 Low ESR cap C1:

It is recommended to place a low ESR decoupling capacitor of $\leq 1\mu\text{F}$ close to the device to absorb transient peaks.

17.3.2 Large cap C2:

Though half-sleep average current is small (less than 100 μ A), its peak current from internal periodical burst refresh can reach up to the level of 25mA. The peak current duration can last for few tens of microseconds. During this period if the system regulator cannot supply such large peaks, it is important to place a 4.7 μ F-10 μ F cap to cover the burst refresh current demand and replenish the cap before the next burst of refresh.

17.4 Operating Conditions

Table 9 Operating Characteristics

Parameter	Min	Max	Unit	Notes
Operating Temperature (extended)	-40	105	°C	
Operating Temperature (standard)	-40	85	°C	

17.5 DC Characteristics

Table 10 DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
V _{DD}	Supply Voltage	1.62	1.98	V	
V _{IH}	Input high voltage	V _{DD} -0.4	V _{DD} +0.2	V	
V _{IL}	Input low voltage	-0.2	0.4	V	
V _{OH}	Output high voltage (I _{OH} =-0.2mA)	0.8 V _{DD}		V	
V _{OL}	Output low voltage (I _{OL} =+0.2mA)		0.2 V _{DD}	V	
I _I	Input leakage current		1	μ A	
I _O	Output leakage current		1	μ A	
I _{CC}	Read/Write (144MHz)		11	mA	1,2
	Read/Write (66MHz)		8.5	mA	1,2
	Read/Write (13MHz)		6	mA	1,2
ISB _{EXT}	Standby current (105C)		590	μ A	3
ISB _{STD}	Standby current (85C)		420	μ A	3

- Note :
1. Output load current not included.
 2. 50% bus toggling rate
 3. Standby current is measured when CLK is in DC low state.
 4. Typical ISB_{STDROOM} is 66 μ A.
 5. Typical ISB_{STD_HS} is 30 μ A.

17.6 AC Characteristics

Table 11 Read/Write Timing

Symbol	Parameter	Min	Max	Unit	Notes
t'CLK	CLK period - SPI Read ('h03)	30.3		ns	33MHz
	CLK period - QPI Read ('h0B)	15.1			66MHz
	CLK period - all other operations	7			144MHz*1,2,3
t'CH/t'CL	Clock high/low width	0.45	0.55	t'CLK(min)	
t'KHKL	CLK rise or fall time		1.1	ns	4
t'CPH	CE# HIGH between subsequent burst operations	18		ns	
t'CEM	CE# low pulse width (excluding Halfsleep™ Exit)		8	μs	Standard temp
			3		Extended temp
t'CSP	CE# setup time to CLK rising edge PKG	2.5		ns	2
t'CHD	CE# hold time from CLK rising edge PKG	3		ns	2
t'SP	Setup time to active CLK edge	2		ns	
t'HD	Hold time from active CLK edge	2		ns	
t'CHD_HS	CE# hold time from CLK rising edge for Halfsleep™ Entry command	6		ns	
t'HZ	Chip disable to DQ output high-Z		6	ns	
t'ACLK	CLK to output delay	2	5.5	ns	3
t'KOH	Data hold time from clock falling edge	1.5		ns	
t'HS	Minimum Halfsleep™ duration	150		μs	
t'XHS	Halfsleep™ Exit CE# low to CLK setup time	150		μs	
t'XPHS	Halfsleep™ Exit CE# low pulse width	60		ns	
			tCEM	μs	
t'RST	Time between end of RST CMD to next valid CMD	50		ns	

Note:

1. Only Linear 2048 Burst allows page boundary crossing. Frequency limits are therefore 144MHz max for Wrapped Burst operation, 84MHz max when Linear 2048 Burst commands cross page boundary.
2. System max C_L 15pF for the use of package.
3. For operating frequencies >84MHz, it is highly recommended to utilize CLK falling edge to sample read data or align sampling clock via data pattern tuning (refer to JEDEC JESD84-B50 for an example).
4. Measured from 20% to 80% of VDD



18. Revision History

Vision	Who	Date	Description
1	William CHEN	Apr 27 2023	Initial branded release