128Mbit DDR Octal-SPI Pseudo-SRAM Data Sheet

CSS12808S

Version: 1

Table of Contents

The CSS12808S is general part number of 128Mb Octal-SPI Pseudo-SRAM product family. The package type and detailed part number refers to 3. Package Information, 4 Ordering Information and 4.1 Part Number.

1. Feature and Specification

Single Supply Voltage

VDD=1.62 to 1.98V

DQ=1.62 to 1.98V

Interface: Octal SPI with DDR mode, two bytes transfers per one clock cycle

Performance: Clock rate up to 200MHz, 400MB/s read/write throughput

Organization: 128Mb, 16M x 8bits with 1024 bytes page size

Column address: AY0 to AY9

Row address: AX0 to AX13

Refresh: Self-managed

Operating Temperature Range

Tc = -40°C to +85°C (standard range)

Tc = -40°C to +105°C (extended range)

Maximum Standby Current

600µA @ 105°C

400µA @ 85°C

Typical Standby Current

40µA @ 25°C (Halfsleep™ Mode with data retained)

Low Power Features

Partial Array Self-Refresh (PASR)

Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor

User configurable refresh rate

Ultra Low Power (ULP) Halfsleep™ mode with data retained

Software Reset

Reset Pin Available

Output Driver LVCMOS with programmable drive strength

Data Mask (DM) for write data

Data Strobe (DQS) enabled high speed read operation

Register Configurable write and read initial latencies

Write Burst Length, maximum 1024 bytes, minimum 2 bytes

Wrap & Hybrid Burst in 16/32/64/1K lengths

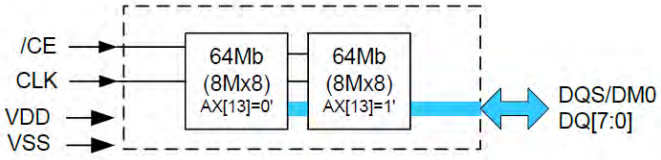
Linear Burst Command

Row Boundary Crossing (RBX)

Read operations can be enabled via Mode Register.

RBX Write is NOT supported

RA[13] Boundary Crossing is NOT supported between 2 dies



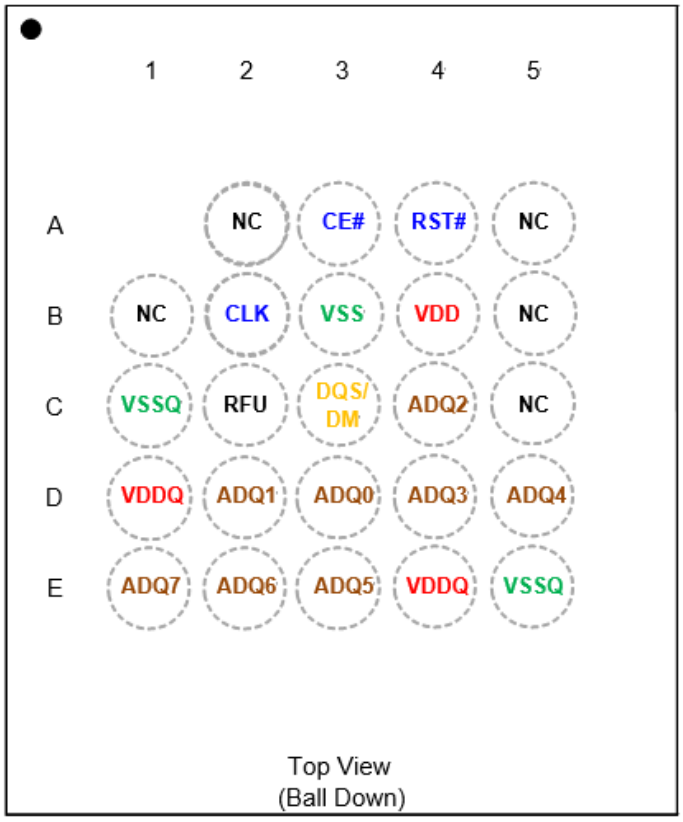
2. Description

The feature of the CSS12808SB is a high speed, low pin count interface. It operates in OPI (Octal peripheral interface) mode with Double Data Rate (DDR) under frequencies up to 200Mhz. It is most suitable for low-power and low-cost applications like wearable or IoT devices. It incorporates a seamless self-managed refresh mechanism.

3. Package Information

The CSS12808SB is available in standard package 24b mini-FBGA 6 x 8 x 1.2mm, ball pitch 1.0mm, ball size 0.4mm.

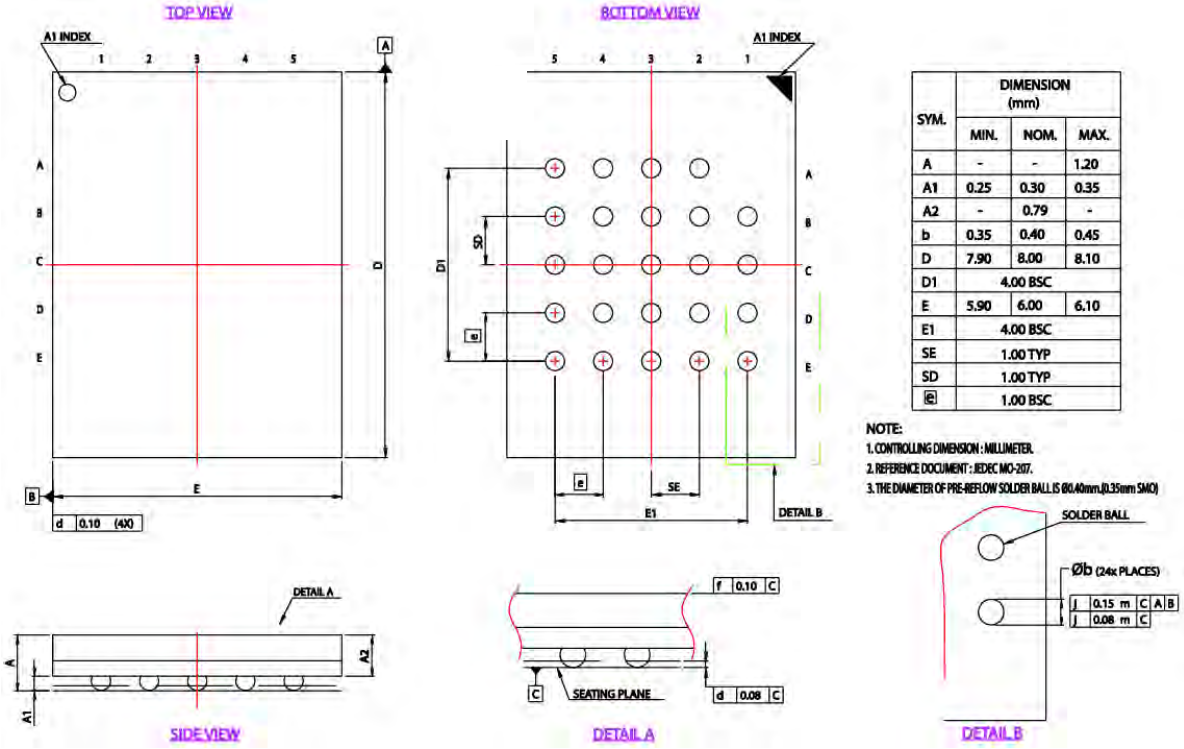
Ball Assignment of 24b mini-FBGA (6x8x1.2mm)(P1.0)(B0.4)



Note:
1. RFU: Reserved for Future Use, which is reserved for 2nd CE#.
2. NC: No Connection internally.

3.1 Package Outline Drawing

3.1.1 24b Mini-FBGA Drawing



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.25	0.30	0.35
A2	-	0.79	-
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
SE	1.00 TYP		
SD	1.00 TYP		
e	1.00 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.
3. THE DIAMETER OF PRE-REFLOW SOLDER BALL IS Ø0.40mm (Ø0.35mm SMO)

4. Ordering Information

Product Naming Rule:

C S S aaa bb c d - e fff g h - II

- C: Company
- S: Product: S-pSRAM
- S: Type: S-SPI Syn. A-Async. D-ADMUX
- aaa: Density: 16-16Mb 64-64Mb 128-128Mb
- bb: Width: x1-01 x4-04 x8-08 x16-16 *x8/x16-17
- c: Power: L:3.3V S:1.8V V:1.6V U:1.2V X:0.6V
- d: Package: S-SOP B-BGA U-USON K-KGD W-WLCSP
- e: Vender Define
- fff: Protocol & Special Spec. Blank:Non
- g: Temp : I : Industrial A : Auto Blank : Commercial
- h: Packing: T: Tape & Reel Blank: Tube or Tray
- II: Reserve for Request Blank:Non

*x8 and x16 switchable
Example:
CSS6404LS-LIT
=>SPI pSRAM 64Mb/QSPI/3.3V/SOP-8/E3/I grade/Tape
CSS25617SB-NIT
=>SPI pSRAM 256Mb/x8 & x16/1.8V/BGA/E7/I grade/Tape
CSD6416SB-FI-A1
=>ADMUX pSRAM 64Mb/x16/1.8V/BGA/C6/I grade/tray

4.1 Part Number:

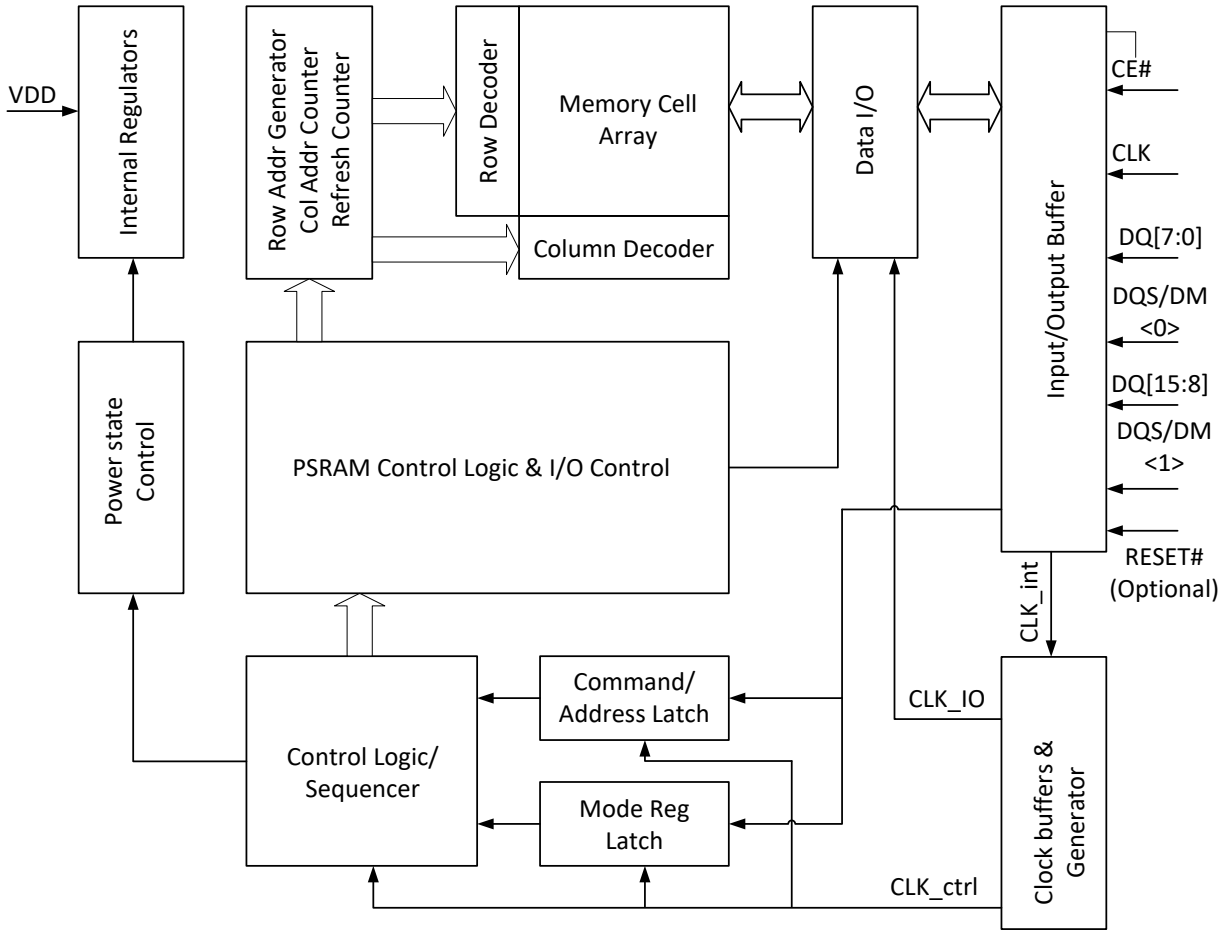
Part Number	Density	Temperature	Note
CSS12808SB-LI	128Mb	-40~85C	24b FBGA
CSS12808SB-LJ	128Mb	-40~105C	24b FBGA
CSS12808SQ-LI	128Mb	-40~85C	QFN
CSS12808SQ-LJ	128Mb	-40~105C	QFN

5. Package Ball Signal Table

Table 1 Signals Table

Symbol	Type	Description	Comments
V_{DD}	Power	Core supply 1.8V	
V_{DDQ}	Power	IO supply 1.8V	
V_{SS}	Ground	Core supply ground	
V_{SSQ}	Ground	IO supply ground	
A/DQ[7:0]	IO	Address/DQ bus [7:0]	
DQS/DM	IO	DQ strobe clock during reads, Data mask during writes. DM is active high. DM=1 means “do not write”.	
CE#	Input	Chip select, active low. When CE#=1, chip is in standby state.	
CLK	Input	Clock signal	
RESET#	Input	Reset signal, active low. Optional, as the pad is internally tied to a weak pull-up and can be left floating.	

6. Block Diagram



7. Powerup Initialization

This Octal DDR products include an on-chip voltage sensor used to start the self-initialization process. V_{DD} and V_{DDQ} must be applied simultaneously. When they reach a stable level at or above minimum V_{DD}, the device is in Phase 1 and will require 150µs to complete its self-initialization process. The user can then proceed to Phase 2 of the initialization described in this section.

During Phase 1 CE# should remain HIGH (track V_{DD} within 200mV); CLK should remain LOW.

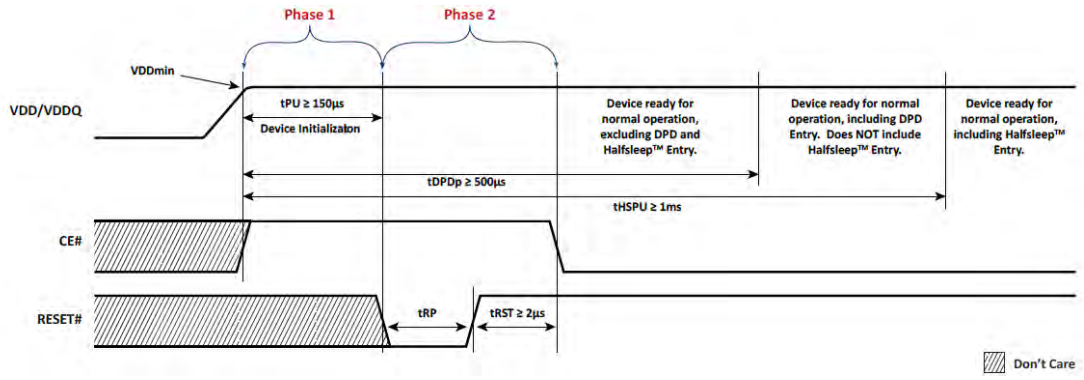
After Phase 2 is completed the device is ready for operation, however Halfsleep™ entry and Deep Power Down (DPD) entry are not available until Halfsleep™ Power Up (tHSPU) or DPD Power Up (tDPDp) duration is observed.

After the Device Reset tRST≧50ns period the device is ready for normal operation.

7.1 Power-Up Initialization Method 1 (via. RESET# pin)

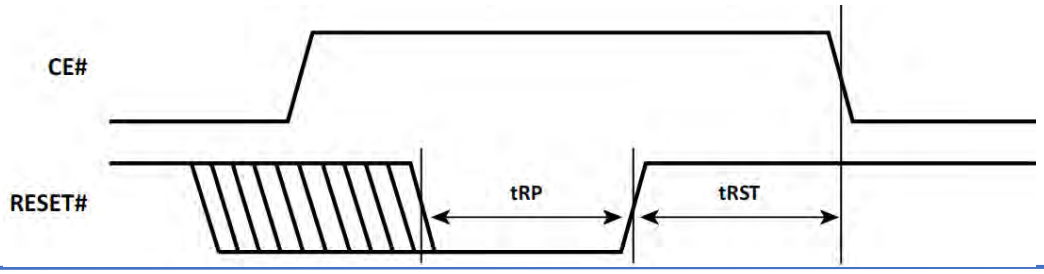
The RESET# pin can be used to initialize the device during Phase 2 as follows:

Figure 1 Power-Up Initialization Method 1 RESET#



The RESET# pin can also be used when CE#=high at any time after the device is initialized to reset all register contents. Memory content is not guaranteed. Timing requirements for RESET# usage are shown below Figure 2.

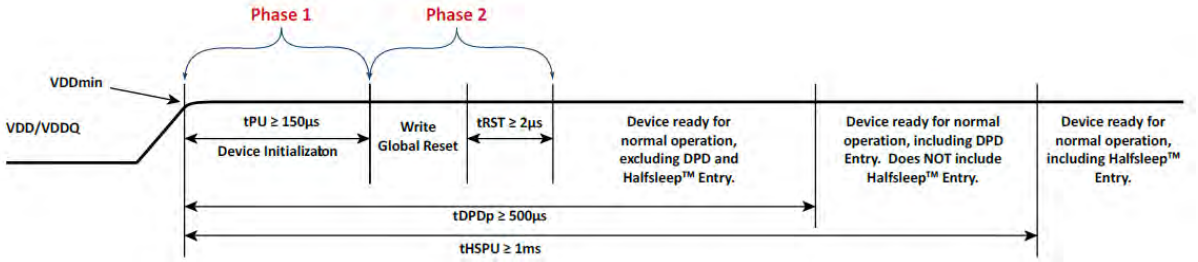
Figure 2 Reset# Timing



7.2 Power-Up Initialization (via. Global Reset)

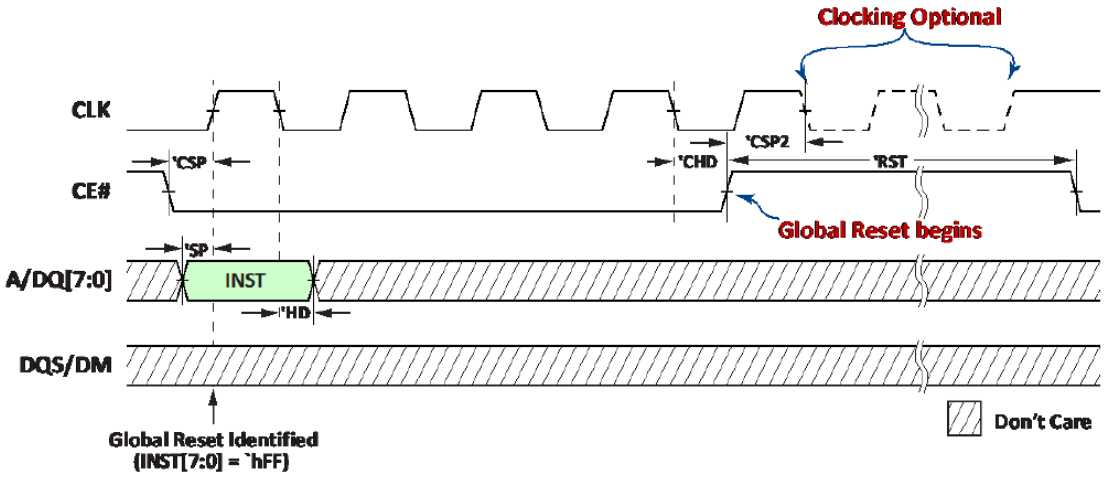
As an alternate power-up initialization method, after the Phase 1 150µs period the Global Reset command can also be used to reset the device in Phase 2 as follows:

Figure 3 Power-Up Initialization Timing with Global Reset



The Global Reset command resets all register contents. Memory content is not guaranteed. The command frame is made of 4 clocked CE# lows. Clocking is optional during tRST. The Global Reset command sequence is shown below. Note that Global Reset command can be used ONLY as Power-up initialization.

Figure 4 Global RESET



8. Interface Description

8.1 Address Space

Octal DDR PSRAM device is byte-addressable. Memory accesses are required to start on even addresses (A[0]=’0). Mode Register accesses allow both even and odd addresses.

8.2 Burst Type and Length

Read and write operations are default Hybrid Wrap 32 mode. Other burst lengths of 16, 32, 64 or 1K bytes in standard or Hybrid wrap modes are register configurable (see Table 16). The device also includes command for Linear Bursting. Bursts can start on any even address. Write burst length has a minimum of 2 bytes. Read has no minimum

length. Both write and read have no restriction on maximum burst length as long as tCEM is met.

8.3 Command/Address Latching

After CE# goes LOW, instruction code is latched on 1st CLK rising edge. Access address is latched on the 3rd, 4th, 5th & 6th CLK edges (2nd CLK rising edge, 2nd CLK falling edge, 3rd CLK rising edge, 3rd CLK falling edge).

8.4 Command Truth Table

The Octal DDR PSRAM recognizes the following commands specified on the INST (Instruction) cycle defined by the Address/DQ pins.

Note that Linear Burst commands, 20h and A0h, ignore burst setting defined by MR8[2:0]. Note that only Linear Burst Read command is capable of performing row boundary crossing (RBX) read function.

Command	1st CLK	2nd CLK		3rd CLK	
Sync Read	00h	A3	A2	A1	A0
Sync Write	80h	A3	A2	A1	A0
Sync Read (Linear Burst)	20h	A3	A2	A1	A0
Sync Write (Linear Burst)	A0h	A3	A2	A1	A0
Mode Register Read	40h	×			MA
Mode Register Write	C0h	×			MA
Global Reset	FFh	×			

Remarks:
× = don't care (V_{IH}/V_{IL})
A3 = unused address bits are reserved
A2 = RA[13:6]
A1 = RA[5:0],CA[9:8]
A0 = CA[7:0]
MA = Mode Register Address

8.5 Read Operation

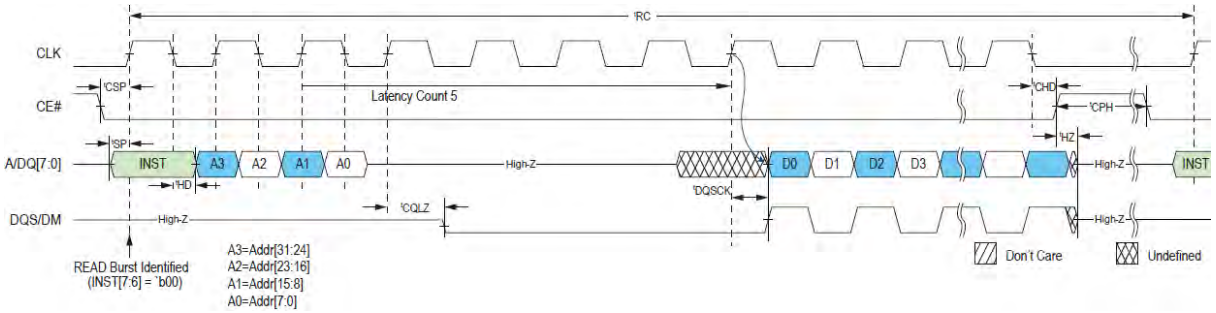
After address latching, the device initializes DQS/DM to '0 from next CLK rising edge of the 3rd clock cycle (A1). Please read Figure 5.

Output data is available after LC latency cycles, as shown in Figure 7 and Figure 8, LC is defined in Table 4 and Table 5. When data is valid, A/DQ[7:0] and DQS/DM follow the timing specified in Figure 9. Synchronous timing parameters are shown in Table 25 & Table 26.

In case of internal refresh insertion, variable latency output data may be delayed by up

to (LC*2) latency cycles as shown in Figure 7. True variable refresh pushout latency can be anywhere between LC to LCx2. The 1st DQS/DM rising edge after read pre-amble indicates the beginning of valid data.

Figure 5 Synchronous Read



If RBX has been enabled (MR8[3] written to 1) and a Linear Burst Command issued, then Wrap settings (MR8[2:0] are ignored and Read operations are allowed to cross row boundaries as shown in Figure 6.

Figure 6 Synchronous Read with RBX (Starting address '3FE)

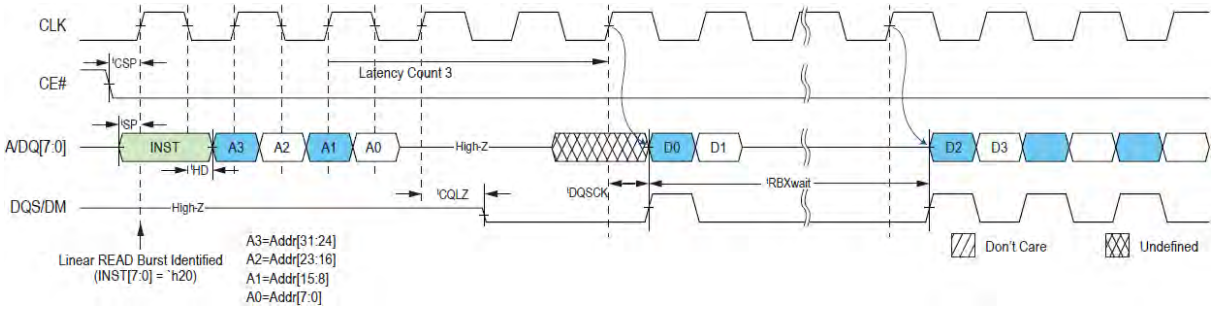


Figure 7 Variable Read Latency Refresh Pushout

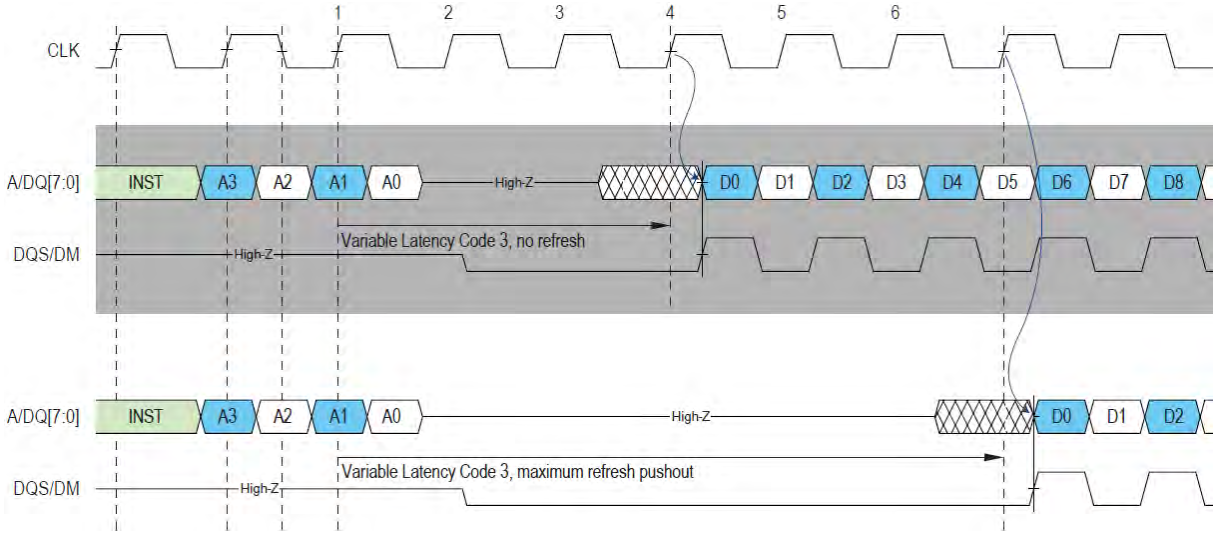


Figure 8 Read Latency & tDQSCK

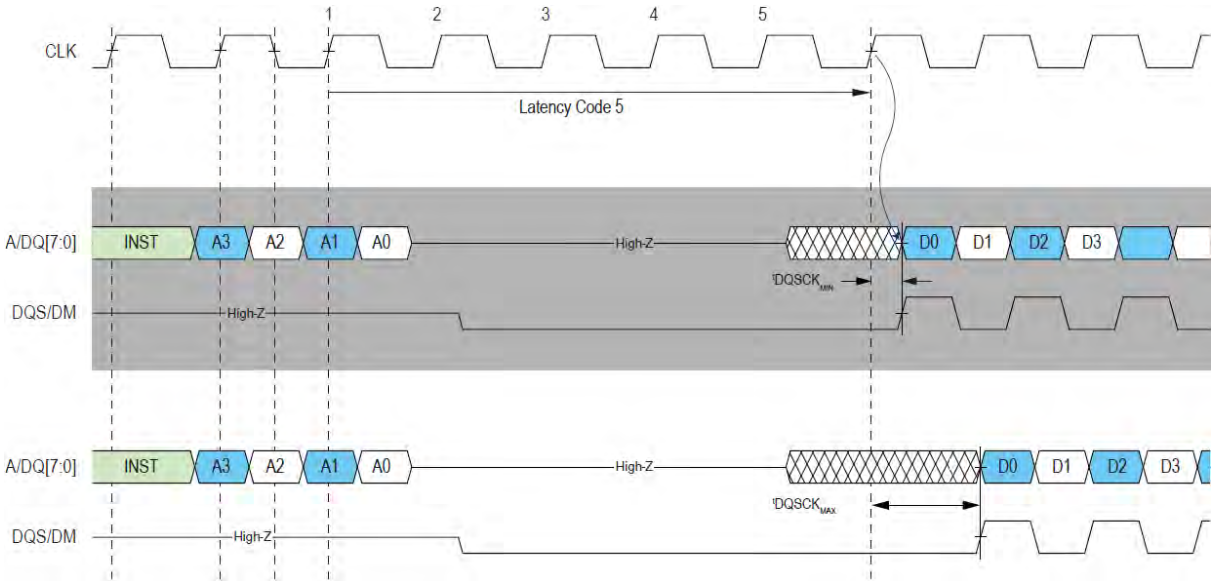
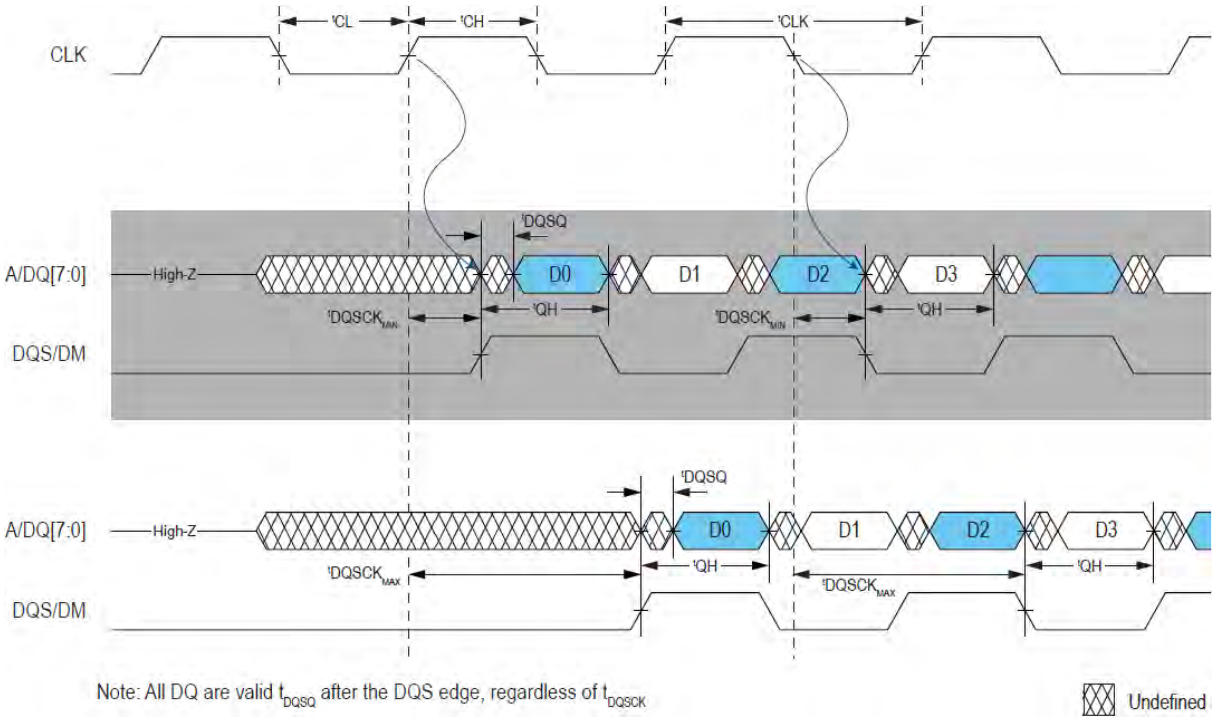


Figure 9 Read DQS/DM & DQ timing



8.6 Write Operation

A minimum of 2 bytes of data must be input in a write operation. In the case of consecutive short burst writes, tRC must be met by issuing additional CE# high time between operations. Single-byte write operations can be performed by masking the un-written byte with DQS/DM as shown in Figure 10.

Figure 10 Synchronous Write followed by any Operation

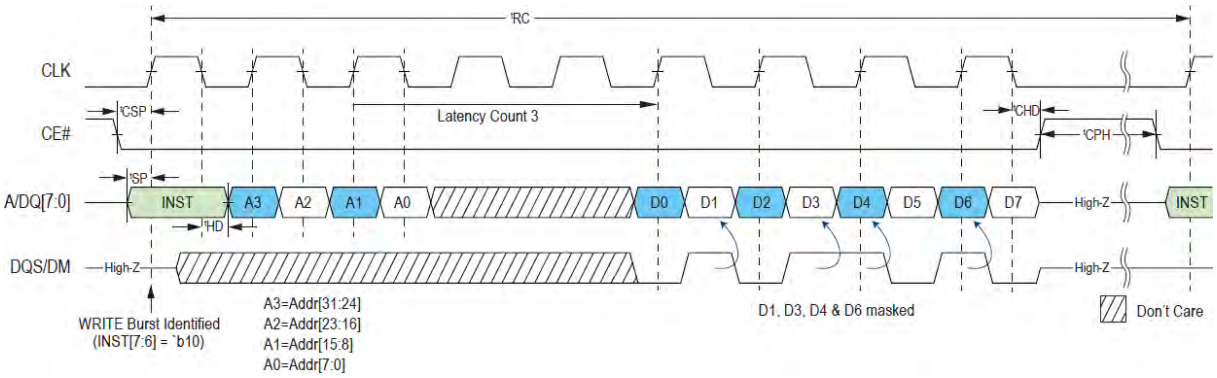
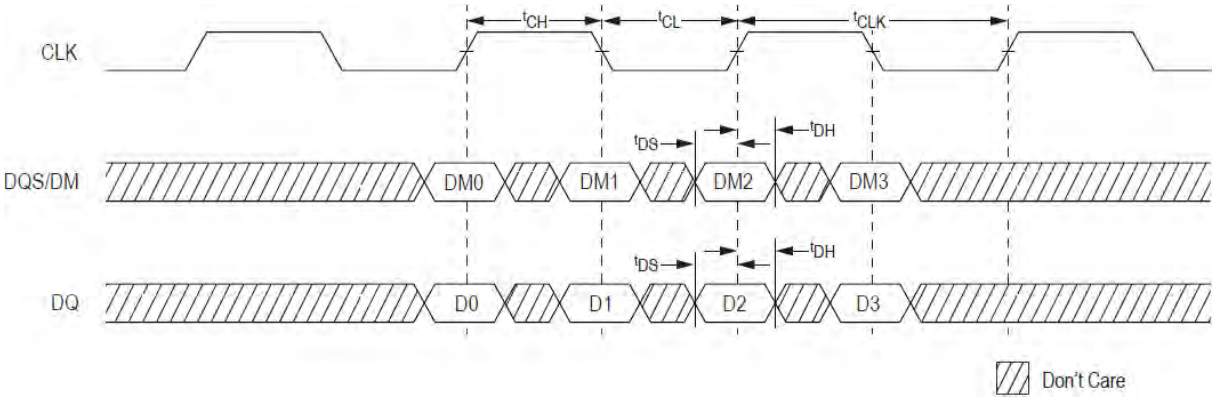


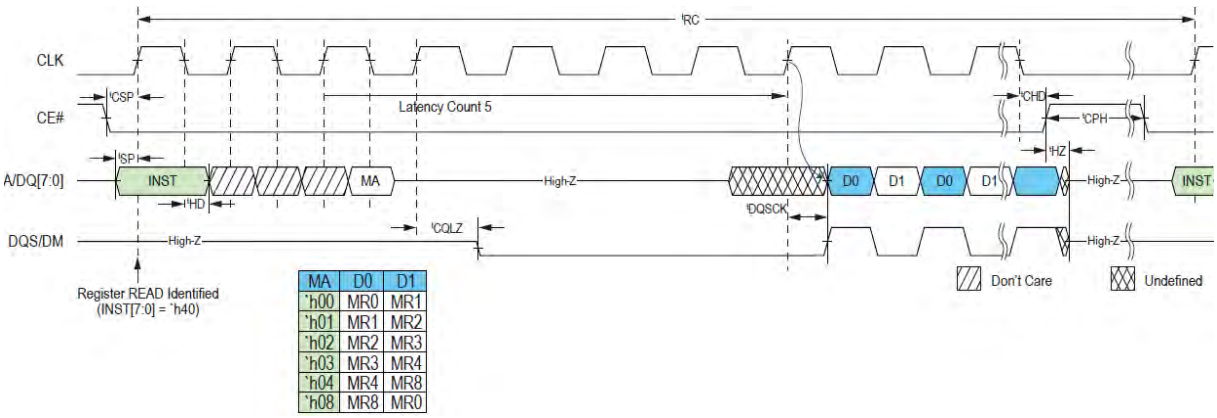
Figure 11 Write DQS/DM & DQ Timing



8.7 Control Register

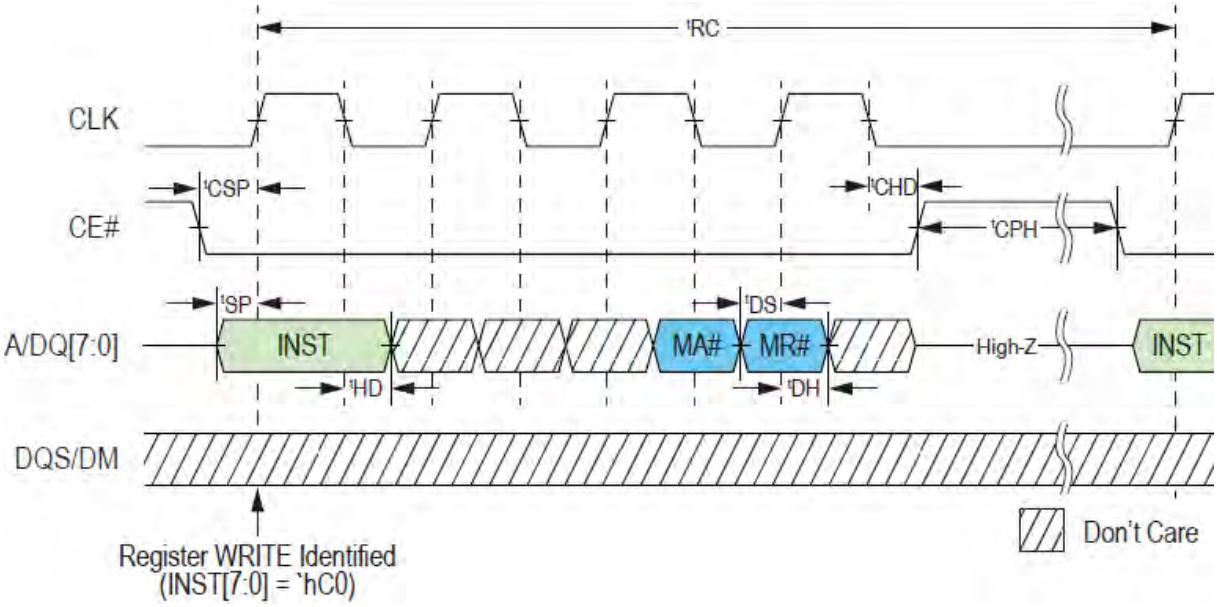
Register Read is shown below Figure 12. Mode Address in command determines which Mode Register is read from as Data0 (see chart in the Figure 12 below).

Figure 12 Register Read



MA	D0	D1
`h00	MR0	MR1
`h01	MR1	MR2
`h02	MR2	MR3
`h03	MR3	MR4
`h04	MR4	MR8
`h08	MR8	MR0

Figure 13 Register Write



Register Writes are Latency 1, whereas Register Reads use the same MR0[5:2] settings as burst reads in Table 4 without push out regardless of variable or fixed defined by MR0[5]. Registers 0, 4 and 8 are read and writable. Registers 1, 2 and 3 are read-only. Register 6 is write-only. Register mapping is shown in Table 2. Note that MR0[6], MR0[7], MR4[4] and MR8[7] must be written to b'0.

Table 2 Mode Register Table

MR No.	MA[7:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	`h00	R/W	'00'		LT	Read Latency Code			Drive Str.	
1	`h01	R	ULP	rsvd.		Vendor ID				
2	`h02	R	GB	rsvd.		Dev ID		Density		
3	`h03	R	RBXen	VCC	SRF	rsvd.				
4	`h04	R/W	Write Latency Code			'0'	RF	PASR		
6	`h06	W	Halfsleep™ & DPD			rsvd.				
8	`h08	R/W	'0'	rsvd.			RBX	BT	BL	

Table 3 Read Latency Type (MR0[5])

Latency Type	
MR0[5]	**LT**
0	Variable (default)
1	Fixed

Table 4 Read Latency Codes MR0[5:2]

	VL Codes (MR0[5]=0)		FL Codes (MR0[5]=1)	Max Input CLK Freq (MHz)	
MR0[4:2]	Latency (LC)	Max push out (LCx2)	Latency (LCx2)	Standard	Extended
000	3	6	6	66	66
001	4	8	8	109	109
010	5 (default)	10	10	133	133
011	6	12	12	166	166
100	7	14	14	200	200
others	reserved			-	-

Table 5 Operation Latency Code Table

Type	Operation	VL (default)		FL
		No Refresh	Refresh	
Memory	Read	LC	Up to LCx2	LCx2
	Write	WLC		WLC
Register	Read	LC		LC
	Write	1		1

Note: see Table 12 for WLC settings.

Table 6 Drive Strength Codes MR0[1:0]

Codes	Drive Strength
‘00	Full (25Ω)
‘01	Half (50Ω default)
‘10	1/4 (100Ω)
‘11	1/8 (200Ω)

Table 7 Ultra Low Power Device mapping MR1[7]

ULP	
‘0	Non-ULP (no Halfsleep™)
‘1	ULP (Halfsleep™ supported)

Table 9 Device ID MR2[4:3]

Codes	Device ID
'00	Generation 1
'01	Generation 2
'10	Generation 3 (default)
others	reserved

Table 10 Row Boundary Crossing Enable (MR3[7])

MR3[7] (read-only)	RBXen
0	RBX not supported
1	RBX supported via MR8[3]=1

Table 11 Self Refresh Flag (MR3[5])

MR3[5] (read-only)	Self Refresh Flag
0	Slow Refresh (allowed via MR4[3]=1, otherwise Fast Refresh)
1	Fast Refresh

MR3[5] is a refresh indicator that corresponds to device internal temperature. This bit will indicate 0 when the temperature is low enough to allow a slow frequency refresh rate.

Table 12 Write Latency MR4[7:5]

MR4[7:5]	Write Latency	Fmax (MHz)
000	3	66
100	4	109
010	5 (default)	133
110	6	166
001	7	200

Default powered up behavior is WL 5

Table 13 Refresh Frequency MR4[3]

MR4[3]	Refresh Frequency
0	Fast (default)
1	Enables Slow Refresh if temperature allows

Table 14 PASR MR4[2:0]

The PASR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

128Mb (64Mbx2)				
Codes	***Refresh Coverage***	***Address Space***	***Size***	***Density***
‘000	Full array (default)	000000h-FFFFFFh	16M x8	128Mb
‘001	Bottom 1/2 array	000000h-7FFFFFh	8M x8	64Mb
‘010	Bottom 1/4 array	000000h-3FFFFFh	4M x8	32Mb
‘011	Bottom 1/8 array	000000h-1FFFFFh	2M x8	16Mb
‘100	None	0	0M	0Mb
‘101	Top 1/2 array	800000h-FFFFFFh	8M x8	64Mb
‘110	Top 1/4 array	C00000h-FFFFFFh	4M x8	32Mb
‘111	Top 1/8 array	E00000h-FFFFFFh	2M x8	16Mb

Table 15 ULP Modes MR6[7:0]

MR6[7:0]	ULP Modes
‘hF0	Halfsleep™
‘hC0	Deep Power Down
others	reserved

Note: see 8.8 Halfsleep™ Mode; 8.9 Deep Power Down Mode for more information.

Table 16 Burst Type MR8[2], Burst Length MR8[1:0]

By default the device powers up in 32 Byte Hybrid Wrap. In non-Hybrid burst (MR8[2]=0), MR8[1:0] sets the burst address space in which the device will continually wrap within. If Hybrid Burst Wrap is selected (MR8[2]=1), the device will burst through the initial wrapped Burst Length once, then continue to burst incrementally up to maximum column address (1K) before wrapping around within the entire column address space. Burst Length (MR8[1:0]) can be set to 16,32,64 & 1K Lengths.

MR8[2]	MR8[1:0]	Burst Length	Example of Sequence of Bytes During Wrap	
			Starting Address	Byte Sequence
'0	'00	Wrap 16	4	[4,5,6,…15,0,1,2,…]
'0	'01	Wrap 32	4	[4,5,6,…31,0,1,2,…]
'0	'10	Wrap 64	4	[4,5,6,…63,0,1,2,…]
'0	'11	Wrap 1K	4	[4,5,6,…1023,0,1,2,…]
'1	'00	Hybrid 16	2	[2,3,4,…15,0,1],16,17,18,…1023,0,1,…
'1	'01	Hybrid 32 (default)	2	[2,3,4,…31,0,1],32,33,34,…1023,0,1,…
'1	'10	Hybrid 64	2	[2,3,4,…63,0,1],64,65,66,…1023,0,1,…
'1	'11	Wrap 1K	2	[2,3,4,…1023,0,1,2,…]

The Linear Burst Commands (INST[5:0]=6'b100000) override MR8[2:0] settings and forces the current array read or write command to do 1K Byte Wrap (equivalent to having MR8[1:0] set to 2'b11). The burst continues linearly from the starting address and at the end of the page, then wraps back to the beginning of the page. This special burst instruction can be used on both array write and read.

Table 17 Row Boundary Crossing Read Enable MR8[3]

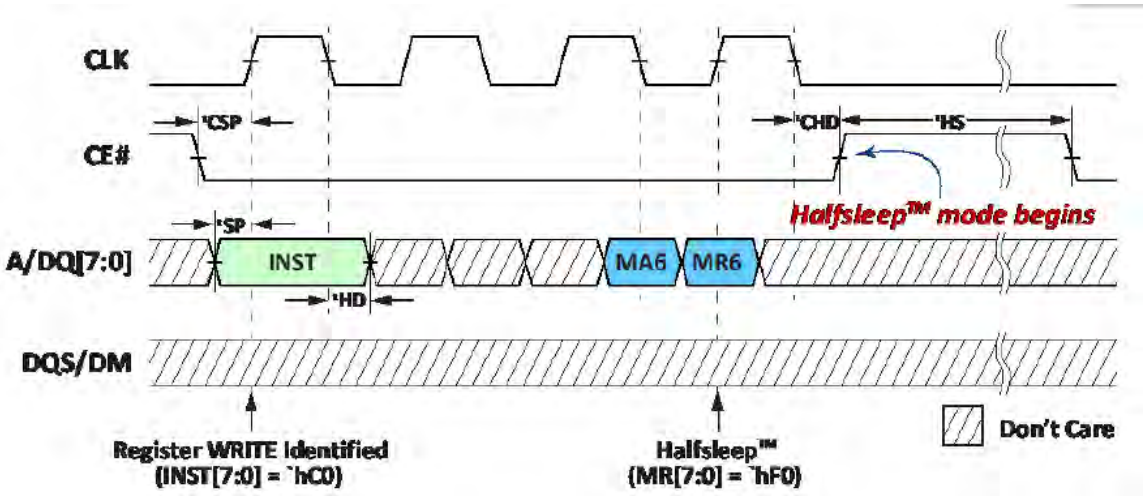
This register setting applies to Linear Burst reads only on RBX enabled devices (MR3[7]=1). Default write and read burst behavior is limited within the 1K (CA='h000 -> 'h3FF) column address space. Setting this bit high will allow Linear Burst reads to cross over into the next Row (RA+1).

MR8[3]	RBX Read
0	Reads stay within the 1K column address space
1	Reads cross row at 1K boundaries

8.8 Halfsleep™ Mode

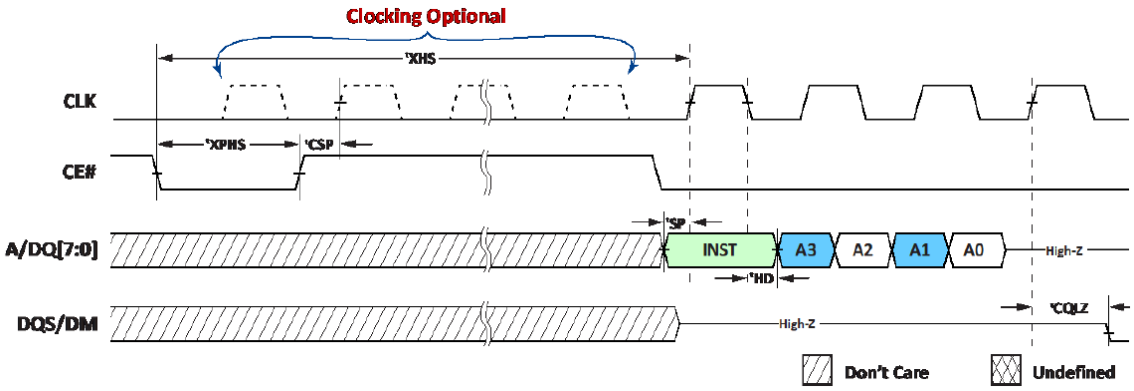
Halfsleep™ Mode is a feature which puts the device in an ultra-low power state, while the stored data is retained. Halfsleep™ Mode Entry is entered by writing 8'hF0 into MR6. CE# going high initiates the Halfsleep™ mode and must be maintained for the minimum duration of tHS. The Halfsleep™ Entry command sequence is shown below.

Figure 14 Halfsleep™ Entry Write (default WL0)



Halfsleep™ Exit is initiated by a low pulsed CE#. Afterwards, CE# can be held high with or without clock toggling until the first operation begins (observing minimum tXHS).

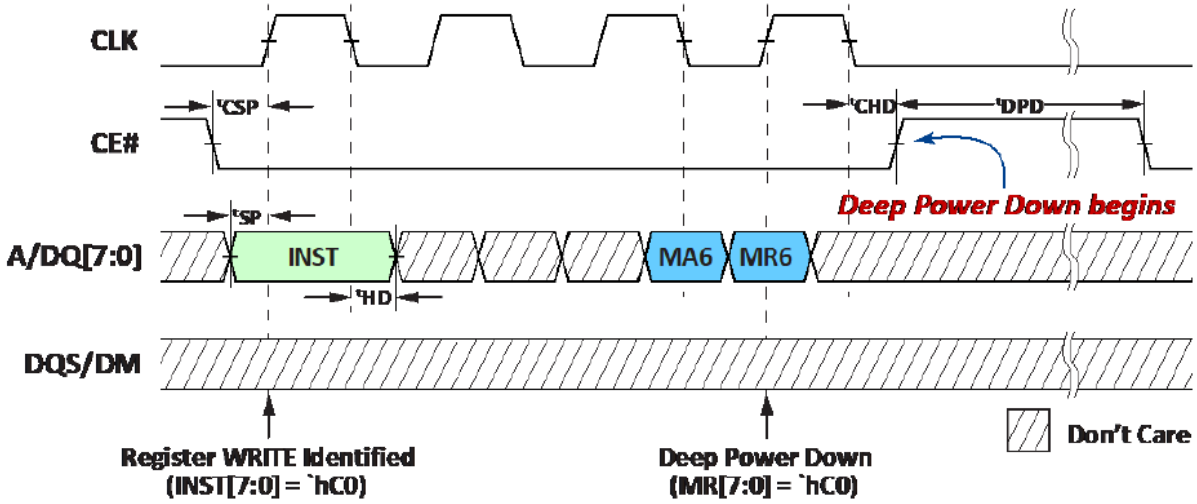
Figure 15 Halfsleep™ Exit (Read Operation shown as example)



8.9 Deep Power Down Mode

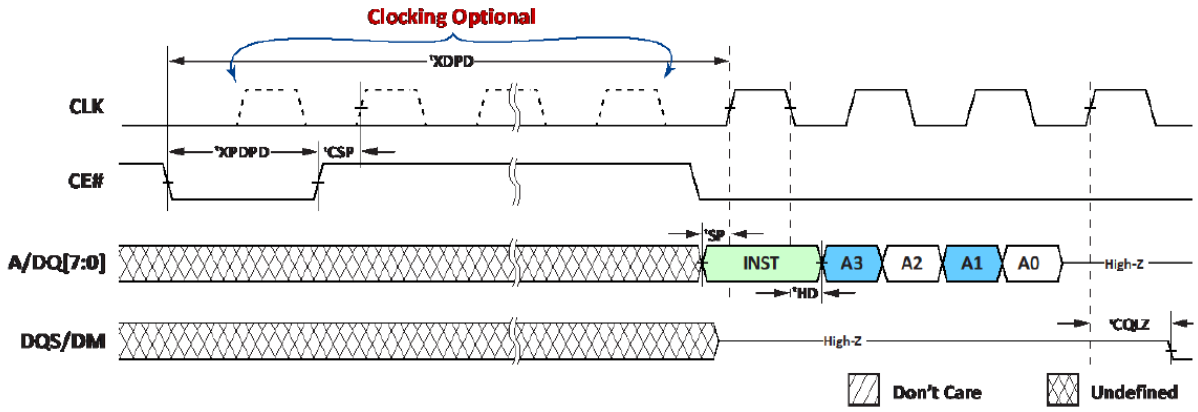
Deep Power Down Mode (DPD) is a feature which puts the device into power down state. DPD Mode Entry is entered by writing 8'hC0 into MR6. CE# going high initiates the DPD Mode and must be maintained for the minimum duration of tDPD. The Deep Power Down Entry command sequence is shown below.

Figure 16 Deep Power Down Entry



Deep Power Down Exit is initiated by a low pulsed CE#. After a CE# DPD Exit, CE# must be held high with or without clock toggling until the first operation begins (observing minimum tXDPD).

Figure 17 Deep Power Down Exit (Read Operation shown as example)



Register values and memory content are not retained in DPD Mode. After DPD mode register values will reset to defaults. tDPDp is minimum period between two DPD Modes (measured from DPD exit to the next DPD entry) as well as from the initial powerup to the first DPD entry.

9. Electrical Specifications

9.1 Absolute Maximum Ratings

Table 18 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage to any ball except V_{DD}, V_{DDQ} relative to V_{SS}	VT	-0.4 to V_{DD}/V_{DDQ}+0.4	V	
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.4 to +2.45	V	
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.4 to +2.45	V	
Storage Temperature	T_{STG}	-55 to +150	°C	1

Note: 1. Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

9.2 Pin Capacitance

Table 19 Package Pin Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	CIN		8	pF	VIN=0V
Output Pin Capacitance	COUT		10	pF	VOUT=0V

Note: spec'd at 25°C.

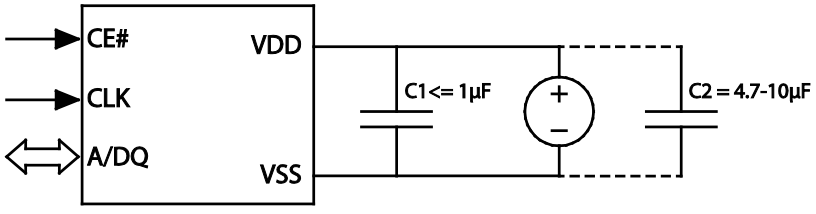
Table 20 Load Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Load Capacitance	C_L		15	pF	

Note: System C_L for the use of package

9.3 Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.



9.3.1 Low ESR cap C1:

It is recommended to place a low ESR decoupling capacitor of <=1µF close to the device to absorb transient peaks.

9.3.2 Large cap C2:

During Half-sleep modes even though half-sleep average currents are very small (less than 100µA), device will internally have low duty cycle burst refresh for an extended period of time of a few tens of microseconds. These refresh current peaks are large. During this period if the system regulator cannot supply large peaks for several microseconds, it is important to place a 4.7µF-10µF cap to take care of burst refresh currents and replenish the charge before next burst of refreshes.

9.4 Operating Conditions

Table 21 Operating Characteristics

Parameter	Min	Max	Unit	Notes
Operating Temperature (extended)	-40	105	°C	
Operating Temperature (standard)	-40	85	°C	

9.5 DC Characteristics

Table 22 DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Supply Voltage	1.62	1.98	V	
V_{DDQ}	I/O Supply Voltage	1.62	1.98	V	
V_{IH}	Input high voltage	V_{DDQ}-0.4	V_{DDQ}+0.2	V	
V_{IL}	Input low voltage	-0.2	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{DDQ}		V	
V_{OL}	Output low voltage (I_{OL}=+0.2mA)		0.2 V_{DDQ}	V	
I_{LI}	Input leakage current		1	µA	
I_{LO}	Output leakage current		1	µA	
ICC	Read/Write @13MHz		6	mA	2
	Read/Write @133MHz		24	mA	2
	Read/Write @166MHz		28.5	mA	2
	Read/Write @200MHz		33	mA	2
ISB_{EXT}	Standby current (105C)		600	µA	1,3
ISB_{STD}	Standby current (85C)		400	µA	3
ISB_{STDDPD}	Standby current (Deep Power Down -40°C to +85°C)		30	uA	8

Note:
1. Spec'd up to 105°C.
2. Current is only characterized.
3. Without CLK toggling. ISB will be higher if CLK is toggling.
4. Slow Refresh.
5. Typical ISBSTDROOM 132uA.
6. Current is only guaranteed after 150ms into Halfsleep™ mode.
7. Typical ISBSTDHS 40uA
8. Typical mean ISBSTDDPD 14uA at 25°C

9.6 ISB Partial Array Refresh Current

Table 23 Typical PASR Current @ 25°C

Standby Current @ 25°C			
PASR	**ISB –typical mean**	**Unit**	**Notes**
Full	132	µA	1,2
1/2	130	µA	1,2
1/4	128	µA	1,2
1/8	120	µA	1,2
Halfsleep™ Current @ 25°C			
PASR	**Halfsleep™-typical**	**Unit**	**Notes**
Full	40	µA	1,2,3
1/2	28	µA	1,2,3
1/4	22	µA	1,2,3
1/8	20	µA	1,2,3

Table 24 Typical PASR Current @ 85°C

Standby Current @ 85°C			
PASR	**ISB –typical mean**	**Unit**	**Notes**
Full	380	µA	2
1/2	300	µA	2
1/4	250	µA	2
1/8	220	µA	2
Halfsleep™ Current @ 85°C			
PASR	**Halfsleep™-typical**	**Unit**	**Notes**
Full	240	µA	2,3
1/2	144	µA	2,3
1/4	96	µA	2,3
1/8	48	µA	2,3

Note: 1. Slow Refresh current is only attainable by enabling Slow Refresh Frequency (see Table 13)
2. PASR Current is only characterized based on 128Mb density without CLK toggling.
3. Spec'd Halfsleep™ current is only guaranteed after 150ms into Halfsleep™ mode.

9.7 AC Characteristics

Table 25 READ/WRITE Timing

		BGA 1.8V Only							
		-7(133Mhz)		-6(166MHz)		-5(200MHz)			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit	Notes
tCLK	CLK period	7.5		6		5		ns	
tCH/tCL	Clock high/low width	0.45	0.55	0.45	0.55	0.45	0.55	tCLK	
tKHKL	CLK rise or fall time		1.2		1		0.8	ns	
tCPH	CE# HIGH between subsequent burst operations	15		18		20		ns	
tCEM	CE# low pulse width (excluding Halfsleep™ exit)		8		8		8	µs	Standard temp
			3		3		3	µs	Extended temp
tCEM	CE# low pulse width	3		3		3		tCLK	Minimum 3
tCSP	CE# setup time to CLK rising edge	2		2		2		ns	
tCSP2	CE# rising edge to next CLK falling edge	1.5		1.5		1.5		ns	
tCHD	CE# hold time from CLK falling edge	2		2		2		ns	
tSP	Setup time to active CLK edge	0.8		0.8		0.8		ns	
tHD	Hold time from active CLK edge	0.8		0.8		0.8		ns	
tHZ	Chip disable to DQ/DQS output high-Z		6		6		6	ns	
tRBXwait	Row Boundary Crossing Wait Time	30	65	30	65	30	65	ns	
tRC	Write Cycle	60		60		60		ns	
tRC	Read Cycle	60		60		60		ns	
tHS	Minimum Halfsleep™ duration	150		150		150		µs	
tXHS	Halfsleep™ Exit CE# low to CLK setup time	150		150		150		µs	
tXPHS	Halfsleep™ Exit CE# low pulsewidth	60		60		60		ns	
			tCEM		tCEM		tCEM	µs	Standard temp
								µs	Extended temp
tDPD	Minimum DPD duration	500		500		500		µs	
tDPDp	Minimum period between DPD Modes	500		500		500		µs	
tXDPD	DPD CE# low to CLK setup time	150		150		150		µs	
tXPDPD	DPD Exit CE# low pulsewidth	60		60		60		ns	
tPU	Device Initialization	150		150		150		µs	
tRP	RESET# low pulse width	1		1		1		µs	
tRST	Reset to CMD valid	2		2		2		µs	

Table 26 DDR Timing Parameters

		BGA 1.8V Only							
		-7(133MHz)		-6(166MHz)		-5(200MHz)			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit	Notes
tCQLZ	Clock rising edge to DQS low	1	6	1	6	1	6	ns	
tDQSCK	DQS output access time from CLK	2	5.5	2	5.5	2	5.5	ns	
tDQSQ	DQS – DQ skew		0.6		0.5		0.4	ns	
tDS	DQ and DM input setup time	0.8		0.8		0.8		ns	
tDH	DQ and DM input hold time	0.8		0.8		0.8		ns	

10. Revision History

Vision	Who	Date	Description
1	William CHEN	Dec 6th 2022	Initial branded release