256Mbit DDR Octal-SPI Pseudo-SRAM Data Sheet

CSS25608S

Version: 1

Table of Contents

The CSS25608S is general part number of 256Mb DDR Octal-SPI Pseudo-SRAM product family. The package type and detailed part number refers to 3. Package Information, 4 Ordering Information and 4.1 Part Number.

1. Feature and Specification

Single Supply Voltage:

V_{DD} =1.62 to 1.98V

V_{DDQ} =1.62 to 1.98V

Interface: Octal SPI with DDR mode, two bytes transfers per one clock cycle

Performance: Clock rate up to 200MHz, (400MBps read/write throughput)

Organization: 256Mb, 32M x 8bits with 2048 bytes per page

Column address: AY0 to AY10

Row address: AX0 to AX13

Refresh: Self-managed

Operating temperature range

Tc = -40°C to +85°C (standard range)

Tc = -40°C to +105°C (extended range)

Typical mean Room Standby Current:

40µA @ 25°C (Halfsleep™ Mode with data retained)

Maximum Standby Current:

1100µA @ 105°C

680µA @ 85°C

Low Power Features:

Partial Array Self-Refresh (PASR)

Auto Temperature Compensated Self- Refresh (ATCSR) self-managed by a built-in temperature sensor

Ultra Low Power Halfsleep™ mode with data retention.

Software reset

Reset pin available

Output driver LVCMOS with programmable drive strength

Data mask (DM) for write operation

Data strobe (DQS) for high speed read operation

Write burst length, maximum 2048 Byte, minimum 2 Byte.

Wrap & hybrid burst in 16/32/64/2K lengths.

Linear Burst Command

Row Boundary Crossing (RBX) read operations enabled via Mode Register

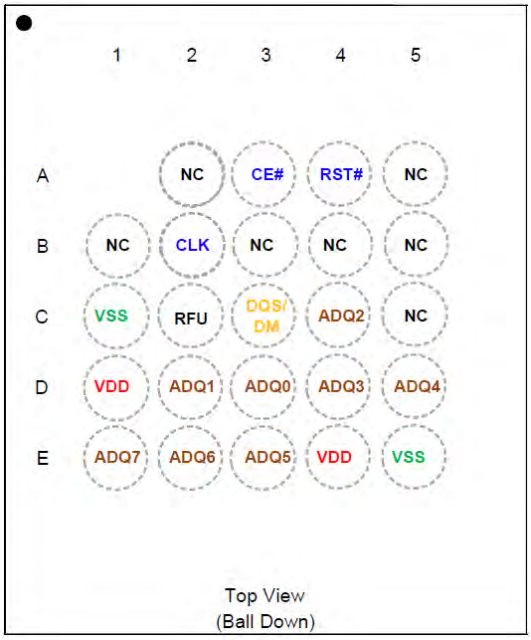
2. Description

The feature of the CSS25608SB is a high speed, low pin count interface. It operates in OPI (Octal peripheral interface) mode with Double Data Rate (DDR) under frequencies up to 200Mhz. It is most suitable for low-power and low-cost applications like oT devices. It incorporates a seamless self-managed refresh mechanism.

3. Package Information

The CSS25608SB is available in standard package 24b mini-FBGA 6 x 8 x 1.2mm, ball pitch 1.0mm, ball size 0.4mm.

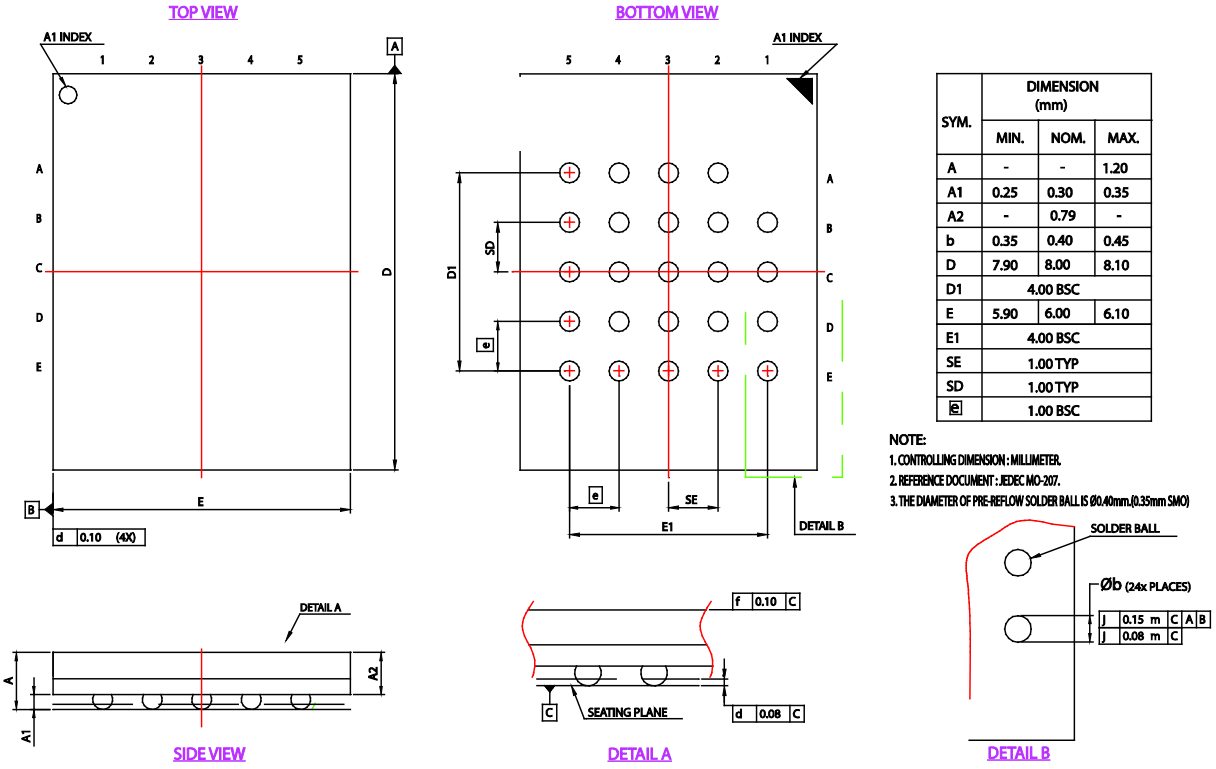
Ball Assignment of 24b mini-FBGA (6x8x1.2mm)(P1.0)(B0.4)



Note:
1. RFU: Reserved for future use, which is reserved for 2nd CE#.
2. NC: No Connection internally.

3.1 Package Outline Drawing

3.1.1 24b Mini-FBGA Drawing



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.25	0.30	0.35
A2	-	0.79	-
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
SE	1.00 TYP		
SD	1.00 TYP		
e	1.00 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.
3. THE DIAMETER OF PRE-REFLOW SOLDER BALL IS Ø0.40mm.(0.35mm SMO)

4. Ordering Information

Product Naming Rule:

C S S aaa bb c d - e fff g h - II

- C: Company
- S: Product: S-pSRAM
- S: Type: S-SPI Syn. A-Async. D-ADMUX
- aaa: Density: 16-16Mb, 64-64Mb, 128-128Mb
- bb: Width: x1-01, x4-04, x8-08, x16-16, *x8/x16-17
- c: Power: L:3.3V, S:1.8V, V:1.6V, U:1.2V, X:0.6V
- d: Package: S-SOP, B-BGA, U-USON, K-KGD, W-WLCSP
- e: Vender Define
- fff: Protocol & Special Spec. Blank:Non
- g: Temp : I : Industrial, A : Auto, Blank : Commercial
- h: Packing: T: Tape & Reel, Blank: Tube or Tray
- II: Reserve for Request Blank:Non

*x8 and x16 switchable
Example:
CSS6404LS-LIT
=>SPI pSRAM 64Mb/QSPI/3.3V/SOP-8/E3/I grade/Tape
CSS25617SB-NIT
=>SPI pSRAM 256Mb/x8 & x16/1.8V/BGA/E7/I grade/Tape
CSD6416SB-FI-A1
=>ADMUX pSRAM 64Mb/x16/1.8V/BGA/C6/I grade/tray

4.1 Part Number:

Table 1 Part Number Description

Part Number	Density	Temperature	Note
CSS25608SB-NI	256Mb	-40~85C	24b FBGA
CSS25608SB-NJ	256Mb	-40~105C	24b FBGA
CSS25608SQ-NI	256Mb	-40~85C	QFN
CSS25608SQ-NJ	256Mb	-40~105C	QFN

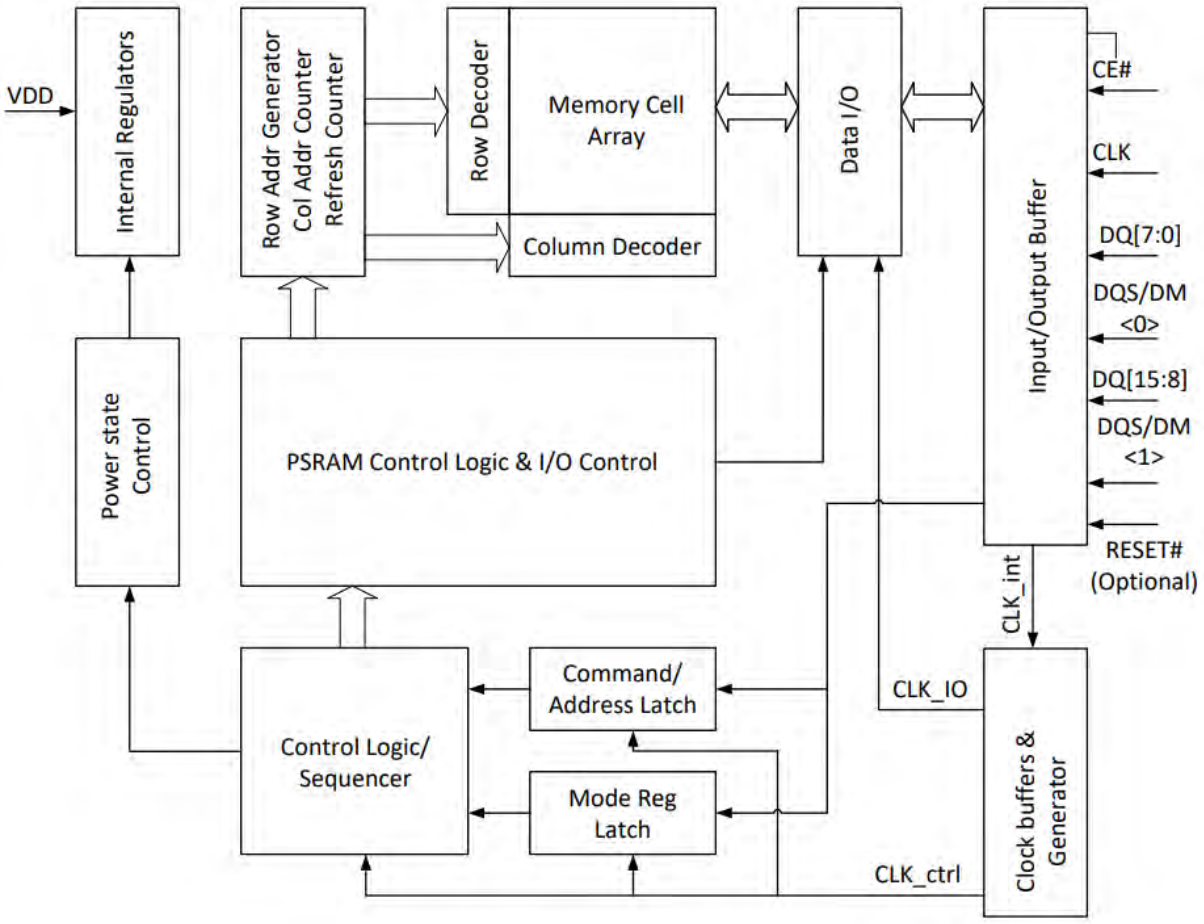
5. Package Ball Signal Table

All signal are listed at Table 2

Table 2 Signals Table

Symbol	Type	Description	Comments
V_{DD}	Power	Core & IO supply 1.8V	V_{DDQ} short to V_{DD} internally.
V_{SS}	Ground	Core& IO supply ground	
A/DQ[7:0]	IO	Address/Data bus [7:0]	
DQS/DM	IO	DQ strobe clock for DQ[7:0] during all reads, Data mask for DQ[7:0] during memory writes. DM is active high. DM=1 means “do not write”.	
CE#	Input	Chip select, active low. When CE#=1, chip is in standby state.	
CLK	Input	Input clock	
RESET#	Input	Reset signal, active low. Optional, as the pad is internally tied to a weak pull-up and can be left floating.	May not be available for all package types

6. Block Diagram



7. Powerup Initialization

Octal DDR products include an on-chip voltage sensor used to start the self-initialization process. VDD and VDDQ must be applied simultaneously. When they reach a stable level at or above minimum VDD, the device is in Phase 1 and it requires 150µs to complete its self-initialization process. System host can then proceed to Phase 2 of the initialization described in section 7.1.

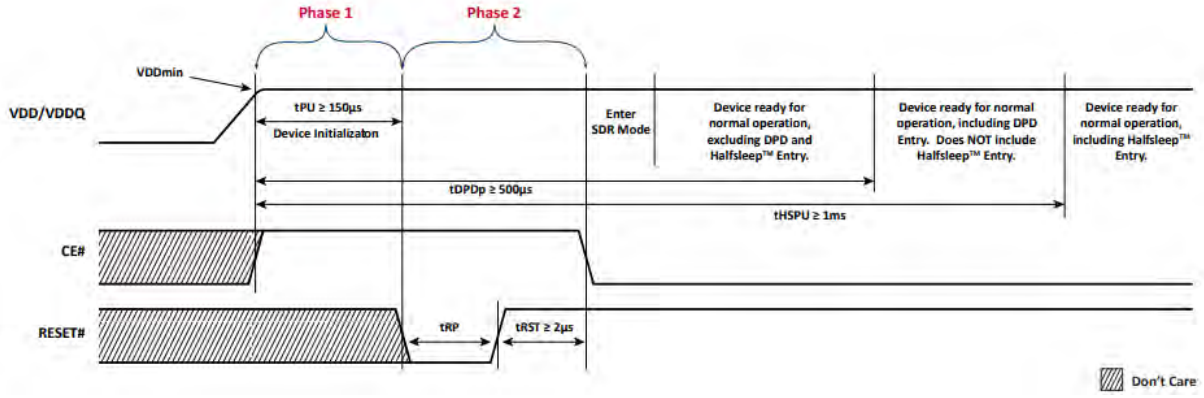
During Phase 1 CE# should remain HIGH (track VDD within 200mV); CLK should remain LOW.

After Phase 2 is complete the device is ready for operation, however Halfsleep™ entry and Deep Power Down (DPD) entry are not available until Halfsleep™ Power Up (tHSPU) or DPD Power Up (tDPDp) durations are observed.

7.1 Power-Up Initialization Method 1 (via. RESET# pin)

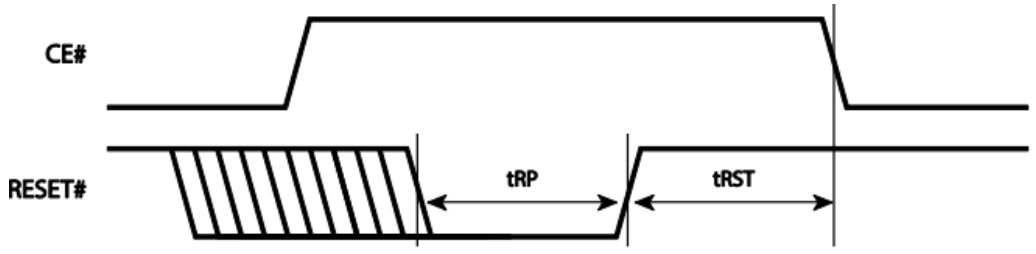
The RESET# pin can be used to initialize the device during Phase 2 as follows:

Figure 1 Power-Up Initialization Method 1 RESET#



The RESET# pin can also be used when CE#=high at any time after the device is initialized to reset all register contents. Memory content is not guaranteed. Timing requirements for RESET# usage are shown below.

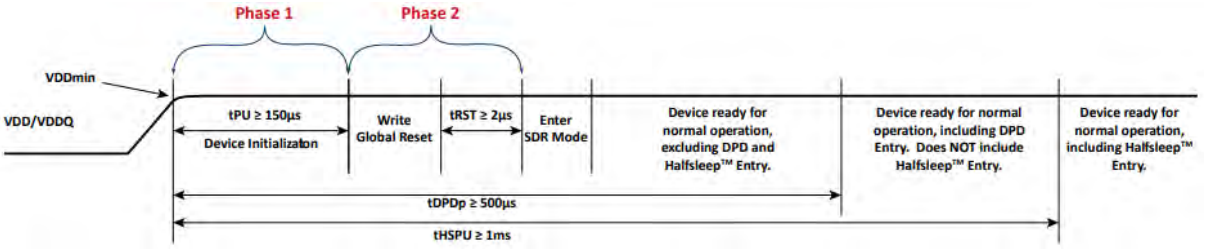
Figure 2 Reset# Timing



7.2 Power-Up Initialization Method 2 (via. Global Reset)

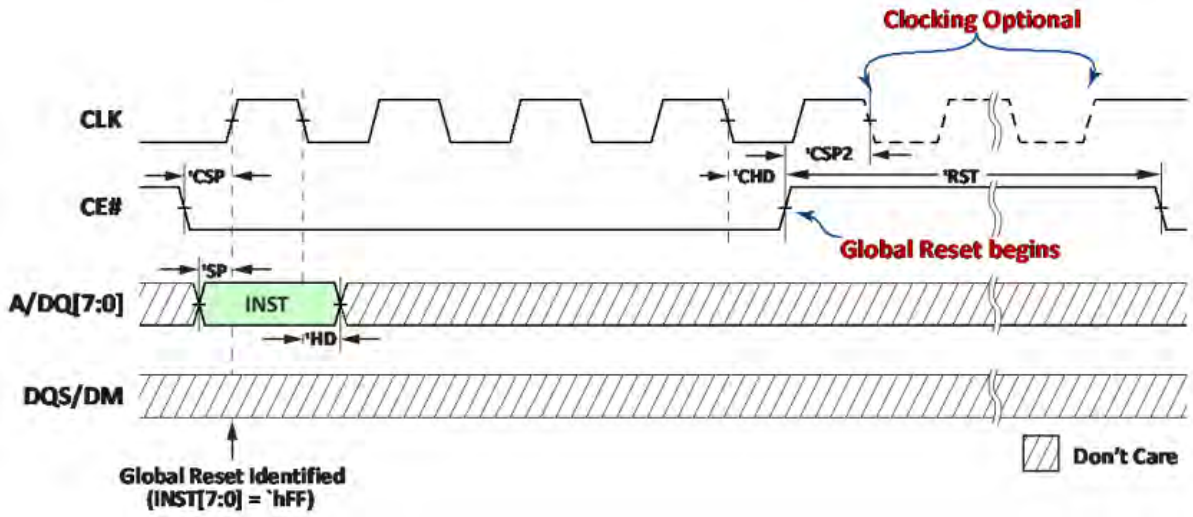
As an alternate power-up initialization method, after the Phase 1 150µs period the Global Reset command can also be used to reset the device in Phase 2 as follows:

Figure 3 Power-Up Initialization Method 2 Timing with Global Reset



The Global Reset command resets all register contents. Memory content is not guaranteed. The command frame is made of 4 clocked CE# lows. Clocking is optional during tRST. The Global Reset command sequence is shown below.

Figure 4 Global RESET



8. Interface Description

8.1 Address Space

Octal DDR PSRAM device is byte-addressable. Memory accesses must start on even addresses (A[0]=’0). Mode Register accesses can start on even or odd address.

8.2 Burst Type and Length

Read and write operations are default Hybrid Wrap 32 mode. Other burst lengths of 16, 32, 64 or 2K bytes in standard or Hybrid wrap modes are register configurable (see Table 17). The device also includes command burst options for Linear Bursting. Bursts can start on any even address. Write burst length requires a minimum of 2 bytes. Read has

no minimum length. Both write and read have no restriction on maximum burst length as long as tCEM is met.

8.3 Command/Address Latching

After CE# goes LOW, instruction code is latched on 1 st CLK rising edge. Access address is latched on the 3rd, 4th , 5th & 6th CLK edges (2nd CLK rising edge, 2nd CLK falling edge, 3rd CLK rising edge, 3rd CLK falling edge).

8.4 Command Truth Table

The Octal DDR PSRAM recognizes commands listed in the following table. Instruction and address are input through A/DQ[7:0] pins. Host must send correct instruction and address format according to the following table.

Note that Linear Burst commands, 20h and A0h, ignore burst setting defined by MR8[2:0]. Note that only Linear Burst Read command is capable of performing row boundary crossing (RBX) read function.

	1st CLK		2nd CLK		3rd CLK	
Command	↑	↓	↑	↓	↑	↓
Sync Read	00h		A3	A2	A1	A0
Sync Write	80h		A3	A2	A1	A0
Linear Burst Read	20h		A3	A2	A1	A0
Linear Burst Write	A0h		A3	A2	A1	A0
Mode Register Read	40h		×			MA
Mode Register Write	C0h		×			MA
Global Reset	FFh		×			

Remarks: × = don't care (V_{IH}/V_{IL})

A3 = 7'bx, RA[13] {unused address bits are reserved}

A2 = RA[12:5]

A1 = RA[4:0],CA[10:8]

A0 = CA[7:0]

MA = Mode Register Address

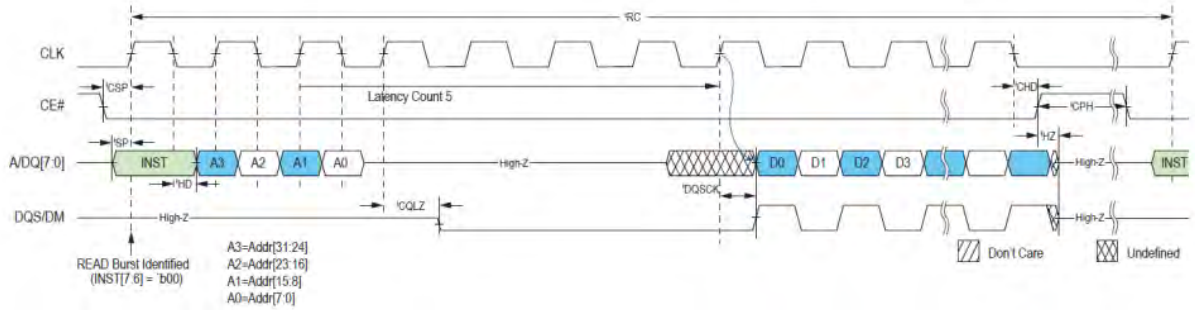
8.5 Read Operation

After address latching, the device initializes DQS/DM to '0 from CLK rising edge of the 3rd clock cycle (A1). See Figure 5 below.

Output data is available after LC latency cycles, as shown in Figure 7 & Figure 8. LC is latency configuration code defined in Table 5 and Table 6. When data is valid, A/DQ[7:0] and DQS/DM follow the timing specified in Figure 9. Synchronous timing parameters are shown in Table 26 & Table 27.

In case of internal refresh insertion, variable latency output data may be delayed by up to (LCx2) latency cycles as shown in Figure 7. True variable refresh pushout latency can be anywhere between LC to LCx2. The 1st DQS/DM rising edge after read pre-amble indicates the beginning of valid data.

Figure 5 Synchronous Read



If RBX is enabled (MR8[3] written to 1) and a Linear Burst Read Command (‘h20) is issued, read operation may cross row boundaries as shown in Figure 6.

Figure 6 Linear Burst Read with RBX (Starting address ‘7FE)

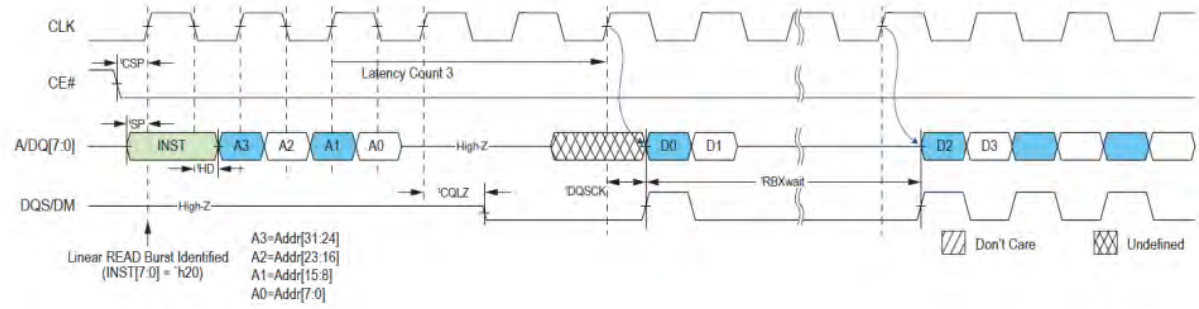


Figure 7 Variable Read Latency Refresh Pushout

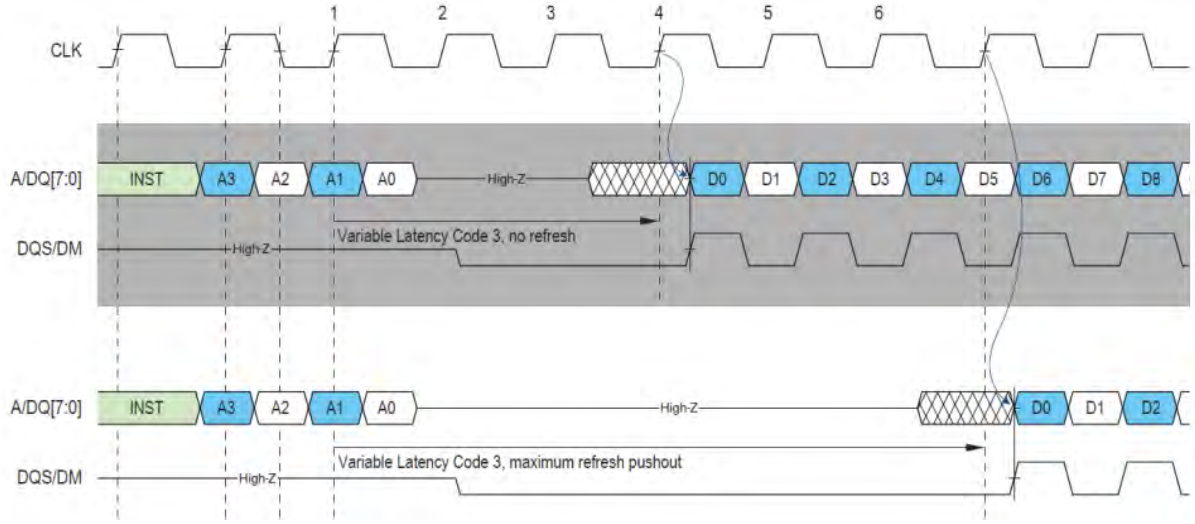


Figure 8 Read Latency & tDQSCK

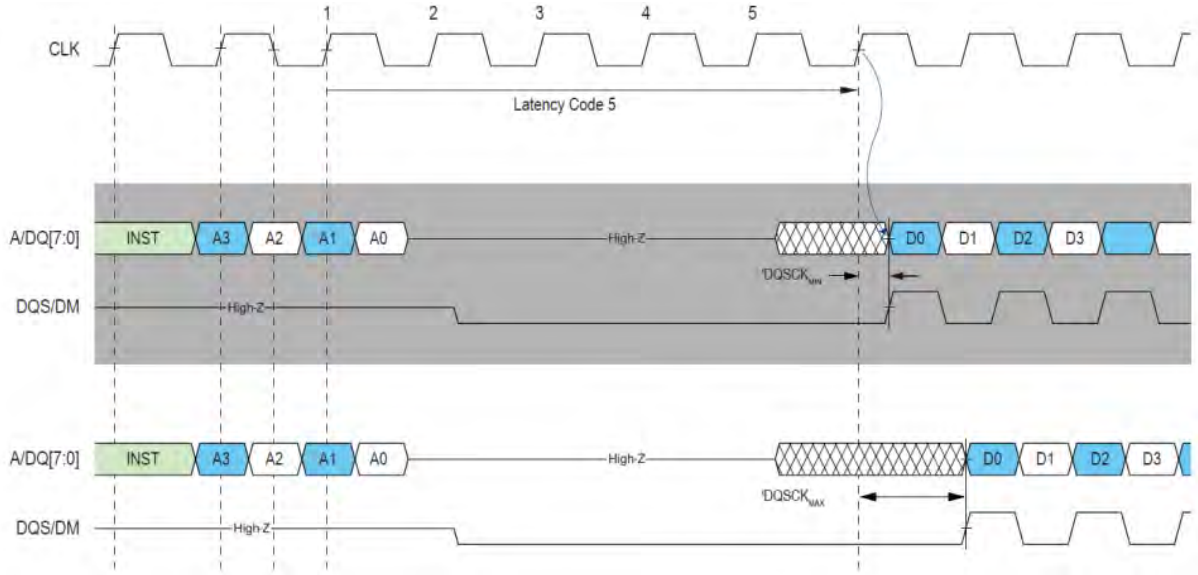
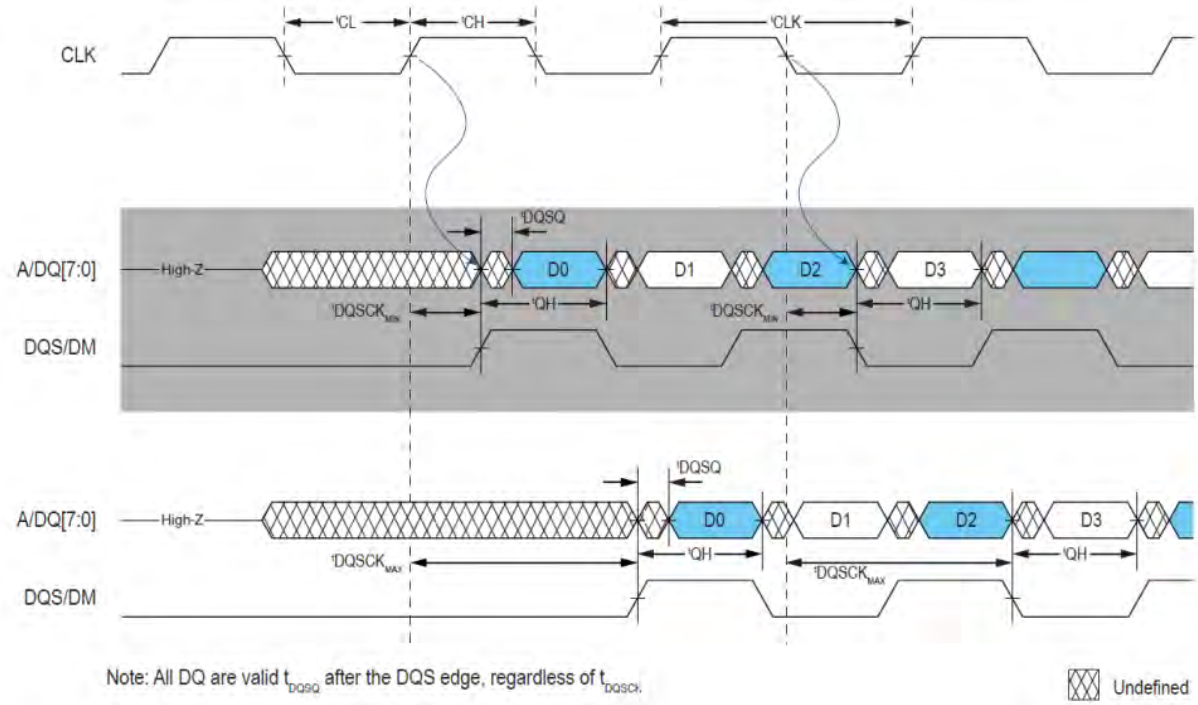


Figure 9 Read DQS/DM & DQ timing



8.6 Write Operation

A minimum of 2 bytes of data must be input in a write operation. In the case of consecutive short burst writes, tRC must be met by issuing additional CE# high time between operations. Single-byte write operations can be done by masking through DQS/DM pin as shown in Figure 10.

Figure 10 Synchronous Write followed by any Operation

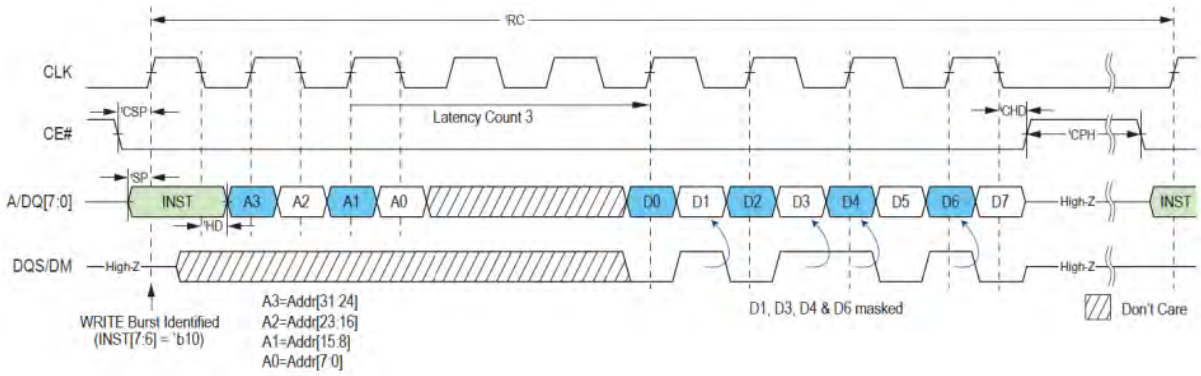
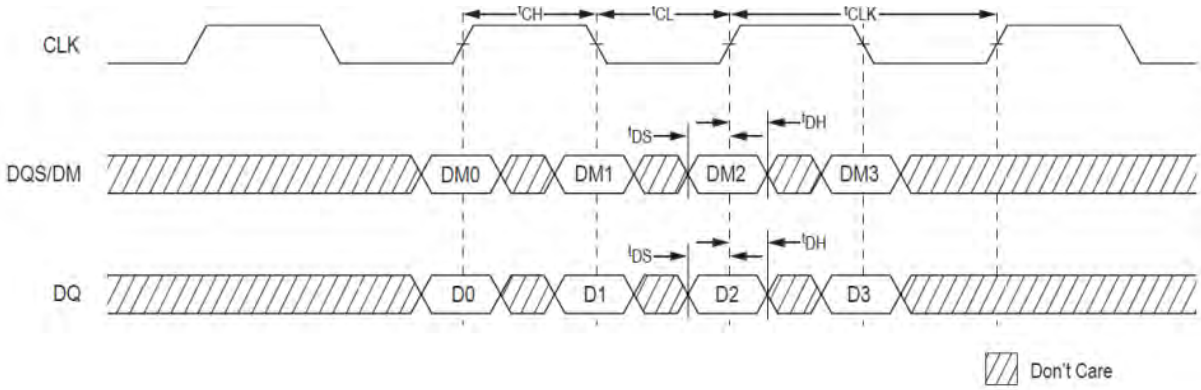


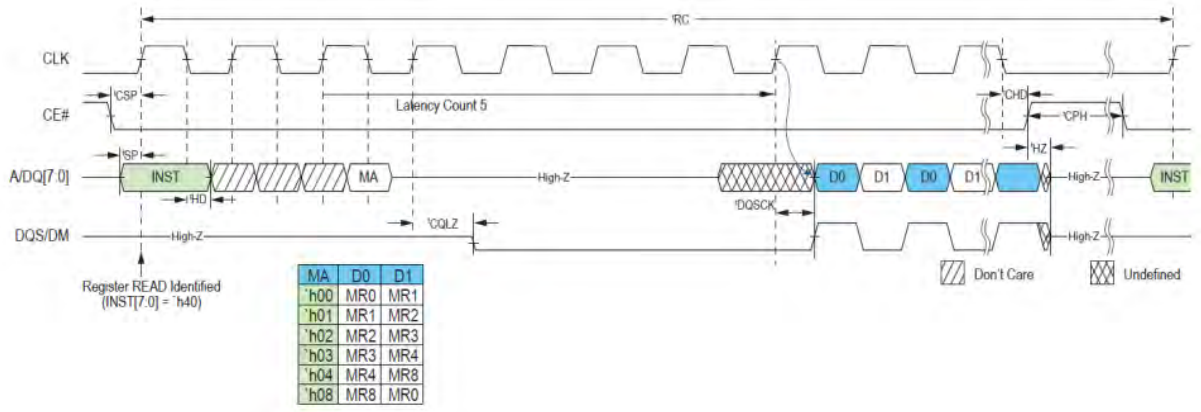
Figure 11 Write DQS/DM & DQ Timing



8.7 Control Register

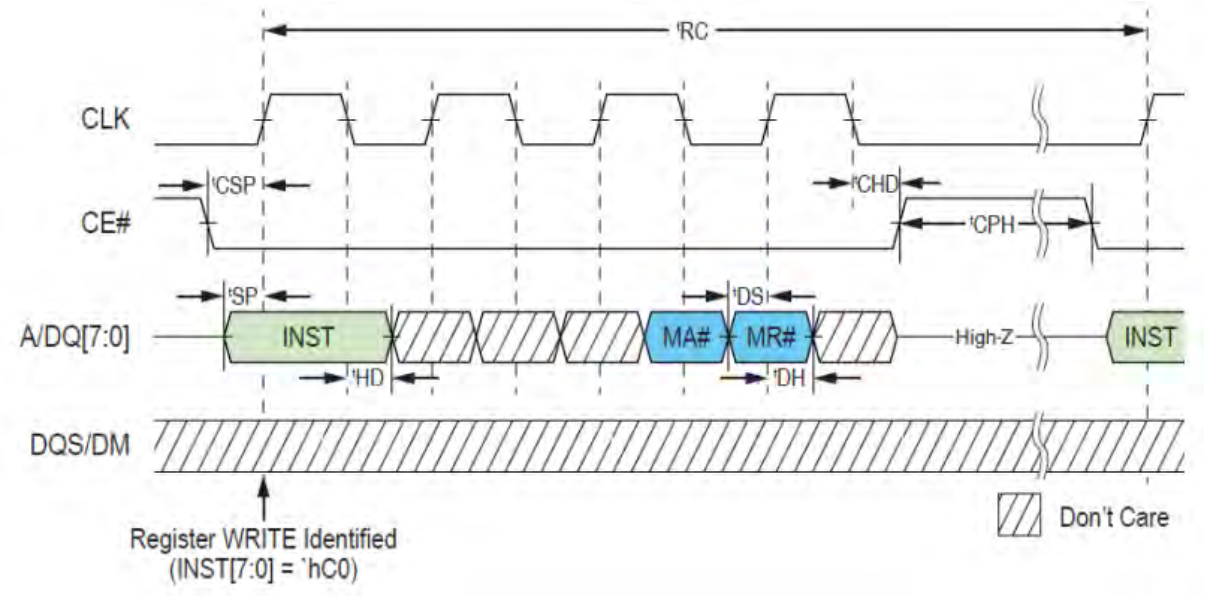
Register Read is shown below. Mode Address in command determines which Mode Register is read from as Data0 (see chart in the Figure below).

Figure 12 Register Read



MA	D0	D1
'h00	MR0	MR1
'h01	MR1	MR2
'h02	MR2	MR3
'h03	MR3	MR4
'h04	MR4	MR8
'h08	MR8	MR0

Figure 13 Register Write



Register Writes are always latency 1. Write Latency Code, MR4[7:5] does not apply to Register writes. Register Reads follow the same read latency settings, defined in MR0[4:2] (see Table 6).

Registers 0, 4 & 8 are read and writable. Registers 1, 2 and 3 are read-only. Register 6 is write-only.

Register mapping is shown in Table 3. All MR0 or MR8 writes must have MR0[7:6] or MR8[7:6] written to `0(s)

Table 3 Mode Register Table

MR No.	MA[7:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	`h00	R/W	'00'		LT	Read Latency Code			Drive Str.	
1	`h01	R	ULP	rsvd.		Vendor ID				
2	`h02	R	KGD			Dev ID		Density		
3	`h03	R	RBXen	0	SRF		rsvd.			
4	`h04	R/W	Write Latency Code			RF rate		PASR		
6	`h06	W	Halfsleep™				rsvd.			
8	`h08	R/W	'0'	'0'	rsvd		RBX	BT	BL	

Table 4 Read Latency Type (MR0[5])

Latency Type	
MR0[5]	**LT**
0	Variable (default)
1	Fixed

Table 5 Read Latency Codes MR0[4:2]

	VL Codes (MR0[5]=0)		FL Codes (MR0[5]=1)	Max Input CLK Freq (MHz)	
MR0[4:2]	Latency (LC)	Max push out (LCx2)	Latency (LCx2)	Standard	Extended
000	3	6	6	66	66
001	4	8	8	109	109
010	5 (default)	10	10	133	133
011	6	12	12	166	166
100	7	14	14	200	200
others	reserved			-	-

Table 6 Operation Latency Code Table

Type	Operation	VL (default)		FL
		No Refresh	Refresh	
Memory	Read	LC	Up to LCx2	LCx2
	Write	WLC		WLC
Register	Read	LC		LC
	Write	1		1

Note: see Table 13 for WLC settings.

Table 7 Drive Strength Codes MR0[1:0]

Codes	Drive Strength
‘00	Full (25Ω)
‘01	Half (50Ω default)
‘10	1/4 (100Ω)
‘11	1/8 (200Ω)

Table 8 Ultra Low Power Device mapping MR1[7]

ULP	
‘0	Non-ULP (no Halfsleep™)
‘1	ULP (Halfsleep™ supported)

Table 10 Device ID MR2[4:3]

Codes	Device ID
‘00	Generation 1
‘01	Generation 2
‘10	Generation 3
‘11	Generation 4 (default)

Table 11 Row Boundary Crossing Enable (MR3[7])

MR3[7] (read-only)	RBXen
0	RBX not supported
1	RBX supported via MR8[3]=1

Table 12 Self Refresh Flag (MR3[5:4])

MR3[5:4] indicates current device refresh rate. Refresh rate depends on temperature and refresh frequency configuration, set by MR4[4:3].

MR3[5:4]	Self Refresh Flag
01	0.5x Refresh
00	1x Refresh
10	4x Refresh
11	Reserved

Table 13 Write Latency MR4[7:5]

Write latency, WLC, is default to 5 after power up. Use MR Write to set write latencies according to write latency table. When operating frequency exceeding Fmax listed in the table will result in write data corruption.

MR4[7:5]	Write Latency Codes (WLC)	Fmax (MHz)
000	3	66
100	4	109
010	5 (default)	133
110	6	166
001	7	200
Others	Reserved	

Table 14 Refresh Frequency Setting MR4[4:3]

MR4[4:3]	Refresh Frequency
x0	Always 4x Refresh (default)
01	Enables 1x Refresh when temperature allows
11	Enable 0.5x Refresh when temperature allows

Note: x= don't care

Table 15 PASR MR4[2:0]

The PASR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

256Mb X8				
Codes	**Refresh Coverage**	**Address Space**	**Size**	**Density**
'000	Full array (default)	0000000h-1FFFFFFh	32M X8	256Mb
'001	Bottom 1/2 array	0000000h-0FFFFFFh	16M X8	128Mb
'010	Bottom 1/4 array	0000000h-07FFFFFh	8M X8	64Mb
'011	Bottom 1/8 array	0000000h-03FFFFFh	4M X8	32Mb
'100	None	0	0M	0Mb
'101	Top 1/2 array	1000000h-1FFFFFFh	16M X8	128Mb
'110	Top 1/4 array	1800000h-1FFFFFFh	8M X8	64Mb
'111	Top 1/8 array	1C00000h-1FFFFFFh	4M X8	32Mb

Table 16 Halfsleep™ MR6[7:0]

MR6[7:0]	ULP Modes
'hF0	Halfsleep™
'hC0	Deep Power Down
others	reserved

Note: see section 8.8 Halfsleep™ Mode and 8.9 Deep Power Down Mode for more information.

Table 17 Burst Type MR8[2], Burst Length MR8[1:0]

By default the device powers up in 32 Byte Hybrid Wrap. In non-Hybrid burst (MR8[2]=0), MR8[1:0] sets the burst address space in which the device will continually wrap within. If Hybrid burst wrap is selected (MR8[2]=1), the device will burst through the initial wrapped burst length once, then continue to burst incrementally up to maximum column address (2K) before wrapping around within the entire column address space. Burst length (MR8[1:0]) can be set to 16,32,64 & 2K Lengths.

MR8[2]	MR8[1:0]	Burst Length	Example of Sequence of Bytes During Wrap	
			Starting Address	Byte Sequence
'0	'00	16 Byte Wrap	4	[4,5,6,…15,0,1,2,…]
'0	'01	32 Byte Wrap	4	[4,5,6,…31,0,1,2,…]
'0	'10	64 Byte Wrap	4	[4,5,6,…63,0,1,2,…]
'0	'11	2k Byte Wrap	4	[4,5,6,…2047,0,1,2,…]
'1	'00	16 Byte Hybrid	2	[2,3,4,…15,0,1],16,17,18,…2047,0,1,…
'1	'01	16 Byte Hybrid Wrap (Default)	2	[2,3,4,…31,0,1],32,33,34,…2047,0,1,…
'1	'10	64 Byte Hybrid	2	[2,3,4,…63,0,1],64,65,66,…2047,0,1,…
'1	'11	2k Byte Hybrid	2	[2,3,4,…2047,0,1,2,…]

The Linear Burst Commands (INST[5:0]=6'b10_0000) forces the current array read or write command to do 2K Byte Wrap (equivalent to having MR8[1:0] set to 2'b11). For non-RBX enabled devices the burst command read/writes linearly from the starting address and wraps back to the beginning of the page upon reaching the end of the page. To access a different page, host must issue a new command.

Table 18 Row Boundary Crossing Read Enable MR8[3]

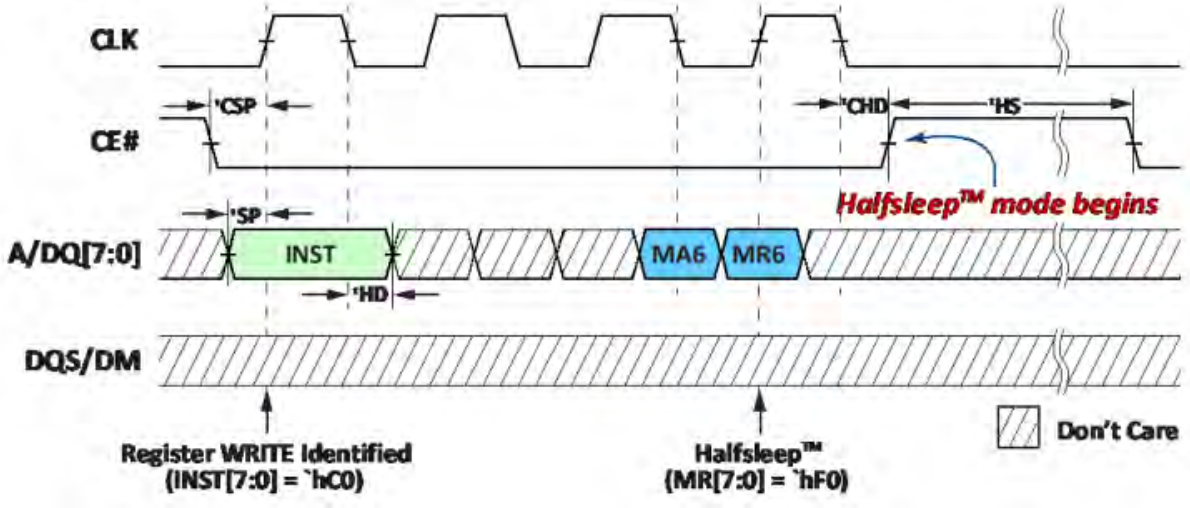
This register setting applies to Linear Burst reads only on RBX enabled devices (MR3[7]=1). Default write and read burst behavior is limited within 2K page (row) address space (CA='h000 -> 'h7FF). Setting this bit high will allow Linear Burst Read command to cross over into the next Row (RA+1).

MR8[3]	RBX Read
0	Reads stay within page (row) boundary
1	Allow reads cross page (row) boundary

8.8 Halfsleep™ Mode

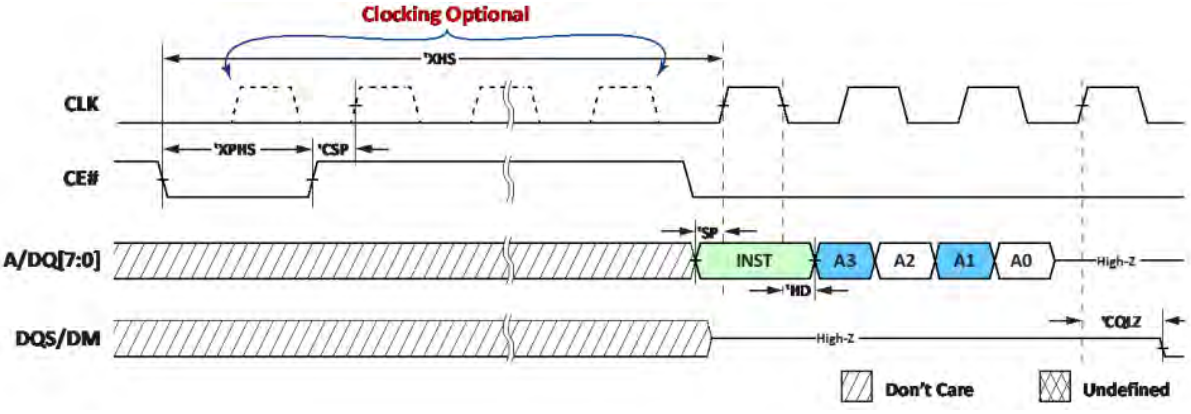
Halfsleep™ Mode puts the device in an ultra-low power state, while the stored data is retained. HalfsleepTM Mode Entry is entered by writing 8'hF0 into MR6. CE# going high initiates the Halfsleep™ mode and must be maintained for the minimum duration of Halfsleep™ time, tHS. The Halfsleep™ Entry command sequence is shown below.

Figure 14 Halfsleep™ Entry Write (latency same as Register Writes, WL1)



Halfsleep™ Exit is initiated by a low pulsed CE#. Afterwards, CE# can be held high with or without clock toggling until the first operation begins (observing minimum Halfsleep™ Exit time, tXHS).

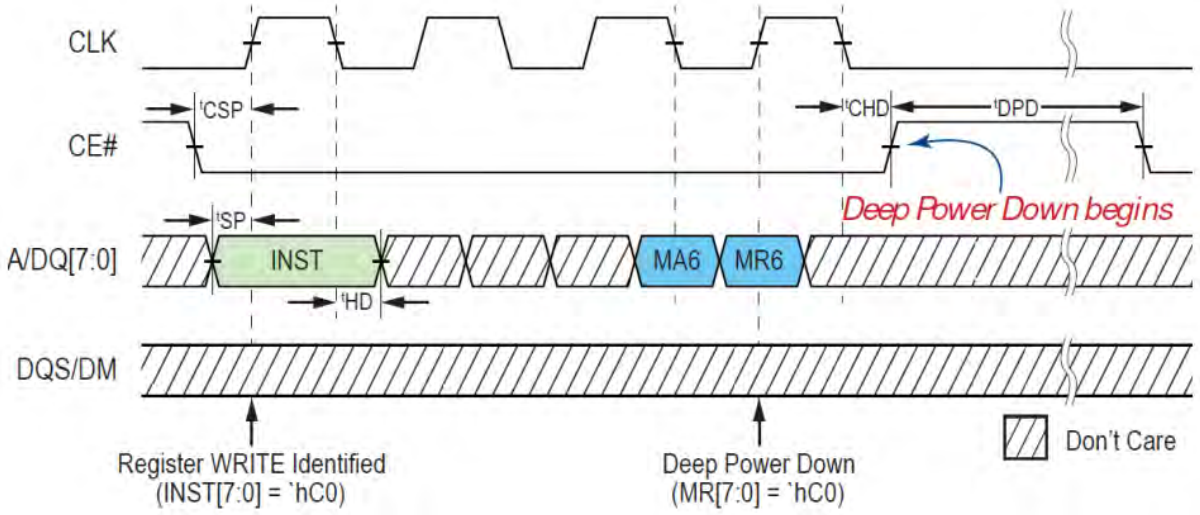
Figure 15 Halfsleep™ Exit (Read Operation shown as example)



8.9 Deep Power Down Mode

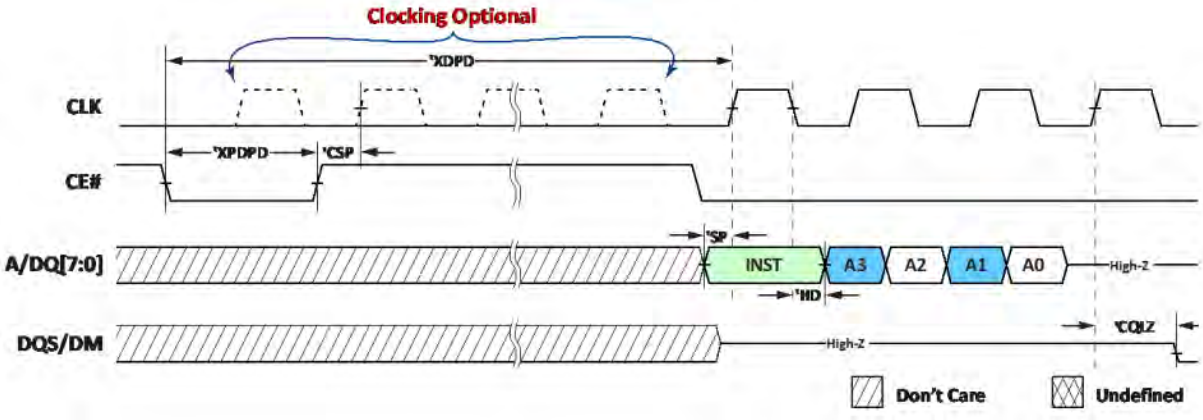
Deep Power Down Mode (DPD) puts the device into power down state. DPD Mode Entry is entered by writing 8'hC0 into MR6. CE# going high initiates the DPD Mode and must be maintained for the minimum duration of Deep Power Down time, tDPD. The Deep Power Down Entry command sequence is shown below.

Figure 16 Deep Power Down Entry



Deep Power Down Exit is initiated by a low pulsed CE#. After a CE# DPD exit, CE# must be held high with or without clock toggling until the first operation begins (observing minimum Deep Power Down Exit time, tXDPD).

Figure 17 Deep Power Down Exit (Read Operation shown as example)



Register values and memory content are not retained in DPD Mode. After DPD mode register values will reset to defaults. tDPDp is minimum period between two DPD Modes (measured from DPD exit to the next DPD entry) as well as from the initial powerup to the first DPD entry.

9. Electrical Specifications

9.1 Absolute Maximum Ratings

Table 19 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage to any ball except V_{DD}, V_{DDQ} relative to V_{SS}	VT	-0.4 to V_{DD}/V_{DDQ}+0.4	V	
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.4 to +2.45	V	
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.4 to +2.45	V	
Storage Temperature	T_{STG}	-55 to +150	°C	1

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

9.2 Pin Capacitance

Table 20 Package Pin Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	CIN		5	pF	VIN=0V
Output Pin Capacitance	COUT		6	pF	VOUT=0V

Note: spec'd at 25°C.

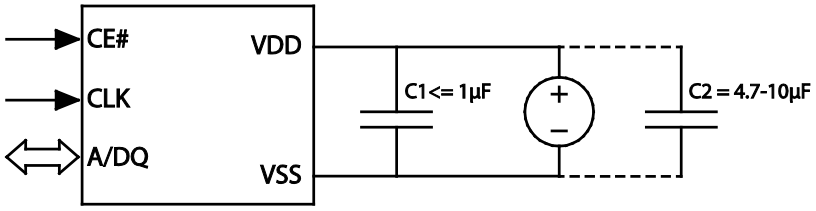
Table 21 Load Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Load Capacitance	C_L		15	pF	

Note: System C_L for the use of package

9.3 Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.



9.3.1 Low ESR cap C1:

It is recommended to place a low ESR decoupling capacitor of <=1µF close to the device to absorb transient peaks.

9.3.2 Large cap C2:

Though half-sleep average current is small (less than 100µA), its peak current from internal periodical burst refresh can reach up to the level of 25mA. The peak current duration can last for few tens of microseconds. During this period if the system regulator cannot supply such large peaks, it is important to place a 4.7µF-10µF cap to cover the burst refresh current demand and replenish the cap before the next burst of refresh.

9.4 Operating Conditions

Table 22 Operating Characteristics

Parameter	Min	Max	Unit	Notes
Operating Temperature (extended)	-40	105	°C	
Operating Temperature (standard)	-40	85	°C	

9.5 DC Characteristics

Table 23 DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Supply Voltage	1.62	1.98	V	
V_{DDQ}	I/O Supply Voltage	1.62	1.98	V	
V_{IH}	Input high voltage	V_{DDQ}-0.4	V_{DDQ}+0.3	V	
V_{IL}	Input low voltage	-0.3	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{DDQ}		V	
V_{OL}	Output low voltage (I_{OL}=+0.2mA)		0.2 V_{DDQ}	V	
I_{LI}	Input Pin leakage current		1	µA	
I_{LO}	Output Pin leakage current		1	µA	
ICC	Read/Write @13MHz		5	mA	1
	Read/Write @133MHz		19	mA	1
	Read/Write @166MHz		22	mA	1
	Read/Write @200MHz		26	mA	1
ISB_{EXT}	Standby current (105C)		1100	µA	2
ISB_{STD}	Standby current (85C)		680	µA	2
ISB_{STDDPD}	Standby current (Deep Power Down -40°C to 85°C)		20	µA	7

Note:
1. Current is only characterized.
2. Without CLK toggling. ISB will be higher if CLK is toggling.
3. 0.5x Refresh.
4. Typical mean $ISB_{STDROOM}$ 90uA.
5. Current is only guaranteed after 150ms into Halfsleep™ mode.
6. Typical ISB_{STDHS} 40uA
7. Typical mean ISB_{STDDPD} 8uA at 25°C

9.6 ISB Partial Array Refresh Current

Table 24 Typical-mean PASR Current @ 25°C

Standby Current @ 25°C			
PASR	**ISB –typical mean**	**Unit**	**Notes**
Full	90	µA	1, 2
1/2	80	µA	1, 2
1/4	75	µA	1, 2
1/8	72	µA	1, 2
Halfsleep™ Current @ 25°C			
PASR	**I Halfsleep™-typical**	**Unit**	**Notes**
Full	40	µA	1,2,3
1/2	30	µA	1,2,3
1/4	25	µA	1,2,3
1/8	22	µA	1,2,3

Table 25 Typical-mean PASR Current @85°C

Standby Current @ 85°C			
PASR	**ISB –typical mean**	**Unit**	**Notes**
Full	530	µA	2
1/2	370	µA	2
1/4	290	µA	2
1/8	250	µA	2
Halfsleep™ Current @ 85°C			
PASR	**I Halfsleep™-typical**	**Unit**	**Notes**
Full	440	µA	2, 3
1/2	300	µA	2, 3
1/4	230	µA	2, 3
1/8	190	µA	2, 3

Note: 1. Current at 25oC is only attainable by enabling 0.5x Refresh Frequency (see Table 15)
2. PASR Current is only characterized without CLK toggling.
3. Spec'd Halfsleep™ current is only guaranteed after 150ms into Halfsleep™ mode.

9.7 AC Characteristics

Table 26 READ/WRITE Timing

		BGA 1.8V Only							
		-7(133MHz)		-6(166MHz)		-5(200MHz)			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
tCLK	CLK period	7.5		6		5		ns	
tCH/tCL	Clock high/low width	0.45	0.55	0.45	0.55	0.45	0.55	tCLK	
tKHKL	CLK rise or fall time		1.2		1		0.8	ns	
tCPH	CE# HIGH between subsequent burst operations	15		18		24		ns	
tCEM	CE# low pulse width (excluding Halfsleep™ exit)		4		4		4	µs	Standard temp
			1		1		1	µs	Extended temp
tCEM	CE# low pulse width	3		3		3		tCLK	Minimum 3
tCSP	CE# setup time to CLK rising edge	2		2		2		ns	
tCSP2	CE# rising edge to next CLK falling edge	1.5		1.5		1.5		ns	
tCHD	CE# hold time from CLK falling edge	2		2		2		ns	
tSP	Setup time to active CLK edge	0.8		0.6		0.5		ns	
tHD	Hold time from active CLK edge	0.8		0.6		0.5		ns	Max .75*tCLK
tHZ	Chip disable to DQ/DQS output high-Z		6		6		6	ns	
tRBXwait	Row Boundary Crossing Wait Time	30	65	30	65	30	65	ns	
tRC	Write Cycle	60		60		60		ns	
tRC	Read Cycle	60		60		60		ns	
tHS	Minimum Halfsleep™ duration	150		150		150		µs	
tXHS	Halfsleep™ Exit CE# low to CLK setup time	150		150		150		µs	
tXPHS	Halfsleep™ Exit CE# low pulse width	60		60		60		ns	
			tCEM		tCEM		tCEM	µs	Standard temp
								µs	Extended temp
tDPD	Minimum DPD duration	500		500		500		µs	
tDPDp	Minimum period between DPD Modes	500		500		500		µs	
tXDPD	DPD CE# low to CLK setup time	150		150		150		µs	
tXPDPD	DPD Exit CE# low pulse width	60		60		60		ns	
tPU	Device Initialization	150		150		150		µs	
tRP	RESET# low pulse width	1		1		1		µs	
tRST	Reset to CMD valid	2		2		2		µs	

Table 27 DDR Timing Parameters

		BGA 1.8V Only							
		-7(133MHz)		-6(166MHz)		-5(200MHz)			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
tCQLZ	Clock rising edge to DQS low	1	6	1	6	1	6	ns	
tDQSCK	DQS output access time from CLK	2	6.5	2	6.5	2	6.5	ns	
tDQSQ	DQS – DQ skew		0.6		0.5		0.4	ns	
tDS	DQ and DM input setup time	0.8		0.6		0.5		ns	
tDH	DQ and DM input hold time	0.8		0.6		0.5		ns	

10. Revision History

Vision	Who	Date	Description
1	William CHEN	Dec 12th 2022	Initial branded release