Nanoscale Materials and Structures for CMOS Devices

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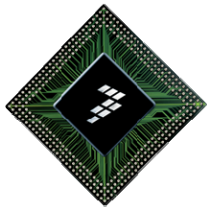

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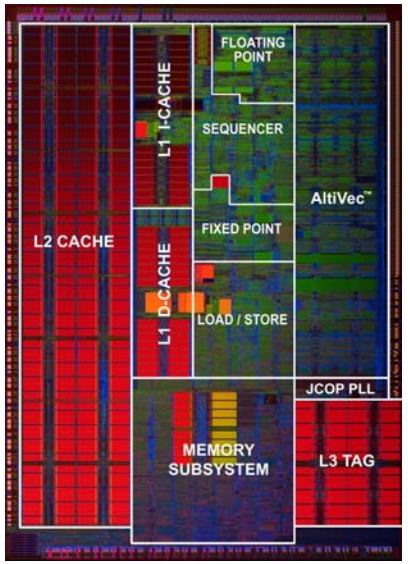
Overview

Introduction:

- Scaling and Moore's law
- Scaling is difficult!



Five **problems** with planar CMOS and their **solutions**:

1. SOI or FINFET to reduce source/drain leakage
2. High mobility channel materials to increase drive current
3. New silicide materials to reduce source/drain contact resistance
4. Metal oxides with high dielectric constants to reduce gate leakage
5. Metal gate electrodes to reduce gate depletion (reduced EOT)

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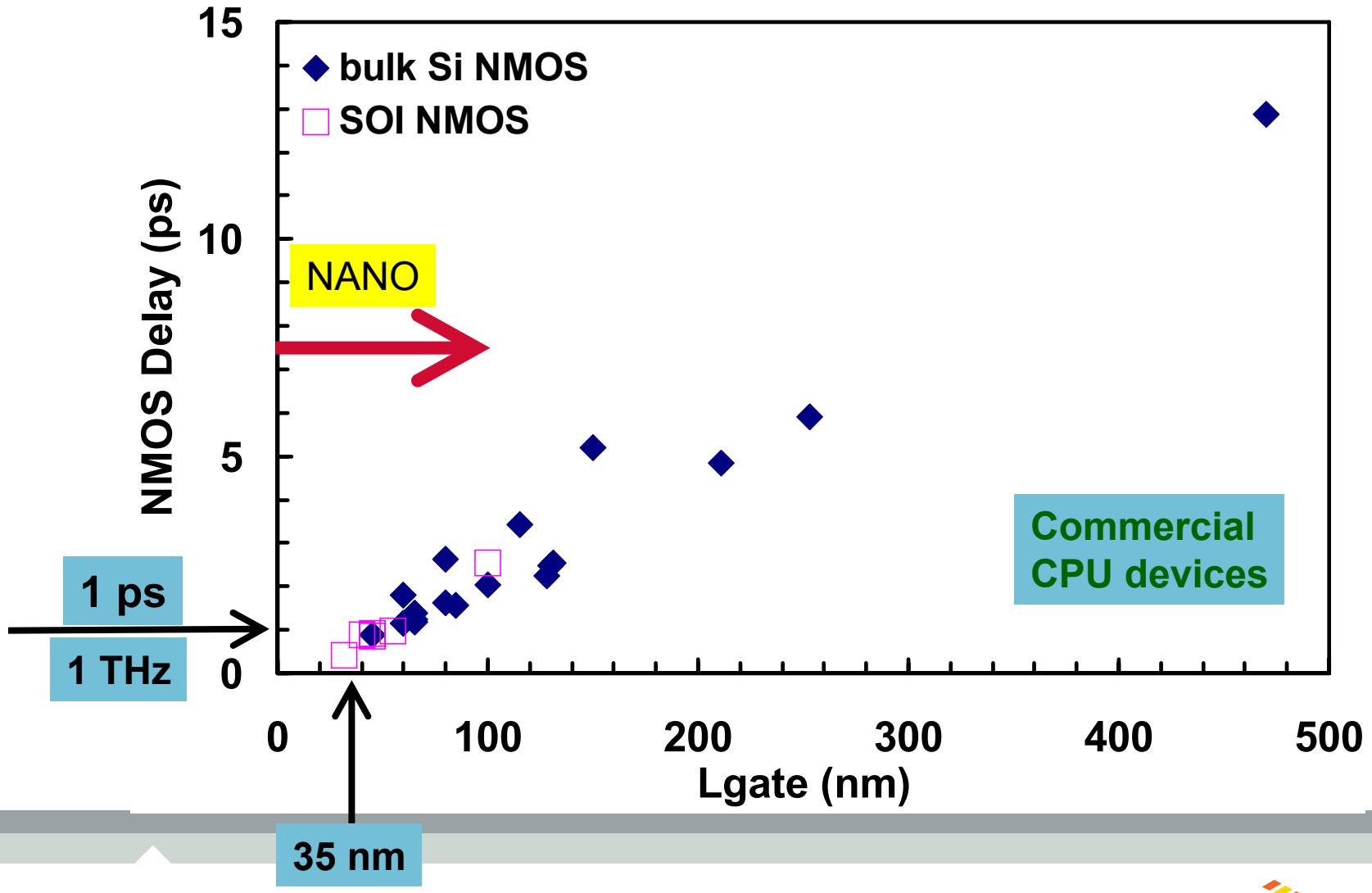
Moore's Law: CMOS technology reaches the nanoscale

Transistors get faster, smaller, and **cheaper** with every generation: **Moore's law.**



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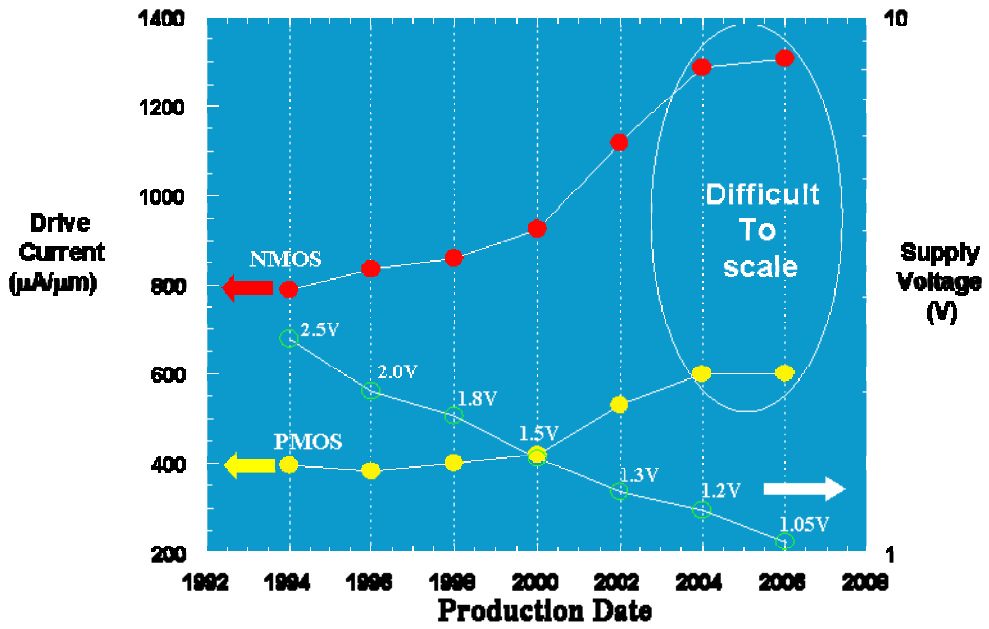
Moore's Law: Why do we scale?



Maintain high drive current while simultaneously dropping supply voltage.

ISuppli Table: Top-25 Suppliers of Semiconductor Worldwide in 2007 (Ranking by Revenue in Millions of U.S. Dollars)

2006 Rank	2007 Rank	Company Name	2006 Revenue	2007 Revenue	Percent Change	Percent of Total	Cumulative Percentage
1	1	Intel	31,542	33,995	7.8%	12.6%	12.6%
2	2	Samsung Electronics	19,842	19,691	-0.8%	7.3%	20.0%
3	3	Texas Instruments	12,600	12,275	-2.6%	4.6%	24.5%
4	4	Toshiba	10,141	12,186	20.2%	4.5%	29.1%
5	5	STMicroelectronics	9,854	10,000	1.5%	3.7%	32.8%
7	6	Hynix	7,865	9,047	15.0%	3.4%	36.1%
6	7	Renesas Technology	7,900	8,001	1.3%	3.0%	39.1%
14	8	Sony	5,129	7,974	55.5%	3.0%	42.1%
15	9	Infineon Technologies	5,119	6,201	21.1%	2.3%	44.4%
8	10	Advanced Micro Devices (AMD)	7,505	5,918	-21.2%	2.2%	46.6%
9	11	NXP	5,707	5,746	0.7%	2.1%	48.7%
11	12	NEC Electronics	5,601	5,742	2.5%	2.1%	50.9%
16	13	Qualcomm	4,529	5,619	24.1%	2.1%	53.0%
10	14	Freescale Semiconductor	5,616	5,264	-6.3%	2.0%	54.9%
13	15	Micron Technology	5,247	4,869	-7.2%	1.8%	56.7%
12	16	Qimonda	5,413	4,005	-26.0%	1.5%	58.2%
19	17	Elpida Memory	3,527	3,838	8.8%	1.4%	59.6%
17	18	Matsushita Electric	4,022	3,800	-5.5%	1.4%	61.1%
18	19	Broadcom	3,668	3,746	2.1%	1.4%	62.4%
25	20	nVidia	2,578	3,466	34.4%	1.3%	63.7%
20	21	Sharp Electronics	3,341	3,401	1.8%	1.3%	65.0%
21	22	IBM Microelectronics	3,172	2,977	-6.1%	1.1%	66.1%
26	23	Marvell Technology Group	2,550	2,777	8.9%	1.0%	67.1%
23	24	Analog Devices	2,603	2,707	4.0%	1.0%	68.1%
22	25	Rohm	2,882	2,633	-8.6%	1.0%	69.1%
		Other Companies:	82,401	83,027	0.8%	30.9%	100.0%
		Total Revenue:	260,355	268,905	3.3%	100.0%	

Revenue, profit, and ROI (return on investment) are the driving forces that define the slope of Moore's law. Science issues are secondary.

"The point of innovation is to make ACTUAL money."

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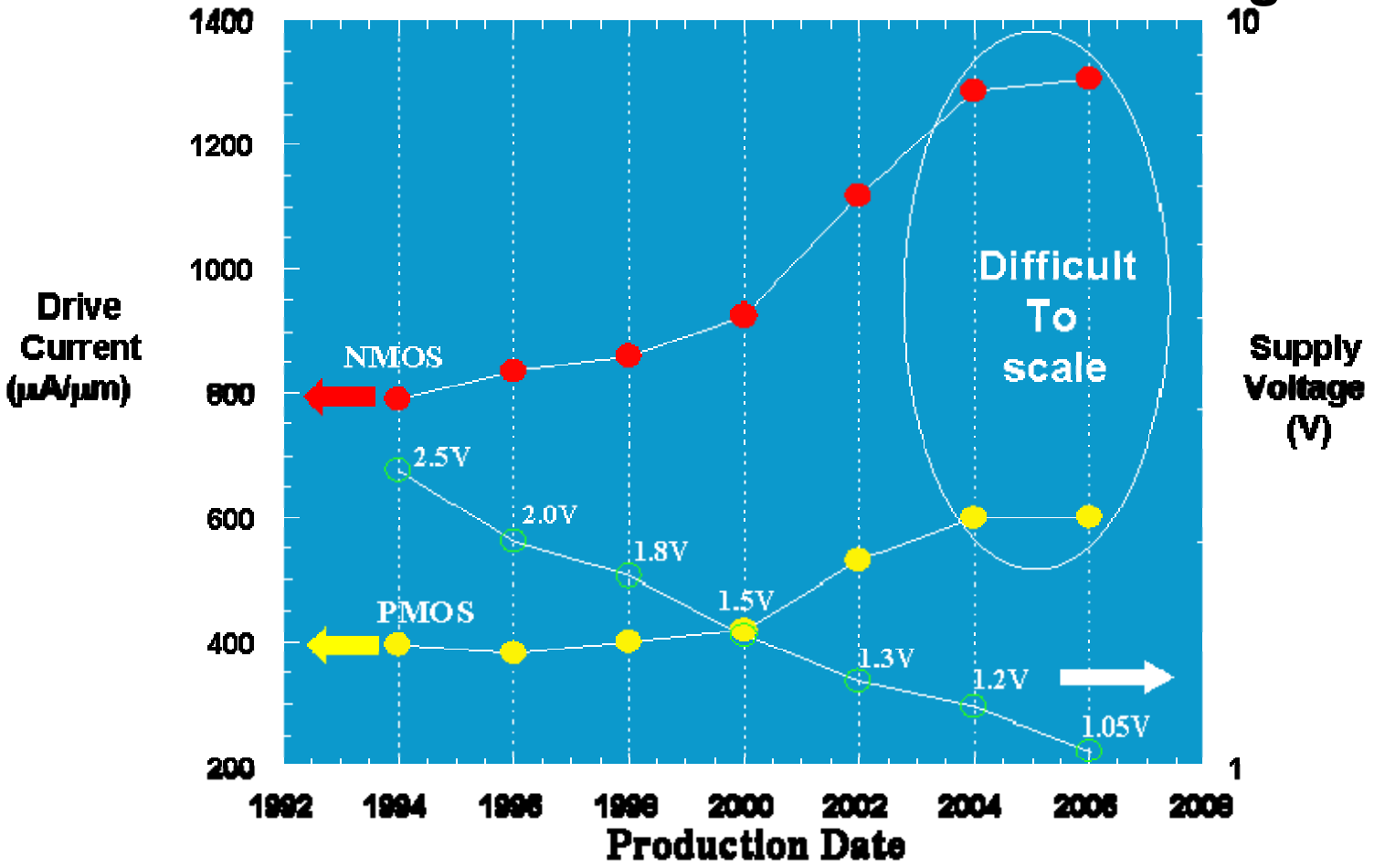
Moore's Law: Scaling is difficult



Maintain high drive current while simultaneously dropping supply voltage.

We can ignore science issues, but they need to be addressed eventually!

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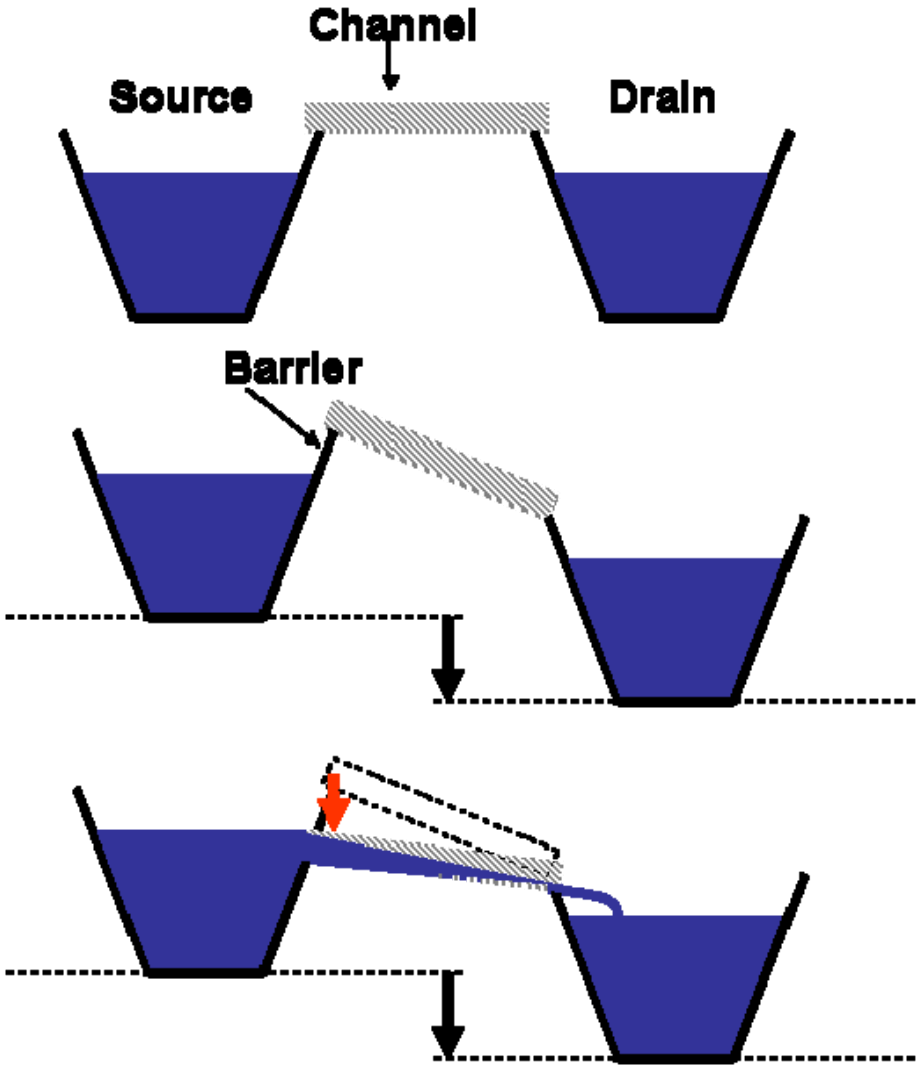
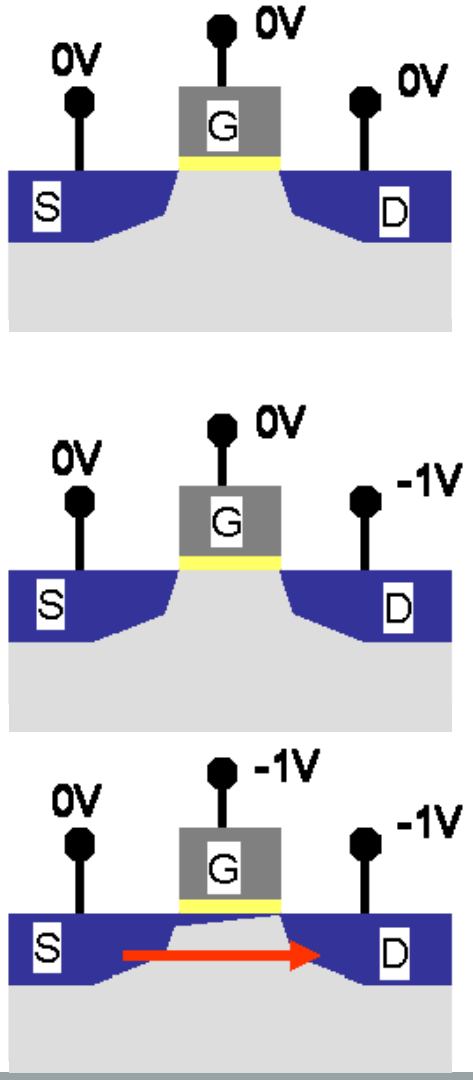
Simple view of a MOSFET





Current flows through MOSFET

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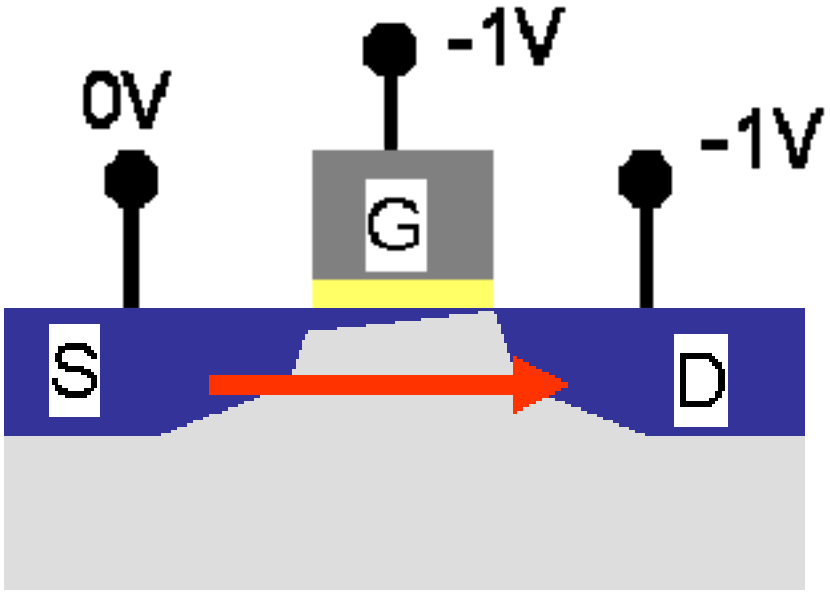
Five problems with planar CMOS

Five **problems** with planar CMOS and their **solutions**:

1. SOI or FINFET to reduce source/drain leakage (I_{off})
2. Strain engineering to increase drive current (I_{on})
3. New silicide materials to reduce parasitic external resistance
4. Metal oxides with high dielectric constants to reduce gate leakage
5. Metal gate electrodes to reduce gate depletion (reduced EOT)



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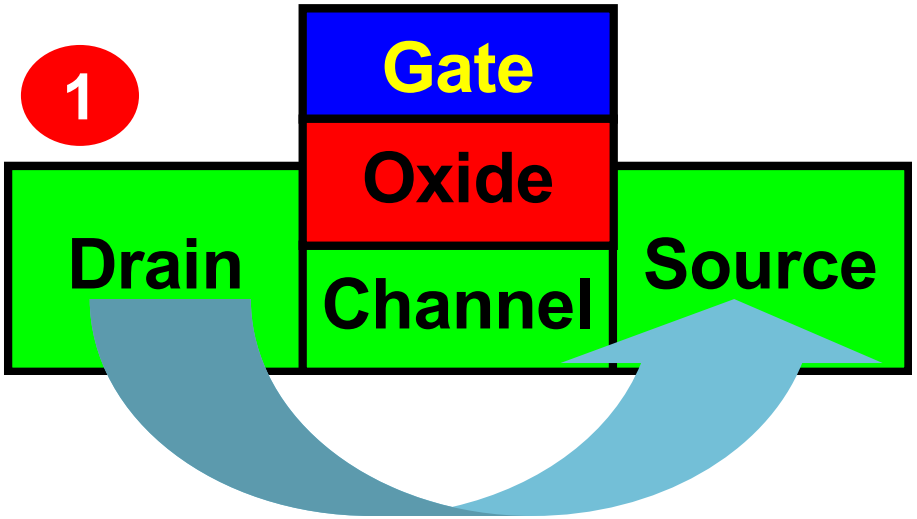
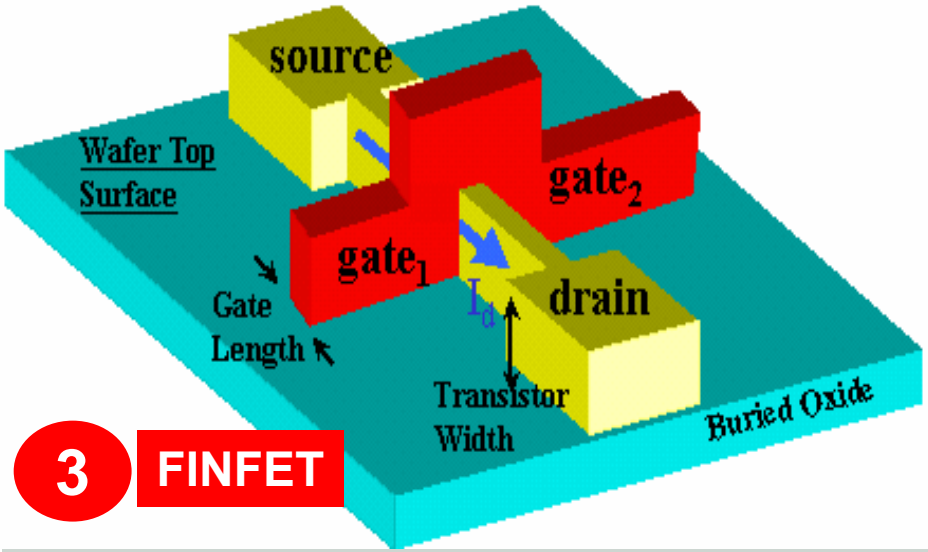
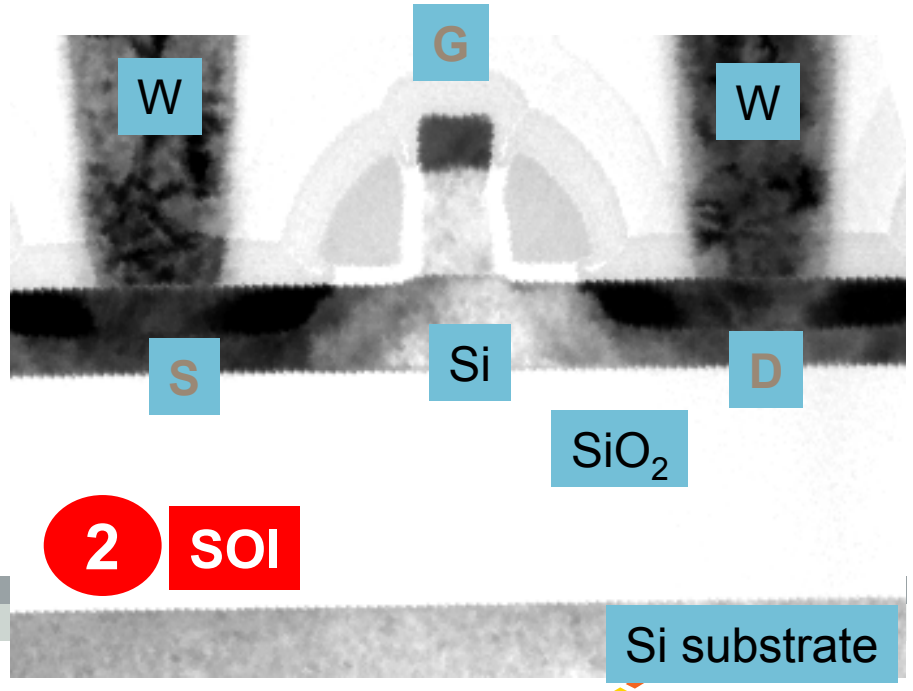
Problem 1: Poor electrostatics increases I_{off}



Problem: Parasitic source-drain leakage through the substrate.

Solution: Silicon-on-insulator (SOI) or double-gate devices (FINFETs)





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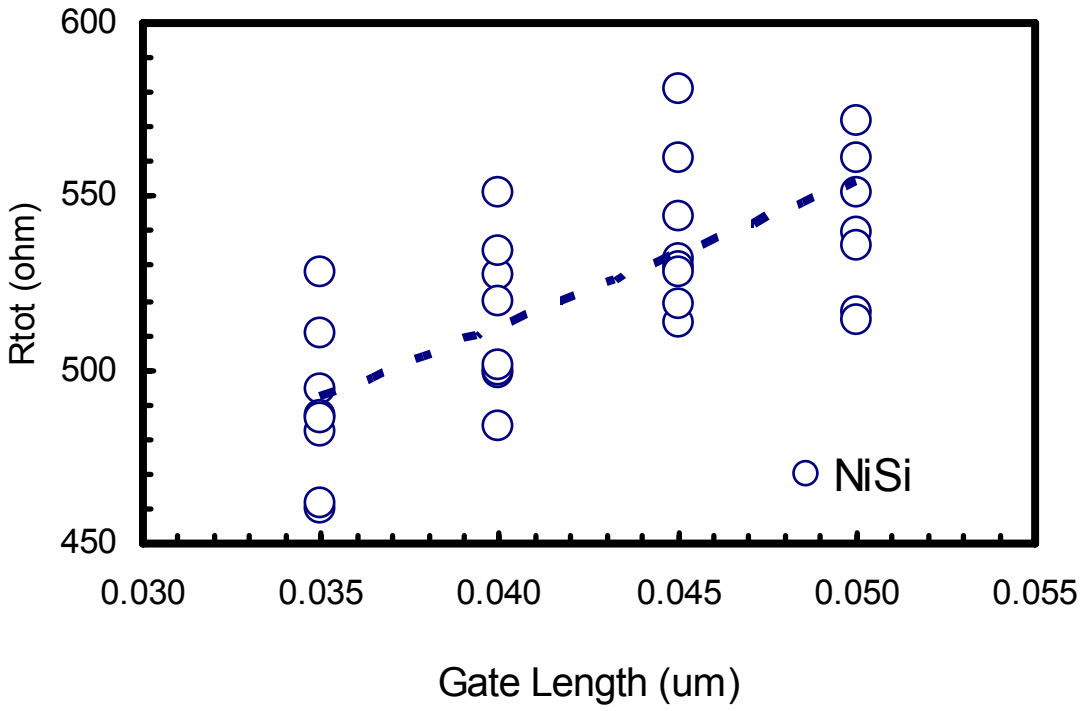
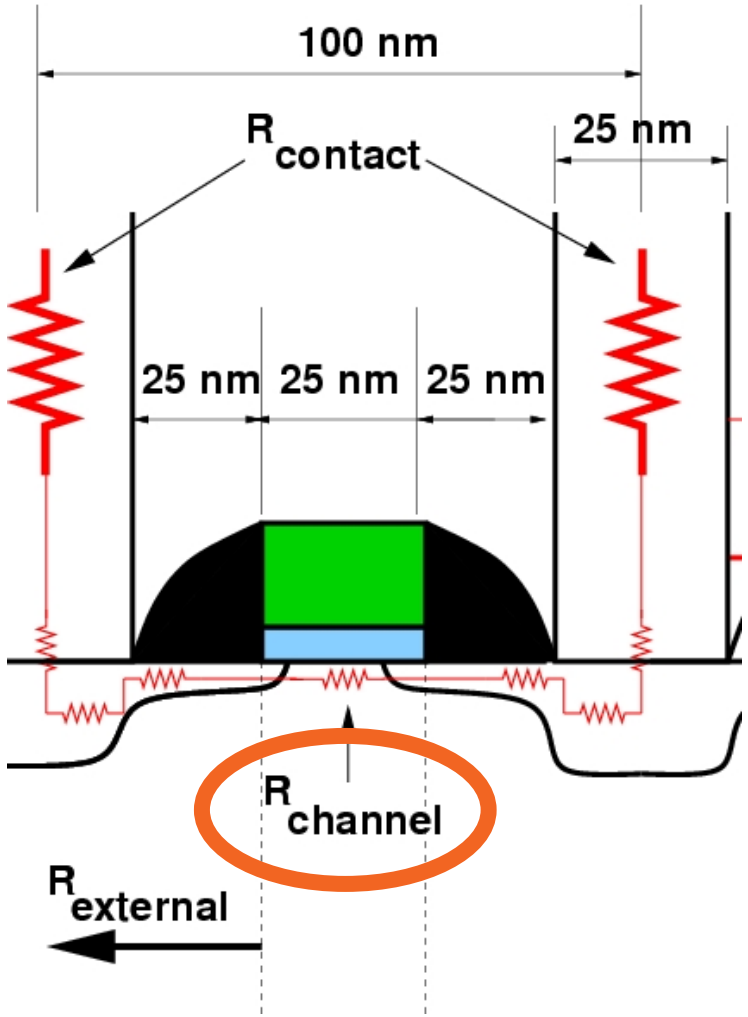
Problem 2: Poor channel mobility decreases I_{on}

Channel mobility limits I_{on}

$R_{tot}=R_{ext}+R_{ch}$
R_{ch} scales with gate length (slope)
R_{ext} does not scale (offset)





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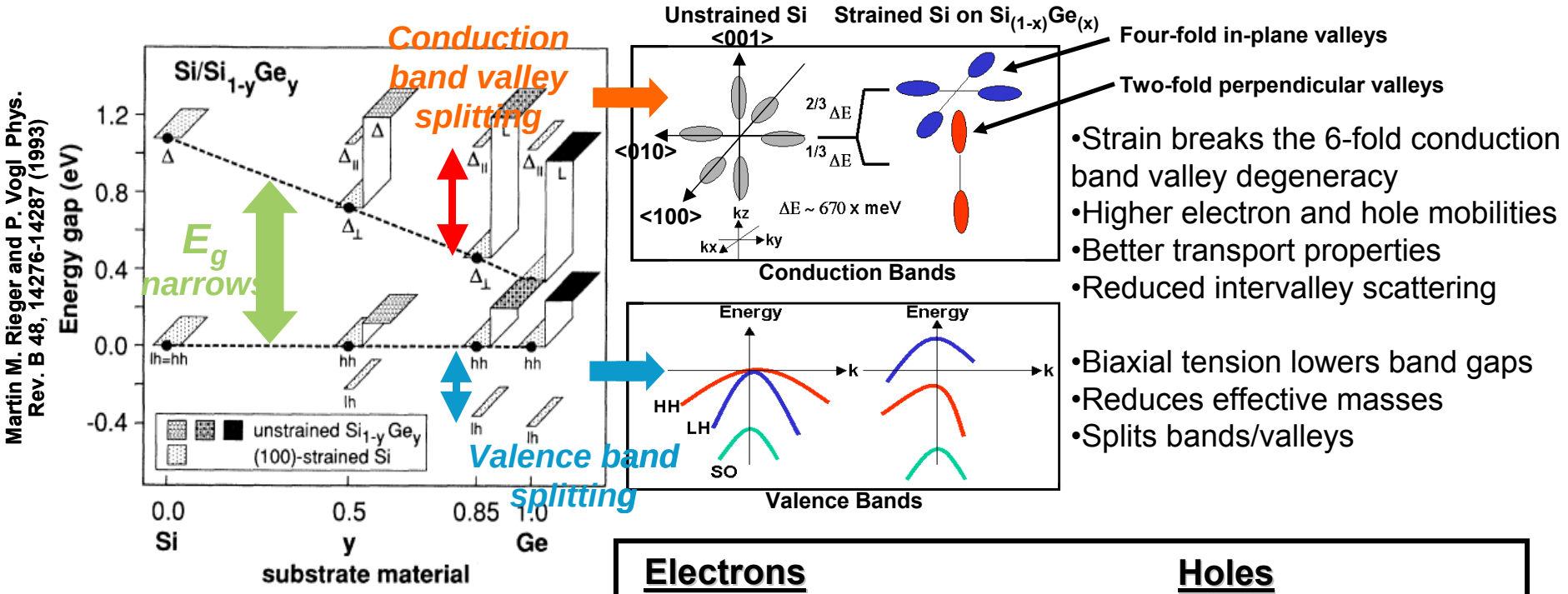
Enhanced channel mobility with stressor elements



- Strain breaks the 6-fold conduction band valley degeneracy
- Higher electron and hole mobilities
- Better transport properties
- Reduced intervalley scattering

- Biaxial tension lowers band gaps
- Reduces effective masses
- Splits bands/valleys

Electrons	Holes
-Reduced (f,g) intervalley electron-phonon scattering	-Reduced interband hole-phonon scattering
-Preferential thermal population of electron states with light transport effective mass	-Reduced hole effective mass due to band warping

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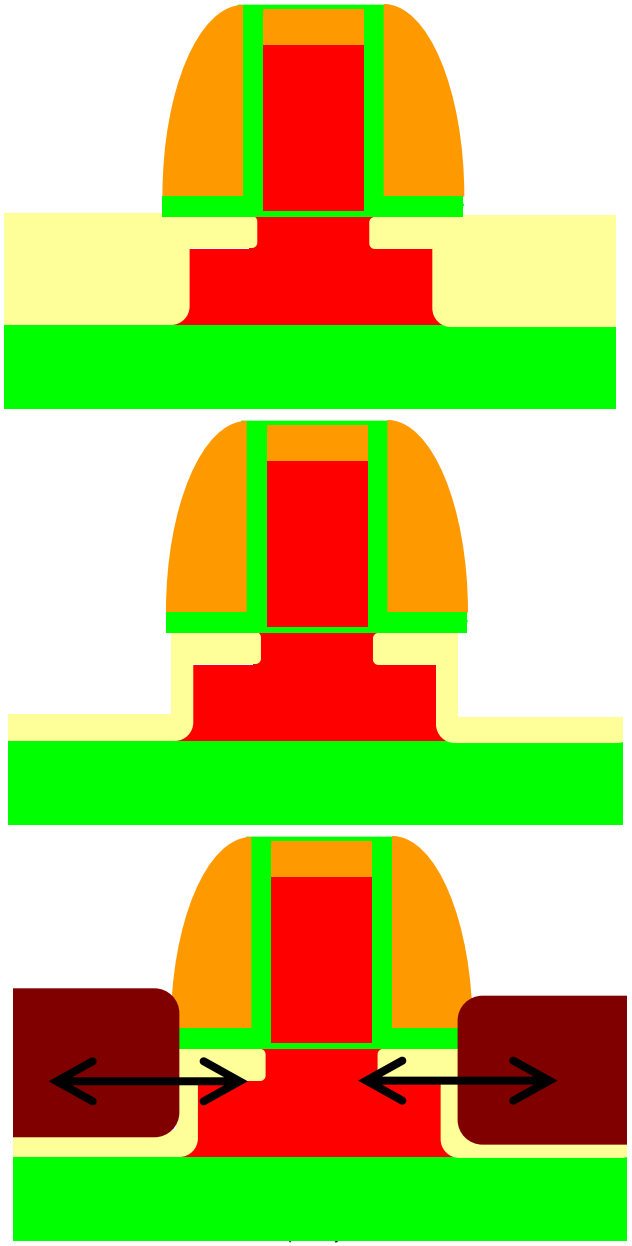
Source-Drain Stressor Integration



- Gate Formation
- Extension, Spacer, S/D Formation
- Dopant Actication Anneal
- Source-drain recess etch
- Si:C or SiGe selective epitaxy
- MEOL + BEOL Processing

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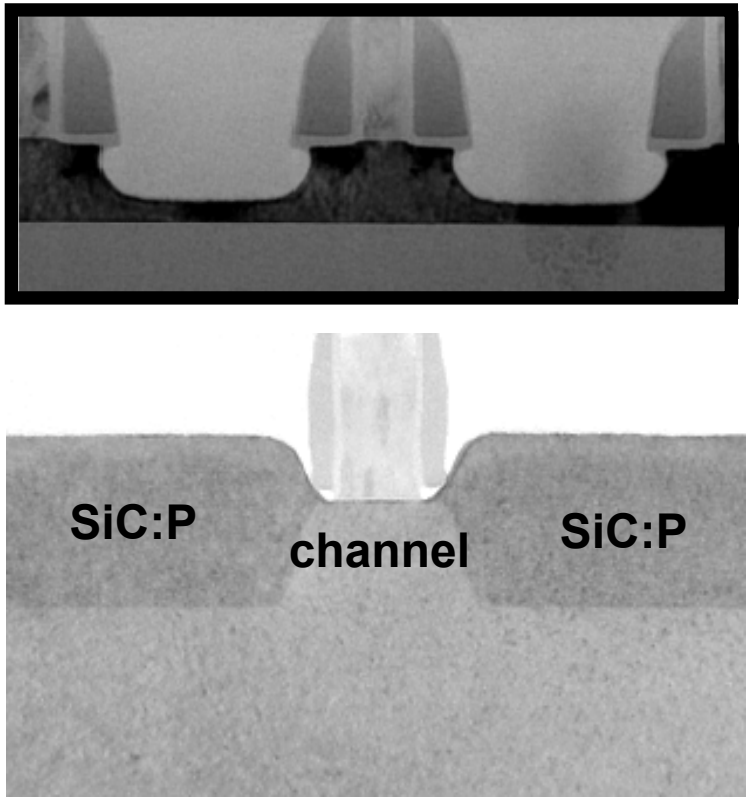
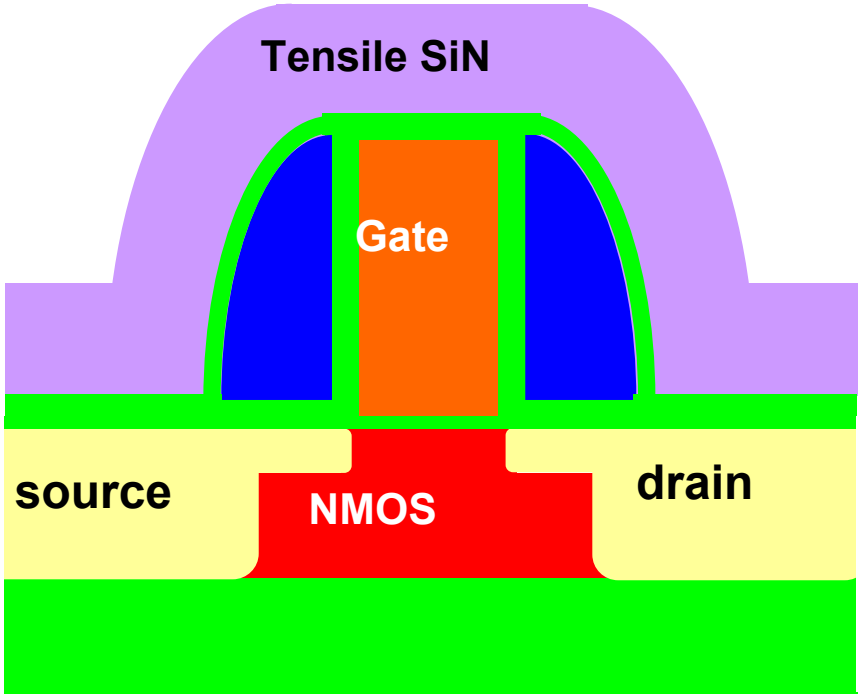
CMOS devices with process-induced stress



Embedded source-drain stressors
(1) SiGe:B for PMOS
(2) Si:C:As for NMOS



Stress memorization technique (SMT) - shown
Dual-stress liners (DSL) – not shown
Stressed silicon nitride layer to enhance mobility:
(1) Compressive nitride for PMOS
(2) Tensile nitride for NMOS

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Problem 3: Parasitic external resistance decreases I_{on}

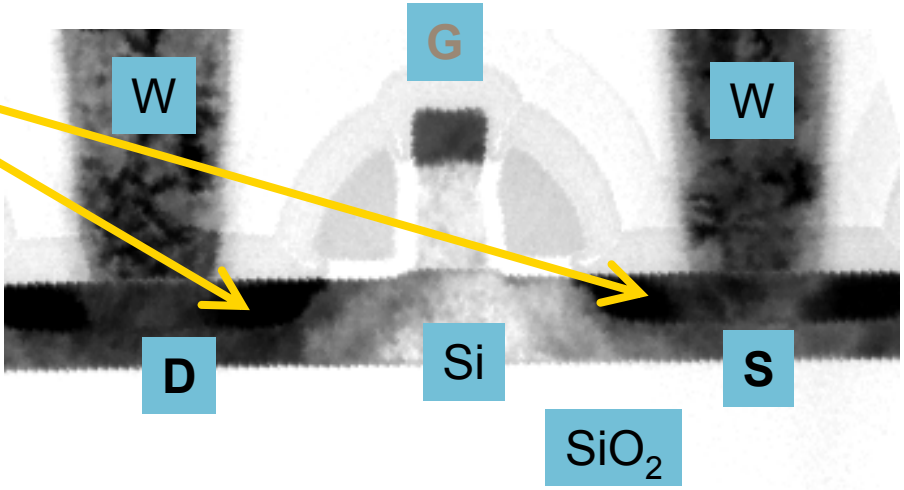
Transition metal (Ti, Co, Ni, Pt, etc) silicides provide Ohmic contacts between the source-drain regions and the metal (W, Cu, Al) interconnects.

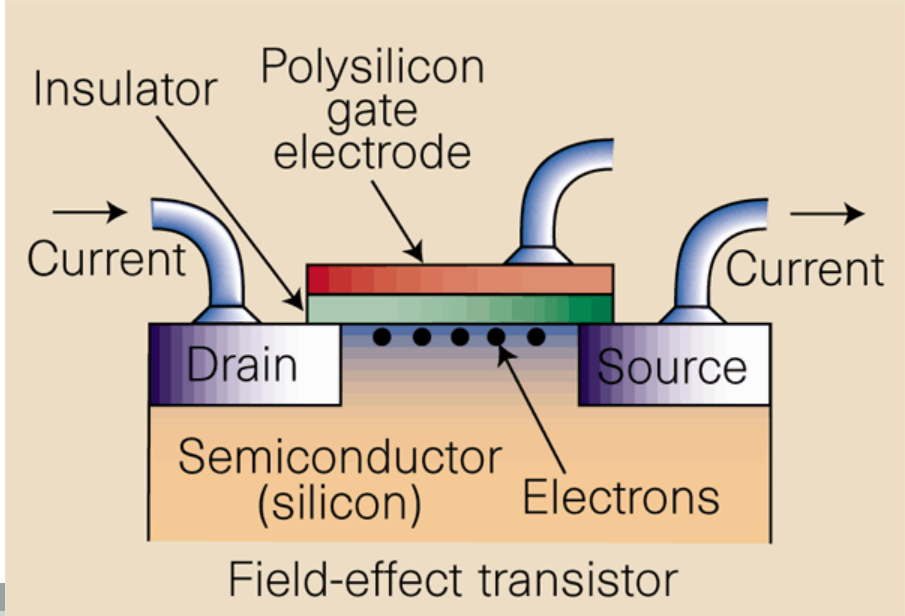
Advantages of Nickel Silicide:

- Low Si consumption (92 Å of Si per 100 Å of Ni).
- Diffusion-controlled reaction mechanism yields uniform coverage, even in thin layers on narrow poly-Si lines.
- Low resistivity of NiSi (1.5 μΩcm).

Disadvantages of Nickel Silicide:

- NiSi is metastable ($NiSi_2$ forms at high temperatures).
- Fast diffusion of Ni in Si at low temperatures (~200°C).
- Agglomeration of thin NiSi films.
- **Schottky barrier of 0.5 V for NFET and PFET.**





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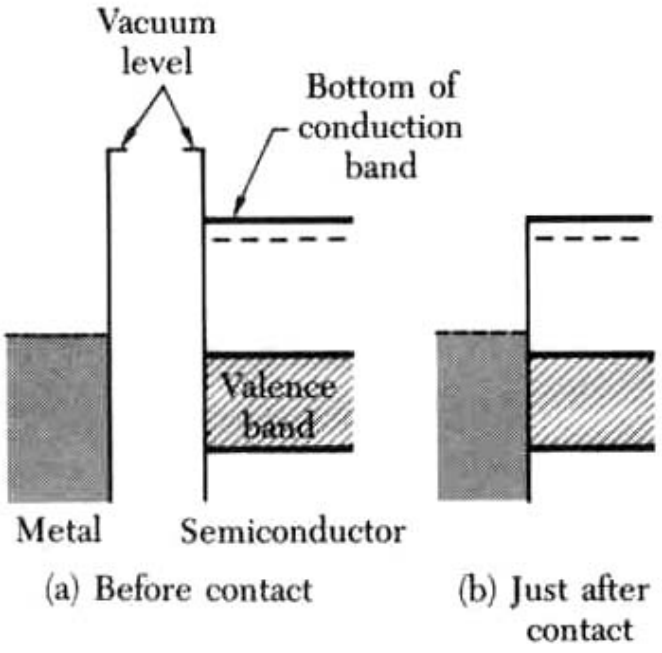
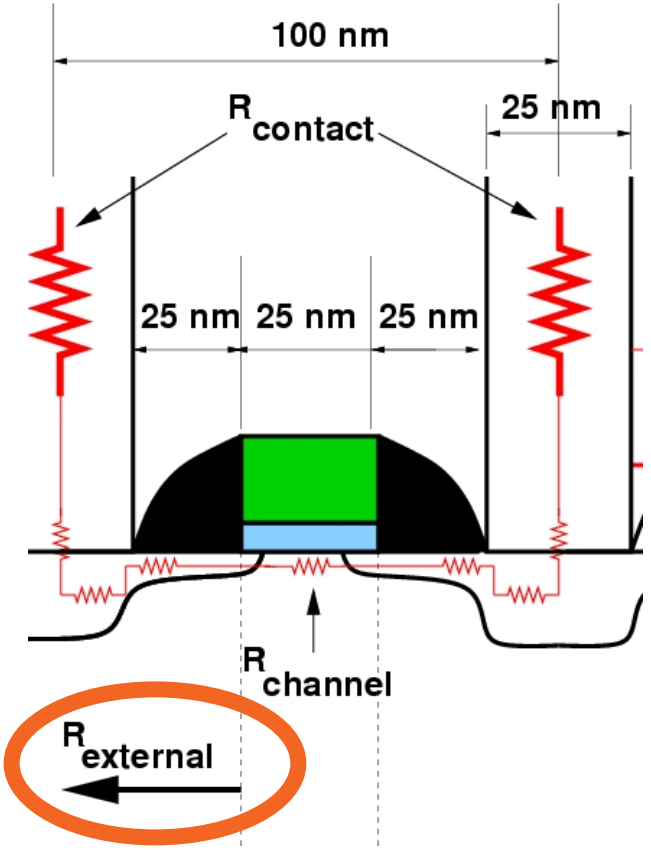
Metal-Semiconductor Contacts: Schottky Barriers

Work function: Distance from Fermi level to vacuum level.
Most contacts are rectifying because of different work functions of the two materials.
Work is needed (power wasted) for a carrier to cross this **Schottky barrier** **(parasitic resistance)**.



Schottky barrier (Kittel)



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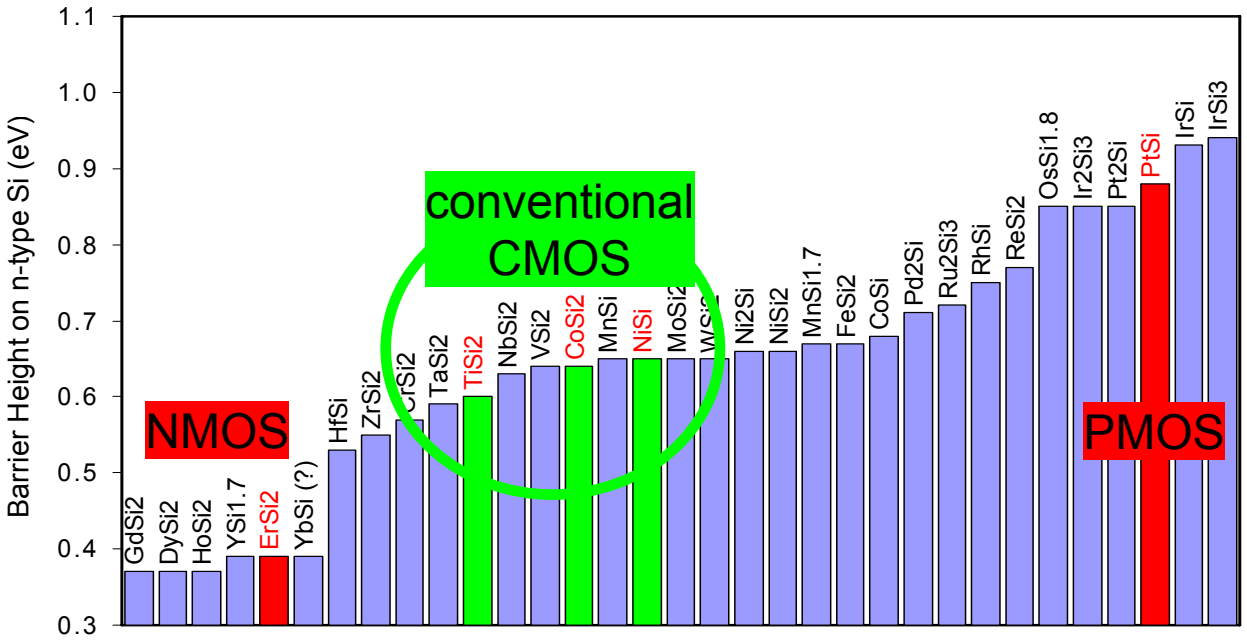
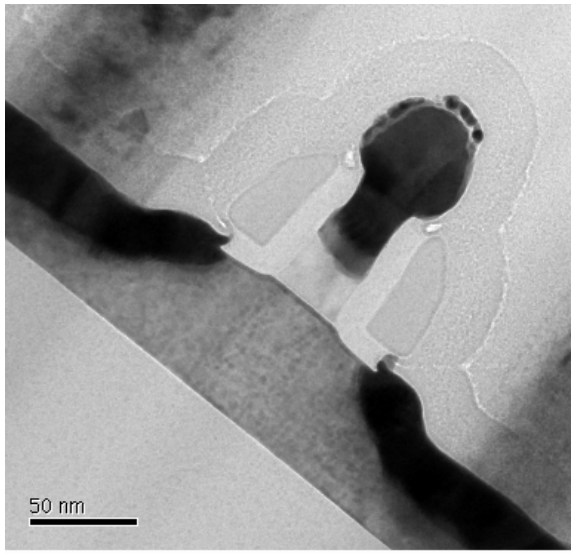
Problem 3: Parasitic external resistance decreases I_{on}



PtSi for PMOS



Future CMOS devices will lose 20% of their power in the contacts.
New materials for low-barrier contacts are crucial to reduce power.

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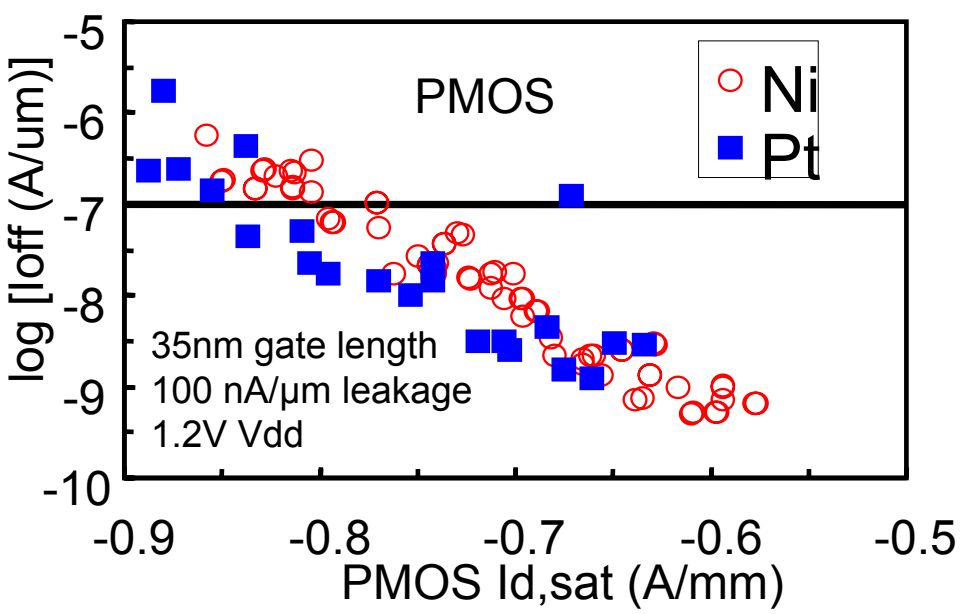
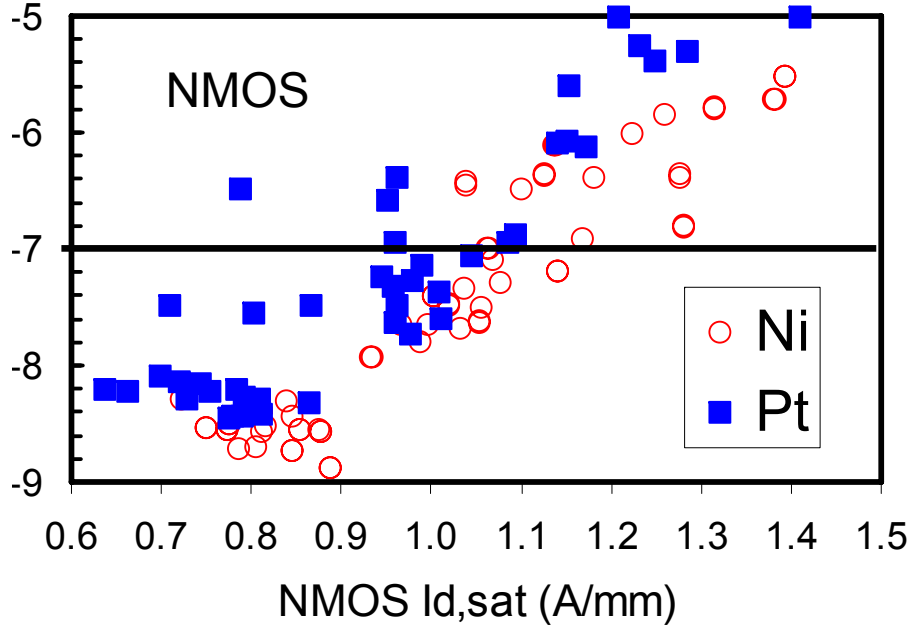
Problem 3: Use PtSi for PMOS contacts

PMOS Performance Improved, NMOS degraded





Relative % change relative to NiSi

	IonIoff
PMOS	8.5%

Relative % change relative to NiSi

	IonIoff
NMOS	-9.0%

Similar improvement for $I_{d,lin}$ and for PMOS devices with SiGe S/D stressors.

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Dual silicide process: PtSi for PMOS, NiSi for NMOS

Baseline CMOS flow to source-drain activation anneal

Pattern hardmask to cover NMOS

Pt deposition, anneal

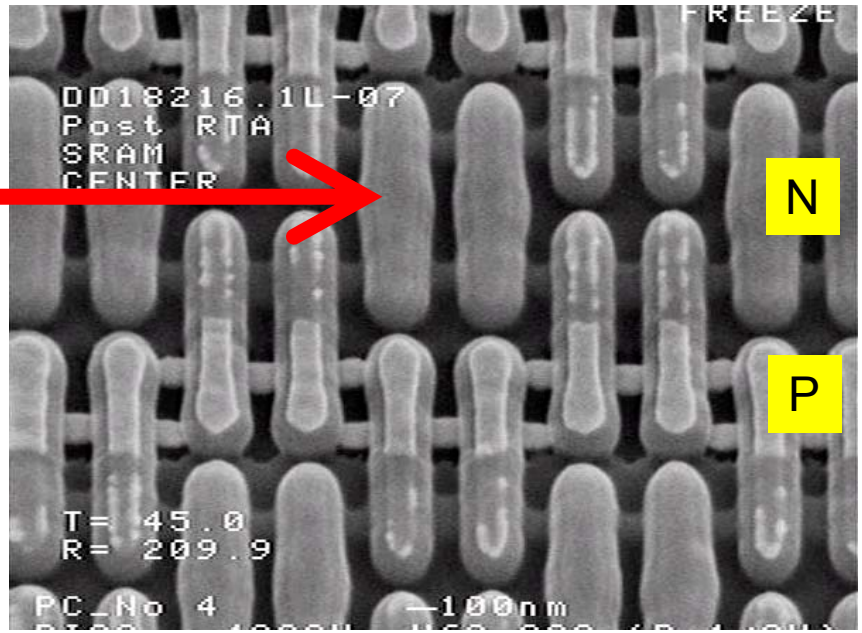
Pt-PtSi selective etch

Remove oxide hardmask

Ni dep, anneal, selective etch

ILD0 module with etch stop stressors, back-end CMOS process

One additional mask:
- PMOS has PtSi
- NMOS unsilicided



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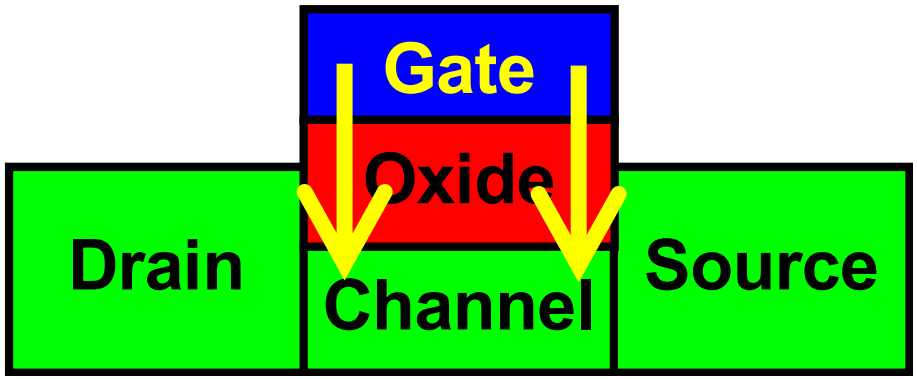
Problems 4/5: Gate leakage, Si/SiO_2 charge depletion



Scaling:

Channel doping increases (channel resistance, Debye length), requires higher gate capacitance to turn device off.

Problem:

Gate oxide thickness needs to shrink to turn the device off.

Tunneling through the gate oxide leads to excess gate leakage.

Solution:

Use metal oxide (HfO_2) with higher dielectric constant than SiO_2.

High-k gate dielectrics are expected to be introduced at the 45nm and 32nm CMOS device generations.

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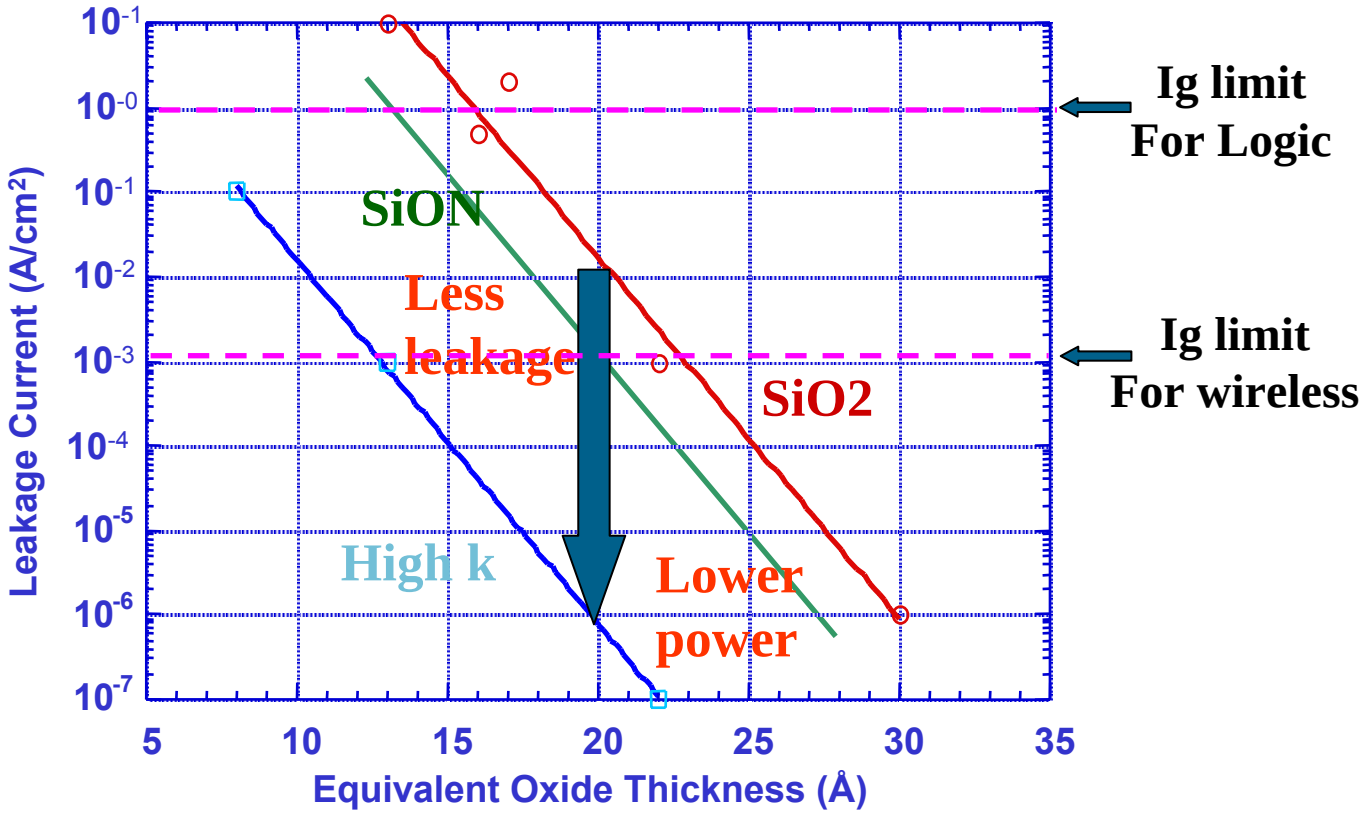
Gate leakage reduction by high-k oxides



Use a thicker gate oxide with a higher dielectric constant to reduce leakage: $C_{ox} = k\varepsilon_o A/t_{ox}$

k means ε, the low-frequency dielectric constant.

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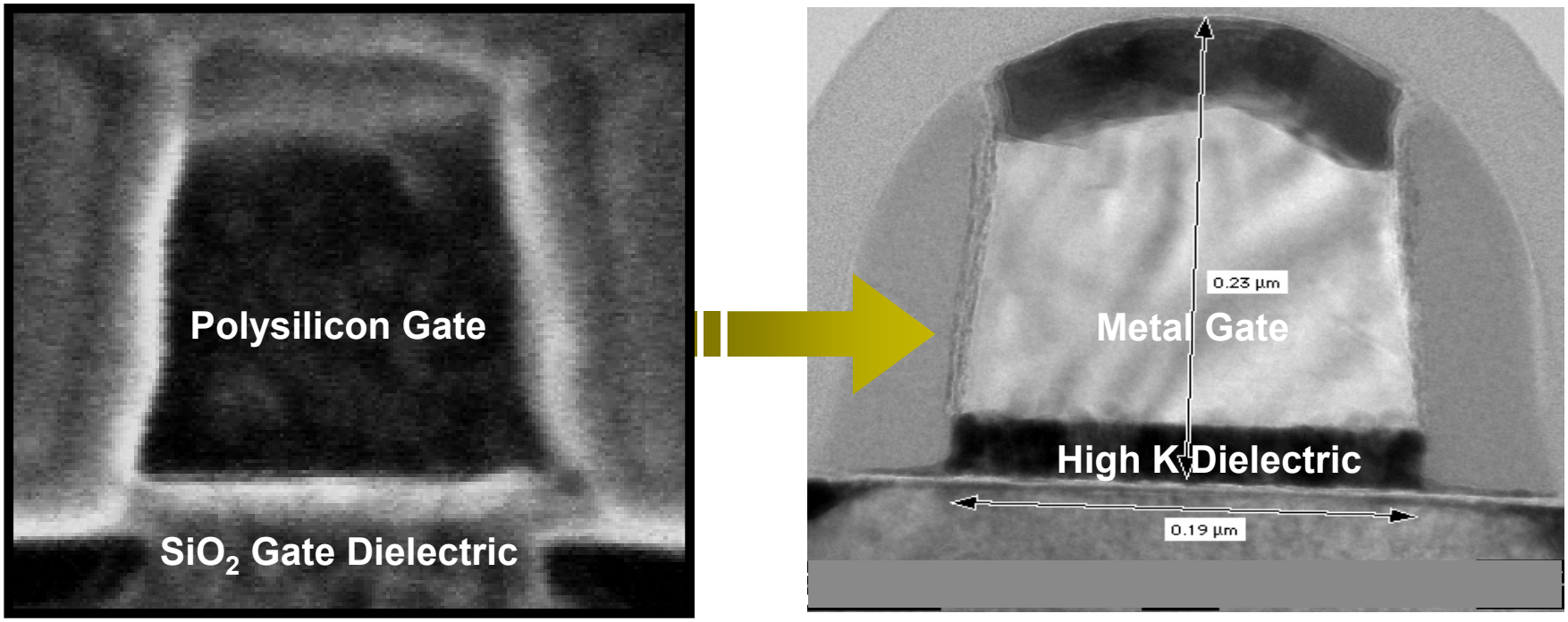
Gate stack replacement



90nm, 65nm

45nm, 32nm

Use a thicker gate oxide with a higher dielectric constant to reduce leakage.

Metal gate avoids charge depletion at metal/oxide interface.

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