

Silicon Motion, Inc.

SM501 MSOC™ Design Guide

Preliminary

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Silicon Motion®, Inc.

SM501 MSOC™ Design Guide

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1 Introduction

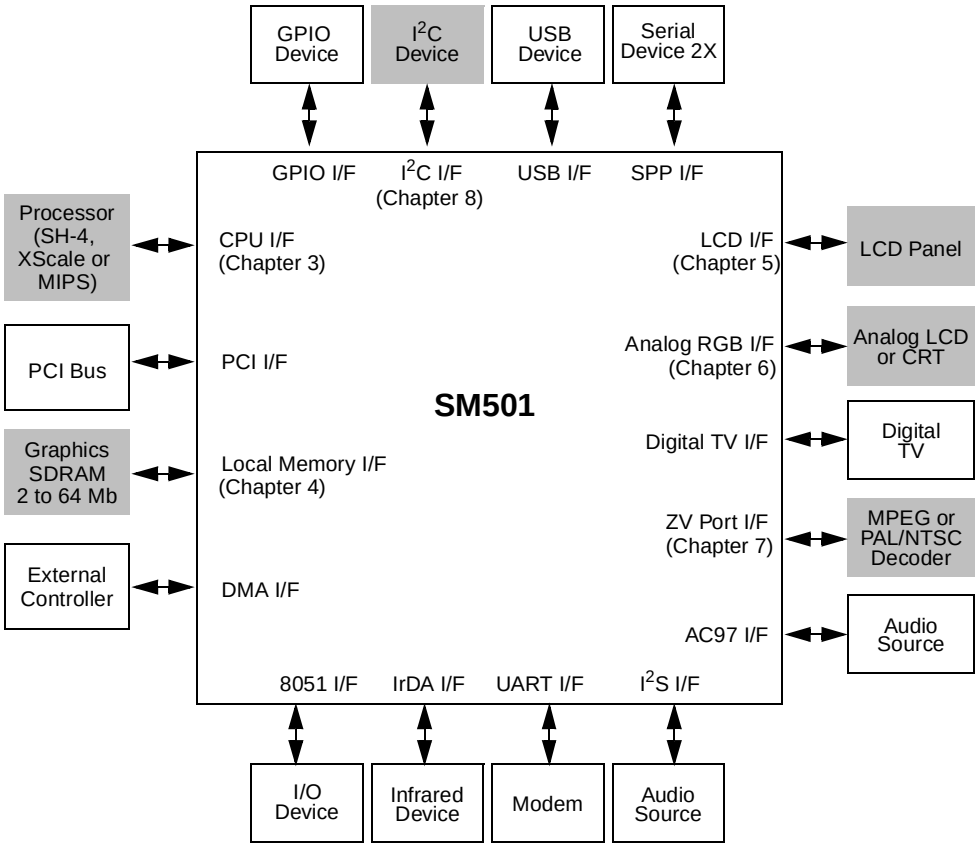
The SM501 is a **M**obile **S**ystem-**o**n-a-**C**hip (MSOC™) device, packaged in a 297-pin BGA. This robust device delivers high-performance video and 2D operation, providing a solution for embedded markets. The SM501 also contains a wide variety of I/Os, such as analog RGB and digital LCD Panel interfaces, an 8-bit parallel interface, USB, UART, IrDA, Zoom Video, AC97 or I^2S, SSP, PWM, and I^2C interfaces. These built-in functionalities help to reduce overall system cost. Additional programmable GPIO bits can be used to interface to external devices as well.

About This Guide

The SM501 Design Guide presents information useful to hardware and system designers who are designing systems using the SM501. It is intended to be used in conjunction with additional documents from Silicon Motion and other IC manufacturers (see "Related Documentation" below for more information about supporting documents).

This guide is organized by external SM501 interfaces. Figure 1-1 shows a block diagram of the SM501 interfaces and the typical external device to which each is connected. The shaded boxes are covered in this document. For design support information on the unshaded boxes, contact Silicon Motion technical support.

Figure 1-1: System Block Diagram



This document contains the following chapters:

- "Signal Descriptions"

  This chapter provides high-level information on the SM501 signals and 297-pin BGA package.

- "CPU Interface"

  This chapter describes the interconnection of the SM501 to various host processors.

- "Local Memory Interface"

  This chapter describes the SM501 local memory interface and how it connects to select memory devices.

- "LCD Interface"

  This chapter describes the SM501 LCD interface, which can drive active and passive LCD panels.

- "Analog RGB Interface"

  This chapter describes the signals and interconnects of the Analog RGB interface, which can drive an external CRT display.

- "ZV Port"

  This chapter describes the signals and interconnects of the Zoom Video Port, which interfaces to most video decoders.

- "I^2C Interface"

  This chapter describes the signals and interconnects of the I^2C interface.

- "Power and Clocking"

  This chapter provides useful information on the power modes and clocks.

Note: This design guide applies to production silicon Rev. AA. For information about specific differences between production silicon and earlier releases, contact Silicon Motion.

Related Documentation

This section is provided to help users locate the necessary documents. Always contact the vendor for the latest versions of these documents and for additional support documentation.

- Silicon Motion, Inc. (SM501 MSOC Device)
  - *SM501 MSOC Databook*, March 2003
    This databook is intended for system designers, software engineers, and hardware designers. It contains detailed information about the SM501's internal registers, special-function modules such as the drawing engine and pulse-width modulator, pin and packaging information, timing diagrams and parameters, and other specifications.
  - *SM501 PCI Demo Board User's Guide*, March 2003
    This user's guide is intended for system designers and software engineers. It describes a board-level design, implementing the SM501 MSOC device. This document describes how to install and configure the demo board. It also provides detailed information on the hardware design, including jumper settings and connector pinouts.
  - *SM501 Programmer's Guide* (to be released Q3 2003)
    The programmer's guide is intended primarily for software engineers who are developing device drivers and other lower-level software. It contains sample code and other information needed by software engineers.
- Renesas Technology (SH-4 Processor)
  - *SH7751 CPU Board HS7751STC01H User's Manual*, Rev. 1.0
  - *SH7751 Series SuperH RISC Engine Hardware Manual*, Rev. 3.0

  Renesas documents are available on-line at: http://www.renesas.com/eng/products/mpumcu/32bit/sh/
- Intel Corporation (XScale Processor)
  - *Intel PXA250 and PXA210 Application Processors Developer's Manual*, February 2002
  - *Intel PXA250 and PXA210 Applications Processors Design Guide*, February 2002
  - *Intel PXA250 and PXA210 Applications Processors Electrical, Mechanical, and Thermal Specification Data Sheet*, February 2002
  - *Intel PXA255 Processor Developer's Manual*, March 2003
  - *Intel PXA255 Processor Design Guide*, March 2003
  - *Intel PXA255 Processor Electrical, Mechanical, and Thermal Specification Data Sheet*, March 2003

  Intel documents are available on-line at http://www.intel.com
- Philips Semiconductors (I^2C Interface)
  - *I^2C Bus Specification*, Version 2.1

  Philips Semiconductors documents are available on-line at http://www.semiconductors.philips.com

2 Signal Descriptions

This chapter provides high-level signal and packaging information for the SM501. Included are a logic diagram illustrating the signals within the SM501 interface, the pinout of the 297-pin Ball Grid Array (BGA) package, and the BGA package mechanical drawing. This chapter also provides a ball to signal listing, which associates all multiplexed pin names with each BGA ball. Detailed descriptions of the signals for the interfaces discussed in this document are found in subsequent chapters.

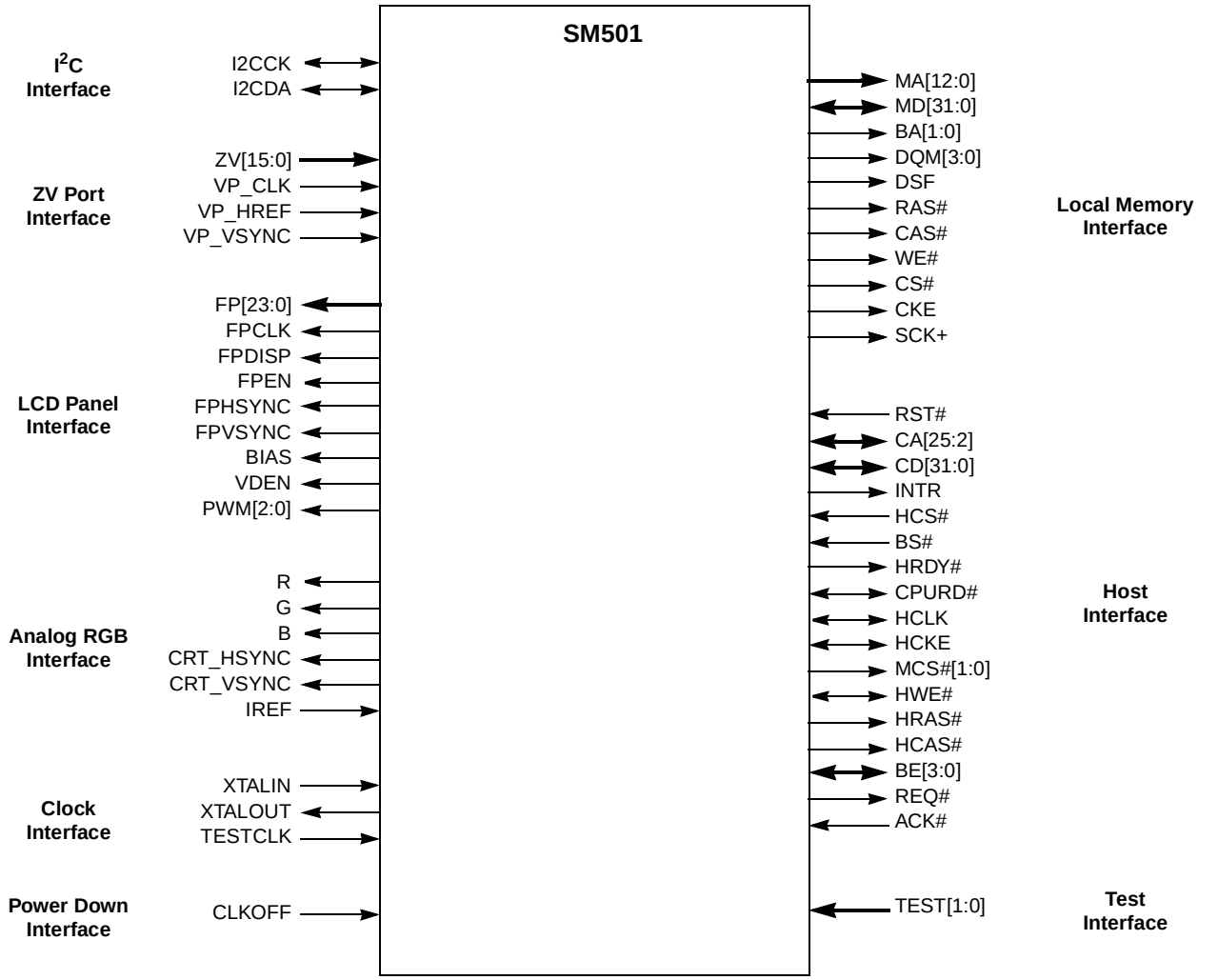
This chapter contains the following sections:

- "SM501 MSOC Logic Diagram"
- "SM501 297-pin BGA Pinout"
- "Numerical BGA Ball List"
- "Packaging"

SM501 MSOC Logic Diagram

Figure 2-1 shows the logic diagram for the SM501 MSOC device. Note that the logic diagram only shows interfaces that are discussed in this document.

Figure 2-1: SM501 MSOC Logic Diagram



SM501 297-pin BGA Pinout

Figure 2-2 shows the pinout of the 297-pin BGA package.

Figure 2-2: Pinout for the SM501

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A	CA5	CA10	CD4	CD1	CD5	CD8	CD12	CA18	CA24	CA19	CD17	CD21	CD23	CD25	CD31	HCLK	BE3	HCKE	CPURD#	BS#	HCAS#
B	CA4	CA9	CA14	CD6	CD3	CD7	CD10	CD14	CA21	CD16	CD20	CD19	CA20	CD27	CD29	BREQ#	BE2	MCS1#	HRDY#	HRAS#	HWE#
C	CA3	CA8	CA13	CD2	CD9	CD13	CA16	CA22	CA25	CD18	CD22	CD24	CD26	CD30	ACK#	RST#	BE1	MCS0#	HCS#	CLK OFF	XTAL IN
D	CA2	CA7	CA12	MVDD2	CA17	CD11	CD15	VDD	CA23	HVDD	CA15	HVDD	CD28	VDD	INTR	HVDD	BE0	HVDD	PLL GND	TEST CLK	XTAL OUT
E	MD0	CA6	CA11	CD0														GPIO 0	GPIO 1	GPIO 2	PLL PWR
F	MD1	MD2	MD3	MVDD														VDD	GPIO 3	GPIO 4	GPIO 5
G	MD4	MD5	MD6	MD7														GPIO 6	GPIO 7	GPIO 8	GPIO 9
H	MD15	MD14	MD13	MVDD														XTAL PWR	GPIO 10	GPIO 11	GPIO 12
J	MD12	MD11	MD10	MD9					MVDD2	GND	GND	GND	VDD					GPIO 13	GPIO 14	GPIO 15	GPIO 16
K	DQM0	DQM1	MD8	MVREF					GND	GND	GND	GND	GND					GVDD	GPIO 17	GPIO 18	GPIO 19
L	WE#	CAS#	RAS#	CS#					GND	GND	GND	GND	GND					GPIO 20	GPIO 21	GPIO 22	GPIO 23
M	BA1	BA0	MA0	MVDD					GND	GND	GND	GND	GND					VDD	GPIO 24	GPIO 25	GPIO 26
N	MA1	MA2	MA3	MA4					MVDD2	GND	GND	GND	VDD					GPIO 27	GPIO 28	GPIO 29	GPIO 30
P	MA5	MA6	MA7	MVDD														GVDD	GPIO 31	GPIO 32	GPIO 33
R	SCK+	MA12	DSF	MA11														GPIO 34	GPIO 35	GPIO 36	GPIO 37
T	SCK-	MA10	MA9	MVDD														GVDD	GPIO 38	GPIO 39	GPIO 40
U	MA8	CKE	DQM2	DQM3														GPIO 41	GPIO 42	GPIO 43	GPIO 44
V	DQS	MD24	MD25	MVDD2	FP3	PVDD	FP12	PVDD	FP21	VDD	FPEN	PVDD	BIAS	AVDD	TEST 0	AVSS	GPIO 45	VDD	GPIO 46	GPIO 47	GPIO 48
W	MD26	MD27	MD28	MD29	FP2	FP6	FP11	FP15	FP20	FP23	FP_VSYNC	VDEN	CRT_HSYNC	CRT_VSYNC	TEST 1	GPIO 49	GPIO 50	GPIO 51	GPIO 52	GPIO 53	GPIO 54
Y	MD30	MD31	MD23	MD22	MD21	FP5	FP10	FP14	FP19	FP22	FP_HSYNC	FP_DISP	R	USB GND	USB PWR	GPIO 55	GPIO 56	GPIO 57	GPIO 58	GPIO 59	GPIO 60
AA	MD20	MD19	MD18	MD17	MD16	FP4	FP7	FP13	FP18	FPCLK	IREF	B	G	USB-	USB+	VP_VSYNC	VP_HREF	VP_CLK	GPIO 61	GPIO 62	GPIO 63

Numerical BGA Ball List

Table 2-1 lists the signal names associated with each package ball in numerical order. Note that some pins have multiple functionalities depending on the operating mode.

Table 2-1: Numerical Pin Designations

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
A1	CA5	B1	CA4	C1	CA3
A2	CA10	B2	CA9	C2	CA8
A3	CD4, PCI_AD4	B3	CA14, PCI_CLKRUN#	C3	CA13
A4	CD1, PCI_AD1	B4	CD6, PCI_AD6	C4	CD2, PCI_AD2
A5	CD5, PCI_AD5	B5	CD3, PCI_AD3	C5	CD9, PCI_AD9
A6	CD8, PCI_AD8	B6	CD7, PCI_AD7	C6	CD13, PCI_AD13
A7	CD12, PCI_AD12	B7	CD10, PCI_AD10	C7	CA16, PCI_PAR
A8	CA18, PCI_C/BE1#	B8	CD14, PCI_AD14	C8	CA22, PCI_STOP#
A9	CA24, PCI_IRDY#	B9	CA21, PCI_DEVSEL#	C9	CA25, PCI_FRAME#
A10	CA19, PCI_C/BE2#	B10	CD16, PCI_AD16	C10	CD18, PCI_AD18
A11	CD17, PCI_AD17	B11	CD20, PCI_AD20	C11	CD22, PCI_AD22
A12	CD21, PCI_AD21	B12	CD19, PCI_AD19	C12	CD24, PCI_AD24
A13	CD23, PCI_AD23	B13	CA20, PCI_C/BE3#	C13	CD26, PCI_AD26
A14	CD25, PCI_AD25	B14	CD27, PCI_AD27	C14	CD30, PCI_AD30
A15	CD31, PCI_AD31	B15	CD29, PCI_AD29	C15	ACK#, PCI_GNT#
A16	HCLK, PCI_CLK	B16	BREQ#, PCI_REQ#	C16	RST#, PCI_RST#
A17	BE3, DQM3	B17	BE2, DQM2	C17	BE1, DQM1
A18	HCKE	B18	MCS1#	C18	MCS0#
A19	CPURD#	B19	HRDY#	C19	HCS#
A20	BS#	B20	HRAS#	C20	CLKOFF
A21	HCAS#	B21	HWE#	C21	XTALIN

Table 2-1: Numerical Pin Designations (Continued)

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
D1	CA2	E18	GPIO0, 8051_AD0	H19	GPIO10, 8051_ALE#
D2	CA7	E19	GPIO1, 8051_AD1	H20	GPIO11, 8051_WAIT#
D3	CA12	E20	GPIO2, 8051_AD2	H21	GPIO12, 8051_A8
D4	MVDD2	E21	PLLPWR	J1	MD12
D5	CA17, PCI_C/BE0#	F1	MD1	J2	MD11
D6	CD11, PCI_AD11	F2	MD2	J3	MD10
D7	CD15, PCI_AD15	F3	MD3	J4	MD9
D8	VDD	F4	MVDD	J9	MVDD2
D9	CA23, PCI_TRDY#	F18	VDD	J10	GND
D10	HVDD	F19	GPIO3, 8051_AD3	J11	GND
D11	CA15, PCI_IDSEL	F20	GPIO4, 8051_AD4	J12	GND
D12	HVDD	F21	GPIO5, 8051_AD5	J13	VDD
D13	CD28, PCI_AD28	G1	MD4	J18	GPIO13, 8051_A9
D14	VDD	G2	MD5	J19	GPIO14, 8051_A10
D15	INTR, PCI_INTA#	G3	MD6	J20	GPIO15, 8051_A11
D16	HVDD	G4	MD7	J21	GPIO16, ZV0, TEST0
D17	BE0, DQM0	G18	GPIO6, 8051_AD6	K1	DQM0
D18	HVDD	G19	GPIO7, 8051_AD7	K2	DQM1
D19	PLLGND	G20	GPIO8, 8051_RD#	K3	MD8
D20	TESTCLK	G21	GPIO9, 8051_WR#	K4	MVREF
D21	XTALOUT	H1	MD15	K9	GND
E1	MD0	H2	MD14	K10	GND
E2	CA6	H3	MD13	K11	GND
E3	CA11	H4	MVDD	K12	GND
E4	CD0, PCI_AD0	H18	XTALPWR	K13	GND

Table 2-1: Numerical Pin Designations (Continued)

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
K18	GVDD	M18	VDD	R2	MA12
K19	GPIO17, ZV1, TEST1	M19	GPIO24, AC97_RST#	R3	DSF
K20	GPIO18, ZV2, TEST2	M20	GPIO25, AC97_SYNC, I2S_WS	R4	MA11
K21	GPIO19, ZV3, TEST3	M21	GPIO26, AC97_BITCLK, IS2_BITCLK	R18	GPIO34, SSP0_FRMOUT
L1	WE#	N1	MA1	R19	GPIO35, SSP0_FRMIN
L2	CAS#	N2	MA2	R20	GPIO36, SSP0_CLK
L3	RAS#	N3	MA3	R21	GPIO37, UART0_TXD, IrDA0_TXD
L4	CS#	N4	MA4	T1	SCK-
L9	GND	N9	MVDD2	T2	MA10
L10	GND	N10	GND	T3	MA9
L11	GND	N11	GND	T4	MVDD
L12	GND	N12	GND	T18	GVDD
L13	GND	N13	VDD	T19	GPIO38, UART0_RXD, IrDA0_RXD
L18	GPIO20, ZV4, TEST4	N18	GPIO27, AC97_SDOUT, I2S_SOUT	T20	GPIO39, UART0_CTS
L19	GPIO21, ZV5, TEST5	N19	GPIO28, AC97_SDIN, I2S_SDIN	T21	GPIO40, UART0_RTS
L20	GPIO22, ZV6, TEST6	N20	GPIO29, PWM0, TEST8	U1	MA8
L21	GPIO23, ZV7, TEST7	N21	GPIO30, PWM1, TEST9	U2	CKE
M1	BA1	P1	MA5	U3	DQM2
M2	BA0	P2	MA6	U4	DQM3
M3	MA0	P3	MA7	U18	GPIO41, SSP1_TXD, UART1_TXD, IrDA1_TXD
M4	MVDD	P4	MVDD	U19	GPIO42, SSP1_RXD, UART1_RXD, IrDA1_RXD
M9	GND	P18	GVDD	U20	GPIO43, SSP1_FRMIN, UART1_CTS
M10	GND	P19	GPIO31, PWM2, TEST10	U21	GPIO44, SSP1_FRMOUT, UART1_RTS
M11	GND	P20	GPIO32, SSP0_TXD	V1	DQS
M12	GND	P21	GPIO33, SSP0_RXD	V2	MD24
M13	GND	R1	SCK+	V3	MD25

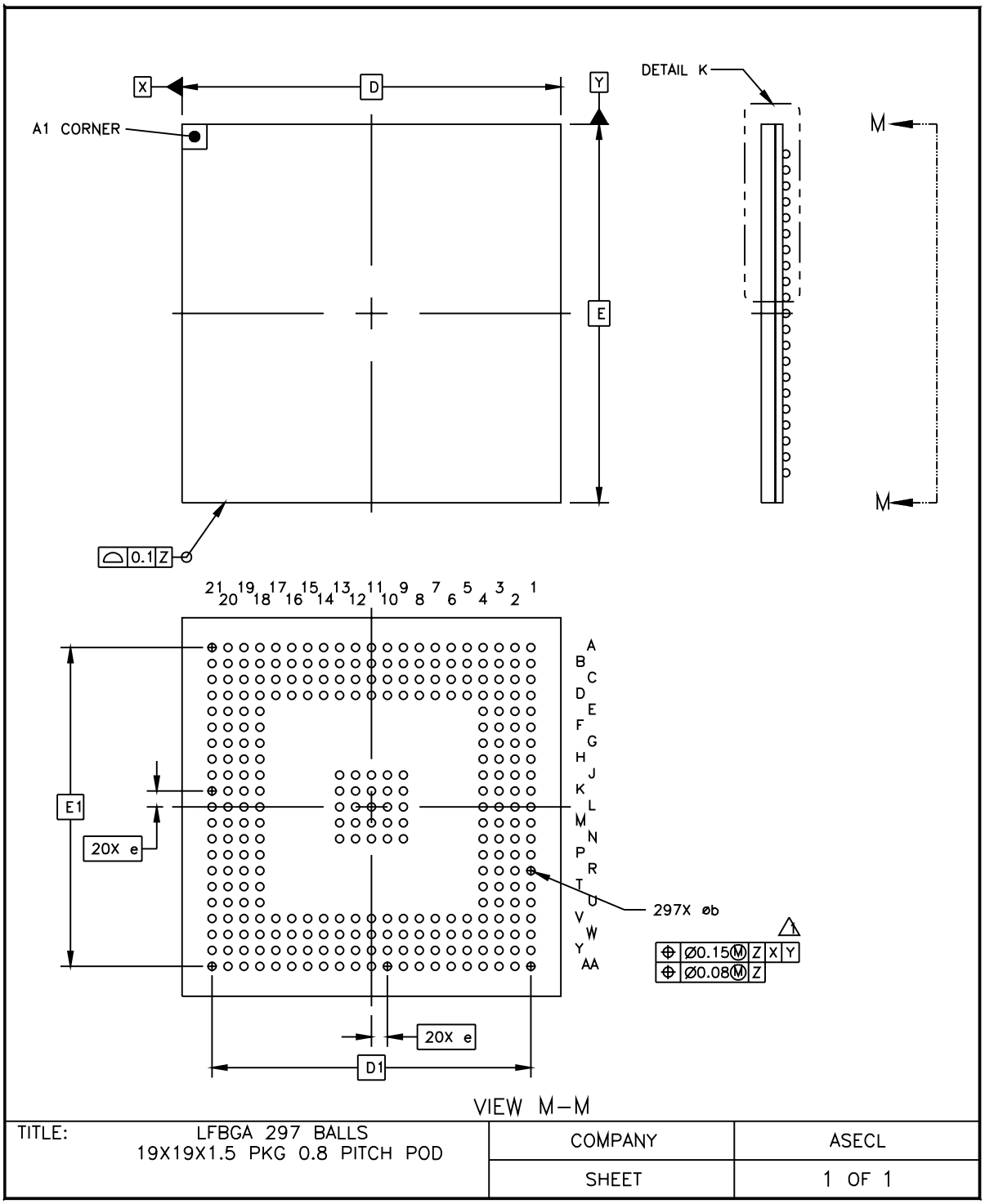
Table 2-1: Numerical Pin Designations (Continued)

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
V4	MVDD2	W10	FP23	Y16	GPIO55, TEST11, DCRTCLK
V5	FP3	W11	FPVSYNC	Y17	GPIO56, DCRTD0, TEST12, ZV8, FP0
V6	PVDD	W12	VDEN	Y18	GPIO57, DCRTD1, TEST13, ZV9, FP1
V7	FP12	W13	CRT_HSYNC	Y19	GPIO58, DCRTD2, TEST14, ZV10, FP8
V8	PVDD	W14	CRT_VSYNC	Y20	GPIO59, DCRTD3, TEST15, ZV11, FP9
V9	FP21	W15	TEST1	Y21	GPIO60, DCRTD4, TEST16, ZV12, FP16
V10	VDD	W16	GPIO49, 8051_P1[1]	AA1	MD20
V11	FPEN	W17	GPIO50, 8051_P1[2]	AA2	MD19
V12	PVDD	W18	GPIO51, 8051_P1[3]	AA3	MD18
V13	BIAS	W19	GPIO52, 8051_P1[4]	AA4	MD17
V14	AVDD	W20	GPIO53, 8051_P1[5]	AA5	MD16
V15	TEST0	W21	GPIO54, 8051_INTR#	AA6	FP4
V16	AVSS	Y1	MD30	AA7	FP7
V17	GPIO45, SSP1_CLK	Y2	MD31	AA8	FP13
V18	VDD	Y3	MD23	AA9	FP18
V19	GPIO46, I2CCK	Y4	MD22	AA10	FPCLK
V20	GPIO47, I2CDA	Y5	MD21	AA11	IREF
V21	GPIO48, 8051_P1[0]	Y6	FP5	AA12	B
W1	MD26	Y7	FP10	AA13	G
W2	MD27	Y8	FP14	AA14	USB-
W3	MD28	Y9	FP19	AA15	USB+
W4	MD29	Y10	FP22	AA16	VP_VSYNC
W5	FP2	Y11	FPHSYNC	AA17	VP_HREF
W6	FP6	Y12	FPDISP	AA18	VP_CLK
W7	FP11	Y13	R	AA19	GPIO61, DCRTD5, TEST17, ZV13, FP17
W8	FP15	Y14	USBGND	AA20	GPIO62, DCRTD6, TEST18, ZV14
W9	FP20	Y15	USBPWR	AA21	GPIO63, DCRTD7, TEST19, ZV15

Packaging

The SM501 MSOC device is packaged in a 297-pin BGA using 0.8mm ball spacing (see Figure 2-3). The total package size is 19x19mm.

Figure 2-3: SM501 297-pin BGA Package Outline



3 CPU Interface

This chapter describes the SM501 CPU Interface, which supports several Host processors. For systems with an Intel XScale, Renesas SH-4, or NEC MIPS V_R4122/4131 CPU, the SM501 connects through a 32-bit SRAM-like memory interface to the CPU. The SM501 CPU interface also can attach directly to the PCI bus.

This chapter contains the following sections:

- "Overview"
- "Interfacing to Renesas SH-4 Processors"
- "Interfacing to Intel XScale Processors"
- "Interfacing to NEC MIPS Processors"

Overview

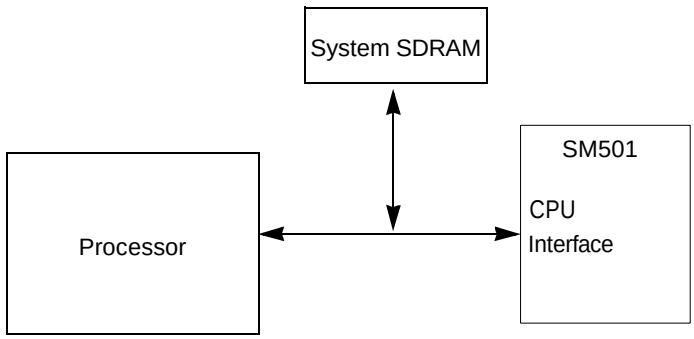
The SM501 supports two mutually exclusive modes of interfacing to the host CPU. The first option is to configure the SM501 as a memory-mapped device connected to the host memory interface (see Figure 3-1). In this configuration, the SM501 supports a 32-bit data bus. With a typical Intel XScale processor interface, this configuration has a peak bandwidth of 400 MB/s. Table 3-1 shows the processors currently supported.

Table 3-1: Processors Supported by the SM501

Manufacturer	Models	Generic Term	See Page:
Renesas	SH770X and SH775X	SH-4	3-4
Intel	PXA250 and PXA255	XScale	3-11
NEC	VR4122 and VR4131	MIPS	3-22

The second option is to configure the SM501 as a PCI device. In this mode, the SM501 supports PCI-1X and 2X for a maximum bus throughput of 250 MB/s. Contact Silicon Motion technical support for information on interfacing to the PCI bus.

Figure 3-1: Memory-Mapped System Architecture



Configuring the SM501

At the rising edge of the Reset signal, the SM501 reads the values of GPIO pins to determine its configuration. External pull-up or pull-down resistors are used to set the values of the pins. The pull-up or pull-down resistors should not affect the GPIO lines when they are used for other purposes. However, the system design should ensure that these GPIO lines are not driven during the SM501 reset period to avoid erroneous configuration settings.

Processor Type

GPIO[2:0] select the type of processor to which the SM501 is connected as shown in Table 3-2. See the sections on the individual processors later in this chapter for circuit diagrams showing external and internal resistor values.

Table 3-2: SM501 Host Interface Bus, Configuration

GPIO Pin			Host Bus Function
2	**1**	**0**	
X	X	1	PCI Interface
0	**0**	**0**	**SH-4 (default)**
0	1	0	XScale
1	0	0	Unassigned
1	1	0	MIPS

Other System Parameters

GPIO[7:3] and GPIO[15:12] are read at power-on to configure other system parameters as shown in Table 3-3.

Table 3-3: GPIO Configuration Pins

Pin	Description	Design Notes
GPIO3	Clock select: 0: Internal PLL. 1: External test clock.	The clock source is an internal PLL driven from 12/24 MHz crystal, so this pin should be set to 0. To prevent input float, pull the test clock input down with a 100K resistor.
GPIO4	Ready polarity control: 0: Active low. 1: Active high.	For SH-4 only.
GPIO[6:5]	Local memory column size: 0x: 256 words. 10: 512 words. 11: 1024 words.	
GPIO7	Clock divider reset control: 0: Do not reset clock divider. 1: Reset clock divider.	This parameter is used for test purposes only.
GPIO12	Chip select pins: 0: Drive MCS# pins. 1: Do not drive MCS# pins	See “Local Memory” on page 3-17 for more details about local memory and the use of the MCS# pins.

Table 3-3: GPIO Configuration Pins (Continued)

Pin	Description	Design Notes
GPIO [15:13]	Local memory size select: 000: 4MB. 001: 8MB. 010: 16MB. 011: 32MB. 100: 64MB. 101: 2MB.	

Interface Signal Summary

Table 3-4 summarizes the signals in the SM501 host interface. More detailed descriptions of each signal and connection information are provided in the processor-specific sections later in this chapter.

Table 3-4: Host Interface Signal Summary

Symbol	I/O	Active	Function
RST#	In	Low	Resets the SM501.
CA[25:2]	In/Out	--	Bidirectional address bus.
CD[31:0]	In/Out	--	Bidirectional data bus.
INTR	Out	PD[1]	Request interrupt service from processor.
HCS#	In	Low	Host chip select to enable the SM501.
BS#	In	PD	Pin function depends on processor type and system design.
HRDY#	Out	Low	Host bus ready.
CPURD#	In/Out	PD	Pin function depends on processor type and system design.
HCLK	In/Out	--	Host clock input, drives clock lines as output for bus master mode.
HCKE	In/Out[2]	--	Host clock enable.
MCS#[1:0]	Out	Low	The SM501 selects the SDRAM memory chip.
HWE#	In/Out	Low	Host write enable.
HRAS#	Out	Low	Host RAS.
HCAS#	Out	Low	Host CAS.
BE[3:0]	In/Out	Low	Byte enable.
REQ#	Out	PD	Bus request.
ACK#	In	PD	Bus acknowledge.

1. PD = Processor dependent. See the processor-specific sections below.
2. Output when bus master in MIPS systems.

Interfacing to Renesas SH-4 Processors

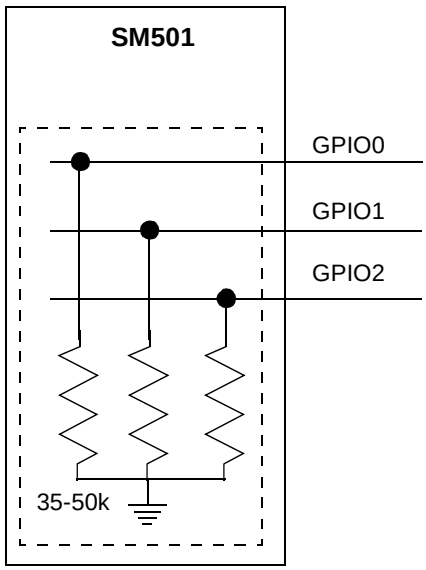
This section provides information for interfacing the SM501 to the Renesas SH-3 (SH770X) and SH-4 (SH775x) processors. It covers these topics:

- Configuration
- Hardware Connections
- Host Interface Signals
- Memory Map and Chip Select
- Other Design Considerations

Configuration

The SM501 has internal resistors that pull GPIO[2:0] Low. If no external resistors are installed on these lines, the SM501 defaults to the SH-4 configuration as shown in Figure 3-2.

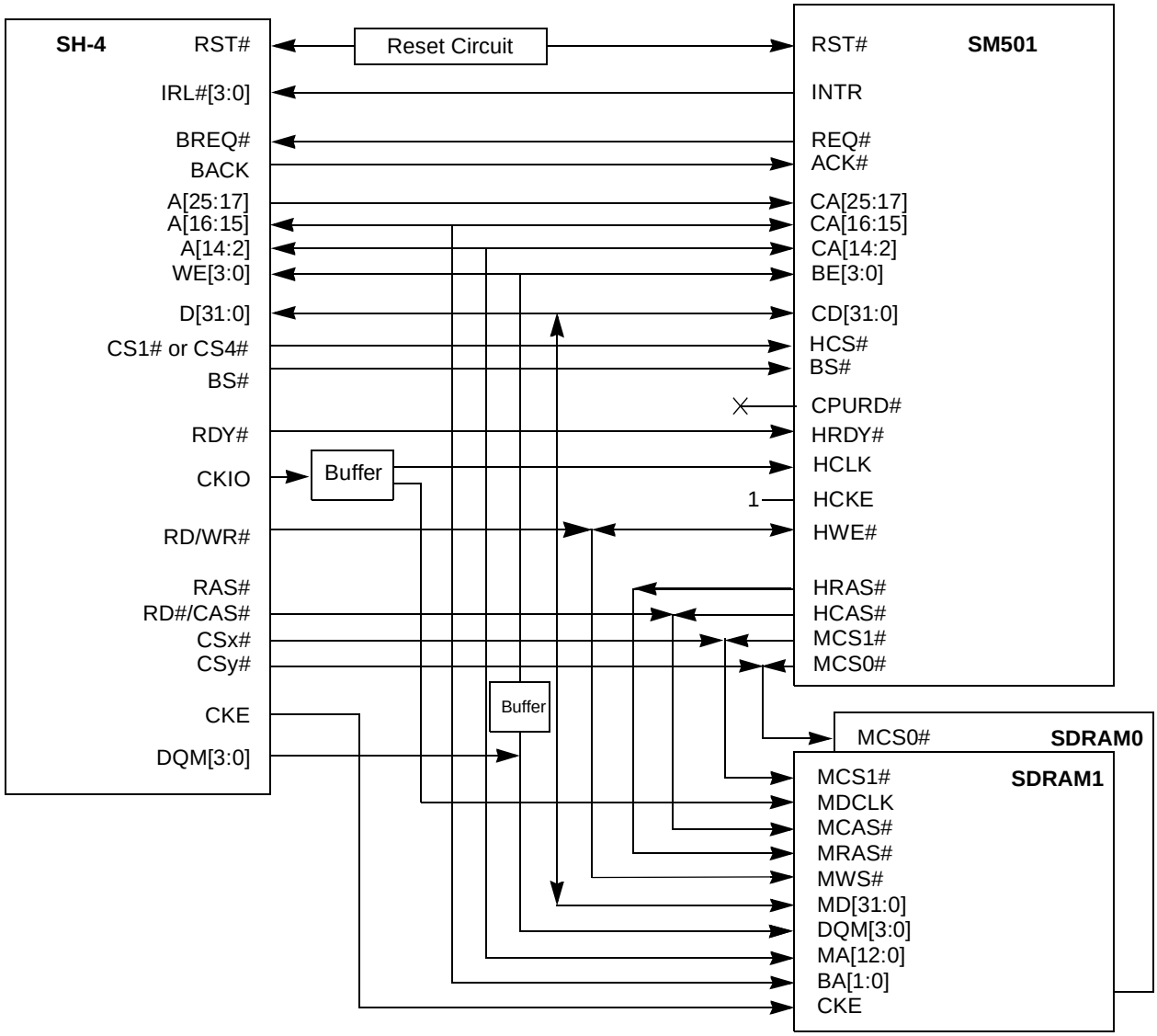
Figure 3-2: Configuring the SM501 for the SH-4 Processor



Hardware Connections

Figure 3-3 shows typical SM501 host interface connections for a system using the SH-4 processor and SDRAM. For a typical clock buffer circuit, see Figure 3-4. For a typical buffer circuit for the DQM lines, see Figure 3-7.

Figure 3-3: SM501 Connections to SH-4 Processor and SDRAM



Host Interface Signals

Table 3-5: CPU Interface Signal Descriptions for SH-4 Interface

SM501 Pin	Connects to:		SH-4 Pin Type	Design Notes
	SDRAM	SH-4		
CD[31:0]	MD[31:0]	D[31:0]	I/O	SH-4 data pins connect to both memory and the SM501.
CA[14:2]	MA[12:0]	A[14:2]	OZ	SH-4 register BCR1[15] must be set to 0 to allow the address lines to go high impedance when the SM501 is bus master.
CA[16:15]	BA[1:0]	A[16:15]	O	Bank address driven by the SM501 in master mode or SH-4 in slave mode.
CA[25:17]	NC	MA[25:17]	O	These lines are not connected to the SDRAM and are not used in master mode.
BE[3:0]	CAS/ DQM[3:0]	WE[3:0]	O	Byte enable: In slave mode, the SM501 uses BE to decode the lower two bits of the address. In master mode, the SM501 drives DQM lines. These signals should be isolated externally in the two modes as shown in Figure 3-7.
RST#	NC	RESET#	OC	This signal is not only a copy of the CPU reset signal, but is also asserted for soft reset events such as sleep and watchdog reset. If the SM501 does not use soft resets, then RST# should be connected directly to the SH-4 signal RESET#.
HCLK		CKIO (buffered)	O	See “Bus Clock” on page 3-8 for more information on
HCKE	NC	NC		This signal should be pulled high on the SM501 board to enable the clock.
HCS#	NC	CS4# or CS1#	O	In slave mode, the SM501 HCS# signal must be driven by SH-4. Use either CS1# or CS4#. See “Memory Map and Chip Select” on page 3-7 for more information.
HBS#	NC	BS#	O	Used only in slave mode.
HRDY#	NC	RDY	I	Used only in slave mode.
REQ#	NC	BREQ#	I	The SM501 asserts this signal to request bus ownership.
ACK#	NC	BACK#	O	The SH-4 asserts this signal to grant bus ownership.
INTR	NC	IRL[3:0] # or GPIO pin	O	See “Interrupts” on page 3-10 for more information about using interrupts in SH-4 systems.
CPURD#	NC	OE#	O	Not used with the SH-4.

Table 3-5: CPU Interface Signal Descriptions for SH-4 Interface (Continued)

SM501 Pin	Connects to:		SH-4 Pin Type	Design Notes
	SDRAM	SH-4		
HWE#	MWS#	RD/WR#	OCZ	Write enable: In slave mode, the SM501 uses this signal to determine data direction (read or write). In master mode, the SM501 must drive the SDRAM MWS# signals, so these signals must be isolated externally. SH-4 register BCR1[14] must be set to 0 to allow the RD line to go to high impedance when the SM501 is bus master.
MCS0#	MS0#	CS*x*#	O	Selects first SDRAM. *x* is system dependent.
MCS1#	MS1#	CS*y*#	O	Selects second SDRAM. *y* is system dependent.
RAS#	MRAS#	RAS#	OCZ	SH-4 register BCR1[14] must be set to 0 to 3-state the RAS# and CAS# lines when the SM501 is bus master.
CAS#	MCAS#	RD#/CAS#	OCZ	

Memory Map and Chip Select

The SM501 can support both the 32-bit (SH7751) or 64-bit (SH7750) host bus interface. This document describes the 32-bit interface. For design information related to the 64-bit interface, contact Silicon Motion technical support.

The SH-4 can interface to a number of external memory devices including ROM, burst ROM, DRAM, SDRAM, SRAM and byte-control SRAM. The SM501 supports two operating modes:

- Master: Corresponds to the SH-4 SDRAM mode. The SM501 operates as an SDRAM controller and can control two memory areas of the SH-4 SDRAM.
- Slave: Corresponds to the SH-4 byte-control SRAM mode.

The memory map of the SM501 is divided into a local memory space and a memory-mapped I/O (MMIO) space for the SM501 control registers. The memory space includes the display frame buffer and all other local memory. The size of the SM501 memory space can range from 2MB to 64MB. MMIO is mapped to the top of the memory space with a fixed offset of 0x03E0 0000.

The SH-4 supports a 29-bit external memory space, with seven chip select lines and 26 address lines. The physical memory address and memory-mapped I/O of the SM501 are mapped as shown in Table 3-6.

Table 3-6: SM501 in SH-4 Memory Map

Static Chip Select	CS#	Memory Space	Memory-Mapped I/O Space
1	1	0x0400 0000 – 0x07FF FFFF	0x07E0 0000 - 0x07FF FFFF
4	4	0x1000 0000 – 0x13FF FFFF	0x13E0 0000 – 0x13FF FFFF

The SH-4 manages the memory space as seven independent 64Mbyte areas. The byte-enable SRAM function is only supported in areas 1 and 4, therefore, signal HCS# should be connected to either CS1# or CS4# on the SH-4 if the SM501 is intended to run in slave mode.

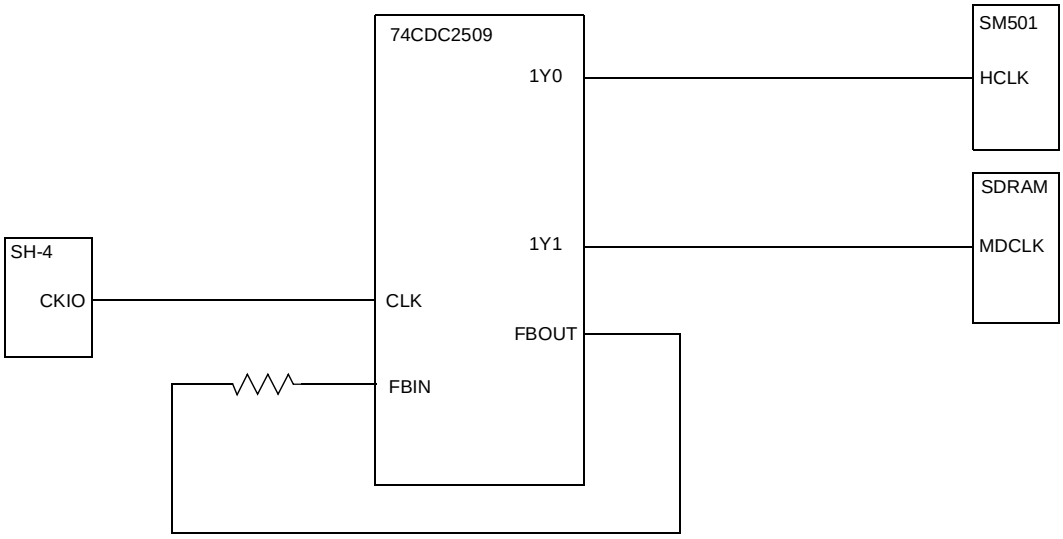
Other Design Considerations

Bus Clock

The SH-4 clock output CKIO drives both the SDRAM and the SM501. This clock output is usually buffered using a circuit similar to Figure 3-4. Due to differences in trace lengths and propagation delay, the clock seen by the SM501 may not be in phase with the SDRAM. This slight phase shift should not cause problems in slave mode.

When the SM501 is the bus master, signal HCLK is an output and can be used to drive the clock input MDCLK of the SDRAM. However, CKIO from the SH-4 is always active, even when the SH-4 relinquishes the bus to the SM501. Therefore, if the SM501 is to function as both slave and master, the design must prevent the SH-4 and the SM501 attempting to drive the MDCLK lines at the same time in master mode.

Figure 3-4: Typical Host Clock Buffering Circuit



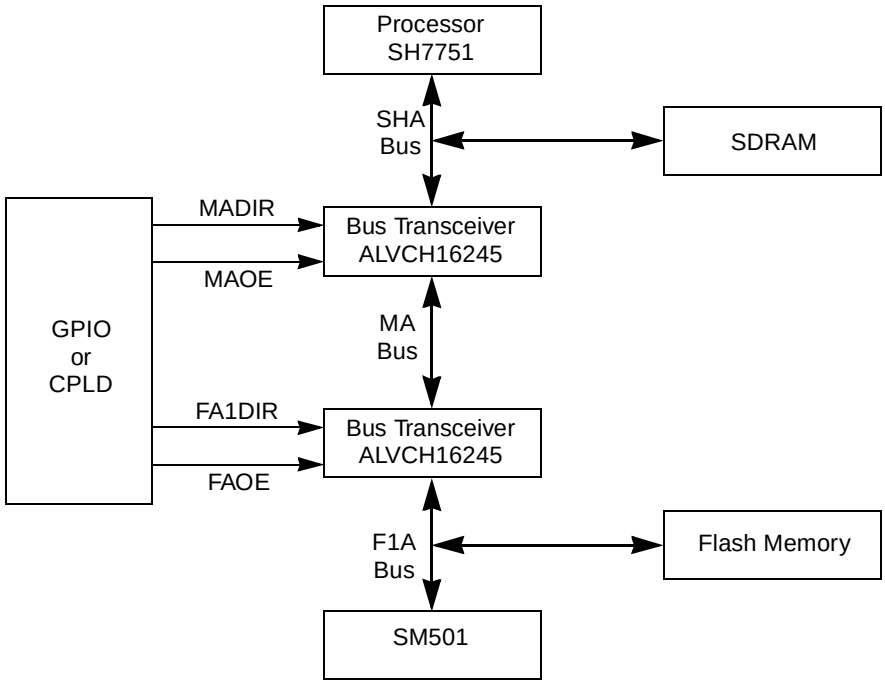
Two possible solutions are:

- Use the SH-4 clock as the bus clock in master mode. The clock phase at the SM501 and SDRAM clock inputs must be adjusted to be in phase.
- Use the SM501 clock as the bus clock in master mode. Switching circuitry must ensure that the SH-4 clock is disconnected from the SDRAM.

Address Buffering

While the address lines of the SH-4 can in principle be directly connected to the SM501, the loading in a typical design make this impractical. A recommended approach is to buffer the address lines as shown in Figure 3-5. The buffer direction and output are controlled so that the address is sent to the SM501 in slave mode, and the SM501 drives the address lines to SDRAM. On the SH-4, control bit 15 must be set to 0 in BCR1 so that the SH-4 3-states the address lines when it releases the bus.

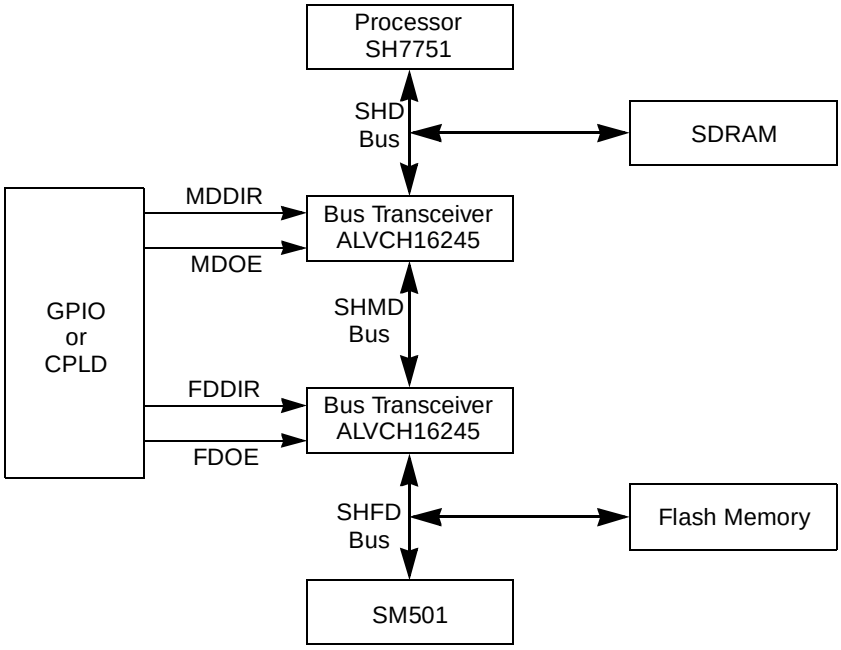
Figure 3-5: Typical Address Buffering Circuit (Based on Hitachi Development Platform)



Data Buffering

Like the address, the data lines of SH-4 may need to be buffered. The data lines can be buffered through two stages of buffers as shown in Figure 3-6. The buffer direction and output are controlled by a CPLD that also controls address directions and output enable.

Figure 3-6: Typical Data Buffering Circuit (Based on Hitachi Development Platform)

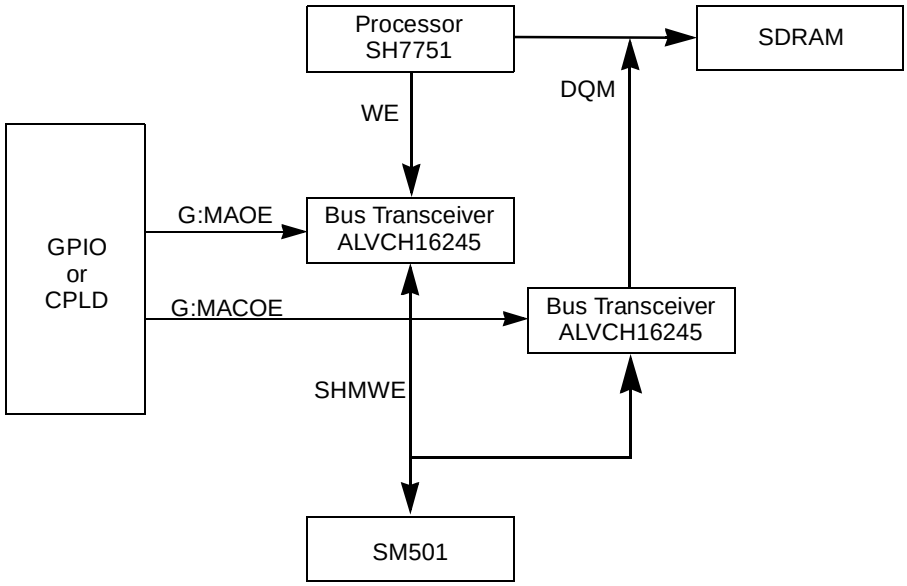


Byte Enable

In slave mode, the address and byte enable signals must arrive at the SM501 at the same time. Therefore, if the address lines are buffered, the byte enable signals must also be buffered. Figure 3-7 shows a typical circuit. Note that the address, data, and byte enable signals should have the same number of buffer levels to ensure correct timing.

Also, bit 14 of SH-4 register BCR[14] must be set to 0 to ensure that DQM#, CAS#, RAS#, and WE# are 3-stated when the SM501 is bus master.

Figure 3-7: Typical Byte Enable Buffering Circuit (Based on Hitachi Development Platform)



Interrupts

The SH-4 has four external interrupt pins, which can function as either a four-level or 16-level interrupt design. For a 4-level design, the SM501 interrupt signal INTR can connect directly to one of the SH-4 interrupt inputs. For a 16-level design, an external circuit is needed to generate the interrupt level for the SH-4.

Interfacing to Intel XScale Processors

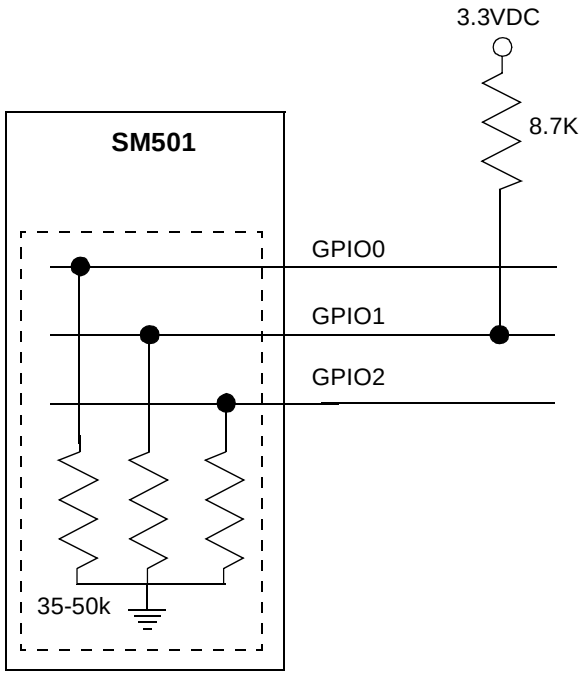
This section provides information for interfacing the SM501 to the Intel XScale processors, PXA250 and PXA255. It covers these topics:

- Configuration
- Hardware Connections
- Host Interface Signals
- Memory Map and Chip Select
- XScale Memory Addressing Modes
- Other Design Considerations

Configuration

Figure 3-8 shows the circuit used to configure the SM501 for the XScale processor. An external resistor is required to pull GPIO1 High.

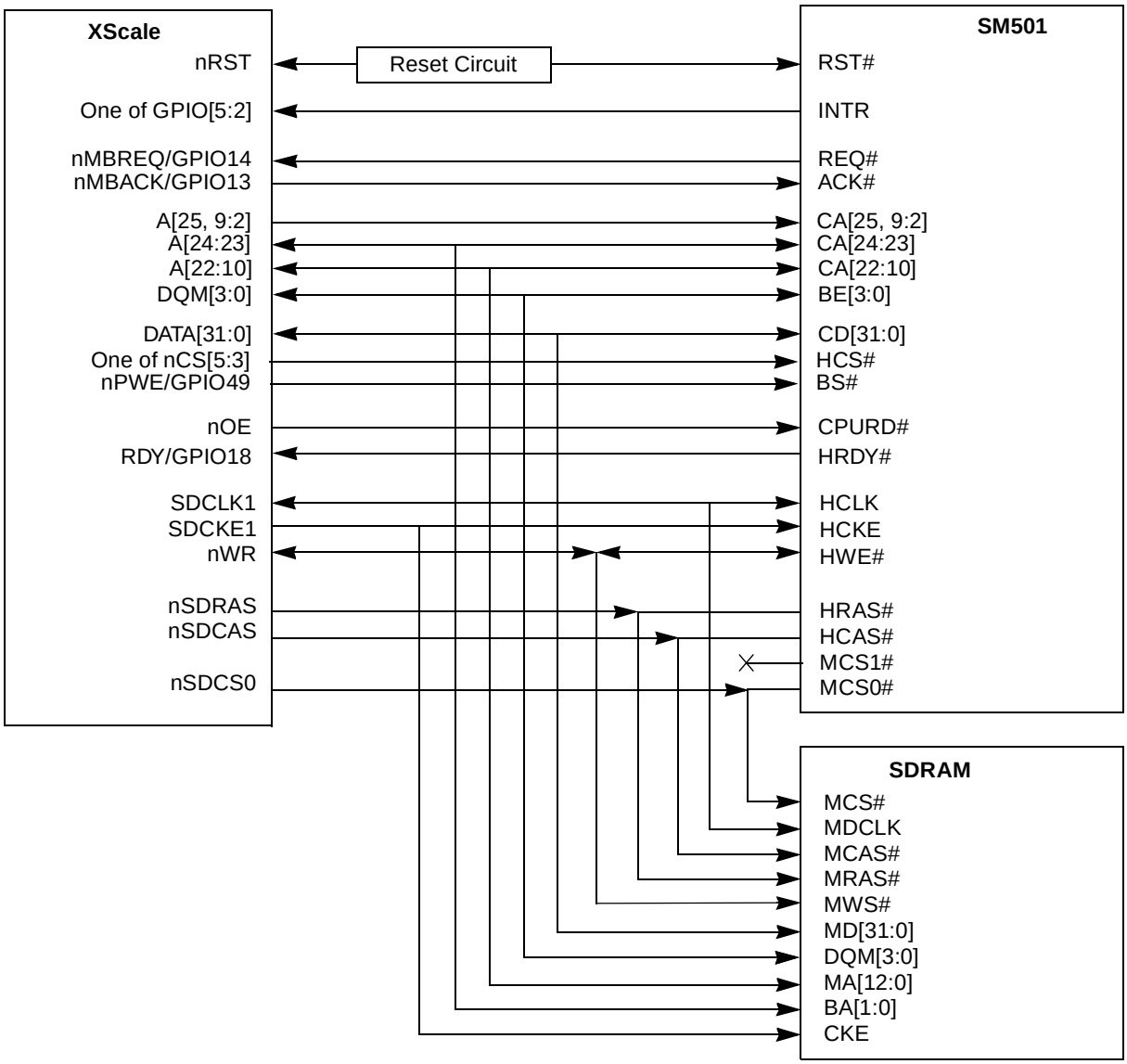
Figure 3-8: Configuring the SM501 for the XScale Processor



Hardware Connections

Figure 3-9 shows typical SM501 host interface connections for a system using the XScale processor and SDRAM in normal addressing mode.

Figure 3-9: SM501 Connections to XScale Processor and SDRAM



Host Interface Signals

Table 3-7 describes each SM501 host interface signal in more detail.

Table 3-7: CPU Interface Signal Descriptions for XScale Interface

SM501 Pin	Connects To:		XScale Pin Type	Design Notes
	SDRAM	XScale		
CD[31:0]	MD[31:0]	MD[31:0]	ICOCZ	CD[31:0] connect to both SDRAM and the SM501.
CA[25]	N/A	MA[25]	OCZ	CA25 does not connect to SDRAM.
CA[24:22]	Normal mode: BA1, BA0, MA12 SA1111 compatible mode: A12, BA1, BA0	MA[24:22]	OCZ	CA[24:22]. CA[24:23] connect to SDRAM BA[1:0] in both modes. In normal operating mode, CA22 connects to SDRAM MA12 (see Figure 3-9). In SA1111 compatible mode, CA24 connects to SDRAM MA12.
CA[21:10]	MA[11:0]	MA[21:10]	OCZ	CA[21:10] also connect to SDRAM MA[11:0]
CA{9:2]	N/A	MA[9:0]	OCZ	No connection to SDRAM.
BE[3:0]	DQM[3:0]	DQM[3:0]	OCZ	SDRAM data mask or byte enable for the SM501: In slave mode, the SM501 requires byte enables to decode the lower 2-bit address. These pins connect to the SM501 byte enable BE[3:0]. In master mode, the SM501 should drive SDRAM DQM[3:0].
HCLK	MCLK	SDCLK1	OCZ	Host clock: In slave mode, the SM501 may need the host clock input to synchronize data transfer. In master mode, the SM501 drives this line for system SDRAM, and the XScale CPU 3-states its clock output.
HCKE	CKE	SDCKE1	OC	Clock enable: Output from XScale. In bus master mode, after REQ goes high, the SM501 uses this signal to determine when to start driving the bus.
HCS#	N/A	One of nCS[5:1]	ICOCZ	Chip select to select the SM501 in bus slave mode. On XScale processor, program MSCx[RTx] bit to 0b100 for VLIO. Choose the CS line as a dedicated chip select for the SM501 and program it for VLIO.
HBS#	N/A	nPWE/ GPIO49	ICOCZ	Write enable. The SM501 can determine if the access is write or read. Connect nPWE to HBS.
HWE#	WE#	nWE	OCZ	Memory write enable. The SM501 uses this signal to control the SDRAM access in bus master mode.
CPURD#	N/A	nOE	OCZ	Memory output enable. Used to control memory device output. In slave mode as VLIO, the SM501 must control its output and OE# toggle for each beat of a burst. In master mode, the SM501 should drive it for external data buffers when buffers are used.

Table 3-7: CPU Interface Signal Descriptions for XScale Interface (Continued)

SM501 Pin	Connects To:		XScale Pin Type	Design Notes
	SDRAM	XScale		
N/A	N/A	RD/nWR	OCZ	XScale signal is not used for VLIO. In bus master mode, after issuing GNT, the XScale CPU drives RD/WR# Low.
HRDY#	N/A	RDY/GP18	ICOCZ	Ready: In slave mode, the SM501 uses to notify XScale when the read data is ready or when the write data can be accepted. Configure GPIO18 before using this pin as RDY.
INTR	N/A	GPIO pin	ICOCZ	Interrupt: Since the XScale processor has no dedicated interrupt input, a GPIO pin is used for this purpose. See “Interrupts” on page 3-10 for more information about interrupts.
RST#	N/A	(nRESET_OUT)	(OC)	Driven by system reset circuit or, optionally, CPU reset output.
REQ#	N/A	MBREQ/ GP14	ICOCZ	GPIO14 can be configured as a bus request signal. Connect GPIO14 to SM501 REQ# pin.
ACK#	N/A	MBGNT/ GP13	ICOCZ	GPIO13 can be configured as a bus grant signal. Connect GPIO13 to the SM501 ACK# pin.
MCS0#	CS# of first SDRAM partition	nSDCS0	OCZ	In bus master mode, the SM501 drives this line to select SDRAM chips. In slave mode, the SM501 will 3-state this line. Connect the SM501 MCS0# signal directly to SDRAM CS# pins (a serial dumping resistor may be added). Also, pull this line up using a weak resistor to hold the line stable during the short period when this line is 3-stated while bus mastership is swapped.
MCS1#	N/A	N/A	OCZ	The XScale CPU has multiple chip select pins but only nSDCS0 can be 3-stated. The SM501 must be able to drive the SDRAM chip select when it is bus master, which requires that the XScale chip select pin on that line be 3-stated. Therefore, the SM501 can only support one partition of the XScale’s SDRAM in the bus master mode.
RAS#	RAS#	nSDRAS	OCZ	During bus master mode, the SM501 drives these lines to control SDRAM. In slave mode, the SM501 will 3-state this line. Connect the SM501 RAS# and CAS# signals directly to SDRAM RAS# and CAS# pins (serial dumping resistor may be added). Pull the lines up with weak resistors to hold the line stable when they go to 3-state mode while bus mastership is swapped.
CAS#	CAS#	nSDCAS	OCZ	

Memory Map and Chip Select

The XScale external memory interface supports a range of memory and I/O interfaces, including SDRAM, page-mode flash, SMROM, page-mode ROM, SRAM, SRAM-like variable latency I/O (VLIO), 16-bit PCMCIA and others. The memory type is configured using the XScale memory configuration registers (see XScale documentation for more information).

The XScale manages its memory space as two independent areas selected by the SDCS# and CS# lines. Four SDCS# lines select SDRAM partitions and six CS# lines select static chips. Each SDCS# or CS# line addresses a 64M byte memory space.

The memory map of the SM501 is divided into a local memory space and a memory-mapped I/O (MMIO) space for the SM501 control registers. The memory space includes the display frame buffer and all other local memory. The size of the SM501 memory space can range from 2MB to 64MB. MMIO is mapped to the top of the memory space with a fixed offset of 0x03E0 0000.

The XScale processor supports a 32-bit external memory space. The upper 6 bits of the address are used to determine the chip select lines and lower 26 bits address memory devices. The physical memory address and memory-mapped I/O of the SM501 are mapped as shown in Table 3-8.

Table 3-8: SM501 in XScale Memory Map

Static Chip Select	CS#	Memory Space	Memory-Mapped I/O Space
1	1	0x0400 0000 – 0x07FF FFFF	0x07E0 0000 – 0x07FF FFFF
2	2	0x0800 0000 – 0x0BFF FFFF	0x0BE0 0000 – 0x0BFF FFFF
3	3	0x0C00 0000 – 0x0FFF FFFF	0x0FE0 0000 – 0x0FFF FFFF
4	4	0x1000 0000 – 0x13FF FFFF	0x13E0 0000 – 0x13FF FFFF
5	5	0x1400 0000 – 0x17FF FFFF	0x17E0 0000 – 0x17FF FFFF

All XScale CS# lines default to GPIO after power-on reset. To use these pins as CS# lines, change the configuration in the XScale registers.

XScale Memory Addressing Modes

The XScale processor supports two SDRAM addressing modes, normal and SA1111-compatible. The addressing mode changes the order of the CPU address bits that are driven on the SDRAM address pins. Refer to the *Intel Developer's Manual* for more details. When the SM501 is functioning as bus master, it must drive the SDRAM using the same bank and address signals as the XScale processor. The SM501 and the XScale processor should be configured in the same address mode. If possible, Silicon Motion recommends using the normal bank address mode due to the larger bank size.

Figure 3-10 and Table 3-9 show typical connections for normal and SA1111-compatible modes to SDRAM with a physical architecture of 2 bank addresses, 13 row addresses, 9 column addresses, and a 32-bit data width. For information on interfacing to other SDRAM configurations, refer to the *Intel Developer's Manual*.

Figure 3-10: Typical SDRAM Addressing

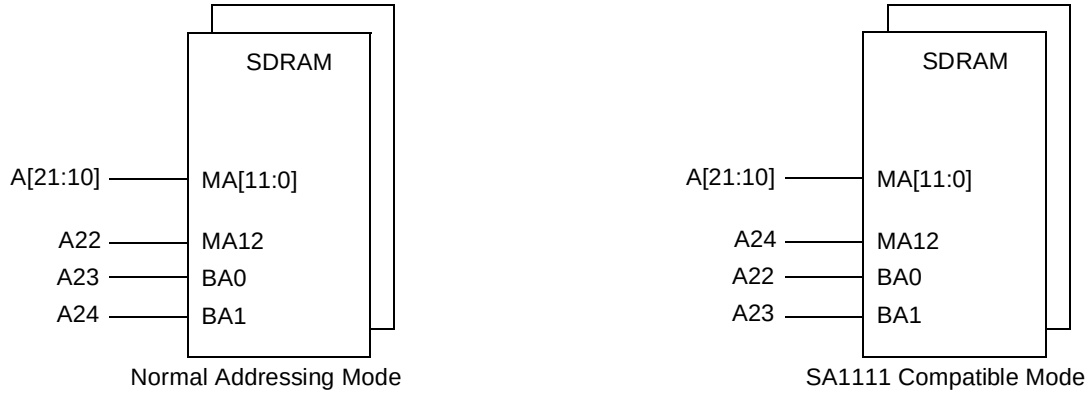


Table 3-9: Typical SDRAM Pin Connections

SDRAM Pin	Normal Addressing Mode				SA1111 Compatible Mode			
	Addr	Bank	Row	Column	Addr	Bank	Row	Column
BA1	CA24	A25			CA23	A24		
BA0	CA23	A24			CA22	A23		
MA12	CA22		A23		CA24		A22	
MA11	CA21		A22		CA21		A21	
MA10	CA20		A21		CA20		A20	
MA9	CA19		A20		CA19		A19	
MA8	CA18		A19	A10	CA18		A18	A25
MA7	CA17		A18	A9	CA17		A17	A9
MA6	CA16		A17	A8	CA16		A16	A8
MA5	CA15		A16	A7	CA15		A15	A7
MA4	CA14		A15	A6	CA14		A14	A6
MA3	CA13		A14	A5	CA13		A13	A5
MA2	CA12		A13	A4	CA12		A12	A4
MA1	CA11		A12	A3	CA11		A11	A3
MA0	CA10		A11	A2	CA10		A10	A2

Local Memory

The SM501 is programmable to allow the use of external local memory or the embedded memory that is supplied in some models of the SM501. Only one of these memories can be used at a time. However, in some applications, it may be useful to design the board with the option to use either one for testing purposes. Figure 3-11 shows a suggested circuit diagram to allow the use of either memory. Table 3-10 explains how to select the local memory option using the GPIO12 pin of the SM501 and the resistors. For production boards, the first two configurations are recommended.

Figure 3-11: Suggested Circuit for External Local Memory

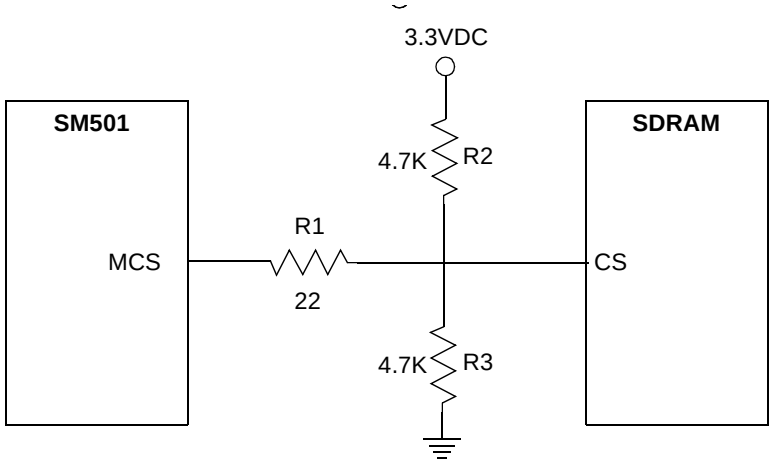


Table 3-10: Configuration Choices for SM501 Local Memory

Implemented on Board	Selected for Use	GPIO12 at Reset	R1	R2	R3
Embedded		0	No	No	No
External			Yes	No	No
Both	Embedded		No	Yes	No
Both	External	1	No	No	Yes

Bus Master

The SM501 can operate as a bus master for the system memory bus. This section describes the sequence of transfer and shows which memory modes are supported by the SM501.

Bus Ownership Transfer

A specific sequence of events takes place when the SM501 takes over and relinquishes ownership of the memory bus. Table 3-11 summarizes the event sequence.

Table 3-11: Sequencing for Transfer of Bus Ownership

Time[1]	XScale	SM501
Design	Connect SDRAM address according to selected addressing mode, normal or SA1111 compatible	
After power-on	Set MDCNFG:SA1111 bit in memory configuration register to match hardware	
	Set SDRAM mode register for burst type = sequential, M9 = 0	Program memory controller
SM501 Requests Bus Ownership		
		Assert BREQ
	If SDCLK and SDCKE are turned on, refresh SDRAM	
	If MDCNFG:SA1111=1, set SDRAM burst length = 1	
t1	Deassert SDCKE	
t1 + 1	3-state SDRAM outputs	
t1 + 2	Assert MBGNT	
t1 + 3		Drive SDRAM outputs
t1 + 4	Assert MDCKE	
		If MDCNFG:SA1111=0, set SDRAM burst length =1 or 8[2]
SM501 Releases Bus Ownership		
		Deassert BREQ
t2	Deassert SDCKE	
t2 + 1	Deassert MBGNT	
t2 + 2		3-state SDRAM outputs
t2 + 3	Drive SDRAM outputs	
t2 + 4	Assert MDCKE. SDRAM uses memclk	
	If SDCLK and SDCKE are turned on, refresh SDRAM	
	If MDCNFG:SA1111=1, set SDRAM burst length = 4	

1. Time in memclk cycles.
2. See Table 3-12 for Supported SDRAM Modes.

Supported SDRAM Modes

Table 3-12 shows the SDRAM modes supported by the SM501. The SM501 parameters are set in the DRAM Control register and should match the settings in the XScale configuration register. See the *SM501 MSOC Databook* for more information.

Table 3-12: XScale SDRAM Modes Supported by the SM501

Parameter	Setting	Supported by the SM501
Burst length	1 (recommended)	Yes
	2	No
	4	No
	8	Yes
	Full page	No
Burst type	Sequential (recommended)	Yes
	Interleave	No
CAS latency	2 (recommended)	Yes
	3	Yes
Write burst mode	Programmed burst length (recommended)	Yes
	Single location access	No

Other Design Considerations

Chip Select

In bus slave mode, the SM501 operates as a 32-bit clocked VLIO device in the XScale static memory space. The SM501 is selected using the XScale CS# signals. CS0# is reserved for bootable memory and typically should not be used to select the SM501. The SM501 can be placed in the memory-mapped partitions selected by CS1# to CS5#. (If possible, system designers should assign a dedicated CS# line to the SM501 since it requires up to 64 Mbytes of space.)

In bus master mode, the SM501 works as an SDRAM controller and controls two SDRAM memory partitions (corresponding to two SDCS# lines). However, only one XScale SDRAM select can be 3-stated during bus master mode. The SM501 can only control one partition of SDRAM (one SDCS# line).

Host Clock Enable Input

Unlike other VLIO devices, the SM501 needs a clock input to synchronize its READ and WRITE access when it is operating as a bus slave. The clock should not use the SDCLK0 and SDCKE0 for CS# partitions as recommended in the *Intel Developer's Manual*. The SM501 drives the SDRAM clock during bus master mode and its host clock input is connected to SDCLK1 which is also used by the SDRAM.

The SM501 HCKE signal must be connected to SDCKE1. The XScale processor drives SDCKE1 continually, so the SM501 uses SDCKE1 as an input to determine when to start driving the bus after bus ownership is requested.

Because the host clock enable signal is always driven by the XScale processor, this signal is an input only to the SM501. Host clock enable will be low during the bus ownership swap.

Bus Clocking

For VLIO devices, the XScale processor samples the data ready input RDY for both read and write accesses. In slave mode, the SM501 functions as a VLIO and drives the RDY signal when the data is ready (READ operation) or ready to accept data (WRITE). However, the SM501 needs a clock input to synchronize its READ and WRITE access during bus slave mode as described in “Host Clock Enable Input”. The clock frequency should be equal to or greater than the XScale internal memory clock frequency and can use the same SDCLK1 signal that the system SDRAM uses. In this case, the clock line that connects to the SM501 will be bidirectional (during bus master mode, the SM501 drives this line to system SDRAM). Therefore, increasing the clock frequency is limited, and the PCB design can become complicated. Beginning with Rev. AA, the SM501 has an option to use its internal memclk for this purpose, so that HCLK can be used as an output during bus master mode. This option simplifies the PCB design and allows higher clock frequency.

SDCLK

The SDRAM should use SDCLK2 or SDCLK1 as described in the XScale documentation. The Variable Latency I/O should use SDCLK0 (Synchronous) or no clock. Since the SM501 has to drive the SDRAM clock on the same line, SDCLK1 should be used.

Interrupts

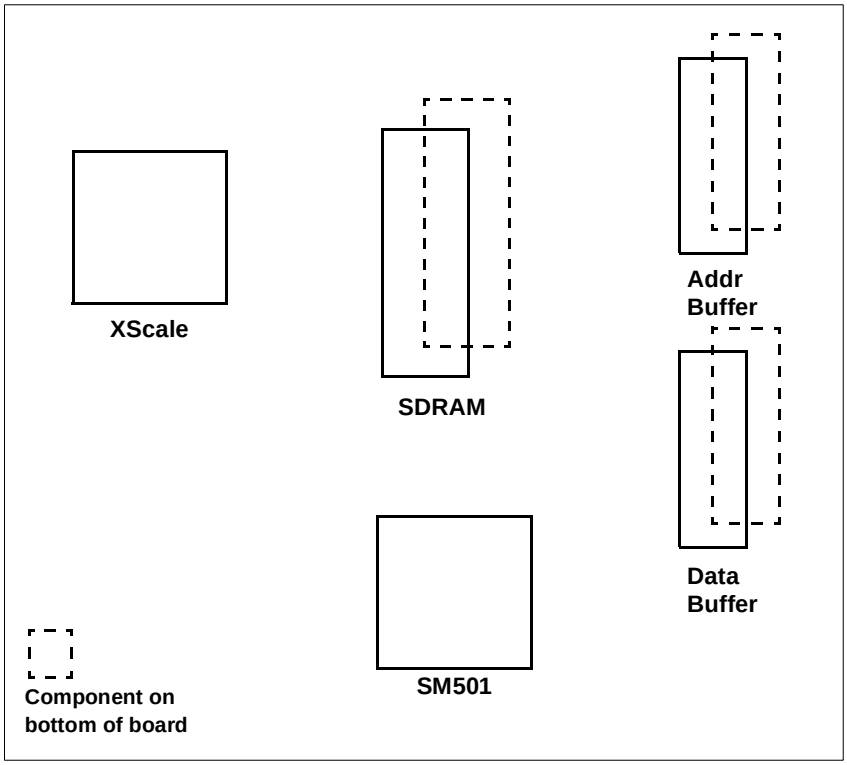
The XScale processor does not have a dedicated interrupt input, but rather uses one of its GPIO pins. Therefore, the SM501 interrupt output INTR should be connected to one of these pins. Since GPIO[14:2] on the XScale have no other dedicated functions, they are the recommended ones to use. However, any GPIO pin can be used with the appropriate hardware and software design.

Host Bus Loading and Chip Placement

In a typical system design, the CPU local bus (address and data) may be heavily loaded. The clock, address and data may not be directly connected to the SM501, and serial damping resistors or buffers may be needed. However, the best practice is to connect the XScale SDRAM and the SM501 directly without buffering and to use a buffered bus for other devices on board. Careful placement of the devices on the board is required.

Figure 3-12 shows a suggested placement arrangement for the components with the XScale processor, SDRAM, and the SM501 in close proximity. Whether the XScale processor or the SM501 is bus master, there are three drive loads. Therefore, the trace lengths and loading should meet the requirement in the XScale design guide.

Figure 3-12: Recommended Placement of Components on Board



Interfacing to NEC MIPS Processors

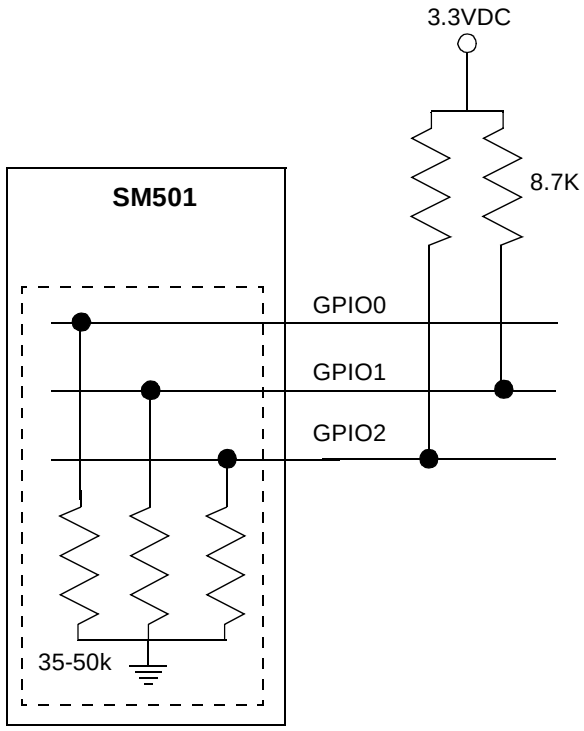
This section provides information for interfacing the SM501 to the NEC VR4122 and VR4131 MIPS processors. It covers these topics:

- Configuration
- Hardware Connections

Configuration

Figure 3-13 shows the circuit used to configure the SM501 for the MIPS processors. External resistors are required to pull GPIO1 and GPIO2 High.

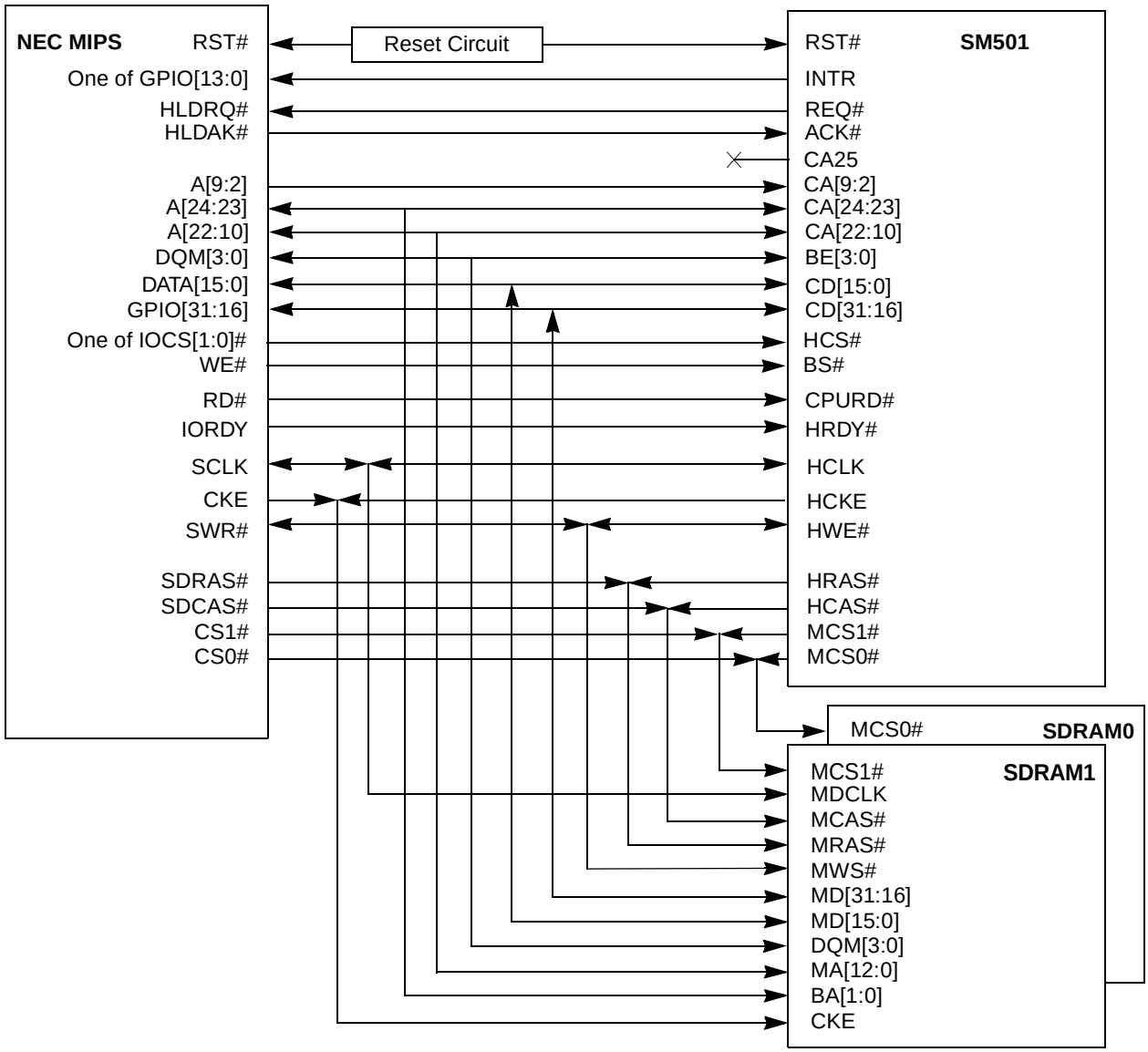
Figure 3-13: Configuring the SM501 for the MIPS Processor



Hardware Connections

Figure 3-3 shows typical SM501 host interface connections for a system using the MIPS processor and SDRAM.

Figure 3-14: SM501 Connections to MIPS Processor and SDRAM



4 Local Memory Interface

The SM501 includes a local memory interface to drive an external local memory of 2 to 64 Mbytes in size. This chapter provides basic information for designing an external local memory. For detailed timing information, consult the documentation provided by the memory device manufacturer.

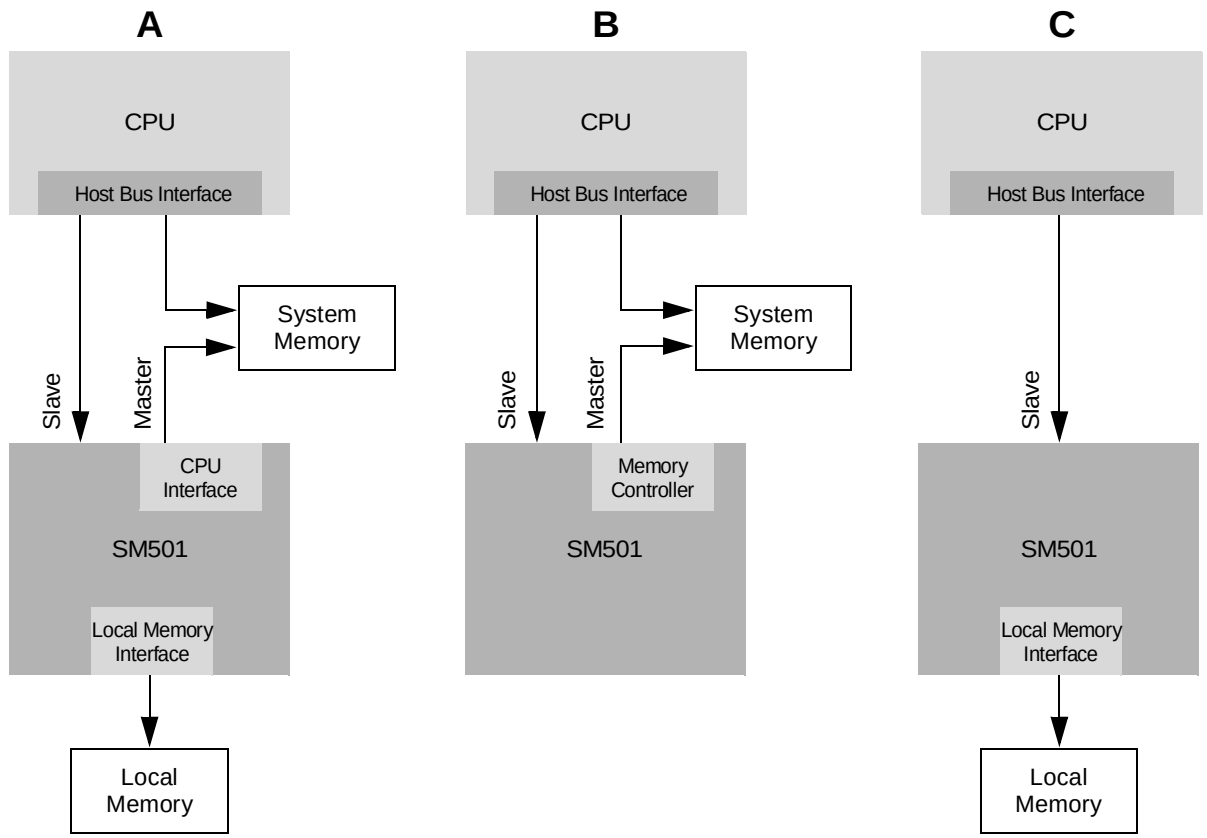
This chapter contains the following sections:

- "Memory Architectures"
- "Local Memory Interface Signals"
- "Configuring the Local Memory Interface"

Memory Architectures

The SM501 supports three different system configurations, two of which are Unified Memory Architecture (UMA) where the system memory and frame buffer share the memory. Figure 4-1 shows the possible configurations.

Figure 4-1: System Configurations



Configuration A uses dedicated memories and has the highest performance. The System SDRAM contains the system memory and the local SDRAM contains the frame buffer. The SM501 acts as a slave on the Host Bus Interface of the CPU. It controls the local SDRAM. The SM501 can also access the system SDRAM by acquiring the bus and act as a master.

Configuration B is an UMA architecture where the system SDRAM contains both the system memory and the frame buffer. The SM501 acts as a slave on the Host Bus Interface of the CPU. The CPU can burst to the system SDRAM as normal, and the SM501 can access the system SDRAM by acquiring the bus and act as a master. Bandwidth is very limited in this configuration since both the CPU and the SM501 compete for the same Host Bus Interface.

Configuration C is the preferred UMA architecture where the local SDRAM contains both the system memory and frame buffer. Since the local SDRAM bus runs at 150 MHz, there is more bandwidth in this configuration than in configuration B. The SM501 acts as a slave on the Host Bus Interface of the CPU.

For information on how the SM501 functions as a bus master and slave, see Chapter 3, CPU Interface.

Local Memory Interface Signals

Table 4-1 describes the signals of the local memory interface. Figure 4-2 shows the connection diagram for a typical SDRAM organized as 4 M x 32.

Figure 4-2: Connections Between SM501 and 4M x 32 SDRAM

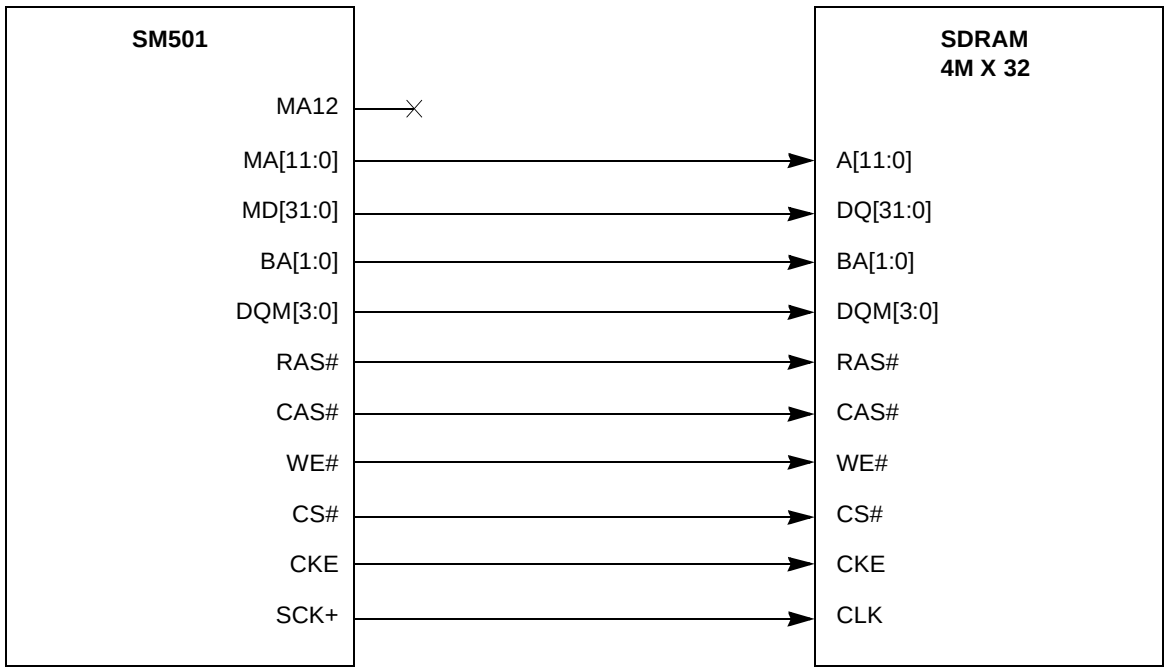


Table 4-1: Local Memory Interface Signal Descriptions

Pin Name	I/O	Pin Number	Description
MA[12:0]	O	R2, R4, T2, T3, U1, P3, P2, P1, N4, N3, N2, N1, M3	Memory address bus. These lines select the word within the memory array. The SM501 can address memory devices with up to 8M words.
MD[31:0]	I/O	Y2, Y1, W4, W3, W2, W1, V3, V2, Y3, Y4, Y5, AA1, AA2, AA3, AA4, AA5, H1, H2, H3, J1, J2, J3, J4, K3, G4, G3, G2, G1, F3, F2, F1, E1	Memory data bus. Bidirectional to support reads and writes. The SM501 supports memory devices up to 32-bit wide.
BA[1:0]	O	M1, M2	Bank address. The SM501 supports memory devices with up to 4 banks.
DQM[3:0]	O	U4,U3, K2, K1	Data bus mask.
DSF	O	R3	Block write. Used only with SGRAM devices.
RAS#	O	L3	Row address select.
CAS#	O	L2	Column address select.
WE#	O	L1	Write enable.
CS#	O	L4	Chip select.
CKE	O	U2	Clock enable.
SCK+	O	R1	Positive Memory clock.
SCK-	O	T1	Negative Memory clock (not used).

Configuring the Local Memory Interface

The configuration of the local memory interface is set using the DRAM Control Register (MMIO_base + 0x000010. This section discusses the bits of this register that control parameters for the local memory interface. Note that other bits of this register control parameters for the CPU interface. See the *SM501 MSOC Databook* for complete descriptions of the DRAM Control Register.

Memory Size

The SM501 must be configured with the size of the local memory. Bits [15:13] of the DRAM Control Register set the size of the local memory as shown in Table 4-2. Note that the size can also be determined by the power-on values of GPIO[15:13], but writing a value to the DRAM Control Register overrides the power-on setting.

Table 4-2: Configuring the Size of Local Memory

DRAM Control Register Bit or GPIO Pin at Power-Up			Memory Size in Mbytes
15	14	13	
0	0	0	4
0	0	1	8
0	1	0	16
0	1	1	32
1	0	0	64
1	0	1	2
1	1	X	Undefined

Memory Device Architecture

The SM501 must be configured for the physical architecture of the memory device(s) used in the local memory, including the number of banks and the column size. Note that the SM501 supports only sequential addressing, not interleaved addressing.

Bit 1 of the DRAM Control Register sets the number of banks in the local memory. Set bit 1 = 0 for a four-bank memory or set bit 1 = 1 for a two-bank memory. The power-on default is 0 (four-bank memory).

Bit 5 of the DRAM Control Register sets the width of the memory device data bus. Set bit 1 = 0 for a 32-bit data bus. The SM501 does not support a 64-bit data bus. The power-on default is 0 (32-bit data bus).

Bits [12:11] of the DRAM Control Register set the column size of the local memory as shown in Table 4-3. Note that the size can also be determined by the power-on values of GPIO[12:11], but writing a value to the DRAM Control Register overrides the power-on setting.

Table 4-3: Configuring the Column Size of Local Memory

DRAM Control Register Bit or GPIO Pin at Power-Up		Column Size
12	**11**	
0	0	256
0	1	Undefined
1	0	512
1	1	1024

Memory Device Timing

The SM501 must be configured for the timing characteristics of the memory devices in the local memory. Table 4-4 summarizes these configuration settings using bits of the DRAM Control Register.

Table 4-4: Configuring the Timing Parameters of Local Memory

Bit(s)	Name	Description
18	WP_X	External Memory Write to Precharge Delay. 0: 2 clocks. 1: 1 clock.
16	Rfsh	Local Memory Refresh to Command Delay. 0: 10 clocks. 1: 12 clocks.
10	BwC	Local Memory Block Write Cycle Time. 0: 1 clock. 1: 2 clocks.
9	BwP	Local Memory Block Write to Precharge Delay. 0: 4 clocks. 1: 1 clock.
8	AP	Internal Memory Active to Precharge Delay. 0: 6 clocks. 1: 7 clocks.
7	Rst	Internal Memory Reset. 0: Reset. 1: Normal.
6	RA	Internal Memory Remain in Active State. 0: Remain active. 1: Do not remain active.
0	WP	Internal Memory Write to Precharge Delay. 0: 2 clocks. 1: 1 clock.

Block Write Enable

When the local memory is implemented as SGRAM devices, the block write feature should be enabled by setting bit 17 of the DRAM Control Register to 1. For other devices, block write should be disabled (bit 17 = 0). The power-on default value of this bit is 0 (block write disabled).

5 LCD Interface

The SM501 integrates a concurrent video processor to control an LCD display. The SM501 LCD interface can be configured to drive one of the following:

- An 18-bit or 24-bit active matrix (TFT) panel
- An 8-bit or 12-bit passive (CSTN) panel, which is supported by a dithering engine providing an effective 18-bit resolution
- An LVDS or TMDS transmitter, which connects directly to an LCD panel

The maximum supported panel size is 1280 x 1024. Panel power sequencing is provided through either hardware or software control.

This chapter provides a detailed description of the signals that comprise the LCD interface, and describes how to configure it. Sample interconnects for different LCD panels are included, followed by some design considerations.

This chapter contains the following sections:

- "Terminology"
- "LCD Signals"
- "Configuring the LCD Interface"
- "Connecting to the LCD Interface"
- "LCD Design Considerations"

Terminology

The following terms are used within this chapter:

- **Alpha Blending** — A means of blending two layers together. The fundamental equation is:

  (α * *c*) + (1 - α) * (original pixel),

  where *c* is the 4-bit color that points into the 18-bit lookup table. In practical terms, 4-bit alpha blending means that for two given display layers, one layer is dominant (for example, the video layer) and the other layer (for example, the video alpha layer) has 16 levels of transparency from 100% to 0% that can be applied to the colors in that layer.
- **bpp** — bits per pixel
- **CSTN** — Color Super Twist Nematic
- **LCD** — Liquid Crystal Display
- **LUT** — LookUp Table
- **LVDS** — Low Voltage Differential Signaling
- **RGB** — Red, Green, Blue
- **RGB 5:6:5** — 16-bit color mode, where Red has 5 bits, Green has 6 bits, and Blue has 5 bits.
- **RGB 8:8:8** — 32-bit color mode, where Red has 8 bits, Green has 8 bits, and Blue has 8 bits. The upper 8 bits are unused.
- **TFT** — Thin Film Transistor

- **TMDS** — Transition Minimized Differential Signaling

LCD Signals

Table 5-1 defines the operation of the LCD signals. This table also lists the alternate names for the shared functionalities.

Table 5-1: LCD Signal Descriptions

LCD Pin Name	I/O	Pin Number	Shared GPIO Pin	Register Bit	Description
FP23	O	W10	–	–	Flat Panel Data output. • R7 in 24-bit TFT mode. • R5 in 18-bit TFT mode. • R0, R4, and R8 in 12-bit CSTN mode. • TXIN5 with external LVDS.
FP22	O	Y10	–	–	Flat Panel Data output. • R6 in 24-bit TFT mode. • R4 in 18-bit TFT mode. • G0, G4, and G8 in 12-bit CSTN mode. • TXIN27 with external LVDS.
FP21	O	V9	–	–	Flat Panel Data output. • R5 in 24-bit TFT mode. • R3 in 18-bit TFT mode. • B0, B4, and B8 in 12-bit CSTN mode. • TXIN6 with external LVDS.
FP20	O	W9	–	–	Flat Panel Data output. • R4 in 24-bit TFT mode. • R2 in 18-bit TFT mode. • R1, R5, and R9 in 12-bit CSTN mode. • TXIN4 with external LVDS.
FP19	O	Y9	–	–	Flat Panel Data output. • R3 in 24-bit TFT mode. • R1 in 18-bit TFT mode. • R0, B2, and G5 in 8-bit CSTN mode. • G1, G5, and G9 in 12-bit CSTN mode. • TXIN3 with external LVDS.
FP18	O	AA9	–	–	Flat Panel Data output. • R2 in 24-bit TFT mode. • R0 in 18-bit TFT mode. • G0, R3, and B5 in 8-bit CSTN mode. • B1, B5, and B9 in 12-bit CSTN mode. • TXIN2 with external LVDS.
FP17	O	AA19	GPIO61	$GPIO_{63:32}$ Control, bit 29	Flat Panel Data output. • R1 in 24-bit TFT mode. • TXIN1 with external LVDS. In order for this signal to function as a Flat Panel output, the indicated bit in the $GPIO_{63:32}$ register must be set to 1.
FP16	O	Y21	GPIO60	$GPIO_{63:32}$ Control, bit 28	Flat Panel Data output. • R0 in 24-bit TFT mode. • TXIN0 with external LVDS. In order for this signal to function as a Flat Panel output, the indicated bit in the $GPIO_{63:32}$ register must be set to 1.

Table 5-1: LCD Signal Descriptions (Continued)

LCD Pin Name	I/O	Pin Number	Shared GPIO Pin	Register Bit	Description
FP15	O	W8	–	–	Flat Panel Data output. • G7 in 24-bit TFT mode. • G5 in 18-bit TFT mode. • B0, G3, and R6 in 8-bit CSTN mode. • R2, R6, and R10 in 12-bit CSTN mode. • TXIN11 with external LVDS.
FP14	O	Y8	–	–	Flat Panel Data output. • G6 in 24-bit TFT mode. • G4 in 18-bit TFT mode. • R1, B3, and G6 in 8-bit CSTN mode. • G2, G6, and G10 in 12-bit CSTN mode. • TXIN10 with external LVDS.
FP13	O	AA8	–	–	Flat Panel Data output. • G5 in 24-bit TFT mode. • G3 in 18-bit TFT mode. • G1, R4, and B6 in 8-bit CSTN mode. • B2, B6, and B10 in 12-bit CSTN mode. • TXIN14 with external LVDS.
FP12	O	V7	–	–	Flat Panel Data output. • G4 in 24-bit TFT mode. • G2 in 18-bit TFT mode. • B1, G4, and R7 in 8-bit CSTN mode. • R3, R7, and R11 in 12-bit CSTN mode. • TXIN13 with external LVDS.
FP11	O	W7	–	–	Flat Panel Data output. • G3 in 24-bit TFT mode. • G1 in 18-bit TFT mode. • R2, B4, and G7 in 8-bit CSTN mode. • G3, G7, and G11 in 12-bit CSTN mode. • TXIN12 with external LVDS.
FP10	O	Y7	–	–	Flat Panel Data output. • G2 in 24-bit TFT mode. • G0 in 18-bit TFT mode. • G2, R5, and B7 in 8-bit CSTN mode. • B3, B7, and B11 in 12-bit CSTN mode. • TXIN9 with external LVDS.
FP9	O	Y20	GPIO59	$GPIO_{63:32}$ Control, bit 27	Flat Panel Data output. • G1 in 24-bit TFT mode. • TXIN8 with external LVDS. In order for this signal to function as a Flat Panel output, the indicated bit in the $GPIO_{63:32}$ register must be set to 1.
FP8	O	Y19	GPIO58	$GPIO_{63:32}$ Control, bit 26	Flat Panel Data output. • G0 in 24-bit TFT mode. • TXIN7 with external LVDS. In order for this signal to function as a Flat Panel output, the indicated bit in the $GPIO_{63:32}$ register must be set to 1.
FP7	O	AA7	–	–	Flat Panel Data output. • B7 in 24-bit TFT mode. • B5 in 18-bit TFT mode. • TXIN17 with external LVDS.

Table 5-1: LCD Signal Descriptions (Continued)

LCD Pin Name	I/O	Pin Number	Shared GPIO Pin	Register Bit	Description
FP6	O	W6	–	–	Flat Panel Data output. • B6 in 24-bit TFT mode. • B4 in 18-bit TFT mode. • TXIN16 with external LVDS.
FP5	O	Y6	–	–	Flat Panel Data output. • B5 in 24-bit TFT mode. • B3 in 18-bit TFT mode. • TXIN22 with external LVDS.
FP4	O	AA6	–	–	Flat Panel Data output. • B4 in 24-bit TFT mode. • B2 in 18-bit TFT mode. • TXIN21 with external LVDS.
FP3	O	V5	–	–	Flat Panel Data output. • B3 in 24-bit TFT mode. • B1 in 18-bit TFT mode. • TXIN20 with external LVDS.
FP2	O	W5	–	–	Flat Panel Data output. • B2 in 24-bit TFT mode. • B0 in 18-bit TFT mode. • TXIN19 with external LVDS.
FP1	O	Y18	GPIO57	$GPIO_{63:32}$ Control, bit 25	Flat Panel Data output. • B1 in 24-bit TFT mode. • TXIN18 with external LVDS. In order for this signal to function as a Flat Panel output, the indicated bit in the $GPIO_{63:32}$ register must be set to 1.
FP0	O	Y17	GPIO56	$GPIO_{63:32}$ Control, bit 24	Flat Panel Data output. • B0 in 24-bit TFT mode. • TXIN15 with external LVDS. In order for this signal to function as a Flat Panel output, the indicated bit in the $GPIO_{63:32}$ register must be set to 1.
BIAS	O	V13	–	–	Flat Panel Voltage Bias. For TFT panels, this signal indicates whether or not the panel bias voltage should be turned on (BIAS = HIGH). For CSTN panels, this output can control the panel contrast.
FPCLK	O	AA10	–	–	Flat Panel Pixel Clock. The active edge of FPCLK is programmable. The LCD panel uses this clock when loading pixel data into its Line Shift register. This signal connects to the TXCLK input of the LVDS transmitter.
FPDISP	O	Y12	–	–	Flat Panel Display Enable. This signal is used as a data enable when the pixel clock needs to latch pixel data.
FPEN	O	V11	–	–	Flat Panel Enable. When High, this output can be used in some applications to inform the external power controller to turn on +12V power to the external power inverter.

Table 5-1: LCD Signal Descriptions (Continued)

LCD Pin Name	I/O	Pin Number	Shared GPIO Pin	Register Bit	Description
FPHSYNC	O	Y11	–	–	Flat Panel TFT Horizontal Sync/STN Line Pulse. For TFT displays, this pin connects to the Horizontal Sync input of the LCD panel. For STN displays, this output connects to the Line Clock input of the LCD panel. This output indicates the end of a horizontal line of pixels being transferred from the Line Shift register to the screen. The panel needs to increment its line pointers and begin a new line.
FPVSYNC	O	W11	–	–	Flat Panel TFT Vertical Sync/STN Frame Pulse. For TFT displays, this output connects to the Vertical Sync input of the LCD panel. For STN displays, this output connects to the Frame Clock input of the LCD panel. This output indicates the start of a new frame of pixels. The panel needs to reset its line pointers to the top of the screen.
PWM2	O	P19	GPIO31	$GPIO_{31:0}$ Control, bit 31	Power Width Modulator 2. This output provides brightness control to the LCD panel. In order for this signal to function as a PWM output, the indicated bit in the $GPIO_{31:0}$ register must be set to 1.
PWM1	O	N21	GPIO30	$GPIO_{31:0}$ Control, bit 30	Power Width Modulator 1. This output provides brightness control to the LCD panel. In order for this signal to function as a PWM output, the indicated bit in the $GPIO_{31:0}$ register must be set to 1.
PWM0	O	N20	GPIO29	$GPIO_{31:0}$ Control, bit 29	Power Width Modulator 0. This output provides brightness control to the LCD panel. In order for this signal to function as a PWM output, the indicated bit in the $GPIO_{31:0}$ register must be set to 1.
VDEN	O	W12	–	–	Flat Panel VDD Enable. This output controls the power on/off operation. The SM501 drives this output LOW to inform the panel voltage controller to turn off the panel power.

Configuring the LCD Interface

The following registers configure the SM501 for LCD operation:

- Panel Display Control register (MMIO_base + `0x080000`)
- Miscellaneous Control register (MMIO_base + `0x000004`)
- $GPIO_{31:0}$ Control register (MMIO_base + `0x000008`)
- $GPIO_{63:32}$ Control register (MMIO_base + `0x00000C`)
- Panel Horizontal Total (MMIO_base + `0x080024`)
- Panel Horizontal Sync (MMIO_base + `0x080028`)
- Panel Vertical Total (MMIO_base + `0x08002C`)
- Panel Vertical Sync (MMIO_base + `0x080030`)
- PWM 0 register (MMIO_base + `0x010020`)
- PWM 1 register (MMIO_base + `0x010024`)
- PWM 2 register (MMIO_base + `0x010028`)

Refer to the *SM501 MSOC Databook* for complete details on these registers.

Supported LCD Panel Types and Devices

The SM501 supports two basic types of LCD panels: passive and active matrix. Table 5-2 summarizes the supported panel types.

Table 5-2: SM501-Supported LCD Panels

Technology	Panel	Meaning	Types
Passive	CSTN	Color Super Twist Nematic	• 8-bit CSTN • 12-bit CSTN
Active	TFT	Thin Film Transistor	• 18-bit TFT • 24-bit TFT

In addition to the LCD panels listed in Table 5-2, the SM501 LCD interface can operate with an LVDS or TMDS transmitter. Table 5-3 lists how to select one of these five options.

Table 5-3: LCD Interface Configuration

Display Type	Configuration
18-bit TFT	• Set bit 25 of the Miscellaneous Control Register to 18-bit (0). • Set bits [29:24] of the $GPIO_{63:32}$ Control register to zeros. • Set bits [19:18] of the Panel Display Control register to TFT panel (00).
24-bit TFT	• Set bit 25 of the Miscellaneous Control Register to 24-bit (1). • Set bits [29:24] of the $GPIO_{63:32}$ Control register to ones. • Set bits [19:18] of the Panel Display Control register to TFT panel (00).
8-bit CSTN	• Set bits [19:18] of the Panel Display Control register to 8-bit STN panel (10).
12-bit CSTN	• Set bits [19:18] of the Panel Display Control register to 12-bit STN panel (11).
LVDS/TMDS Transmitter	• Set bits [29:24] of the $GPIO_{63:32}$ Control register to ones.

LCD Signal Configurations

Polarities

The active states of the FPEN, BIAS, and VDEN signals are individually configurable as high or low, depending on the settings of bits 27, 26, and 24 in the Panel Display Control register, respectively.

The active edges of the FPHSYNC and FPVSYNC pulses can be configured as high or low, depending on the settings of bits 12 and 13 in the Panel Display Control register, respectively.

The FPCLK signal is configurable as having an active high or active low edge, depending on the setting of bit 14 in the Panel Display Control register.

Enables

When bit 0 of the System Control register is cleared, the LCD panel interface is enabled.

Bit 25 of the Panel Display Control register enables the panel control signals (FPCLK, FPDISP, FPHSYNC, FPVSYNC) and data lines. When bit 25 disables these signals, they are all driven LOW.

Bit 8 of the Panel Display Control register controls the panel timing. When the panel is in power-saving mode, the timing from the SM501 must be disabled. In the power-saving sequence, the panel signals are first disabled through bit 25, and then this bit is cleared to disable the panel timing.

Horizontal and Vertical Parameters

As stated in the subsection above, the polarity of the horizontal and vertical sync outputs is programmable. In addition, the following parameters need to be known for proper display (refer to Figure 5-1 and Figure 5-2 for the placement of these parameters):

- Horizontal Pulse Time (HPT)

  FPHSYNC pulse in pixels. Each pixel is equivalent to one pixel clock.
- Horizontal Time (HT)

  Total number of pixels – 1 in a horizontal line (including all displayable and non-displayable areas).
- Vertical Pulse Time (VPT)

  FPVSYNC pulse in lines. Each line is equivalent to one horizontal time.

  Start of the active edge of the FPVSYNC pulse in lines – 1.
- Vertical Time (VT)

  Total number of lines – 1 in a screen (including all displayable and non-displayable areas).

Figure 5-1: Horizontal Parameters

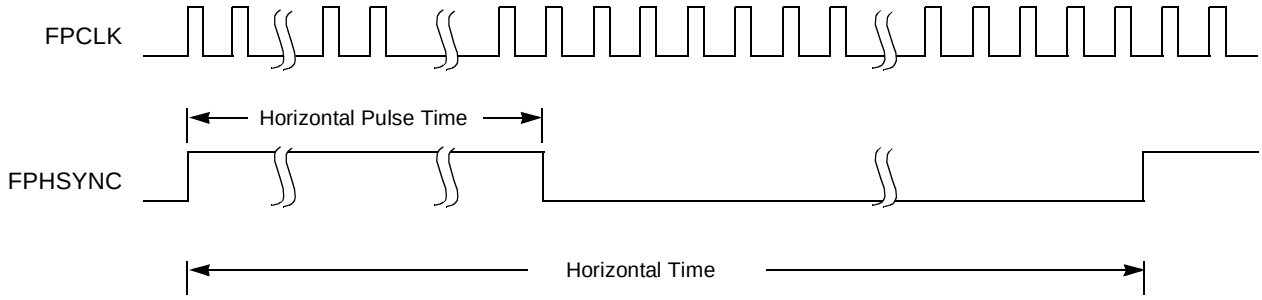
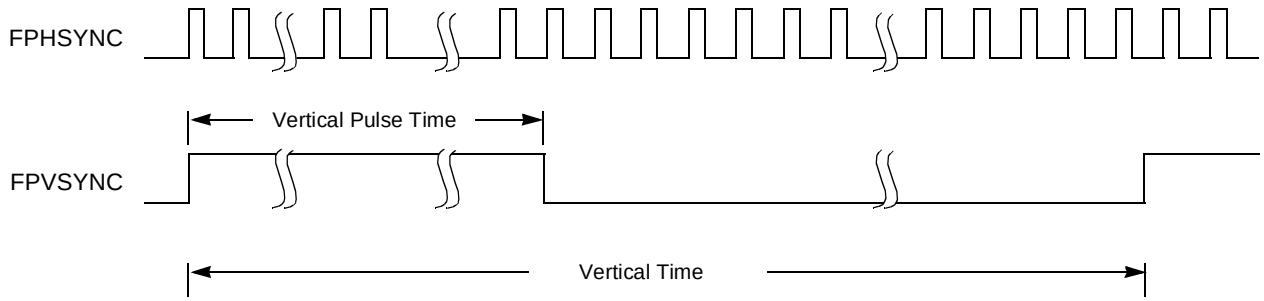


Figure 5-2: Vertical Parameters



Pulse Width Modulation (PWM) Signals

Three independent PWM outputs (PWM[2:0]) are provided for handling brightness control of the LCD panel. Each output has its own control register. Two PWMs have each three independently selectable frequencies. The third PWM has three selectable frequency multiples that are synchronized to the video SYNC signal.

The PWM signals can generate a square wave by programming the PWM registers. This square wave is used to control the voltage of the backlight.

Interrupt Handling

The SM501 can be programmed to recognize Panel Vertical Sync interrupts by enabling bit 1 in the Interrupt Mask register (MMIO_base + `0x000030`). Bit 1 of the Interrupt Status register (MMIO_base + `0x00002C`) is set to one when an active edge of FPVSYNC is encountered. Bit 1 of the Raw Interrupt Clear register (MMIO_base + `0x000028`) must be cleared to clear the interrupt condition.

The SM501 also can be programmed to recognize interrupts from each of the three PWM outputs.

Color Key

Bit 9 of the Panel Display Control register enables the color key. The color key is used to distinguish between the graphic and video images.

Gamma Control

Gamma control can be enabled only in RGB 5:6:5 and RGB 8:8:8 modes. Because the LCD has nonlinear signal-to-light intensities or intensity-to-signal characteristics, the gamma control feature compensates for this nonlinearity.

Horizontal and Vertical Panning

Automatic horizontal panning is enabled when bit 4 of the Panel Display Control register is set. The horizontal panning direction is configurable as either left-to-right or right-to-left as determined by bit 5.

Automatic vertical panning is enabled when bit 6 of the Panel Display Control register is set. The vertical panning direction is configurable as either top-to-bottom or bottom-to-top as determined by bit 7.

TFT Dithering

Dithering is the simulation of a color from a combination of other colors when the required color is not in the current color palette. Dithering is enabled by bit 20 of the Panel Control register. Dithering must be enabled when using STN panels. Dithering is not required for TFT panels.

The SM501 can perform dithering using either a 4-gray level dithering pattern or an 8-gray level dithering pattern, as specified by bit 23 of the Panel Control register. Table 5-4 lists the number of gray levels based on the panel type and the dithering pattern, if any.

Table 5-4: Gray Levels for STN and TFT Panels

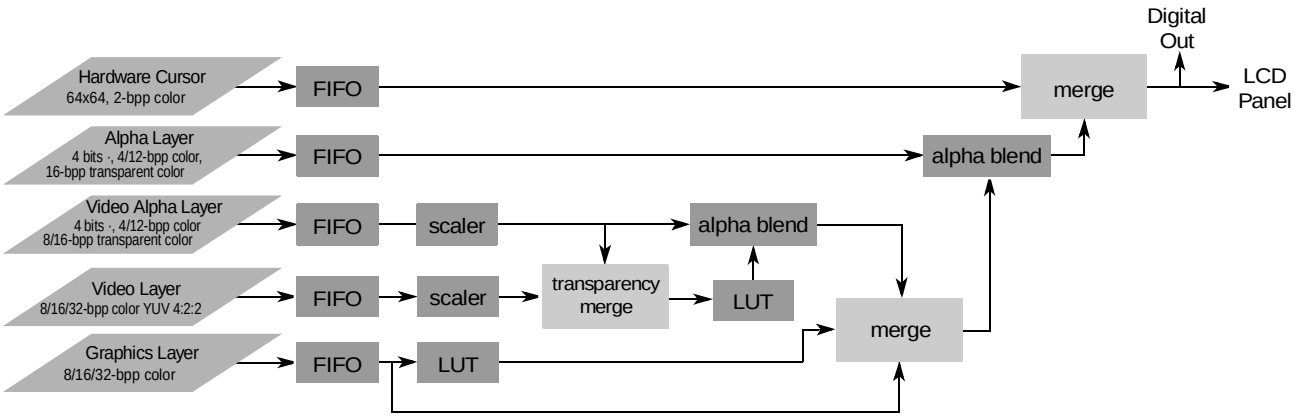
Panel Type	Dithering Pattern (Bit 23)	Number of Gray Levels
CSTN (Dithering always enabled)	4 gray level	4
	8 gray level	8
12-bit TFT[1]	Dithering disabled	16
	4 gray level	64
	8 gray level	128
18-bit TFT[2]	Dithering disabled	64
	4 gray level	256
	8 gray level	512
24-bit TFT	Dithering disabled	256
	4 gray level	1024
	8 gray level	2048

1. Dithering increases the resolution for a 12-bit TFT to 18 bits.
2. Dithering increases the resolution for an 18-bit TFT to 24 bits.

Video Layers

Figure 5-3 shows the five video layers that make up a display on an LCD panel. Each layer has its own FIFO. The layers are blended and/or merged together into a frame buffer, which is displayed on the LCD panel.

Figure 5-3: Video Layers



The five layers shown in Figure 5-3 are described in more detail below:

Primary Graphics Layer

This layer displays text or drawings on the primary output (LCD panel). It is enabled by bit 2 of the Panel Display Control register. This layer supports smooth scrolling and auto-wrapping. The pixel colors in this layer are formatted as one of the following (as determined by bits [1:0] of the Panel Display Control register):

- 8-bit index (index into RGB 8:8:8 lookup table)
- 16-bpp RGB 5:6:5
- 32-bpp RGB 8:8:8

The color value of every pixel in this layer (8-bit with 8-bit index, 16-bit with 16-bit RGB 5:6:5, or 32-bit with 32-bit RGB 8:8:8) is compared with the contents of the Panel Color Key register. If the color value matches the register's value, then the pixel color is transparent and the pixel from the Primary Video layer is shown instead.

Video Layer

This layer overlays a video image or graphics on top of the Primary Graphics layer. It supports bilinear upscaling and downscaling. The pixel colors in this layer are formatted as one of the following:

- 8-bit index (index into RGB 8:8:8 lookup table)
- 16-bpp RGB 5:6:5 or YUV 4:2:2
- 32-bpp RGB 8:8:8

Video Alpha Layer

This layer alpha-blends and/or color-keys an image on top of the Video layer output. It supports bilinear upscaling and downscaling. The pixel colors in this layer are formatted as one of the following:

- 8-bpp (4-bit alpha, 4-bit index color) or 8-bit index (index into RGB 8:8:8 lookup table)
- 16-bpp (4-bit alpha, 4-bit Red, 4-bit Green, 4-bit Blue) or RGB 5:6:5

Each pixel's color in the Video Alpha layer is compared with the contents of either an internal 8-bit transparency register (for 8-bit index) or a 16-bit transparency register (for 16-bit RGB 5:6:5 mode). If a color matches the register's value, then that pixel is transparent.

In 16-bit RGB 5:6:5 mode only, an internal 4-bit planar blending register blends all non-transparent pixels on the plane to one planar alpha value.

Alpha Layer

This layer alpha-blends and/or color-keys an image on top of the Primary Graphics and Video layer outputs. The pixel colors in this layer are formatted as one of the following:

- 16-bpp (4-bit alpha, 4-bit Red, 4-bit Green, 4-bit Blue)
- RGB 5:6:5

In 16-bit RGB 5:6:5 mode only, each pixel's color is compared to the contents of an internal 16-bit transparency register. If a color matches the register's value, then that pixel is transparent.

In 16-bit RGB 5:6:5 mode only, an internal 4-bit planar blending register blends all non-transparent pixels on the plane to one planar alpha value.

Hardware Cursor Layer

This layer displays a cursor on the digital output. One single 64x64 pixel cursor with 2-bpp color (00 = transparent, 01 = color 0, 10 = color 1, 11 = color 2) is mapped into a 32-bit RGB 8:8:8 color map. The hardware cursor address is in the Panel HWC Address register. The cursor's screen location is in the Panel HWC Location register. The colors are defined in the Panel HWC Color 1 & 2 register and the Panel HWC Color 3 register.

Connecting to the LCD Interface

This section provides more detail on active and passive displays and includes several sample interconnections between the SM501 and different LCD panels.

Active (TFT) Displays

The SM501 supports both 18-bit and 24-bit TFT panels. Depending on the mode selected, each pixel is defined by 18 or 24 data bits. The data bits provide the intensity level of the red, green, and blue elements for each pixel. The SM501 supports 24-bit RGB 8:8:8, 9-bit RGB 3:3:3, and 12-bit RGB 4:4:4 (configured through bits [22:21] of the Panel Display Control register).

Table 5-5 lists the SM501 Active Display pins and their corresponding TFT panel pins.

Table 5-5: SM501 and Corresponding TFT Pins

SM501 Pin		TFT Pin
24-bit TFT	FP[23:16]	R[7:0]
	FP[15:18]	G[7:0]
	FP[7:0]	B[7:0]
18-bit TFT	FP[23:18]	R[5:0]
	FP[15:10]	G[5:0]
	FP[7:2]	B[5:0]
FPCLK		Clock
FPDISP		Data Enable (DE)
FPVSYNC		Vertical Sync (VSYNC)
FPHSYNC		Horizontal Sync (HSYNC)

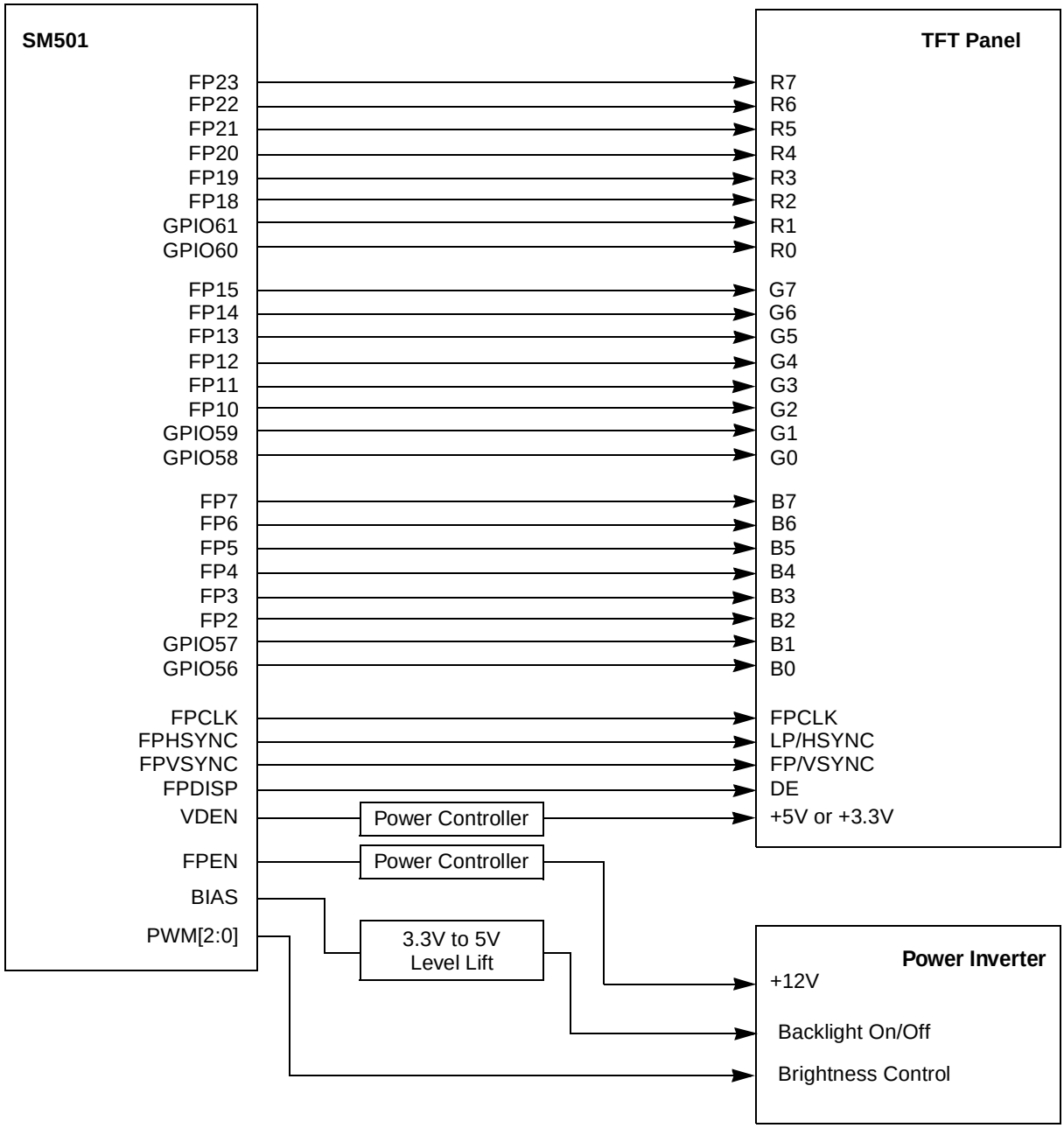
Note the following with regards to the interface to a TFT panel:

1. Software fully controls the timings of VDEN, FPEN, and BIAS.
2. The TFT panel does not use Vbias. The BIAS control used here controls the On/Off switch of the backlights. Program its timing so backlight is on after 12V is applied to the inverter.
3. The SM501 provides three PWM signals that can be used to control brightness.

Interconnection to a 24-bit TFT Panel

Figure 5-4 shows a typical interface between the SM501 and a 24-bit TFT panel.

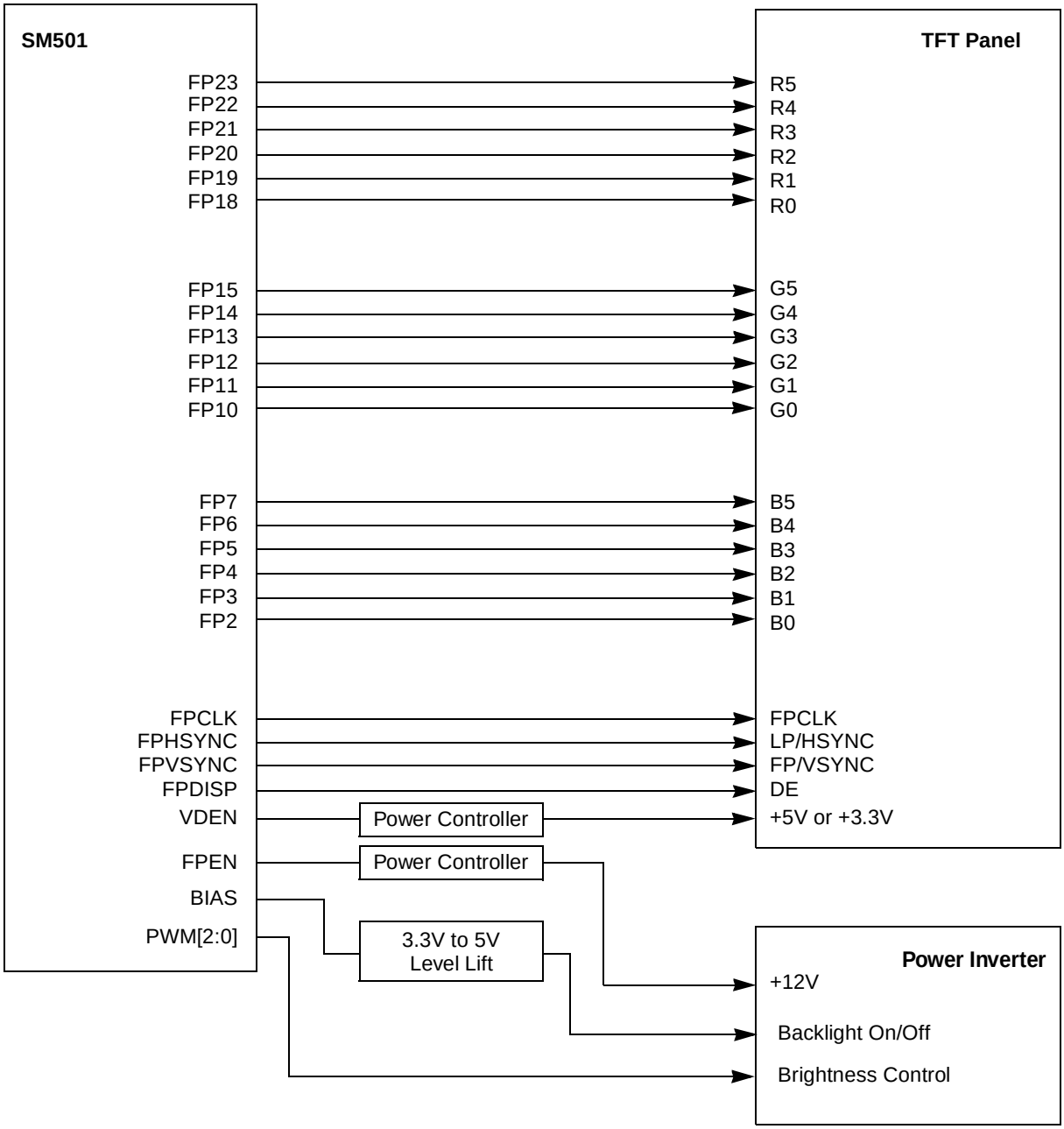
Figure 5-4: Typical 24-bit TFT Panel Interface (RGB 8:8:8)



Interconnection to an 18-bit TFT Panel

Figure 5-5 shows a typical interface between the SM501 and an 18-bit TFT panel.

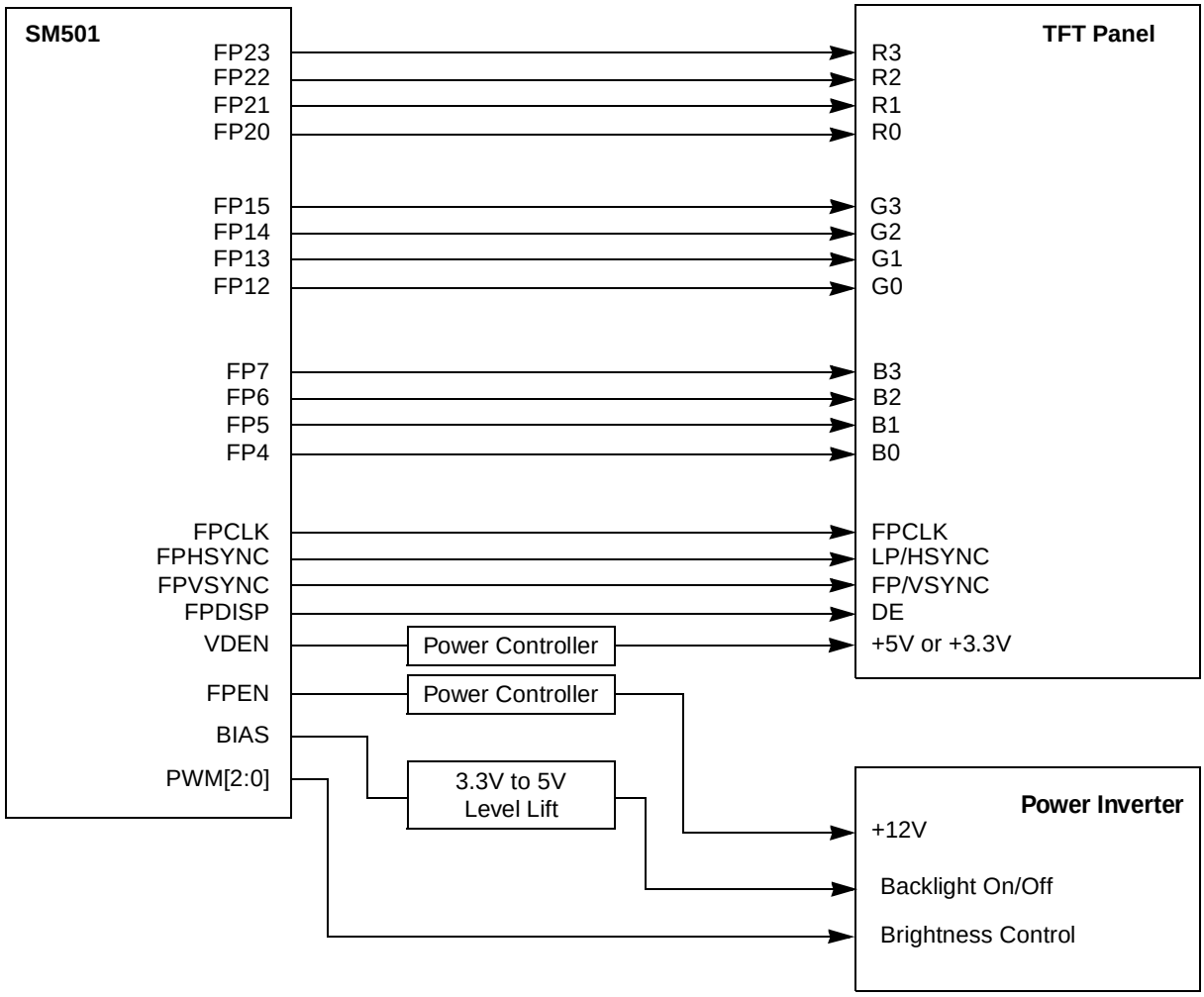
Figure 5-5: Typical 18-bit TFT Panel Interface (RGB 6:6:6)



Interconnection to a 12-bit TFT Panel

Figure 5-6 shows a typical interface between the SM501 and a 12-bit TFT panel.

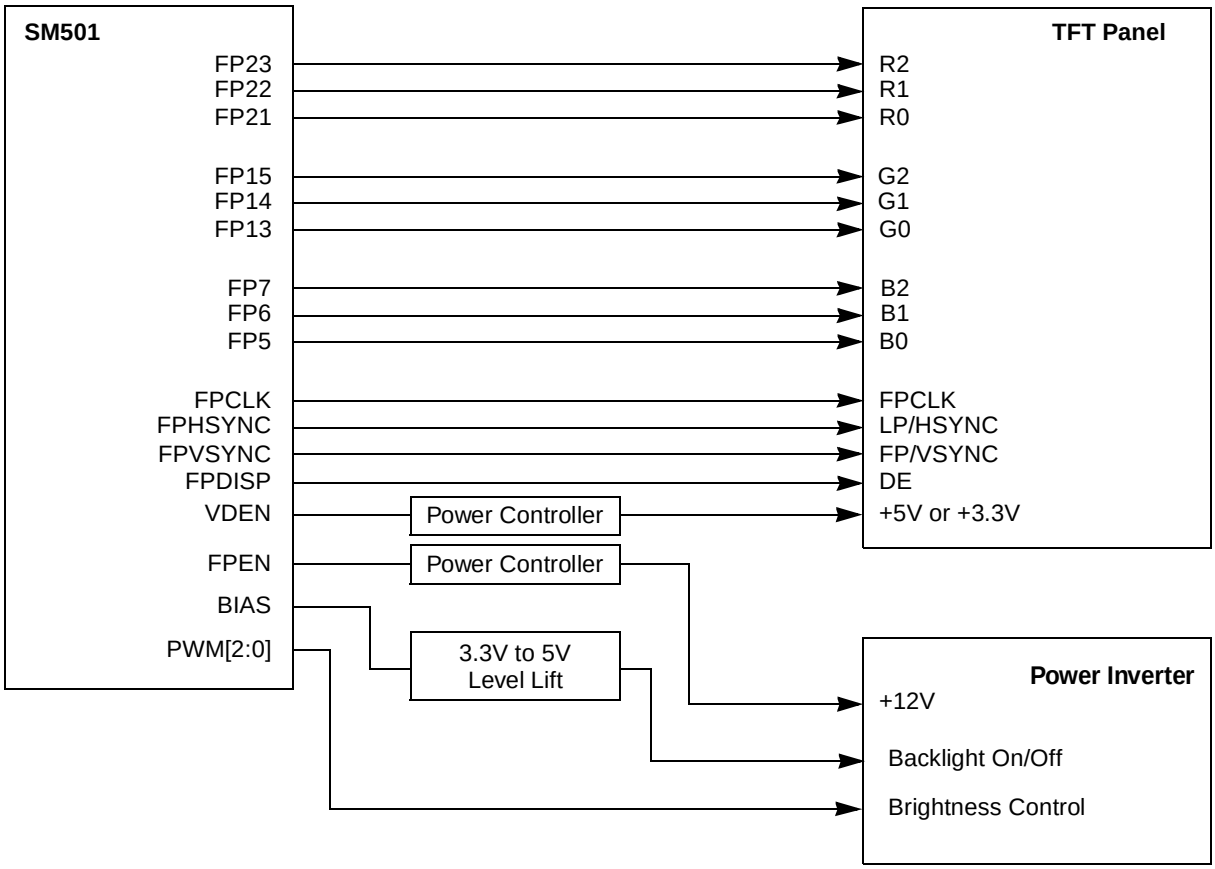
Figure 5-6: Typical 12-bit TFT Panel Interface (RGB 4:4:4)



Interconnection to a 9-bit TFT Panel

Figure 5-7 shows a typical interface between the SM501 and a 9-bit TFT panel.

Figure 5-7: Typical 9-bit TFT Panel Interface (RGB 3:3:3)



Passive (CSTN) Displays

The SM501 supports both 8-bit and 12-bit CSTN panels. Depending on the mode selected, each pixel is defined by 8 or 12 data bits. Dithering controls the different gray levels.

Table 5-6 lists the SM501 Passive Display pins and their corresponding CSTN panel pins.

Table 5-6: Passive Display Pins

SM501 Pin		CSTN Panel Pin
8-bit CSTN	FP[19:18]	D[7:6]
	FP[15:10]	D[5:0]
12-bit CSTN	FP[23:18]	D[11:6]
	FP[15:10]	D[5:0]
FPDISP		Bias
FPCLK		Pixel Clock
FPHSYNC		Line Clock
FPVSYNC		Frame Clock

Interconnection to an 8-bit CSTN Panel

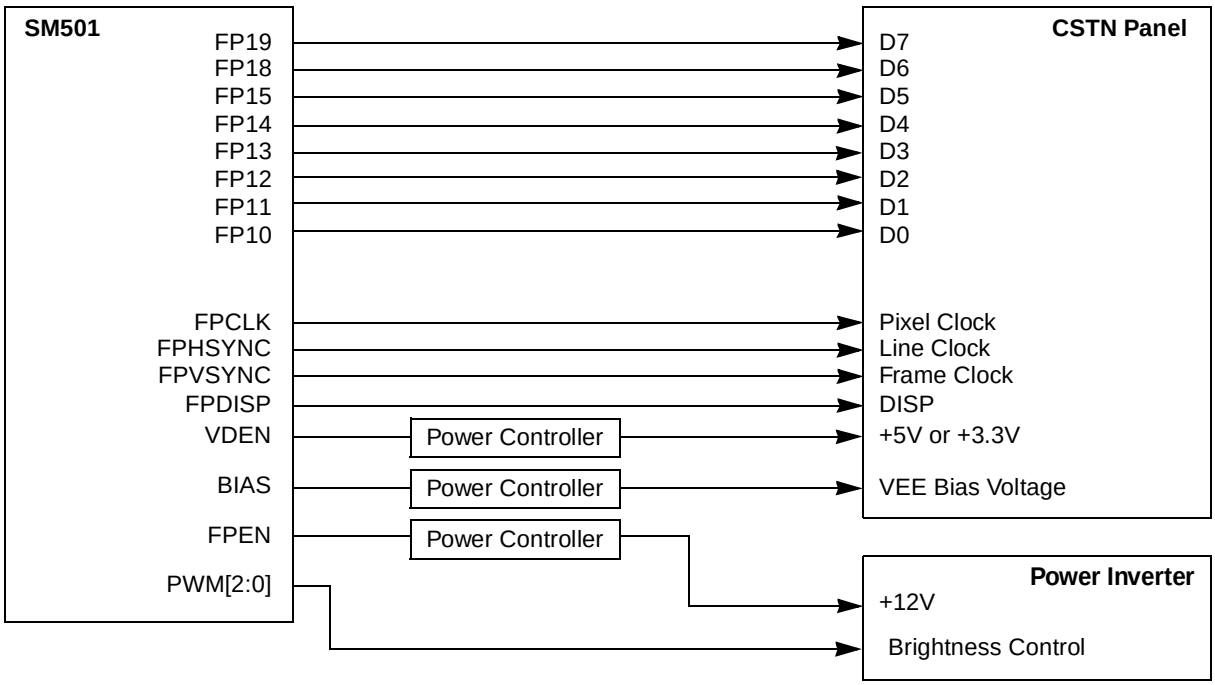
RGB data is sent on the 8-bit CSTN data bus in three clock cycles as indicated in Table 5-7.

Table 5-7: RGB Data Bit Multiplexing to 8-bit CSTN Panel

SM501 Pin	First Clock	Second Clock	Third Clock
FP19	R0	B2	G5
FP18	G0	R3	B5
FP15	B0	G3	R6
FP14	R1	B3	G6
FP13	G1	R4	B6
FP12	B1	G4	R7
FP11	R2	B4	G7
FP10	G2	R5	B7

Figure 5-8 shows a typical interface between the SM501 and an 8-bit CSTN panel.

Figure 5-8: Typical 8-bit CSTN Panel Interface



Interconnection to a 12-bit CSTN Panel

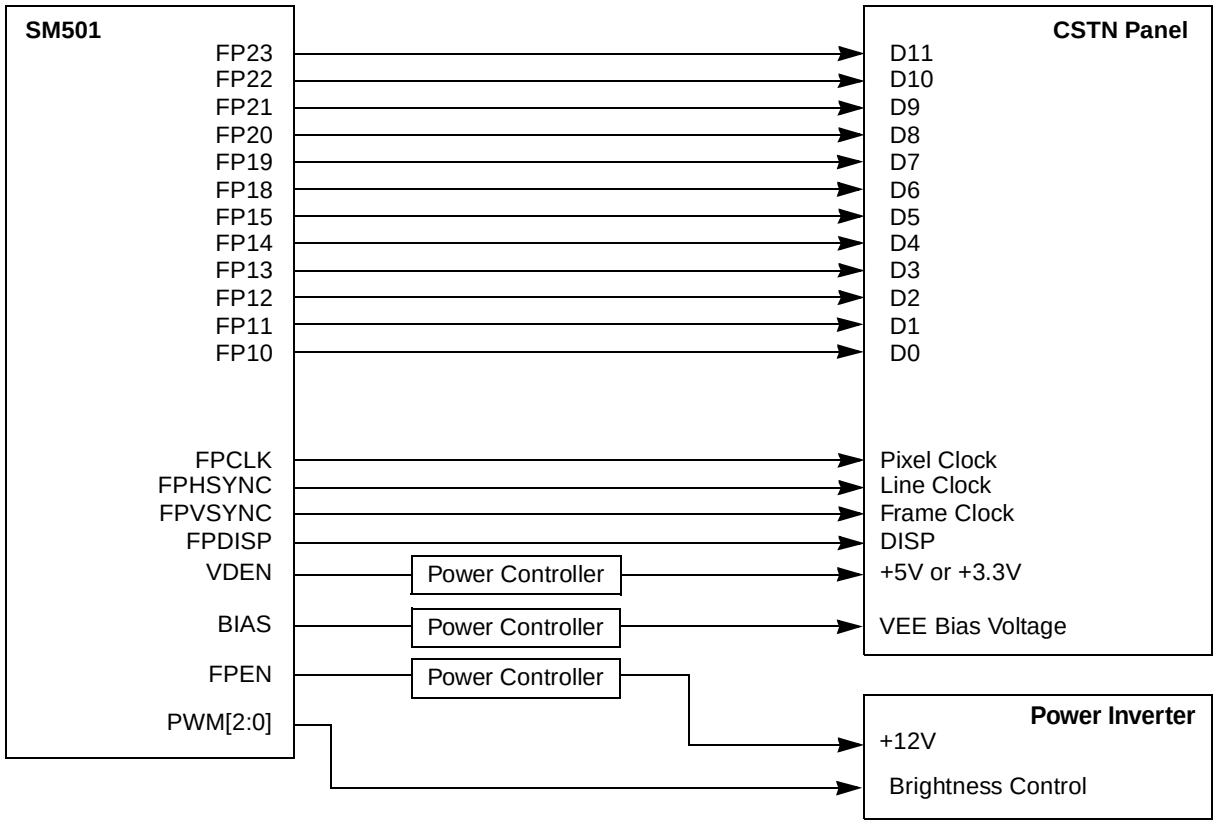
RGB data is sent on the 12-bit CSTN data bus in three clock cycles as indicated in Table 5-8.

Table 5-8: RGB Data Bit Multiplexing to 12-bit CSTN Panel

SM501 Pin	First Clock	Second Clock	Third Clock
FP23	R0	R4	R8
FP22	G0	G4	G8
FP21	B0	B4	B8
FP20	R1	R5	R9
FP19	G1	G5	G9
FP18	B1	B5	B9
FP15	R2	R6	R10
FP14	G2	G6	G10
FP13	B2	B6	B10
FP12	R3	R7	R11
FP11	G3	G7	G11
FP10	B3	B7	B11

Figure 5-9 shows a typical interface between the SM501 and a 12-bit CSTN panel.

Figure 5-9: Typical 12-bit CSTN Panel Interface

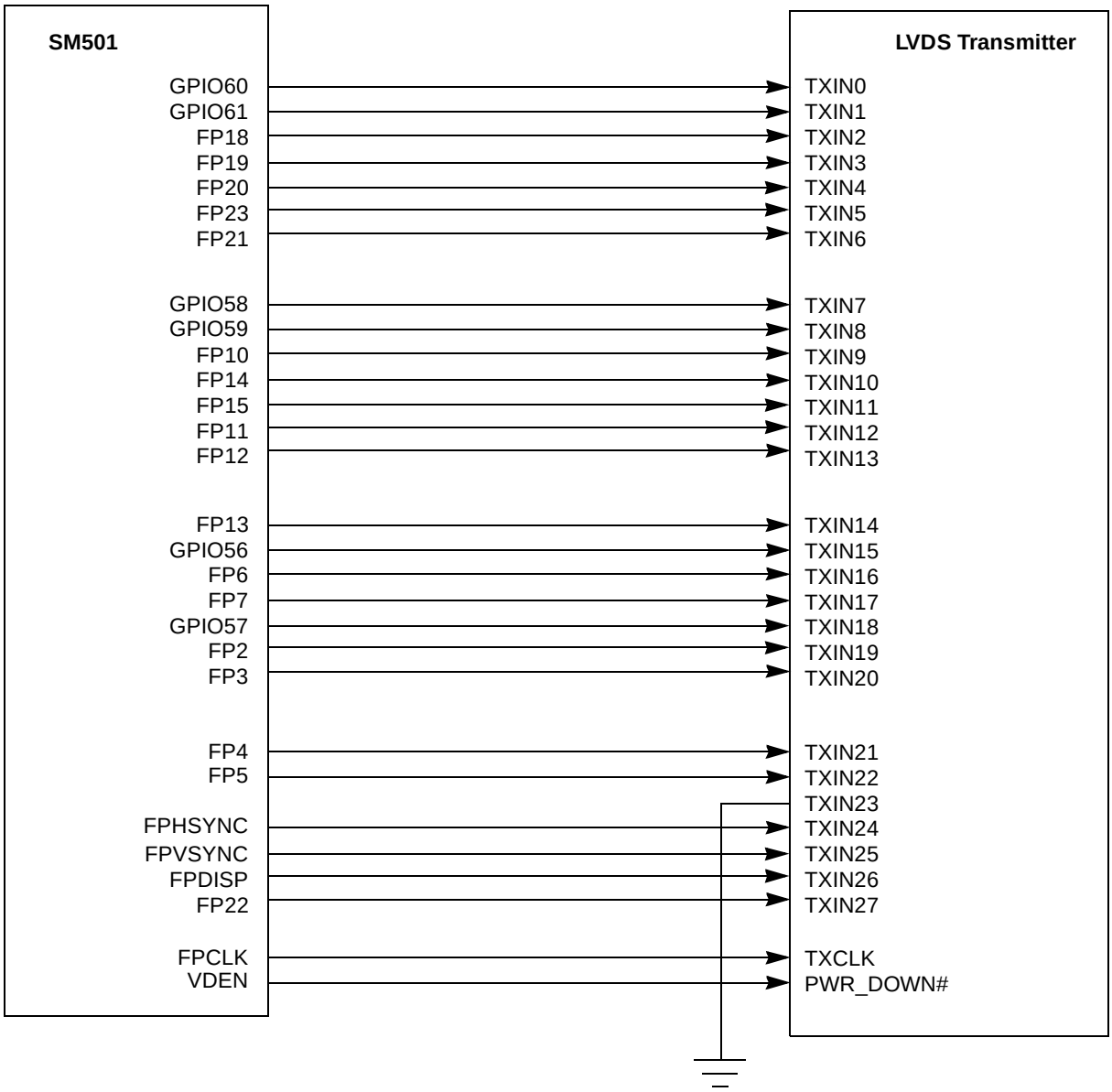


LVDS or TMDS Transmitter Interconnection

The SM501 can send digital data from its display interface to an LVDS or TMDS transmitter, which connects to the display panel. The LVDS interface has been standardized by IEEE and allows the display to be up to 8m away from the computer.

Figure 5-10 shows a typical interface between the SM501 and a National Semiconductor DS90C385 24-bit LVDS Transmitter.

Figure 5-10: Typical 24-bit LVDS Interface (DS90C385)



LCD Design Considerations

This section covers some additional topics to consider when designing with an LCD panel.

Signal Layout Recommendations

The following recommendations are provided with regard to the routing of LCD signals:

- Minimize the trace length of the LCD panel signals while providing enough spacing between signals in order to avoid crosstalk.
- Add buffers along the data path between the SM501 and the LCD panel if a long trace length cannot be avoided or if the routing is inefficient. The buffers can increase the LCD panel signal strength and help to synchronize signal timing. Signal timing typically is not a critical issue with LCD panels because their transmission rates are not tight.

Noise Minimization

Minimizing noise is an important step in your LCD panel design. Recommendations for two problem areas are given below.

Touchscreen Control Lines

When present, touchscreen control lines can be injected with noise from the LCD panel and its control signals, resulting in spurious touch interrupts or loss of resolution. To avoid this noise, shield all touchscreen control lines when the LCD panel is mounted.

Backlight Inverters

Backlighting is used to make the LCD readable in low-light conditions. Backlight inverters in LCD panels are a potential source of noise due to frequent voltage inversions from their high voltage source. The following recommendations help reduce the potential for spurious noise:

- Place the inverter as far as possible from the LCD data lines and system board.
- Ensure that the inverter is shielded.
- If possible, disable the inverter via software when there is no activity over a predetermined amount of time.

Contrast Voltage Adjustment

Many displays provide a pin to use for adjusting their contrast voltage via a potentiometer. This capability can introduce screen artifacts if the configuration does not meet the voltage and current specifications defined by the LCD manufacturer. Refer to the LCD panel manufacturer’s documentation for recommended contrast voltage circuits.

Power-Down Precautions

Panel damage can occur if the BIAS signal is present without the active panel FPHSYNC and FPVSYNC signals. Ensure that the BIAS supply is at zero volts before removing the sync signals.

LVDS and TMDS Layout Considerations

Note the following when implementing a design with an LVDS or a TMDS device:

- Avoid sharp 90-degree edges to reduce changes in impedance for high-frequency signals.
- Keep differential pairs parallel and close to one another to maintain identical electrical lengths.
- Place the graphics controller as close as possible to the LVDS/TMDS connector interface.
- Place all termination resistors as close as possible to the LVDS/TMDS device.
- Separate digital signals from the LVDS/TMDS differential pair signals to avoid crosstalk by using different plane or use ground planes between digital signals and LVDS/TMDS signals.

6 Analog RGB Interface

The SM501 Analog RGB block contains a 24-bit DAC (RGB 8:8:8) that drives an external analog RGB interface. The Analog RGB interface provides data and control signals for a CRT. The 200MHz DAC supports a maximum resolution of 1280 x 1024.

This chapter provides a detailed description of the signals that comprise the Analog RGB interface, and describes how to configure it. Sample interconnects are included along with some design considerations.

This chapter contains the following sections:

- "Analog RGB Interface Signals"
- "Configuring the Analog RGB Interface"
- "Analog RGB Interconnections"
- "Analog RGB Design Considerations"

Analog RGB Interface Signals

Table 6-1 defines the operation of the Analog RGB signals.

Table 6-1: Analog RGB Signal Descriptions

Pin Name	I/O	Pin Number	Description
B	O	AA12	This signal is the blue CRT output.
G	O	AA13	This signal is the green CRT output.
R	O	Y13	This signal is the red CRT output.
CRT_HSYNC	O	W13	This signal is the horizontal sync for the CRT.
CRT_VSYNC	O	W14	This signal is the vertical sync for the CRT.
IREF	I	AA11	This input is the reference current for the SM501. A 420Ω resistor placed from IREF to ground sets the reference current. Refer to Figure 6-4 for a sample interconnection.

Configuring the Analog RGB Interface

The following registers configure parameters for the Analog RGB interface:

- System Control register (MMIO_base + `0x000000`)
- CRT Display Control register (MMIO_base + `0x080200`)
- Power Mode 0 Clock register (MMIO_base + `0x000044`) or Power Mode 1 Clock register (MMIO_base + `0x00004C`)
- CRT Horizontal Total (MMIO_base + `0x08020C`)

- CRT Horizontal Sync (MMIO_base + `0x080210`)
- CRT Vertical Total (MMIO_base + `0x080214`)
- CRT Vertical Sync (MMIO_base + `0x080218`)
- CRT Signature Analyzer (MMIO_base + `0x08021C`)
- CRT Monitor Detect (MMIO_base + `0x080224`)
- Raw Interrupt Clear register (MMIO_base + `0x000028`)
- Interrupt Status register (MMIO_base + `0x00002C`)
- Interrupt Mask register (MMIO_base + `0x000030`)

Refer to the *SM501 MSOC Databook* for complete details on these and other CRT registers.

CRT Signal Configurations

Polarities

The active edges of the CRT_HSYNC and CRT_VSYNC pulses can be configured as high or low, depending on the settings of bits 12 and 13 in the CRT Display Control register, respectively.

Enables

When bit 2 of the System Control register is cleared, the CRT interface is enabled.

Bit 8 of the CRT Display Control register enables the CRT timing. When the CRT is in power-saving mode, the timing from the SM501 must be disabled. In the power-saving sequence, this bit is cleared to disable the CRT timing.

Horizontal and Vertical Parameters

As stated in the subsection above, the polarity of the horizontal and vertical sync outputs is programmable. In addition, the following parameters need to be known for proper display (refer to Figure 6-1 and Figure 6-2 for the placement of these parameters):

- Horizontal Sync Width

  Width of the CRT_HSYNC pulse in pixels. Each pixel is equivalent to one pixel clock.
- Horizontal Display End

  Number of pixels – 1 to the end of the visible row.
- Horizontal Sync Start

  Start of the active edge of the CRT_HSYNC pulse in pixels – 1.
- Total Horizontal Width

  Total number of pixels – 1 in a horizontal line (including all displayable and non-displayable areas).
- Vertical Sync Height

  Height of the CRT_VSYNC pulse in lines. Each line is equivalent to one horizontal width.
- Vertical Sync Start

  Start of the active edge of the CRT_VSYNC pulse in lines – 1.
- Vertical Display End

  Number of lines – 1 to the end of the visible display.
- Total Vertical Height

  Total number of lines – 1 in a screen (including all displayable and non-displayable areas).

Figure 6-1: CRT Horizontal Parameters

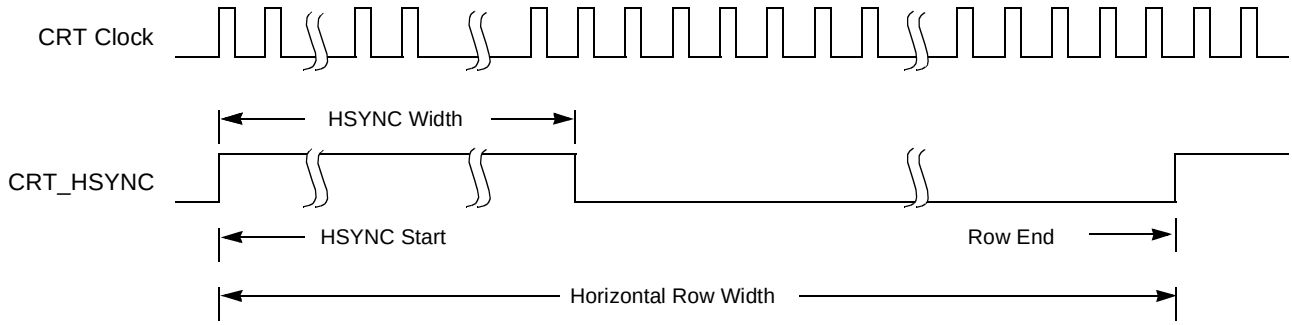
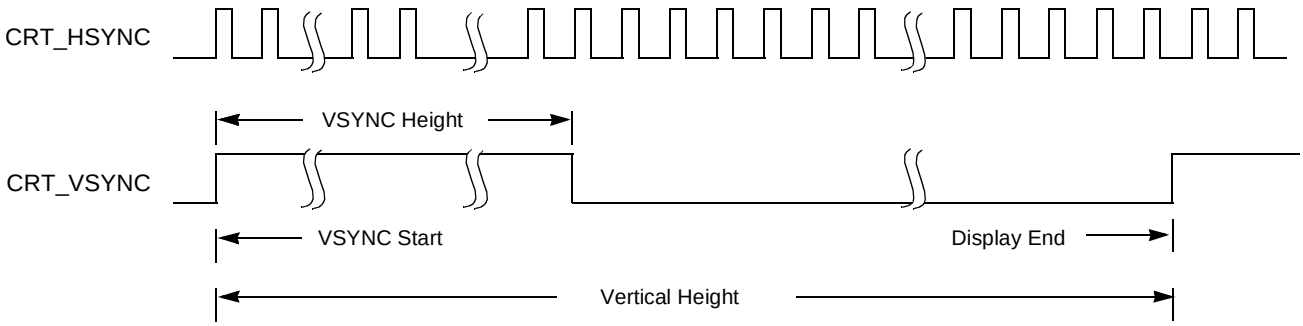


Figure 6-2: CRT Vertical Parameters



Signature Analyzer

When the signature analyzer is enabled, the SM501 checks the video data for the correct data, which is specified in bits [31:16] of the CRT Signature Analyzer register. The red, green, and blue data streams can be checked individually.

Monitor Detect

When Monitor Detect is enabled, the SM501 reads back RGB 8:8:8 data and determines whether the monitor is on or not based on the voltage levels of the data.

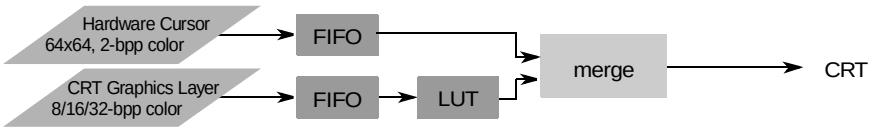
Gamma Control

Gamma control can be enabled only in RGB 5:6:5 and RGB 8:8:8 modes. Because the display device or data source has nonlinear signal-to-light intensities or intensity-to-signal characteristics, the gamma control feature compensates for this nonlinearity.

Video Layers

Figure 6-3 shows the two video layers that make up a CRT display. Each layer has its own FIFO. The layers are merged together into a frame buffer, which is displayed on the CRT.

Figure 6-3: Analog RGB Video Layers and Data Processing



The two layers shown in Figure 6-3 are described in more detail below:

CRT Graphics Layer

Bit 2 in the CRT Display Control register enables the CRT graphics layer. This layer displays text or drawings on the analog output for multi-monitor functions. The pixel colors in this layer are formatted as one of the following (as determined by bits [1:0] of the CRT Display Control register):

- 8-bpp (index into RGB 8:8:8 lookup table)
- 16-bpp RGB 5:6:5
- 32-bpp RGB 8:8:8

Hardware Cursor Layer

This layer displays a cursor on the digital output. One single 64x64 pixel cursor with 2-bpp color (00 = transparent, 01 = color 0, 10 = color 1, 11 = color 2) is mapped into a 32-bit RGB 8:8:8 color map. The hardware cursor address is in the CRT HWC Address register. The cursor's screen location is in the CRT HWC Location register. The colors are defined in the CRT HWC Color 1 & 2 register and the CRT HWC Color 3 register.

Interrupt Handling

The SM501 can be programmed to recognize CRT Vertical Sync interrupts by enabling bit 11 in the Interrupt Mask register. Bit 3 of the Interrupt Status register is set to one when an active edge of CRT_VSYNC is encountered. Bit 3 of the Raw Interrupt Clear register must be cleared to clear the interrupt condition.

Analog RGB Interconnections

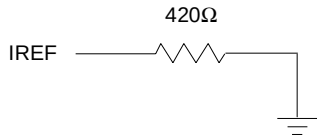
The following Analog RGB interconnections are shown in this section:

- "IREF Interconnection"
- "HSYNC and VSYNC Interconnections"
- "RGB Interconnections"
- "CRT Connector"

IREF Interconnection

The IREF input requires a 420 Ω resistor to ground in order to generate the input reference current (see Figure 6-4).

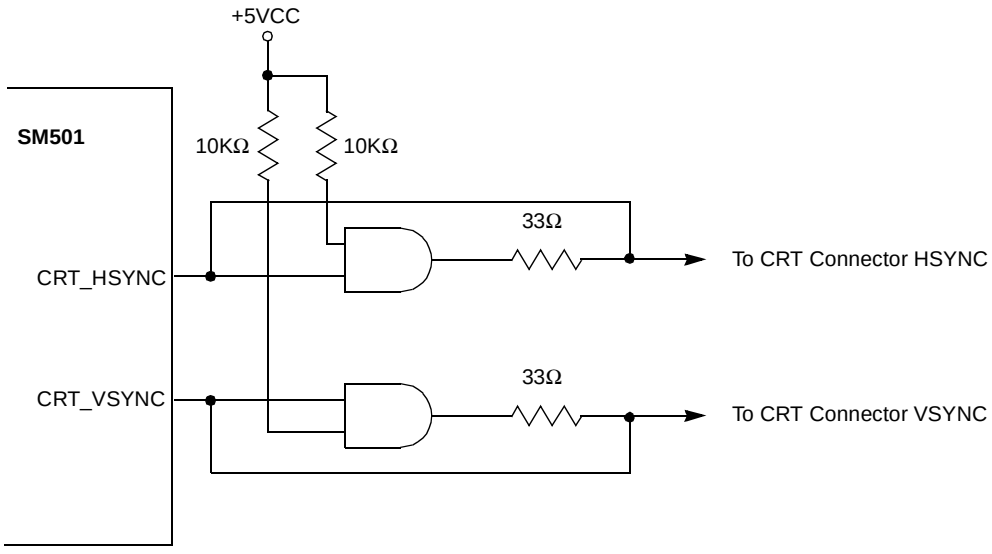
Figure 6-4: IREF Interconnect



HSYNC and VSYNC Interconnections

Figure 6-5 shows a sample diagram of the interconnections between the SM501 CRT Sync pins to the CRT connector.

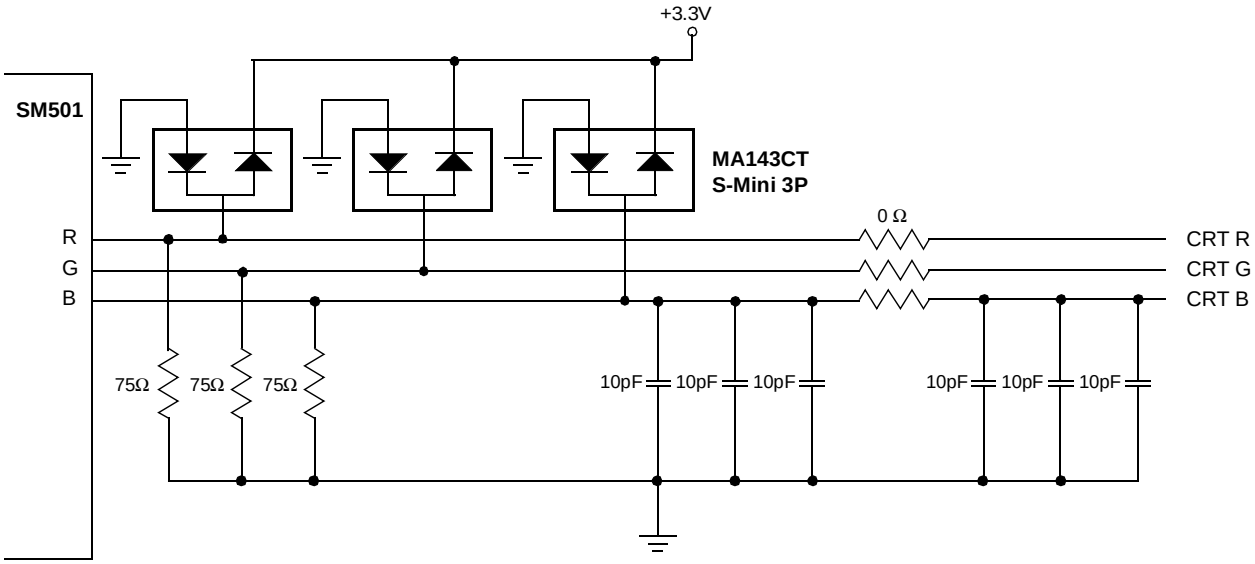
Figure 6-5: CRT Sync Interconnections



RGB Interconnections

Figure 6-6 shows a sample interconnection from the RGB signals to the CRT connector.

Figure 6-6: RGB Interconnections



CRT Connector

Table 6-2 provides a sample pinout for a DB15 CRT connector.

Table 6-2: CRT Connector Pinout

Connector Pin Number	Pin Name	Pin Function	Connector Pin Number	Pin Name	Pin Function
1	R	Red Video. Connect as shown in Figure 6-6.	9	No Connect	Nothing connects here.
2	G	Green Video. Connect as shown in Figure 6-6.	10	GND	Logic Ground. Tie to ground.
3	B	Blue Video. Connect as shown in Figure 6-6.	11	ID output	Typically connected to GND.
4	ID output	Typically connected to GND.	12	SDA	I^2C Serial Data. Connect as shown in Figure 8-4.
5	GND	Tie to ground.	13	HSYNC	Horizontal Sync. Connect as shown in Figure 6-5.
6	GND	Red Ground. Tie to ground.	14	VSYNC	Vertical Sync. Connect as shown in Figure 6-5.
7	GND	Green Ground. Tie to ground.	15	SCL	I^2C Serial Clock. Connect as shown in Figure 8-4.
8	GND	Blue Ground. Tie to ground.			

Analog RGB Design Considerations

Note the following design considerations when using the Analog RGB interface:

- Place the pull-down resistor connected to the IREF pin as closely as possible to the package ball.
- All 75 Ω termination resistors should be placed as closely as possible to their respective R, G, and B package balls.
- All capacitors should be placed as closely as possible to the CRT connector rail pins.
- To protect against voltage spikes or power surges from the CRT, connect the R, G, and B outputs to plus and minus protect diodes (refer to Figure 6-6 on page 6-6 for a sample interconnection).

7 ZV Port

The SM501 Zoom Video Port (ZV Port) can interface with video decoders, such as NTSC/PAL decoders, MPEG-2 decoders, and JPEG codecs. The ZV Port supports resolutions up to 1280x1024. It directly accepts digitized RGB or YUV signals, and does not accept analog signals.

This chapter describes in detail the signals that comprise the ZV Port and how to configure it. Sample interconnects with the Sigma EM8470 MPEG-4 Decoder and the Philips SAA7118E Multistandard Video Decoder are included. Sample test procedures are provided for use in validating operation of the ZV Port.

This chapter contains the following sections:

- "ZV Port Signals" on page 1
- "Configuring the ZV Port" on page 3
- "Connecting to the SM501 ZV Port" on page 8
- "ZV Port Validation" on page 10

ZV Port Signals

Table 7-1 defines the operation of each ZV Port pin. This table also lists the alternate names for the pins that share functionalities.

Note: In 16-bit mode, the ZV[15:8] signals are the most-significant eight video pixel inputs. In 8-bit mode, these signals are not used.

In 16-bit mode, the ZV[7:0] signals are the least-significant eight video pixel inputs. In 8-bit mode, these signals are the only eight video pixel inputs.

In order for the ZV[15:0] signals to function as ZV Port inputs, their corresponding bits in the $GPIO_{63:32}$ or $GPIO_{31:0}$ Control register must be set to 1.

Table 7-1: ZV Port Signal Descriptions

ZV Port Pin Name	I/O	Pin Number	Shared Pin	Register Bit	Description
ZV15	I	AA21	GPIO63	$GPIO_{63:32}$ Control, bit 31	16-bit R[4] video pixel input for RGB 5:6:5 mode or Y[7] video pixel input for YUV 4:2:2 mode.
ZV14	I	AA20	GPIO62	$GPIO_{63:32}$ Control, bit 30	16-bit R[3] video pixel input for RGB 5:6:5 mode or Y[6] video pixel input for YUV 4:2:2 mode.
ZV13	I	AA19	GPIO61	$GPIO_{63:32}$ Control, bit 29	16-bit R[2] video pixel input for RGB 5:6:5 mode or Y[5] video pixel input for YUV 4:2:2 mode.
ZV12	I	Y21	GPIO60	$GPIO_{63:32}$ Control, bit 28	16-bit R[1] video pixel input for RGB 5:6:5 mode or Y[4] video pixel input for YUV 4:2:2 mode.

Table 7-1: ZV Port Signal Descriptions (Continued)

ZV Port Pin Name	I/O	Pin Number	Shared Pin	Register Bit	Description
ZV11	I	Y20	GPIO59	$GPIO_{63:32}$ Control, bit 27	16-bit R[0] video pixel input for RGB 5:6:5 mode or Y[3] video pixel input for YUV 4:2:2 mode.
ZV10	I	Y19	GPIO58	$GPIO_{63:32}$ Control, bit 26	16-bit G[5] video pixel input for RGB 5:6:5 mode or Y[2] video pixel input for YUV 4:2:2 mode.
ZV9	I	Y18	GPIO57	$GPIO_{63:32}$ Control, bit 25	16-bit G[4] video pixel input for RGB 5:6:5 mode or Y[1] video pixel input for YUV 4:2:2 mode.
ZV8	I	Y17	GPIO56	$GPIO_{63:32}$ Control, bit 24	16-bit G[3] video pixel input for RGB 5:6:5 mode or Y[0] video pixel input for YUV 4:2:2 mode.
ZV7	I	L21	GPIO23	$GPIO_{31:0}$ Control, bit 23	16-bit G[2] video pixel input for RGB 5:6:5 mode, U[7] video pixel input for YUV 4:2:2 mode, or V[7] video pixel input for YUV 4:2:2 mode.
ZV6	I	L20	GPIO22	$GPIO_{31:0}$ Control, bit 22	16-bit G[1] video pixel input for RGB 5:6:5 mode, U[6] video pixel input for YUV 4:2:2 mode, or V[6] video pixel input for YUV 4:2:2 mode.
ZV5	I	L19	GPIO21	$GPIO_{31:0}$ Control, bit 21	16-bit G[0] video pixel input for RGB 5:6:5 mode, U[5] video pixel input for YUV 4:2:2 mode, or V[5] video pixel input for YUV 4:2:2 mode.
ZV4	I	L18	GPIO20	$GPIO_{31:0}$ Control, bit 20	16-bit B[4] video pixel input for RGB 5:6:5 mode, U[4] video pixel input for YUV 4:2:2 mode, or V[4] video pixel input for YUV 4:2:2 mode.
ZV3	I	K21	GPIO19	$GPIO_{31:0}$ Control, bit 19	16-bit B[3] video pixel input for RGB 5:6:5 mode, U[3] video pixel input for YUV 4:2:2 mode, or V[3] video pixel input for YUV 4:2:2 mode.
ZV2	I	K20	GPIO18	$GPIO_{31:0}$ Control, bit 18	16-bit B[2] video pixel input for RGB 5:6:5 mode, U[2] video pixel input for YUV 4:2:2 mode, or V[2] video pixel input for YUV 4:2:2 mode.
ZV1	I	K19	GPIO17	$GPIO_{31:0}$ Control, bit 17	16-bit B[1] video pixel input for RGB 5:6:5 mode, U[1] video pixel input for YUV 4:2:2 mode, or V[1] video pixel input for YUV 4:2:2 mode.
ZV0	I	J21	GPIO16	$GPIO_{31:0}$ Control, bit 16	16-bit B[0] video pixel input for RGB 5:6:5 mode, U[0] video pixel input for YUV 4:2:2 mode, or V[0] video pixel input for YUV 4:2:2 mode.

Table 7-1: ZV Port Signal Descriptions (Continued)

ZV Port Pin Name	I/O	Pin Number	Shared Pin	Register Bit	Description
VP_CLK	I	AA10	–	–	Pixel Clock. VP_CLK is the reference clock for data on the ZV[31:0] video pixel bus. The clock edge on which data is captured is programmable (see "Configuring the ZV Port" below).
VP_HREF	I	Y11	–	–	Horizontal Sync. A falling or rising edge on this input indicates the end of the current scan line and the beginning of the next. The active edge is programmable (see "Configuring the ZV Port" below).
VP_VSYNC	I	W11	–	–	Vertical Sync. A rising or falling edge on this input indicates the end of the current capture field and the beginning of the next one. The active edge is programmable (see "Configuring the ZV Port" below). The state of HSYNC determines whether the current capture field is ODD (VP_HREF is High on the active edge of VP_VSYNC) or EVEN (VP_HREF is Low on the active edge of VP_VSYNC).

Configuring the ZV Port

The Capture Control register (MMIO_base + `0x090000`) determines various operating conditions of the ZV Port (see Table 7-2). Refer to the Capture Control register description in the *SM501 MSOC Databook* for complete details.

Table 7-2: Summary of Selected Capture Control Register Bits

Programmable Parameter	Capture Control Register Bit	Description
Video Capture Enable	Bit 0	This bit enables (1) or disables (0) video capturing.
Capture Control Select	Bit 3	This bit determines whether video capture is continuous (0) or conditional (1).
Double Buffering Enable	Bit 4	This bit enables (1) or disables (0) double buffering.
Bob Interlaced Data Capturing Enable	Bit 5	This bit enables (1) or disables (0) Bob interlaced data capturing.
Weave Interlaced Data Capturing Enable	Bit 6	This bit enables (1) or disables (0) Weave interlaced data capturing.
Field Swap Enable	Bit 7	This bit enables (1) or disables (0) field swapping.
Capture Data Format	Bit 8	The capture data format is programmable as either RGB (1) or YUV (0).

Table 7-2: Summary of Selected Capture Control Register Bits (Continued)

Programmable Parameter	Capture Control Register Bit	Description
8-bit or 16-bit Video Capture Mode	Bit 9	The ZV Port can be configured to operate in either 8-bit (1) or 16-bit (0) capture mode.
Byte Swap Enable	Bit 10	This bit enables (1) or disables (0) byte swapping.
UV Swap Enable	Bit 11	This bit enables (1) or disables (0) UV swapping.
VP_CLK Input Clock Polarity	Bit 12	The polarity of VP_CLK is programmable as either active High (0) or active Low (1).
VP_HREF Polarity	Bit 13	The VP_HREF polarity is programmable as either active High (0) or active Low (1).
VP_VSYNC Polarity	Bit 14	The VP_VSYNC polarity is programmable as either active High (0) or active Low (1).
VP_VSYNC Active Edge	Bit 15	Either the rising edge (0) or falling edge (1) of VP_VSYNC determines a field change.
Vertical Shrinking Enable	Bit 16	This bit enables (1) or disables (0) vertical shrinking.
Horizontal Shrinking Enable	Bit 17	This bit enables (1) or disables (0) horizontal shrinking.
Horizontal Averaging Enable	Bit 18	This bit enables (1) or disables (0) horizontal averaging.

Video Capture Enable

Video capture is enabled when bit 0 of the Capture Control register (MMIO_base + `0x090000`) is set and the appropriate ZV Port data bits are enabled in the $GPIO_{63:32}$ Control (MMIO_base + 0x00000C) and $GPIO_{31:0}$ Control (MMIO_base + 0x000008) registers.

Video capture is either continuous or conditional, depending on the setting of bit 3 in the Capture Control register.

The capture size is specified in the Capture Size register (MMIO_base + `0x090008`). Bits [26:16] determine the number of lines to capture. Bits [10:0] determine the number of pixels to capture.

Video Capture Mode

The standard ZV Port uses an 8-bit interface at 50 MHz. The eight-bit video input data is located on ZV[7:0]. Eight additional bits from in the GPIO interface (ZV[15:8]) can be appended to provide a 16-bit ZV interface at up to 65 MHz. Bit 9 in the Capture Control register determines whether the data bus for the ZV Port is 8 bits wide (1) or 16 bits wide (0).

Video Capture Data Format

Bit 8 of the Capture Control register determines whether the captured data is in RGB (1) or YUV (0) format. The ZV Port supports the following data formats:

- YUV 4:2:2
- YUV 4:2:2 with byte swapping
- RGB 5:6:5

Interlaced or Non-Interlaced Operation

The ZV Port performs Non-Interlaced operation when bits 6 and 5 of the Capture Control register are both cleared. The ZV Port performs Interlaced operation when either bit 6 or bit 5 is set (refer to “Interlaced Data Capturing” for more information on the two types of interlacing.

Interlaced Data Capturing

There are two methods of capturing interlaced data: Weave and Bob.

Weave interlaced data capturing is enabled when bit 6 of the Capture Control register is set to one. In Weave mode, scan lines from both even and odd fields are stored in the same frame buffer.

Bob interlaced data capturing is enabled when bit 5 of the Capture Control register is set to one. In Bob mode, the even and odd fields are stored in separate frame buffers.

Note: Weave and Bob interlacing cannot be enabled at the same time.

Video Capture Buffers and Addressing

The SM501 can perform either single or double frame buffer capture. Bit 4 in the Capture Control register determines whether single (0) or double (1) buffering is enabled. Double buffering provides access to two buffers, Buffer 0 and Buffer 1. Single buffering provides access to one buffer, Buffer 0. Bit 25 in the Capture Control register indicates whether the SM501 is capturing data in Buffer 0 (0) or Buffer 1 (1).

Bit 27 in the Capture Buffer 0 Address register (MMIO_base = `0x09000C`) and Capture Buffer 1 Address register (MMIO_base + `0x090010`) indicates whether the respective buffer is in local memory (0) or external memory (1). Selection of local memory stores video data in the on-chip Video Capture FIFO.

The Capture Buffer 0/1 Address registers also contain the memory address for the respective buffer. The lower four bits of each capture buffer’s address are hardwired to zeros, providing 128-bit alignment. Bit 26 in these registers also controls which buffer’s chip select is used for external memory, CS0 or CS1.

The Capture Buffer Offset register (MMIO_base + `0x090014`) determines how many 128-bit aligned bytes there are per line in the capture buffer(s).

The Capture FIFO Control register (MMIO_base + `0x090018`) is used when one of the capture buffers is configured as local memory. Bits [2:0] in this register control the FIFO request level. The value of these bits determines when the SM501 will generate a FIFO read request based on how empty the FIFO is.

Bit 31, the S bit, in the Capture Buffer 0/1 Address registers has two functions, depending on whether or not the respective buffer is active. For the active buffer, bit 31 indicates if that buffer is capturing data (1) or not (0). For the inactive buffer, bit 31 indicates that video capture for that buffer is currently disabled (0).

Clipping

The amount of data that is captured can be reduced by clipping a specified number of pixels after VP_HREF and/or a specified number of lines after VP_VSYNC.

The Capture Clipping register (MMIO_base + `0x090004`) controls the horizontal and vertical clipping. Bits [25:16] determine the number of lines to skip after the active edge of VP_VSYNC. Bits [15:10] determine the number of pixels to skip after the active edge of VP_HREF.

Horizontal Averaging

Bit 18 in the Capture Control register is the enable for horizontal averaging. This function is used when the frame buffer horizontal size does not match the display width. When this function is enabled, <the SM501 performs averaging of adjacent pixels.

Vertical and Horizontal Shrinking

The ZV Port supports vertical and horizontal shrinking each with a video scale factor of 2:1, but does not support scaling up. The video display interface supports 4:1 shrinking and 1:8 scaling.

Bits 17 and 16 in the Capture Control register are enables for vertical and horizontal shrinking, respectively. When either bit is enabled, 2:1 horizontal or vertical shrinking of the video data occurs. The captured data is scaled down. Note that the ZV Port does not scale up captured data.

Byte, Field, and UV Swapping

Byte swapping is enabled when bit 10 of the Capture Control register is set to one. When this mode is enabled, ZV[7:0] and ZV[15:8] bytes on the video bus are swapped.

Field swapping is enabled when bit 7 of the Capture Control register is set to one. When this mode is enabled, the ODD and EVEN fields are switched.

UV swapping is enabled when bit 11 of the Capture Control register is set to one. When this mode is enabled, the U and V chrominance values are swapped.

Vertical and Horizontal Timings

This section describes the operation of the VP_VSYNC and VP_HREF signals. The active edges (phases) of these two signals are programmable as well as which edge of VP_VSYNC determines a field change.

Vertical Timing

The active edge of VP_VSYNC (determined by bit 15 of the Capture Control register) indicates when one frame ends and the next one begins. The following events occur on this edge:

- The state of VP_HREF determines whether the next field is even or odd.
- The capture line counter is reset to 0.
- The appropriate Capture Buffer 0/1 Address register is loaded with the starting address of either Capture Buffer 0 or Capture Buffer 1, depending on which one is active.

If video capture is enabled, the SM501 counts scan lines until it reaches the specified number of lines to skip in bits [25:16] of the Capture Clipping register, if any. At this point, normal video capture starts and continues until the active edge of VP_VSYNC occurs or until the number of scan lines is equal to the value specified in

bits [26:16] of the Capture Size register. Lines that are skipped due to shrinking are not counted. The only lines that are counted are those whose pixels are stored.

Horizontal Timing

The active edge of VP_HREF (determined by bit 13 of the Capture Control register) indicates the end of a scan line. The following events occur on this edge:

- The Capture FIFO is flushed. Any data from the previous scan line is written into the frame buffer. This step takes several microseconds.
- On the first VP_CLK once video is active, the start address of the new line is loaded with the sum of either the Capture Buffer Offset from MMIO_base + `0x090014` or two times this value if interlacing is enabled added to the previous Capture Buffer address.

When video is active (as determined by the state of VP_HREF), the SM501 counts the number of pixels (VP_CLKs) until reaching the number of pixels to skip after VP_HREF, which are specified in bits [9:0] of the Capture Clipping register. This operation is called left-edge clipping. At this point, pixels are captured with horizontal data reduction until the next active VP_HREF edge or until the number of pixels is equal to the value specified in bits [10:0] of the Capture Size register.

Connecting to the SM501 ZV Port

This section shows how to connect the SM501 ZV Port to two decoders. It contains the following subsections:

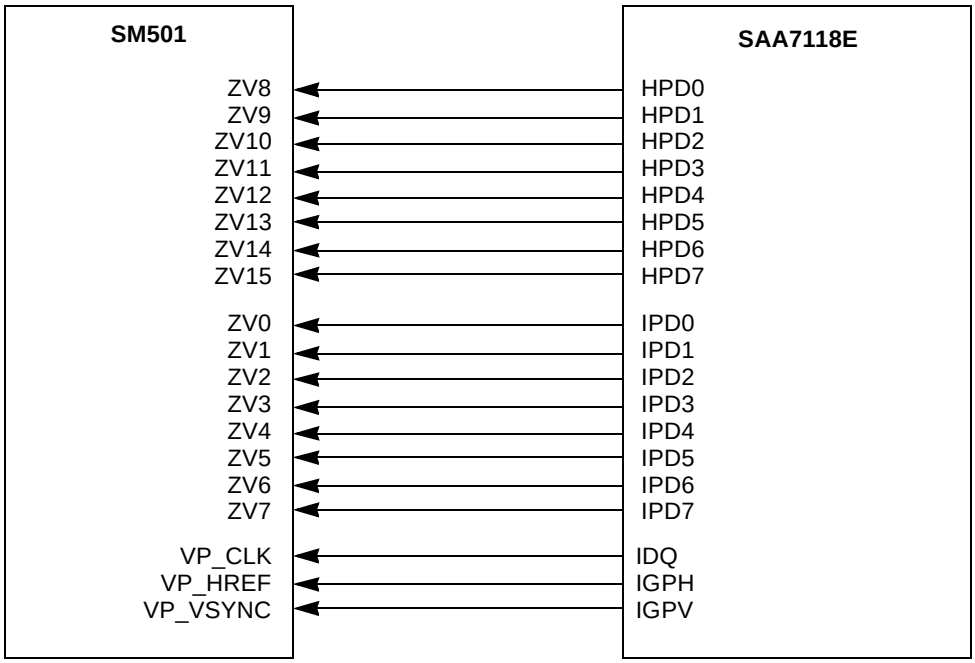
- "Interconnection to Philips SAA7118E Video Decoder"
- "Interconnection to Sigma EM8470 MPEG-4 Decoder"

Note that the SM501 ZV Port can tolerate both 3.3V and 5V decoders.

Interconnection to Philips SAA7118E Video Decoder

Figure 7-1 illustrates an example of a 16-bit interface between the Philips SAA7118 video encoder and the ZV Port.

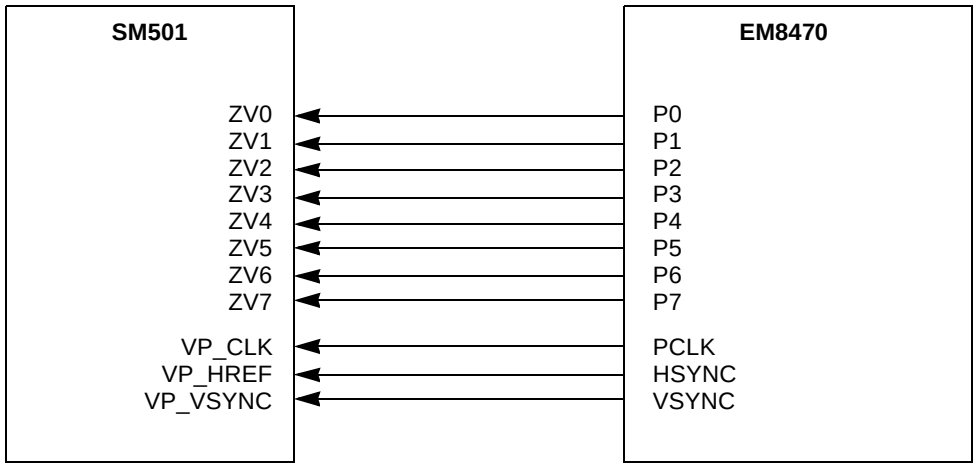
Figure 7-1: 16-bit Interface between the SM501 ZV Port and SAA7118E



Interconnection to Sigma EM8470 MPEG-4 Decoder

Figure 7-2 shows a sample 8-bit interconnection between the SM501 ZV Port and the Sigma Designs EM8470 MPEG-4 Decoder.

Figure 7-2: Interface between the SM501 ZV Port and the EM8470



ZV Port Validation

This section provides three test cases that can be used to validate your ZV Port configuration. It contains the following subsections:

- "Test Environment"
- "Modifications of Sigma Design Registry in Platform.reg"
- "Test Case Details"

Test Environment

Table 7-3 lists the environment on which the test cases were run.

Table 7-3: Validation Test Environment

Parameter	Configuration
Development Workstation	Platform Builder 4.0
Target System	Intel PII system with 64MB RAM
VGA	SM501 MSOC device, Rev. A
Decoder	• Sigma Design EM8470 PCI board with 16-bit output port modification • Sigma Design EM8470 PCI board with 8-bit output port
Drivers	• SM501 CE driver release version Alpha1 dated 2/28/2003 for the x86 platform • Sigma Design driver release version 1.0.12.19 for the x86 platform
Utilities	• SM501 Video Port demo utility (`VGXVPE.exe`) version 20030224 for the x86 platform • SM501 Register Dump utility (`Smutilce.exe`) version 20030214 for the x86 platform **Note:** These two utilities must be copied into the `\Release` directory so they can be run on the Development Workstation.
Video Clip	`Toronto.mpg`

Modifications of Sigma Design Registry in Platform.reg

The `Platform.reg` file contains the registry information for the Sigma Design device. Select either the 16-bit or 8-bit code listed below, depending on which video capture mode is selected.

For 16-bit Video Capture Mode

```
;#########################################################################
;# 16bitsVMI;     - 0 for 8bits, 1 for 16 bits
;# Default :
"16bitsVMI" = dword:00000001
;#########################################################################
;# SyncEnable
;# - 2: VSync enabled, HSync disabled, VVLD/HS=HS enabled,
;# - 1: VSync enabled, HSync enabled, VVLD/HS=VVLD enabled,
;# - 0: VSync, HSync, VVLD/HS=VVLD disabled.
;# Default :
;#"SyncEnable" = dword:00000000
"SyncEnable" = dword:00000001
;#########################################################################
```

For 8-bit Video Capture Mode

```
;#########################################################################
;# 16bitsVMI;     - 0 for 8bits, 1 for 16 bits
;# Default :
"16bitsVMI" = dword:00000000
;#########################################################################
;# SyncEnable
;# - 2: VSync enabled, HSync disabled, VVLD/HS=HS enabled,
;# - 1: VSync enabled, HSync enabled, VVLD/HS=VVLD enabled,
;# - 0: VSync, HSync, VVLD/HS=VVLD disabled.
;# Default :
;#"SyncEnable" = dword:00000000
"SyncEnable" = dword:00000001
;#########################################################################
```

Test Case Details

Table 7-4 summarizes the test cases used to validate three different ZV Port configurations. The conditions and procedures for each test case are described in detail following the table.

Table 7-4: Test Cases

Test Case	Data Input	Frequency	Video Output to SM501	Video Capture by SM501
1	YUV 4:2:2	27 MHz	16 bits	16 bits
2	YUV 4:2:2	27 MHz	16 bits	16 bits (8 bits at a time)
3	YUV 4:2:2	27 MHz	8 bits	16 bits (8 bits at a time)

Test Case #1

The test conditions for Test Case #1 are as follows:

- The 16-bit source data to the SM501 16-bit ZV Port is from Sigma Design's 16-bit output port via a 16-bit mapping cable.
- Both PCI cards are inserted into the PCI slots.
- The Sigma Design device is programmed to output 16-bit data, and the SM501 device is programmed to capture 16-bit input from the `NK.bin` image.

Follow these steps to perform the validation for Test Case #1:

1. Open MediaPlayer and play the `Toronto.mpg` file.
2. Open `VGXVPE.exe` to show the video via the ZV Port input.
3. The MPEG-1 video clip is normal.

Test Case #2

The test conditions for Test Case #2 are as follows:

- The 16-bit source data to the SM501 16-bit ZV Port is from Sigma Design's 16-bit output port via a 16-bit mapping cable.
- Both PCI cards are inserted into the PCI slots.
- The Sigma Design device is programmed to output 16-bit data, and the SM501 device is programmed to capture 16-bit input from the `NK.bin` image.

Follow these steps to perform the validation for Test Case #2:

1. Open MediaPlayer and play the `Toronto.mpg` file.
2. Open `VGXVPE.exe` to show the video via ZV Port input. The MPEG-1 video clip is playing normally.
3. Read the SM501 Capture Control Register using the `Smutilce.exe` utility on the Development Workstation. The command is:

```
Windows CE>s smutilce r o 90000 1
```

The read back value is:

```
0x0400E431
```

Which indicates a capture size of 16 bits for YUV mode.

4. Using the `Smutilce.exe` utility, set bit 9 of the Capture Control register to 1 and set Bits[11:10, 8] to 0 to configure an 8-bit capture size for YUV mode. The command is:

```
Windows CE>s smutilce w o 90000 0400E231
```

5. The video is shrunk and only displays on the left half of the screen with the wrong color. The right half of the screen does not have updated data, resulting in a frozen screen.

Test Case #3

The test conditions for Test Case #3 are as follows:

- The 8-bit source data to the SM501 8-bit ZV Port is from Sigma Design's 8-bit output port via an 8-bit mapping cable.
- Both PCI boards are inserted into the PCI slots.
- The Sigma Design EM8470 device is programmed to output 8-bit data, and the SM501 device is programmed to capture 16-bit input in this `NK.bin` image.

Follow these steps to perform the validation for Test Case #3:

1. Open MediaPlayer and play the `Toronto.mpg` file.
2. Open `VGXVPE.exe` to show the video via the ZV Port input. The MPEG-1 video clip image is not correct, displaying a green color only.
3. Read the SM501 Capture Control Register using the `Smutilce.exe` utility on the Development Workstation. The command is:

```
Windows CE>s smutilce r o 90000 1
```

The read back value is:

```
0x0400E431
```

Which indicates a capture size of 16 bits for YUV mode.

4. Using the `Smutilce.exe` utility, set bit 9 of the Capture Control Register to 1 and set Bits[11:10, 8] to 0 an 8-bit capture size for YUV mode. The command is:

```
Windows CE>s smutilce w o 90000 0400E231
```

5. The MPEG-1 clip video is playing normally.

8 I²C Interface

The I²C (Inter-IC) bus is a two-pin serial interface developed by Philips Electronics NV. The SM501 is a bus master on its I²C interface using 7-bit addressing. Data is transferred on the I²C bus through a buffered interface. A set of memory-mapped registers provides control and status information.

This chapter provides a detailed description of the signals that comprise the I²C interface, and describes how to configure it. Sample interconnects with the Philips SAA7118E Multistandard Video Decoder are included along with some design considerations.

This chapter contains the following sections:

- "I²C Signals"
- "Configuring the I²C Interface"
- "I²C Sample Interconnection"
- "I²C Design Considerations"

Refer to the I²C Bus Specification for complete information on the operation of the I²C bus.

I²C Signals

Table 8-1 defines the operation of the two I²C signals. This table also lists the alternate names for the shared functionalities.

Table 8-1: I²C Signal Descriptions

I²C Pin Name	I/O	Pin Number	Shared GPIO Pin	Register Bit	Description
I2CCK	I/O	V19	GPIO46	$GPIO_{63:32}$ Control, bit 14	This signal is the serial clock for the I²C bus. It has the same functionality as the SCL signal defined in the I²C specification. In order for this signal to function as a ZV Port input, the listed bit in the $GPIO_{63:32}$ register must be set to 1.
I2CDA	I/O	V20	GPIO47	$GPIO_{63:32}$ Control, bit 15	This signal is the serial I²C data bus. It has the same functionality as the SDA signal defined in the I²C specification. In order for this signal to function as a ZV Port input, the listed bit in the the $GPIO_{63:32}$ register must be set to 1.

Configuring the I²C Interface

The I²C Control register (MMIO_base + `0x010041`) configures the SM501 I²C operation (see Table 8-2). Refer to the I²C Control register description in the *SM501 MSOC Databook* for complete details.

Table 8-2: Configuration of Selected I²C Control Register Bits

Programmable Parameter	I²C Control Register Bit	Description
Controller Enable	Bit 0	This bit enables (1) or disables (0) the SM501 I²C Bus Master.
Bus Speed Mode	Bit 1	The I²C bus can be configured to operate in either Fast (1) or Standard (0) Mode.
Start/Stop Status	Bit 2	Stop (0) or Start (1). Once a Start condition occurs, this bit maintains a value of 1 until a Stop condition occurs.
Interrupt Enable	Bit 4	When this bit is enabled (1), the I²C Bus Master will recognize I²C bus errors.
Interrupt Acknowledge	Bit 5	The I²C Bus Master sets this bit to acknowledge an I²C interrupt.
Repeated Start Enable	Bit 6	This bit enables (1) or disables (0) repeated starts.

I²C Controller Enable

The I²C Controller is enabled when bit 0 of the I²C Control register and bits [15:14] of the $GPIO_{63:32}$ Control register are set to ones. In this case, the SM501 operates as a hardware I²C master.

If bits [15:14] are programmed to use GPIO46 and GPIO47 instead of I2CCK and I2CDA, then the SM501 operates as a software I²C master, and its I²C operation is transparent to the hardware. Bit 0 of the I²C Control register is cleared when the SM501 is a software I²C master.

Fast or Standard Mode

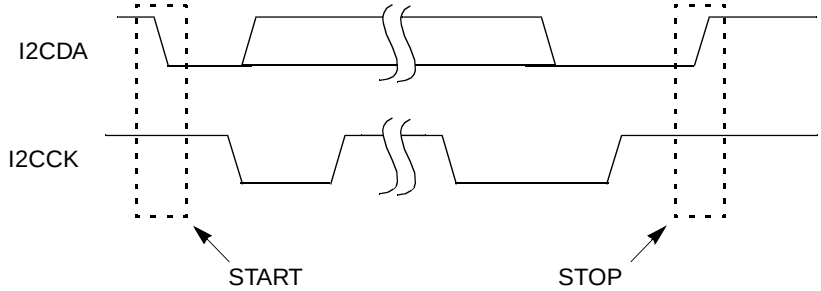
The SM501 I²C bus can be programmed to operate in either Fast Mode (400 Kbits/s) or Standard Mode (100 Kbits/s) as indicated by bit 1 in the I²C Control register.

Start, Stop, and Repeated Start Conditions

A *START* condition occurs when there is a High-to-Low transition on I2CDA when I2CCK is High. A *STOP* condition occurs when I2CDA goes from Low-to-High while I2CCK is High.

Figure 8-1 shows the START and STOP conditions.

Figure 8-1: START and STOP Conditions



After a START condition, the bus is considered to be busy. It will not be free again until a certain amount of time after the STOP condition occurs. An unlimited number of bytes can be transferred between START and STOP conditions.

When enabled by bit 6 in the I^2C Control register, a *repeated START* can be generated in place of a STOP. The SM501 I^2C Controller uses a repeated START to change the transfer direction or to address a different slave. The bus remains busy during a repeated START.

Address and Data Transfers

The SM501 I^2C Controller follows the 7-bit addressing protocol as defined in the I^2C Bus Specification, where the first byte after a START condition provides the slave address and the direction of transfer. Bits [7:0] of the I^2C Slave Address register (MMIO_base + `0x010043`) contain the 7-bit slave address. Bit 0 determines whether the I^2C Controller is performing a read (1) or a write (0).

The SM501 contains 16 8-bit I^2C Data registers that hold either data read from an I^2C slave or data to be written to an I^2C slave. These registers are located within the following address range: MMIO_base + `0x010044` through MMIO_base + `0x010053`.

Figure 8-3 shows the I^2C bus formats for write and read operations. A bus operation is initiated with a START condition followed by the 7-bit slave address and the direction of the operation (read or write). The data transfer begins after the slave acknowledges the operation. The slave generates an acknowledge after every byte of data in a write operation; the SM501 (master) generates an acknowledge after every byte of data in a read operation. The transfer completes with a STOP condition.

Figure 8-2: I^2C Bus Formats

Write Operation

Start	7-bit Slave Address	W	AckS	8-bit Data	AckS	Stop

transferred data = byte + slave acknowledge

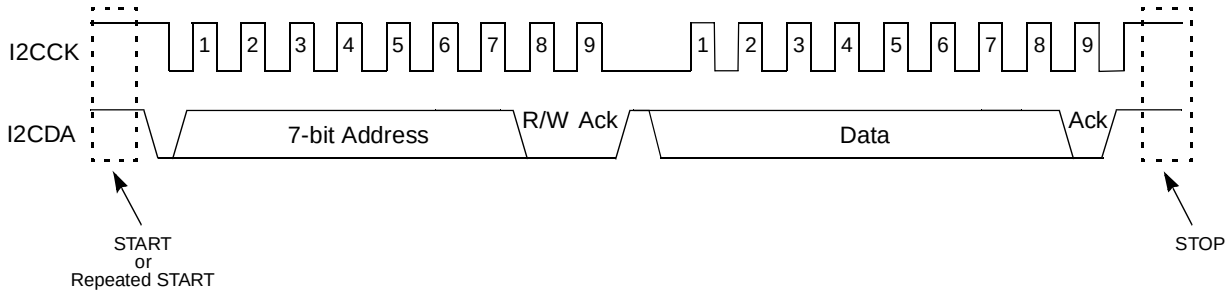
Read Operation

Start	7-bit Slave Address	R	AckS	8-bit Data	AckM	Stop

transferred data = byte + master acknowledge

Figure 8-3 shows the signals during an I^2C data transfer. The SM501 transfers one bit of data on I2CDA every time that I2CCK transitions High.

Figure 8-3: I²C Data Transfer



Byte Count

As an I²C Master, the SM501 manages all data operations; thus it needs to know how many bytes to transfer for each operation. Bits [3:0] of the I²C Byte Count register (MMIO_base + `0x010040`) contain the byte count minus one.

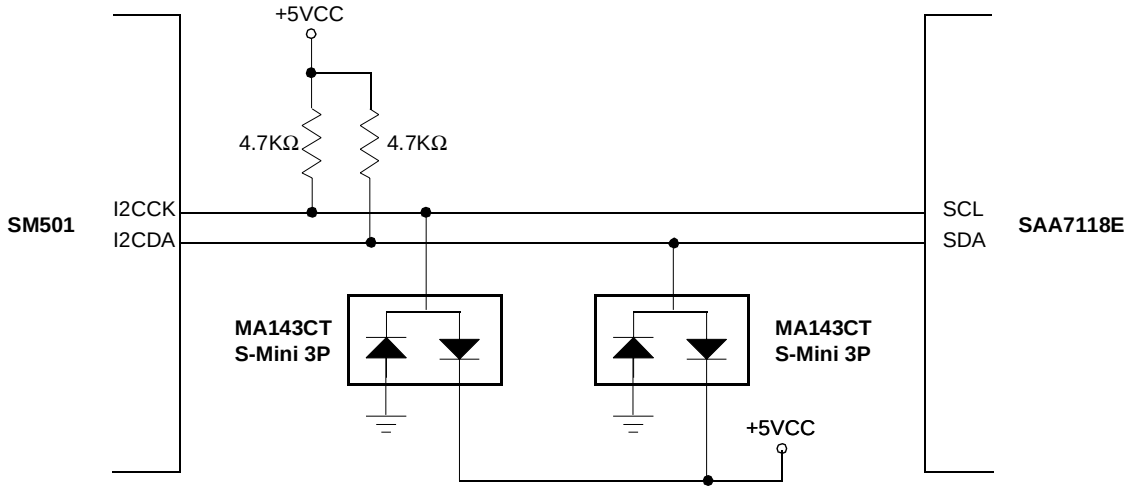
Interrupt Handling

The SM501 can be programmed to recognize I²C interrupts by enabling bit 4 in the I²C Control register. An I²C slave can signal an interrupt by driving active the INTR pin (pin D15). The interrupt status can be read in bit 23 of the Interrupt Status register (MMIO_base + `0x00002C`). The SM501 acknowledges receipt of an I²C interrupt by setting bit 5 of the I²C Control register to one. Once the interrupt condition has been resolved, bit 2 of the I²C Reset register must be cleared to clear the interrupt condition.

I²C Sample Interconnection

Figure 8-4 shows a sample diagram of the interconnections between the SM501 I2CCK and I2CDA pins to a Philips SAA7118E Multistandard Video Decoder.

Figure 8-4: I²C Bus Pin Interconnection



I²C Design Considerations

The SM501 I²C bus uses an open-drain, wired-AND bus configuration so that multiple devices can drive the bus and send status information (arbitration, errors, wait states, and so on). Because the SM501 supports Fast Mode, external pull-up devices must accommodate the shorter maximum permissible rise time for the Fast Mode bus.

The I²C Specification from Philips Electronics makes the following recommendations for pull-up devices based on the bus load:

- For bus loads up to 200 pF, the pull-up device for each bus line can be a resistor.
- For bus loads between 200 pF and 400 pF, the pull-up device can be either a current source (3 mA maximum) or a switched resistor circuit.

9 Power and Clocking

This chapter provides power and clocking information for the SM501 MSOC device. It contains the following sections:

- "Power Specifications"
- "Power-On Reset and Timing"
- "Power Modes"
- "Crystal Specifications"
- "PLL Specifications"
- "Internal Clock Sources"

Power Specifications

This section lists the power pins on the SM501 devices and provides power consumption information. It contains the following subsections:

- "Power Supply Connectivity"
- "Power Consumption Specifications"

Power Supply Connectivity

The SM501 MSOC device requires two or three external voltage levels (1.8V, 3.3V, and possibly 2.5V). Table 9-1 summarizes the different power inputs of the SM501 and lists their typical voltage levels.

Table 9-1: SM501 Power Supplies

Power Input	Typical Voltage Level
AVDD	3.3V
GVDD	3.3V
HVDD	3.3V
MVDD	2.5V / 3.3V
MVDD2	3.3V
PLLPWR	1.8V
PVDD	3.3V
USBPWR	3.3V
VDD	1.8V
XTALPWR	1.8V

Table 9-2 lists the SM501 pins with their associated power pins.

Table 9-2: Pin Power Supplies

SM501 Signal Name	Power Supply
ACK#	HVDD
B	AVDD
BA[1:0]	MVDD
BE[3:0]	HVDD
BIAS	PVDD
BREQ#	HVDD
BS#	HVDD
CA[25:2]	HVDD
CAS#	MVDD
CD[31:0]	HVDD
CKE	MVDD
CLKOFF	HVDD
CPURD#	HVDD
CRT_HSYNC	PVDD
CRT_VSYNC	PVDD
CS#	MVDD
DQM[3:0]	MVDD
DQS	MVDD
DSF	MVDD
FP_DISP	PVDD
FP_HSYNC	PVDD
FP_VSYNC	PVDD
FP[23:18]	PVDD
FP[15:10]	PVDD
FP[7:2]	PVDD
FPCLK	PVDD
FPEN	PVDD
G	AVDD
GPIO[63:0]	GVDD

Table 9-2: Pin Power Supplies (Continued)

SM501 Signal Name	Power Supply
HCAS#	HVDD
HCKE	HVDD
HCLK	HVDD
HCS#	HVDD
HRAS#	HVDD
HRDY#	HVDD
HWE#	HVDD
INTR	HVDD
IREF	AVDD
MA[12:0]	MVDD
MCS[1:0]#	HVDD
MD[31:0]	MVDD2
R	AVDD
RAS#	MVDD
RST#	HVDD
SCK-	MVDD
SCK+	MVDD
TEST0	GVDD
TEST1	GVDD
TESTCLK	HVDD
USB-	USBPWR
USB+	USBPWR
VDEN	PVDD
VP_CLK	GVDD
VP_HREF	GVDD
VP_VSYNC	GVDD
WE#	MVDD
XTALIN	XTALPWR
XTALOUT	XTALPWR

Power Consumption Specifications

The SM501 power consumption depends on the operating voltage, loading, and external switching activity. The power consumed varies depending on which functional blocks are in use and the requirements of data and frequency within the design.

The maximum power consumed is calculated as follows:

- All voltages are at their maximum allowable limits
- All functional blocks are operating at their maximum frequencies and sizes
- All external loads are at their maximum (50 pF for memory interface, 100 pF for the Host interface, and 100 pF for peripherals)

The specifications for typical power consumed are useful when determining battery size and optimizing regulator efficiency. The typical power consumed is calculated as follows:

- All voltages are at their typical values
- External loads are typical (35 pF for all pins except Host interface pins)

Table 9-3 summarizes the power consumption specifications for all SM501 power pins.

Table 9-3: Power Consumption Specifications

Symbol	Description	Min	Typ	Max	Units
P_{VDD}	Power from VDD Supply (Core 1.8V)	TBD	TBD	TBD	W
P_{AVDD}	Power from AVDD Supply (DAC 3.3V)	TBD	TBD	TBD	W
P_{GVDD}	Power from GVDD Supply (GPIO 3.3V)	TBD	TBD	TBD	W
P_{HVDD}	Power from HVDD Supply (Host/PCI 3.3V)	TBD	TBD	TBD	W
P_{MVDD}	Power from MVDD Supply (SDRAM Core 2.5V/3.3V)	TBD	TBD	TBD	W
P_{MVDD2}	Power from MVDD2 Supply (SDRAM I/O 3.3V)	TBD	TBD	TBD	W
P_{PLL}	Power from PLL Supply (PLL 1.8V)	TBD	TBD	TBD	W
P_{PVDD}	Power from PVDD Supply (LCD Panel 3.3V)	TBD	TBD	TBD	W
P_{USB}	Power from USB Supply (USB 3.3V)	TBD	TBD	TBD	W
P_{XTAL}	Power from XTAL Supply (Crystal 1.8V)	TBD	TBD	TBD	W

Power-On Reset and Timing

During power-on reset, the SM501 comes up in a predefined state with all I/Os turned off, running the lowest possible clock. Software is responsible for programming the Power Mode 0 state to the requested state after power-on and for transitioning into the Power Mode 0 state.

Figure 9-1 shows the power-on timing for the reset signal. Table 9-4 lists the power-on timing parameters.

Figure 9-1: Power-on Reset Timing

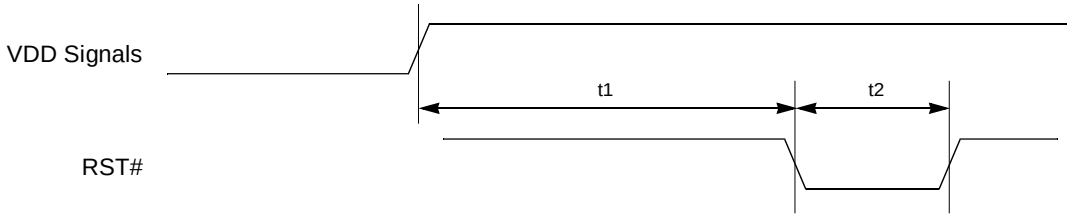


Table 9-4: Power-On Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t1	VDD stabilization time to RST# assertion	5			ms
t2	RST# assertion time	1			ms

Power Modes

There are two operational power modes (Power Mode 0 and Power Mode 1) and one Sleep Mode. Each operational power mode has its own Power Mode Gate register to control the clock gating for each functional block. Each operational power mode also has its own Power Mode Clock register that selects the different clock frequencies for each clock branch. In Sleep Mode, all clocks are shut down.

The power mode switch should be controlled by power management software; for example, Power Mode 0 can be programmed to a high clock rate for maximum performance. Power Mode 1 can be programmed to a lower clock rate for sustaining operation.

The Power Mode Control Register at MMIO_base + `0x000054` determines the power mode selection as follows:

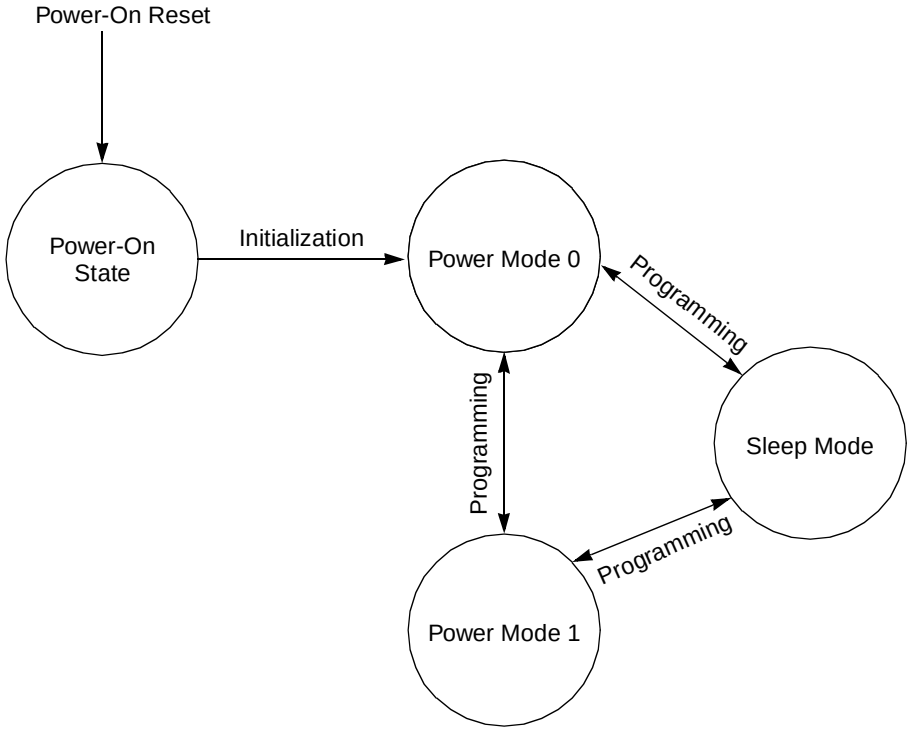
- Bits [1:0] = 00, Power Mode 0 (power on default)
- Bits [1:0] = 01, Power Mode 1
- Bits [1:0] = 10, Sleep Mode (the PLLs and the oscillator are shut down in this mode)
- Bits [1:0] = 11, Reserved

The Mode 0 and Mode 1 power states are the same and are fully under software control. Whenever software decides that the SM501 must change states, it sets up the registers for the non-active power state and then transitions into that state. This way there are an infinite number of power states supported by software, making power management very flexible.

The Sleep power state puts the SM501 into Sleep Mode. In this mode, SDRAM is put into self-refresh mode, and the crystal and PLL circuits are turned off. The GATE_HOST_CLK input pin is asserted by the system integrator to turn off the host clock inside the SM501 in order to reduce power consumption even further if the system integrator decides to do so.

Figure 9-2 shows a state diagram of the different power modes.

Figure 9-2: Power State Diagram



Note: The System Control registers are clocked in the Host clock domain; even shutting off the crystal and PLL circuits does not keep the System Control registers and the host bus from functioning. This way the software always can wake up the SM501 from Sleep Mode. In order to reduce power even more, use the GATE_HOST_CLK input pin for gating the host clock.

In Power Mode 0, the Power Mode 0 Clock Register at MMIO_base + `0x000044` controls the clock settings. The Power Mode 0 Gate Register at MMIO_base + `0x000040` controls clock gating.

In Power Mode 1, Power Mode 1 Clock Register at MMIO_base + `0x00004C` controls the clock settings. The Power Mode 1 Gate Register at MMIO_base + `0x000048` controls clock gating.

There are three ways to power down the SM501 chip (Sleep Mode):

1. For CPU local bus interface only:
   MMIO_base + `0x000068`, bit 6 = 0; disable PCI ACPI mode
   MMIO_base + `0x000054`, bits [1:0] = 10
   PCI Config register 44, bits [1:0] = xx (don't care)

2. For PCI bus interface only, without support PCI ACPI protocol (this method applies only to SM501 Rev C and later):
   MMIO_base + `0x000068`, bit 6 = 0; disable PCI ACPI mode
   MMIO_base + `0x000054` bits [1:0] = 10
   PCI Config register 44, bits [1:0] = xx (don't care)
3. For PCI bus interface only, with support of PCI ACPI protocol:
   MMIO_base + `0x000068`, bit 6 = 0; enable PCI ACPI mode
   MMIO_base + `0x000054`, bits [1:0] = xx (don't care)
   PCI Config register 44, bits [1:0] = 1x (ACPI power down mode)

Crystal Specifications

One external crystal connects to the SM501 MSOC device between the XTALIN and XTALOUT pins. Power for the crystal (1.8V) is supplied through the XTALPWR pin.

Allowable frequencies for the external crystal are 12 MHz and 24 MHz. Bit 24 of the Miscellaneous Control register (MMIO_base + `0x000004`) indicates the crystal frequency to the SM501. The 12-MHz crystal is used in applications where power-savings mode is implemented. When the crystal has a 12-MHz frequency, the SM501 internally doubles the frequency to 24 MHz.

PLL Specifications

The external crystal combined with the on-chip oscillator provides the SM501 clock source. The external crystal frequency is 24 MHz ± 5% when not implementing power savings; otherwise the frequency is 12 MHz ±5%.

The SM501 contains three clock multiply PLLs:

- PLL0

  Input frequency = 24 MHz oscillator
  Output frequency = Input frequency x 4 = 96 MHz fixed

- PLL1

  Input frequency = Output of PLL0 / 2 = 48 MHz
  Output frequency = Input frequency x 6 = 288 MHz fixed

- PLL2

  Input frequency = Output of PLL0 / 2 = 48 MHz
  The output frequency is controlled by the Miscellaneous Timing register, MMIO_base + `0x000068` as follows:

  Bits [5:4] = 00, the output of PLL2 = 48 MHz x 7 = 336 MHz, power on default
  Bits [5:4] = 01, the output of PLL2 = 48 MHz x 6 = 288 MHz
  Bits [5:4] = 10, the output of PLL2 = 48 MHz x 5 = 240 MHz
  Bits [5:4] = 11, the output of PLL2 = 48 MHz x 4 = 192 MHz

Internal Clock Sources

There are five clock branches that can be programmed through the Power Mode 0 Clock, Power Mode 1 Clock, and Miscellaneous Timing registers as indicated in Table 9-5.

Table 9-5: Programmable Clocks

Clock	Description
P2XCLK	2X clock source for the Panel interface timing. The actual rate at which the pixels are shifted out is P2XCLK divided by two.
V2XCLK	2X clock source for the CRT interface timing. The actual rate at which the pixels are shifted out is V2XCLK divided by two.
M2XCLK	Clock source for the local SDRAM controller.
MCLK	Main clock source for all functional blocks, such as the 2D engine, GPIO, Video Engine, DMA Engine.
SYSCLK[1]	Clock source for the system memory (CPU memory) controller. This clock also can be selected as the XScale CPU interface logic clock.

1. The definition of SYSCLK applies to the SM501, Rev C only. The M2XCLK signal on Rev A and B test chips is used to drive the system memory controller.

In the Miscellaneous Timing Register (MMIO_base + `0x000068`):

- Bits [20:16]: SYSCLK control if Power Mode 1 is selected. The power-on default for these bits is `0x09`.
- Bits [12:8]: SYSCLK control if Power Mode 0 is selected. The power-on default for these bits is `0x09`.

Read the Current Gate (MMIO_base + `0x000038`) and Current Clock (MMIO_base + `0x00003C`) registers to see the current clock control selection.

Rules for Switching Clocks

Note the following when changing clock sources or clock rates:

1. Only one clock source should be changed at a time. Wait at least 16 ms when changing from one clock source to another. Otherwise, the normal operation of the internal logic might be disrupted.
2. When adjusting the clock rate, program the PLL selection bit first before changing the divider value for each clock source. For example, to change the P2XCLK clock rate:
   - Set bit 29 first
   - Wait for a minimum of 16 ms (about one VSync time)
   - Adjust bits [28:24].

   The minimum 16 ms wait is necessary for logic to settle down before the clock rate is changed.
3. Wait at least 16 ms after a clock source is changed before any operation that might result in a bus transaction.