SPECIFICATION
FOR
CTP MODULE

MODULE NO: CDS-TG800480C269A-C-A0

Doc.Version:01

Customer Approval:

□ Accept	□ Reject

YEEBO	NAME	SIGNATURE	DATE
Prepare	Electronic Engineer	喻军	2024-12-19
Check	Mechanical Engineer		2025-02-26
Verify			2025-02-27
Approval			2025-02-27

■ APPROVAL FOR SPECIFICATIONS ONLY

☐APPROVAL FOR SPECIFICATIONS AND SAMPLE

WIMRD005-02-D

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1. Revision History

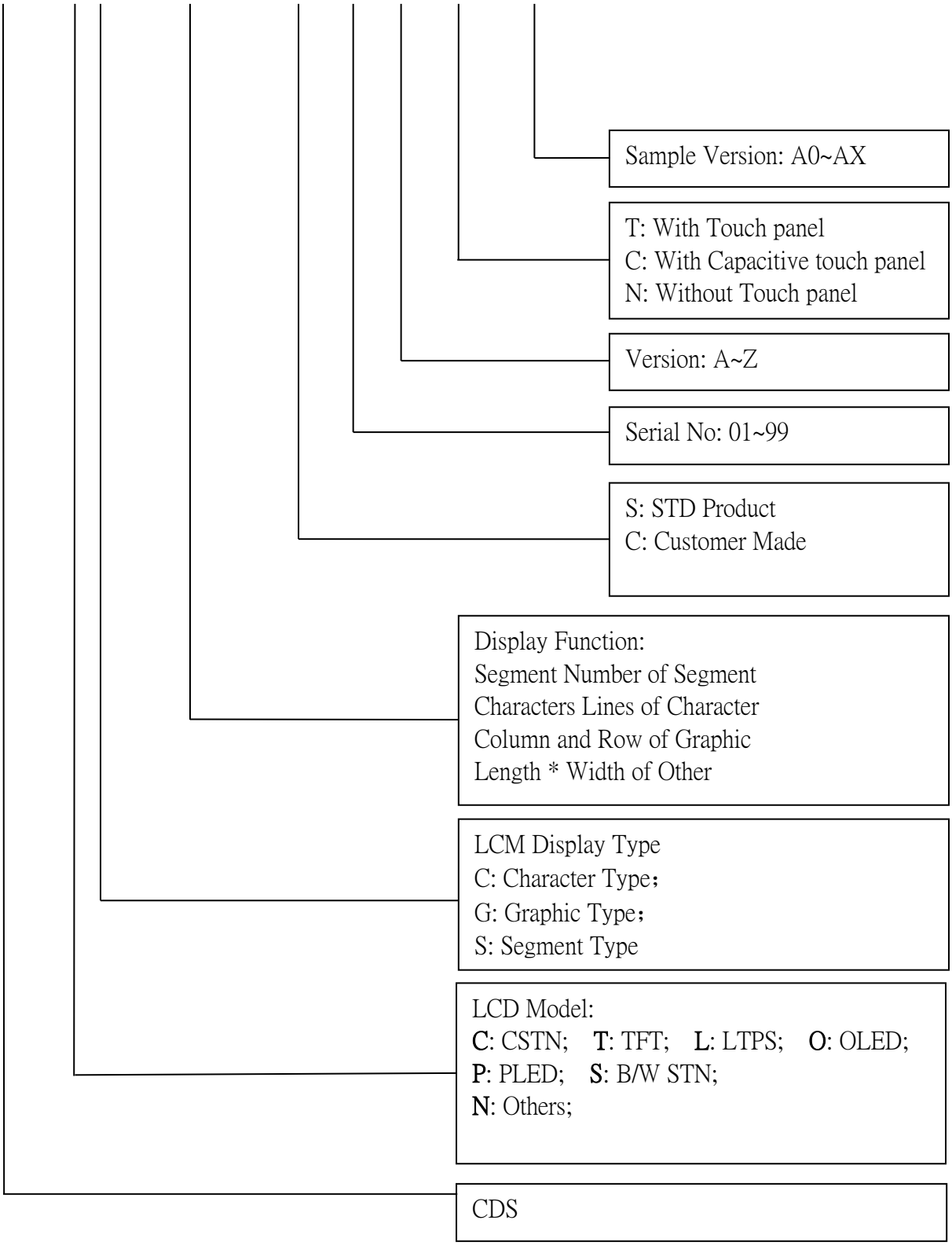
Sample Version	DOC. Version	DATE	DESCRIPTION		CHANGED BY
A0	00	2024-12-19	Spec only	First issue	YJ/ERX
A0	01	2025-02-24	Spec only	Modify Mode name	YJ/ERX

2. General Specification:

3. Module Numbering System:

(example)

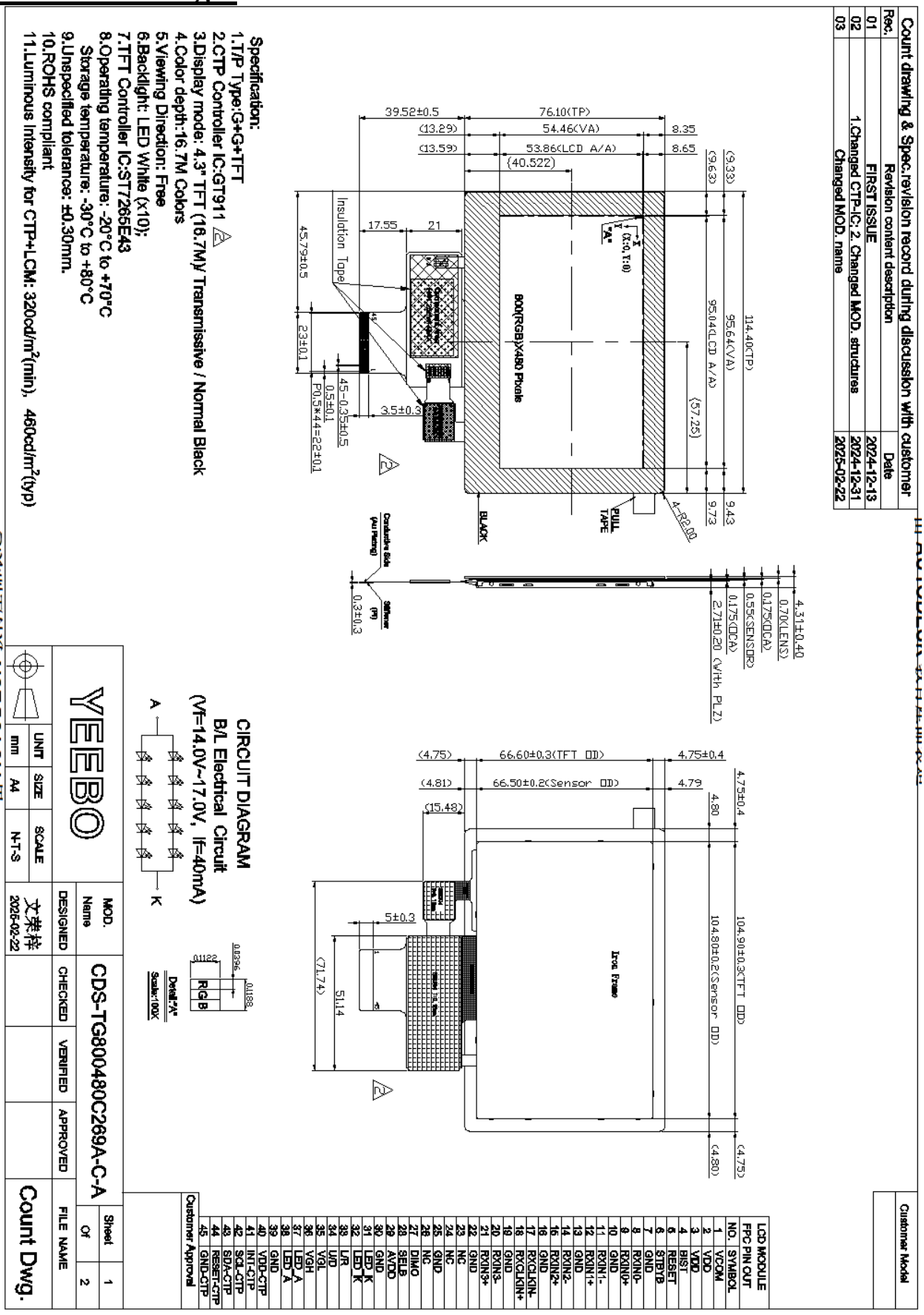
CDS- TG 800480C269 A -C – A0



4. General Specification:

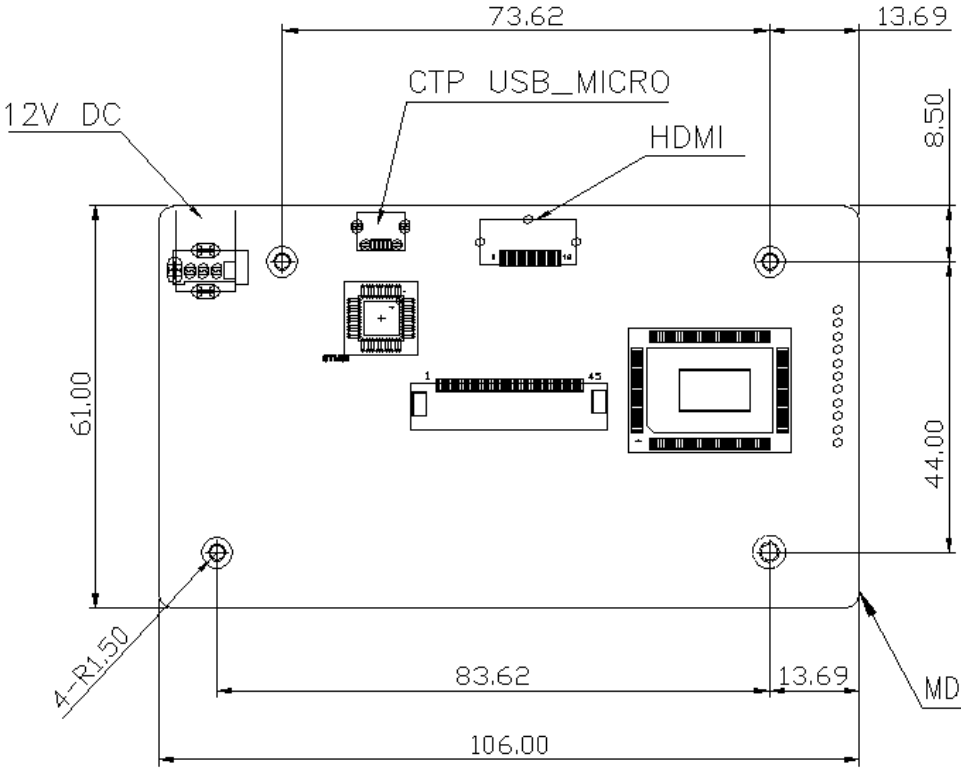
ITEM	CONTENTS
Module Size	114.4(W) * 76.1(H) *4.31(T) mm
Display Size(Diagonal)	4.3 inch
Display Format	800(RGB)* 480 Pixels
Active Area	95.64(W) *53.86(H) mm
View Area	95.64*54.46mm
Pixel Pitch	0.1122 * 0.1188mm
LCD Type	TFT(16.7M) / Transmissive / Normally Black
Viewing Direction:	Free
Drive IC	ST7265-G6-E43
CTP IC	GT911
Weight	TBD
CTP Interface	I^2C

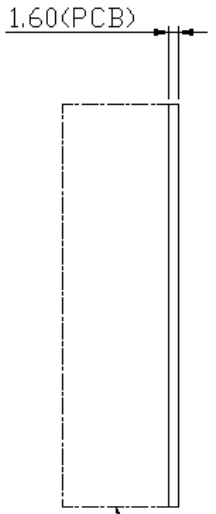
5. LCM drawing:



Count drawing & Spec.revision record during discussion with customer		
Rec.	Revision content description	Date
01	FIRST ISSUE	2024-12-13
02	1.Changed CTP-IC; 2. Changed MOD. structures	2024-12-31
03	Changed MOD. name	2025-02-22

Customer Model





CTP USB_MICRO INTERFACE	
NO.	SYMBOL
1	VDD 5V
2	D-
3	D+
4	ID—GND
5	GND

No.	HDMI Symbol						
1	Data2+	7	Data0+	13	CEC	19	Hot plug detect
2	Data2 shield	8	Data0 shield	14	HEC data-		
3	Data2-	9	Data0-	15	SCL		
4	Data1+	10	Clock+	16	SDA		
5	Data1 shield	11	Clock shield	17	Ground		
6	Data1-	12	Clock-	18	+5V Power		

Customer Approval

YEEBO	MOD. Name	CDS-TG800480C269A-C-A	Sheet	2
			Of	2

UNIT	SIZE	SCALE	DESIGNED	CHECKED	VERIFIED	APPROVED	FILE NAME
mm	A4	N-T-S	文荣祥 2025-02-22				Count Dwg.

6. Electrical Characteristics

6-1 Absolute Maximum Ratings

6-1-1 Absolute Maximum Ratings (TFT) (Ta=25℃ GND=0V)

Item	Symbol	Min.	Type	Max.	Unit	Remark
Power Supply voltage	VDD	-0.3	-	4	Volt	
	VDDI	-0.3	-	4	Volt	
Operating Temperature	Topr	-20	-	+70	℃	
Storage Temperature	Tstg	-30	-	+80	℃	

Note ：The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

6-1-2 Absolute Maximum Ratings (TP)

Item	Symbol	Unit	Value
Input Power Supply 1	PVDD	V	-0.3 ~ +3.4
Input Power Supply 2	AVDD_CP	V	-0.3 ~ +3.4
Input Power Supply 3 (For External mode only)	HVDD	V	-0.3 ~ +25
Parameters maximum writes		Cycle	10,000
ESD target for Human Body Model	HBM	V	4000
ESD target for Machine Model	MM	V	400
Maximum junction temperature	Tj	℃	125
Operating temperature	Topr	℃	-40 ~ +85
Storage temperature	Tstg	℃	-55 ~ +125

External mode : Customer supply HVDD Voltage for TP IC

6-2 Operating Conditions

6-2-1 Operating Conditions (TFT) (Ta=25℃ GND=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply voltage	VDD	-	3.1	3.3	3.6	V
VDDIO voltage	VDDIO	-	3.1	3.3	3.6	V
Charge Pump Supply voltage	PVDD		3.1	3.3	3.6	
VGH voltage	VGH	-	9	15	17	V
VGL voltage	VGL	-	-11.5	-10.5	-7	V
Output voltage deviation	VOD	-	±40	±50	--	mV
Input Voltage	V_{IH}	-	0.7 VDDI	-	VDDI	V
	V_{IL}	-	VSS	-	0.3 VDDI	V
Output Voltage	V_{OH}	-	VDDI-0.4		VDDI	V
	V_{OL}	-	VSS		VDDI+0.4	V
Power Supply Current for LCM	I_{DD}	-	-	40	-	mA

6-2-2 Operating Conditions (TP) (Ta=25℃)

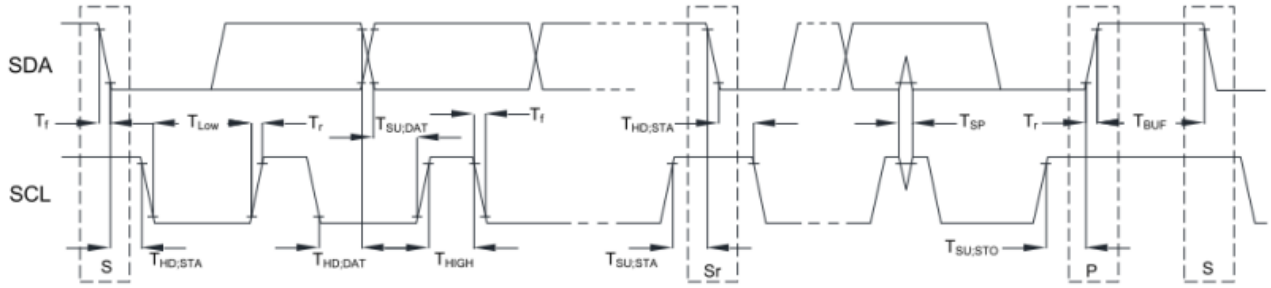
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Input Power Supply 1	PVDD	2.97	3.3	3.4	V	
Input Power Supply 2	AVDD_CP	2.97	3.3	3.4	V	
Input Power Supply 3	HVDD	-	8	10	V	Internal mode
		10	20	25	V	External mode
On-Chip 1.2V Regulator	VDD12	1.08	1.2	1.32	V	
Operating Current	PVDD		90		mA	1
Idle Current	PVDD		20		mA	1
Low Input Logic Level	VIL			0.3* PVDD	V	
High Input Logic Level	VIH	0.7* PVDD			V	

Note 1: The configuration values listed below table were used in the ILITEK's Bench Board to validate the interfaces and derive the operating current.

Test Configuration Table

Item	Typical Value	Note
HVDD	10V	HVDD Internal mode.
Active Mode Report Rate	120Hz	ILI2132 report touch ID to ILITEK's I2C to USB bridge board.
Report Touch ID Number	10	
I2C SCL Clock Rate	400kHz	Fast mode.
Idle Mode	Idle time: 30ms	Support touch wake up function and it depends on self scan rate.
USB Suspend Mode	Suspend time: 300ms	Support Touch wake up function and it depends on host setting

AC Electrical Characteristics(TP):

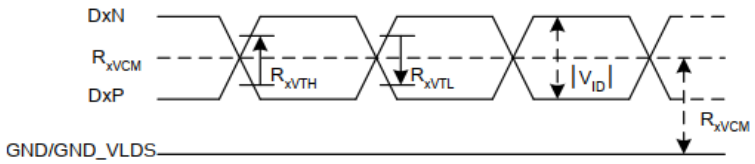


Item	Symbol	100kHz		400kHz		Unit
		Min.	Max.	Min.	Max.	
SCL standard mode clock frequency	FSCL	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock is generated.	THD;STA	4	--	0.6	--	us
LOW period of the SCL clock	TLOW	4.7	--	1.3	--	us
HIGH period of the SCL clock	THIGH	4	--	0.6	--	us
Setup time for a repeat START condition.	TSU;STA	4.7	--	0.6	--	us
Data hold time	THD;DAT	0	--	0	--	us
Data setup time	TSU;DAT	250	--	100	--	ns
Rising time of both SDA and SCL signals	Tr	--	1000	--	300	ns
Falling time of both SDA and SCL signals	Tf	--	300	--	300	ns
Setup time for STOP condition.	TSU;STO	4	--	0.6	--	us
Free time between STOP and START condition	TBUF	4.7	--	1.3	--	us
Pulse width of spikes which must be suppressed by input filter	TSP	--	--	0	50	ns

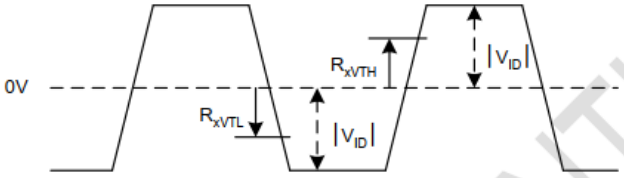
6-3 TIMING Characteristics(TFT)

DC Characteristics for LVDS Receive Circuit:

Single end signals



Differential signals



DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip).

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential Input High Threshold Voltage	R_{xVTH}	-	-	0.1	V	R_{xVCM} = 1.2V
Differential Input Low Threshold Voltage	R_{xVTL}	-0.1	-	-	V	
Input Voltage Range (Singled-End)	R_{xVIN}	0	-	VDD-1.0	V	
Differential Input Common Mode Voltage	R_{xVCM}	$\|V_{ID}\|/2$	-	$2.4-\|V_{ID}\|/2$	V	
Differential Input Voltage	$\|V_{ID}\|$	0.2	-	0.6	V	
Differential Input Leakage Current	RV_{xliz}	-10	-	10	uA	
LVDS Digital Operating Current	I_{VDD_LVDS}	-	10	15	mA	
LVDS Digital Stand-by Current	I_{STBD_LVDS}	-	10	50	uA	
Differential Input Termination Resistance	R_{ID}	90	100	110	Ω	

AC Electrical Characteristics:

AC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

System Operation AC Characteristics:

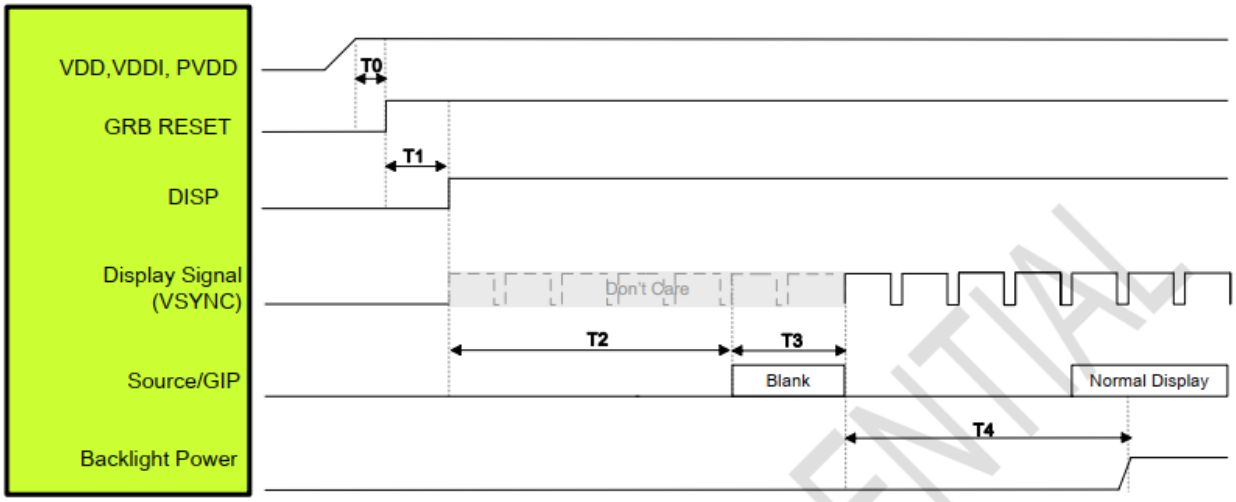
DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip).

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD Power Source Slew Time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB Pulse Width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
SD Output Stable Time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD Output Rise and Fall Time	Tgst	-	-	6	us	Output settled (5%~95%), Loading = 4.7k+29.8pF

6-4 Power Sequence

Power on sequence

11.1.1 1 Power Mode



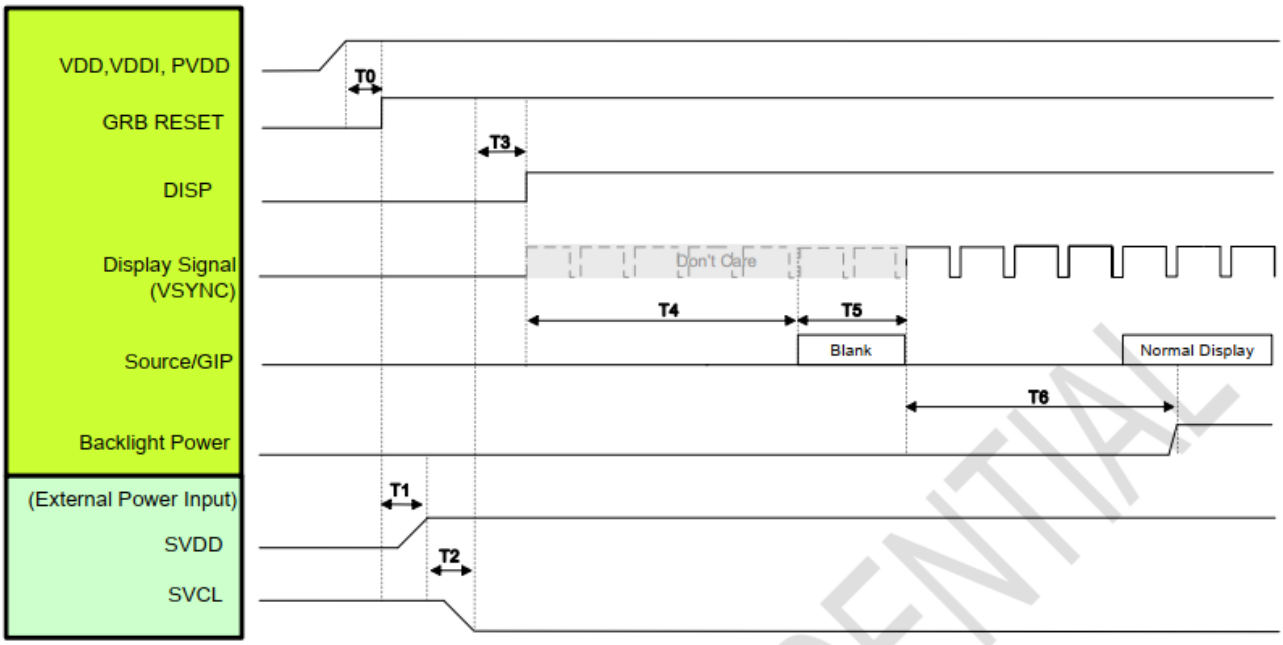
Symbol	Description	Time	Unit
T0	System power stability to GRB RESET signal	≥1	ms
T1	GRB RESET= "High" to DISP="High"	≥10	ms
T2	DISP="High" to Source/GIP scan blank	85	ms
T3	IC scan blanking signal	≥33	ms
T4	Display signal input to Backlight power on (base on Display Signal Frame Rate 60Hz)	≥100	ms

Note: 1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

Power mode with charge pump controller



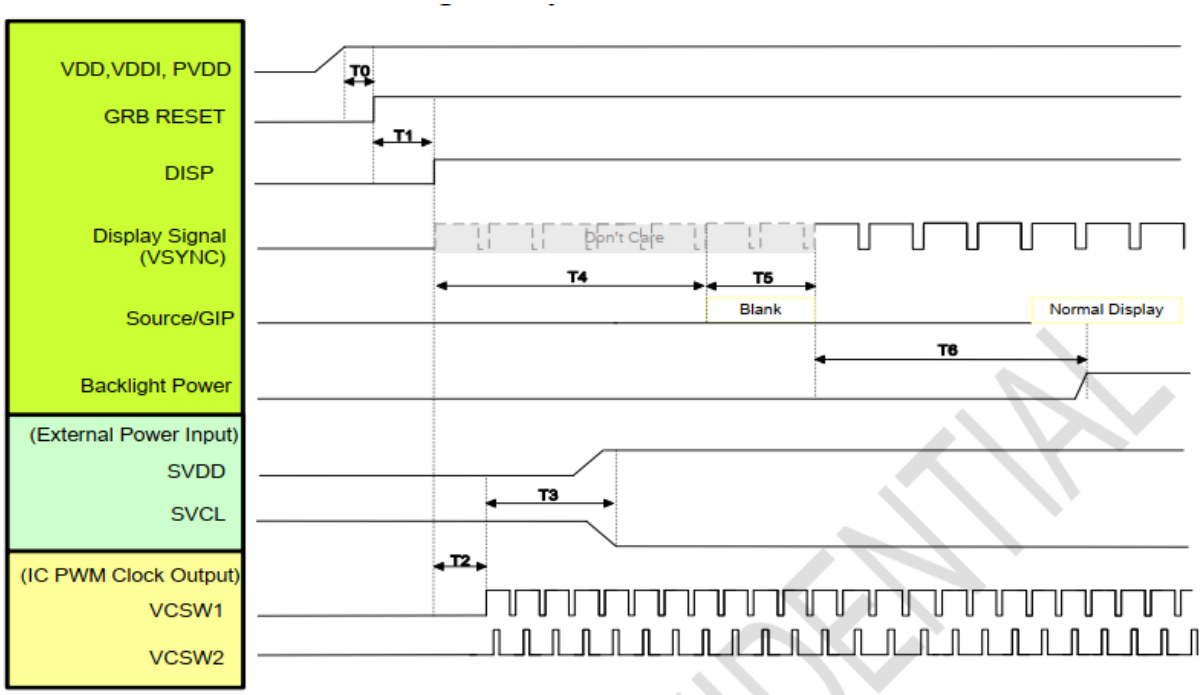
Symbol	Description	Time	Unit
T0	System power stability to GRB RESET signal	≥1	ms
T1	GRB RESET= "High" to SVDD input	≥10	ms
T2	SVDD input to SVCL input	≥1	ms
T3	SVCL input to DISP="High"	≥1	ms
T4	DISP="High" to Source/GIP scan blank	85	ms
T5	IC scan blanking signal	≥33	ms
T6	Display Signal input to Backlight power on (base on Display Signal Frame Rate 60Hz)	≥100	ms

Note: 1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

Power mode with external power supply



Symbol	Description	Time	Unit
T0	System power stability to GRB RESET signal	≥1	ms
T1	GRB RESET= "High" to DISP= "High"	≥10	ms
T2	DISP="High" to IC output PWM clock	1	ms
T3	PWM clock input to SVDD/SVCL stability	≤50	ms
T4	DISP="High" to Source/GIP scan blank	85	ms
T5	IC scan blanking signal	≥33	ms
T6	Display Signal input to Backlight power on (base on Display Signal Frame Rate 60Hz)	≥100	ms

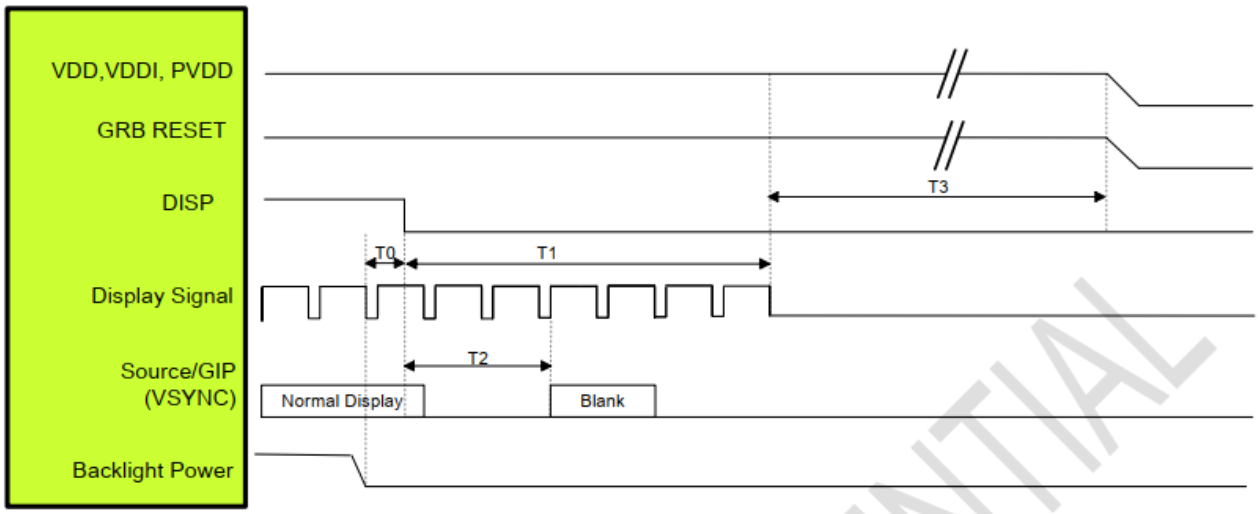
Note: 1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

Power off sequence

11.2.1 1 Power Mode



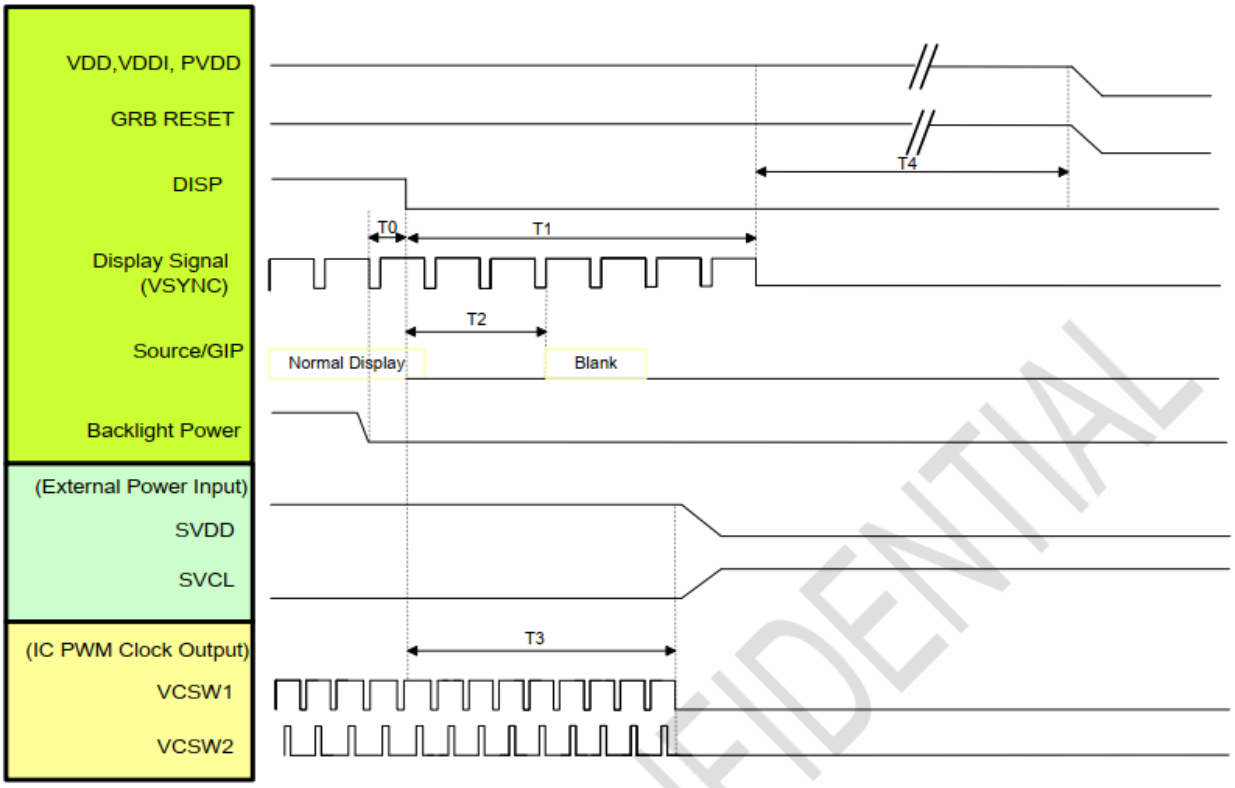
Symbol	Description	Time	Unit
T0	Backlight Power off to DISP="Low"	≥1	ms
T1	DISP="Low" to IC internal voltage discharge complete	≥100	ms
T2	DISP="Low" to Source/GIP scan blank (base on Display Signal Frame Rate 60Hz)	≤50	ms
T3	IC internal voltage discharge is completed to VDD/VDDI/PVDD off	≥0	ms

Note: 1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

Power mode with charge pump controller



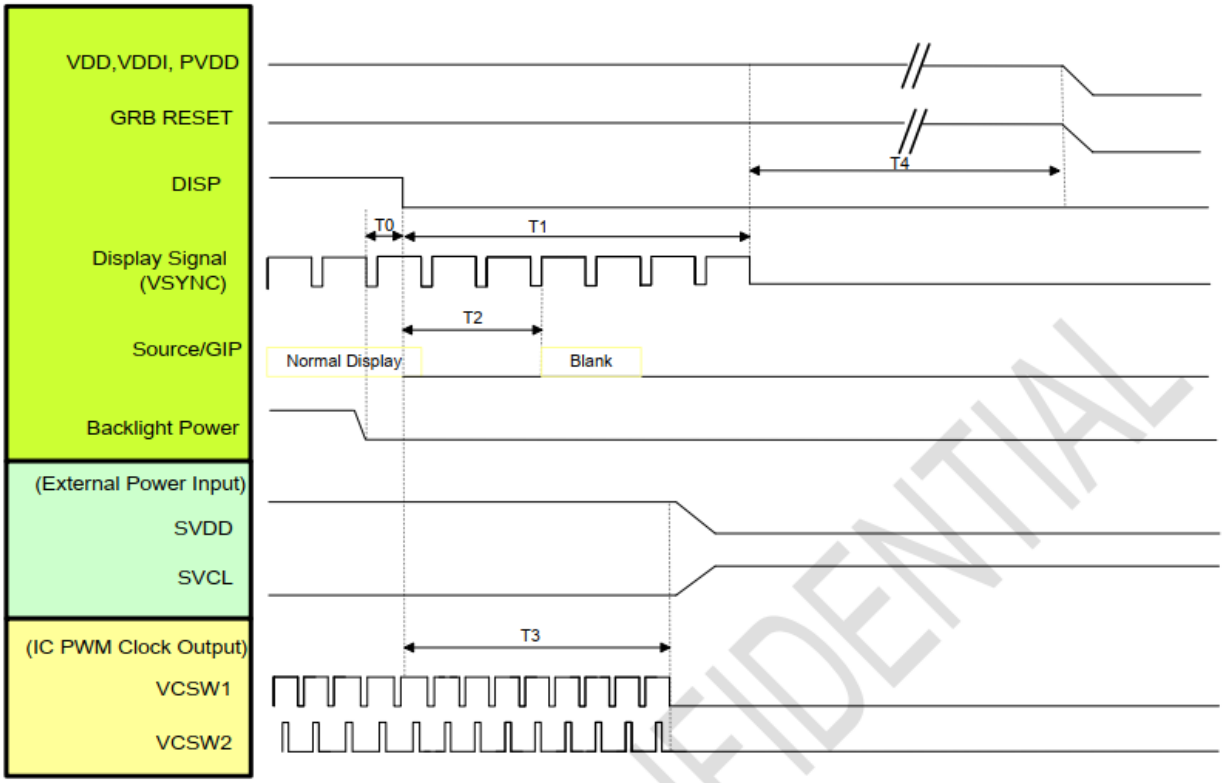
Symbol	Description	Time	Unit
T0	Backlight Power off to DISP="Low"	≥1	ms
T1	DISP="Low" to IC internal voltage discharge complete	≥100	ms
T2	DISP="Low" to Source/GIP scan blank (base on Display Signal Frame Rate 60Hz)	≤50	ms
T3	DISP="Low" to PWM clock stop (base on Display Signal Frame Rate 60Hz)	85	ms
T4	IC internal voltage discharge is completed to VDD/VDDI/PVDD off	≥0	ms

Note: 1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

Power mode with external power supply



Symbol	Description	Time	Unit
T0	Backlight Power off to DISP="Low"	≥1	ms
T1	DISP="Low" to IC internal voltage discharge complete	≥100	ms
T2	DISP="Low" to Source/GIP scan blank (base on Display Signal Frame Rate 60Hz)	≤50	ms
T3	DISP="Low" to SVDD /SVCL Power off	85	ms
T4	IC internal voltage discharge is completed to VDD/VDDI/PVDD off	≥0	ms

Note: 1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

7. Optical Characteristics:

Item		Symbol	Conditions	Specifications			Unit	Note
				Min	Typ	Max		
Transmittance		T(%)	-	-	-	-	%	-
Contrast Ratio		CR	Θ=0 Normal Viewing angle	-	1200	-	-	(2)
Viewing angle	Hor.	Θx+	CR>10	-	80	-	deg.	(1)
		Θx-		-	80	-		
	Ver.	Θy+		-	80	-		
		Θy-		-	80	-		
Response Time		Tr+Td	Ta=25° C=0°		30		ms	

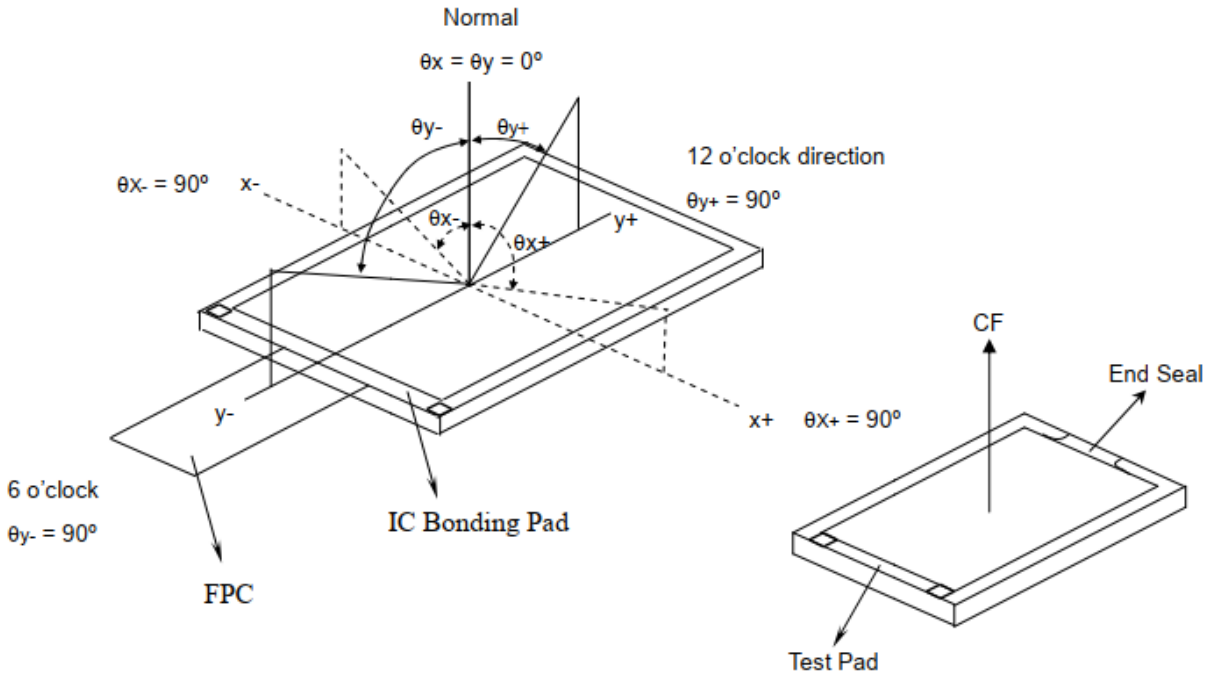
Measuring Condition

1. Measuring surrounding: dark room
2. Ambient temperature: 25±2℃
3. 30 min. Warm-up time.

Color of CIE Coordinate:

Item		**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**
Chromaticity Coordinates (Transmissive)	Red	x	θ = ϕ = 0 ° LED Backlight Color Degree	TBD	TBD	TBD
		y		TBD	TBD	TBD
	Green	x		TBD	TBD	TBD
		y		TBD	TBD	TBD
	Blue	x		TBD	TBD	TBD
		y		TBD	TBD	TBD
	White	x		TBD	TBD	TBD
		y		TBD	TBD	TBD

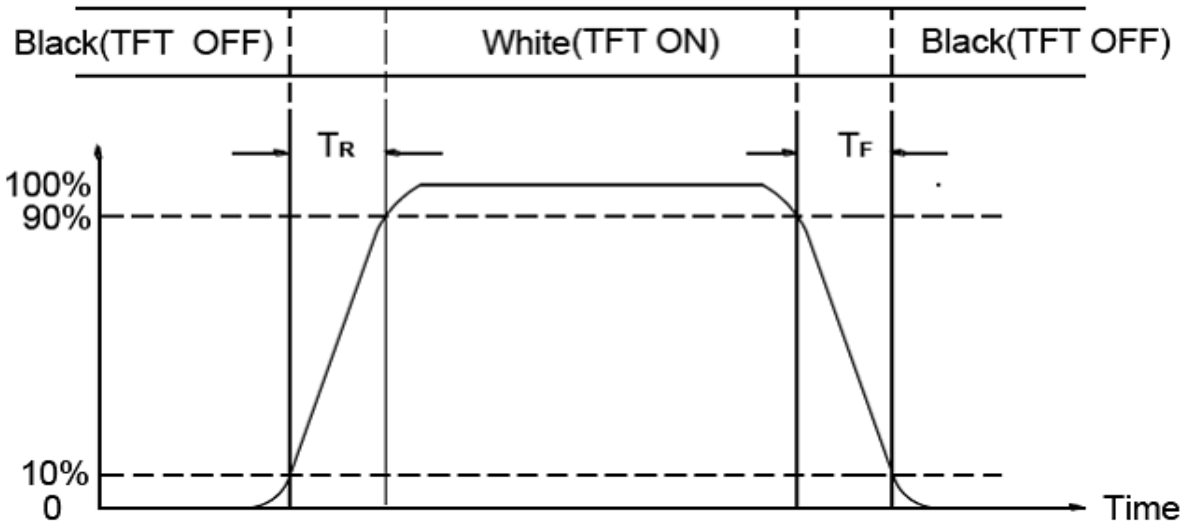
Note 1: Definition of viewing angle range



Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black}}$$

Note (3) Definition of Response Time : Sum of TR and TF



8. Interface Pin Assignment:

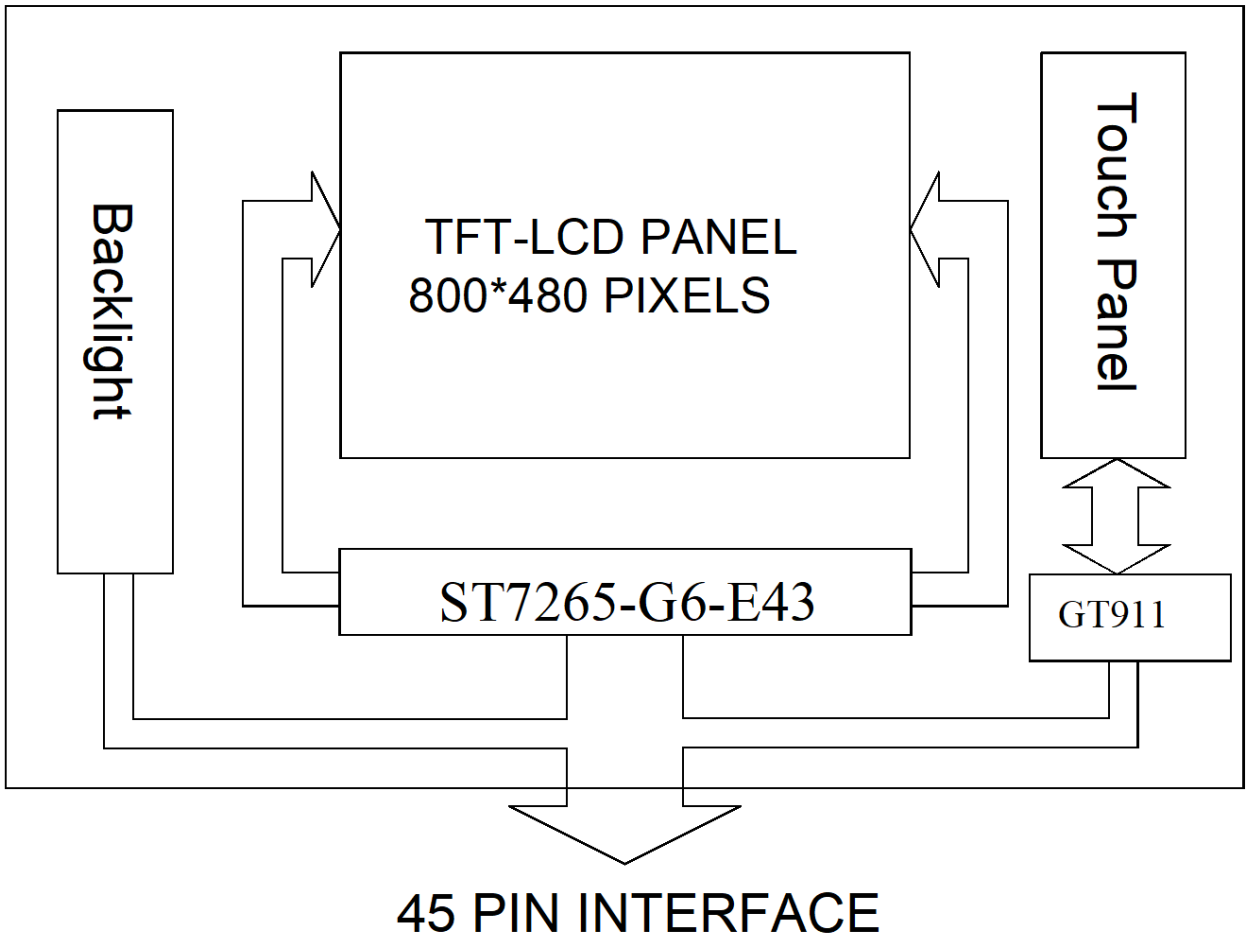
8-1 LCM FPC interface

No.	Symbol	Function
1	VCOM	Common Voltage
2	VDD	Power Voltage
3	VDD	Power Voltage
4	BIST	Normal Operation/BIST pattern select. Normally pull low BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation
5	RESET	Global reset pin. Active Low to enter Reset State. Normally pull high.
6	STBYB	Standby mode & Normally pulled high. STBYB = "1", normal operation STBYB = "0", timing controller, source driver will turn off, all output are High-Z
7	GND	Power Ground
8	RXIN0-	-LVDS differential data input
9	RXIN0+	+LVDS differential data input
10	GND	Power Ground
11	RXIN1-	-LVDS differential data input
12	RXIN1+	+LVDS differential data input
13	GND	Power Ground
14	RXIN2-	-LVDS differential data input
15	RXIN2+	+LVDS differential data input
16	GND	Power Ground
17	RXCLKIN-	-LVDS differential clock input
18	RXCLKIN+	+LVDS differential clock input
19	GND	Power Ground
20	RXIN3-	-LVDS differential data input
21	RXIN3+	+LVDS differential data input
22	GND	Power Ground
23	NC	No Connect
24	NC	No Connect
25	GND	Power Ground
26	NC	No Connect
27	DIMO	Backlight dimmer signal for external controller. DIMO = "0", Turn off external backlight controller DIMO = "1", Logical control signal to turn on external backlight controller
28	SELB	6 bit/8 bit mode select Note1

29	AVDD	Power for Analog Circuit
30	GND	Power Ground
31	LED_K	LED Cathode
32	LED_K	LED Cathode
33	L/R	Horizontal inversion Note2
34	U/D	Vertical inversion Note2
35	VGL	Gate OFF Voltage
36	VGH	Gate on Voltage
37	LED_A	LED Anode
38	LED_A	LED Anode
39	GND	Power Ground
40	VDD-CTP	Voltage for digital circuit
41	INT-CTP	Indicate coordinate data ready
42	SCL-CTP	I2C Serial Clock Power
43	SDA-CTP	I2C Serial Data
44	RESET-CTP	System reset signal input, active low
45	GND-CTP	Power Ground

Note1: If LVDS input data is 6 bits ,SELB must be set to High;
If LVDS input data is 8 bits ,SELB must be set to Low.
Note2: When L/R=”0”, set right to left scan direction.
When L/R=”1”, set left to right scan direction.
When U/D=”0”, set top to bottom scan direction.
When U/D=”1”, set bottom to top scan direction.

9. Block Diagram:



10. Backlight:

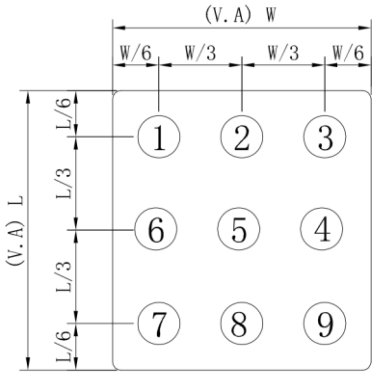
1. Standard Lamp Styles (Edge Lighting Type):
   The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption:
2. The Main Advantages of the LED Backlight are as following:
   2.1 The brightness of the backlight can simply be adjusted.
   By a resistor or a potentiometer.

3. Data About LED Backlight: (Ta=25℃)

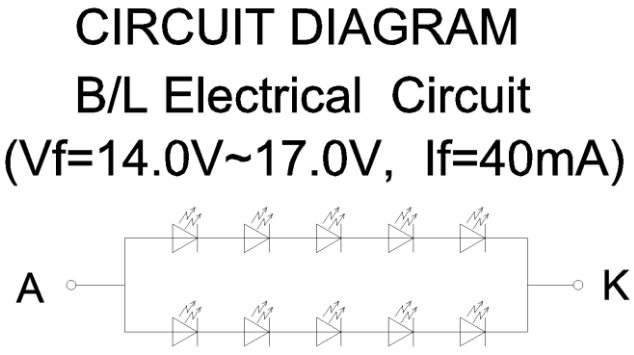
PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
Supply Current	I	-	40	-	mA	-	-
Voltage of the Backlight	V_{BL}	14	15	17	V	If=40mA	-
Luminous Intensity for LCM+CTP	IV	320	460	-	cd/m^2		2
Uniformity for LCM+CTP	-	75	-	-	%		3
LED Life Time	-	20000	-	-	Hr		4
Color	White						

NOTE:
1. Operating temperature 25°C , humidity 50%.
2. Average Luminous Intensity of P1-P13
3. Uniformity = Min/Max * 100%
4. LED life time defined as follows: The final brightness is at 50% of original brightness

Measured Method: (X*Y: Light Area)



Internal Circuit Diagram

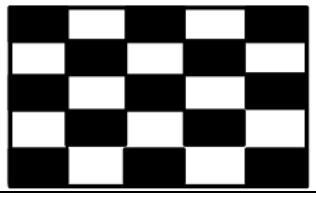


(Effective spatial Distribution)

Using aperture of 1 °, distance 50cm.

11. Standard Specification for Reliability .:

11–1. Standard Specifications for Reliability of LCD Module

No	Item	Description
01	High temperature operation	The sample should be allowed to stand at 70℃ for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
02	Low temperature operation	The sample should be allowed to stand at -20℃ for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
03	High temperature storage	The sample should be allowed to stand at 80℃ for 240 hours under no-load condition, and then returning it to normal temperature condition, and allowing it stand for 2 hours.
04	Low temperature storage	The sample should be allowed to stand at -30℃ for 240 hours under no-load condition, then returning it to normal temperature condition, and allowing it stand for 2 hours.
05	Moisture storage	The sample should be allowed to stand at 60℃,90%RH MAX for 240 hours under no-load condition, then taking it out and drying it at normal temperature for 2 hours.
06	Thermal shock storage	The sample should be allowed to stand the following 10 cycles : -30℃ for 30 minutes → normal temperature for 5 minutes → +80℃ for 30 minutes → normal temperature for 5 minutes, as one cycle.
07	Packing vibration	Frequency range : 10Hz ~ 55Hz Amplitude of vibration : 1.5mm Sweep time: 12 min X,Y,Z 2 hours for each direction.
08	Packing drop test	According to ISTA 1A 2001.
09	Electrical Static Discharge	Air: ±6KV 150pF/330Ω 5 times
		Contact: ±4KV 150pF/330Ω 5 time
10	Imaging sticking	Burn in:5*5 Chess,1h@25C. Inspection Pattern:50% grey, Perpendicular view, after 5 Min,the mura must disappear 

*Sample size for each test item is 3~5pcs

11 - 2. Testing Conditions and Inspection Criteria

For the final test the testing sample must be stored at room temperature for 24 hours, after the tests listed in Table 12.2, Standard specifications for Reliability have been executed in order to ensure stability.

No	Item	Test Model	In section Criteria
01	Current Consumption	Refer To Specification	The current consumption should conform to the product specification.
02	Contrast	Refer To Specification	After the tests have been executed, the contrast must be larger than half of its initial value prior to the tests.
03	Appearance	Visual inspection	Defect free.

11- 3. MTBF

MTBF	Functions, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (25±5℃), normal humidity (50±10% RH), and in area not exposed to direct sun light.

12. Specification of Quality Assurance:

12-1. Purpose

This standard for Quality Assurance should affirm the quality of LCD module products to supply to purchaser by YEEBO CORPORATION (Supplier).

12-2. Standard for Quality Test

a. Inspection:

Before delivering, the supplier should take the following tests, and affirm the quality of product.

b. Electro-Optical Characteristics:

According to the individual specification to test the product.

c. Test of Appearance Characteristics:

According to the individual specification to test the product.

d. Test of Reliability Characteristics:

According to the definition of reliability on the specification for testing products.

e. Delivery Test:

Before delivering, the supplier should take the delivery test.

(i) Test method: According to **ISO2859-1.**General Inspection Level Ⅱ take a single time.

(ii) The defects classify of AQL as following:

Major defect: AQL =0.65

Minor defect: AQL =2.5

Total defects: AQL =2.5

12-3. Non- conforming Analysis & Deal with Manners

a. Non- conforming Analysis:

(i) Purchaser should supply the detail data of non- conforming sample and the non-conforming.

(ii) After accepting the detail data from purchaser, the analysis of non- conforming should be finished in two weeks.

(iii) If supplier can not finish analysis on time, must announce purchaser before 3 days.

b. Disposition of non- conforming:

(i) If find any product defect of supplier during assembly time, supplier must change the good product for every defect after recognition.

(ii) Both supplier and customer should analyze the reason and discuss the disposition of non- conforming when the reason of nonconforming is not sure.

12-4. Agreement items

Both sides should discuss together when the following problems happen.

a. There is any problem of standard of quality assurance, and both sides should think that must be modified.

b. There is any argument item which does not record in the standard of quality assurance.

c. Any other special problem.

12-5. Standard of the Product Appearance Test

a. Manner of appearance test:

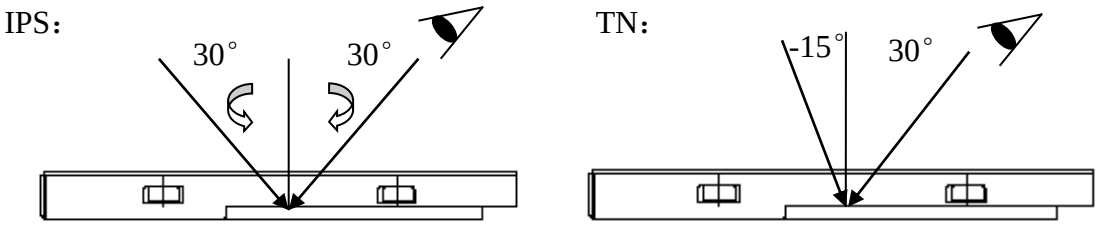
(i)Illumination: External Appearance Inspection : 1000±200 Lux ; Light on inspection : 200± 50 Lux.

(ii)To be a distance about 30±5 cm in front of LCD unit, viewing line should be perpendicula r to the surface of the module judge the visual appearance with human's eyes.

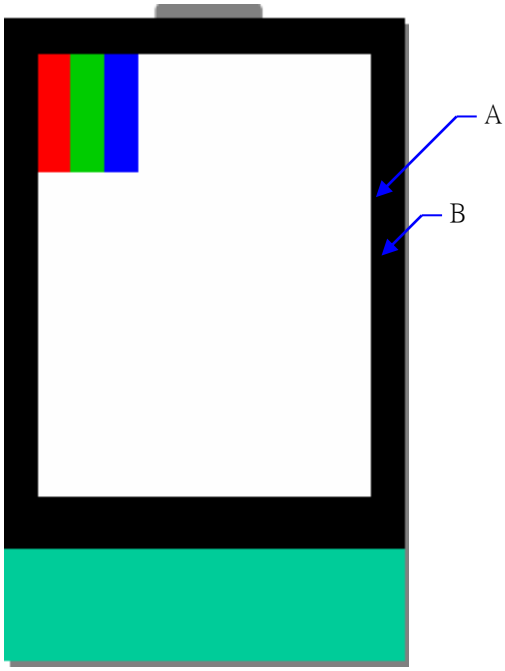
(iii) Scope of inspection perspective:

The inspection angle of IPS screen is within ±30 °of the vertical line on the product surf ace; The TN screen inspection angle is -15 °from the vertical line of the product surface in the 12 o'clock direction to 30 °from the vertical line of the product surface in the 6 o' clock direction.

(iiii)Temperature: 25±5℃ Humidity: 60±10%RH



(iv) Definition of area:



A. Area: Viewing area.

B. Area: Out of viewing area.
(Outside viewing area)

b. Basic principle:

(i) It will accord to the AQL when the standard can no t be described.

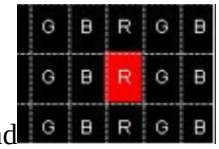
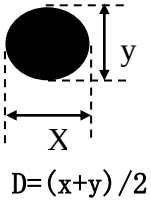
(ii) The sample of the lowest acceptable quality level must be discussed by both supplier and customer when any dispute happened.

(iii) Must add new item on time when it is necessary.

c. Standard of inspection: (Unit: mm)

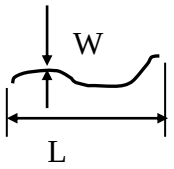
12-6. Inspection specification

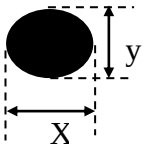
Defect out of viewing area can be neglected.

<table>
<tr><th>NO</th><th>Item</th><th>Specification Unit : mm</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Open
1.2 Short
1.3 T/P failure
1.4 Missing vertical, horizontal segment, segment contrast defect.
1.5 Missing character, dot or icon.
1.6 Display malfunction.
1.7 No function or no display.
1.8 Current consumption exceeds product specifications.
1.9 LCD viewing angle defect.
1.10 Mixed product types.</td><td>0.65</td></tr>
<tr><td>02</td><td>Pixel Defect</td><td>Bright and Black dot define:
  and 
Pixel Defect as below drawing:
<table>
<tr><th>Type</th><th>Acceptable Q’ty</th></tr>
<tr><td>Bright Dot</td><td>N≤1</td></tr>
<tr><td>Two bright dots</td><td>N≤0</td></tr>
<tr><td>Dark Dot</td><td>N≤2</td></tr>
<tr><td>Two Dark dots</td><td>N≤0</td></tr>
<tr><td>Three Dark dots</td><td>N≤0</td></tr>
<tr><td>Total(Bright+Dark dot)</td><td>N≤2</td></tr>
</table>
*Densely spaced: No more than two spots within 10mm.</td><td>2.5</td></tr>
<tr><td>03</td><td>LCD，Touch Panel and Backlight Black and white spots/lines contamination IR Hole (Foreign Material)</td><td>3.1 Round type: As following drawing.
<table>
<tr><th>D(mm)</th><th>Acceptable numbers</th></tr>
<tr><td>D≦0.10</td><td>Accept no dense</td></tr>
<tr><td>0.10< D≦0.30</td><td>2</td></tr>
<tr><td>0.30< D</td><td>0</td></tr>
</table>


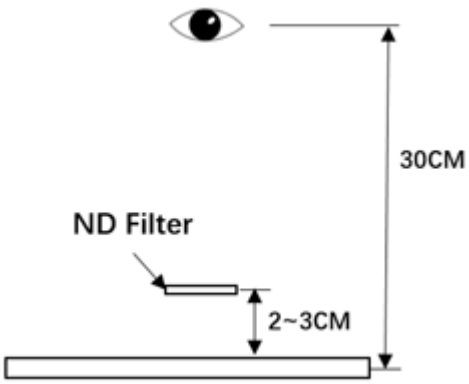
D=(x+y)/2
3 1 1 Not visible through 5% ND filter
3.1.2 Product’s front side checked according to this specification, backside ignored, but light leakage is not allowed.
3.1.3 Printing ink peel off is not allowed.
3.1.4 This is acceptable when surface dirt can be removed by wiping.
3.1.5 Densely spaced: No more than two spots within 5mm.</td><td>2.5</td></tr>
</table>

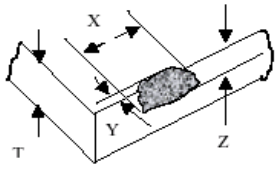
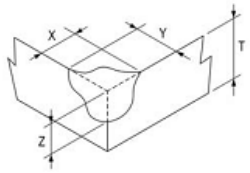
<table>
<tr><th>NO</th><th>Item</th><th>Specification Unit : mm</th><th>AQL</th></tr>
<tr><td rowspan="2">03</td><td rowspan="2">LCD，
Touch Panel a
nd Backlight B
lack and white
spots/lines con
tamination
IR
Hole (Foreign
Material)</td><td>3.2 Tiny bright dot、Dense tiny highlights：
Definition of Tiny bright dot：Φ＜0.10mm；
Ignore, clustered is not allowed(N≦5,D≦5)

*Not visible through 5% ND filter</td><td>2.5</td></tr>
<tr><td>3.3 Line type: As following drawing.
<table><tr><th>Width
(mm)</th><th>Length
(mm)</th><th>Acceptable numbers</th></tr><tr><td>W≤0.03</td><td>---</td><td>Accept no dense</td></tr><tr><td>0.03W≤0.08</td><td>L≤3</td><td>2</td></tr><tr><td>W＞0.08</td><td>---</td><td>NG</td></tr></table> 
The reverse side scratches, not affect to the electronic circuit, cannot find the scratches from the front side is acceptable

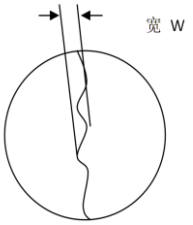
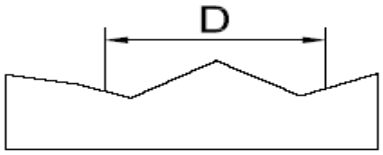
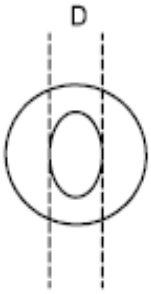
* Densely spaced: No more than two spots within 5mm.</td><td>2.5</td></tr>
<tr><td>04</td><td>Bubbles</td><td><table><tr><th>D(mm)</th><th>Acceptable numbers</th></tr><tr><td>D≤0.2</td><td>Accept no dense</td></tr><tr><td>0.2＜D≤1.00</td><td>2</td></tr><tr><td>D>1.00</td><td>NG</td></tr></table> 
D=(x+y)/2

<table><tr><th></th><th>Bubble size</th><th>Area</th></tr><tr><td>Cover Lens</td><td>The unconnected linear bubbles in the non- viewing area are ignored.</td><td>Out of VA</td></tr><tr><td>Transparent Cover</td><td>The unconnected linear bubbles in the non-viewing area are ignored.</td><td>Out of VA</td></tr></table>
4.1 Densely spaced: No more than two spots within 5mm.
4.2 Outside of the V.A. is disregard.
4.3 Air bubbles between the rubber and the deboning of paper：
According to Φ≤20mm, allowing five, but between adjacent bubbles over >10 mm.</td><td>2.5</td></tr>
<tr><td>05</td><td>Mura</td><td>Not visible through 5% ND filter.

*ND card is 2~3cm from the panel, human eye is 30±5cm from the panel;
The line of sight is moved to the ND card for judgment: if it is not visible for 2-3 seconds - OK, visible – NG
  </td><td>2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Specification Unit : mm</th><th>AQL</th></tr>
<tr><td>06</td><td>Scratches</td><td>Follow NO.3 -3 Line Type.</td><td>2.5</td></tr>
<tr><td>07</td><td>Chipped glass</td><td>Edge breakage can’t affect visual effection (edge breakage can’t cause damage to circuit); over lens have no visual damage
<table><tr><th>conditions</th><th>Acceptable numbers</th></tr><tr><td>X≤1mm,Y≤0.5mm,Z≤T</td><td>2</td></tr></table>   </td><td>2.5</td></tr>
<tr><td>08</td><td>Cracked glass</td><td>The LCD with extensive crack is not acceptable.</td><td>2.5</td></tr>
<tr><td>09</td><td>Backlight elements</td><td>9.1 Illumination source flickers when lit.
9.2 Spots or scratches that appear when lit must be judged. Using LCD spot, lines and contamination standards.
9.3 Backlight doesn’t light or color is wrong.</td><td>2.5
2.5
0.65</td></tr>
<tr><td>10</td><td>Bezel</td><td>Bezel must comply with product specifications.</td><td>2.5</td></tr>
<tr><td>11</td><td>PCB、COB</td><td>11.1 COB seal may not have pinholes larger than 0.2mm or contamination.
11.2 COB seal surface may not have pinholes through to the IC.
11.3 The height of the COB should not exceed the height indicated in the assembly diagram.
11.4 There may not be more than 2mm of sealant outside the seal area on PCB. And there should be no more than three places.
11.5 Parts on PCB must be the same as on the production characteristic chart, There should be no wrong parts, missing parts or excess parts.
11.6 The jumper on the PCB should conform to the product characteristic chart.
11.7 PCBA cosmetic control base on latest IPC standard, IPC-A-610, acceptalbe limit of grade 2.</td><td>2.5
2.5
2.5
2.5
0.65
0.65
2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Specification Unit : mm</th><th>AQL</th></tr>
<tr><td>12</td><td>FPC</td><td>Affect function rejection, do not affect function acceptance.</td><td>2.5</td></tr>
<tr><td>13</td><td>Soldering</td><td>13.1 No cold solder joints, missing solder connections, oxidation or icicle.
13.2 No short circuits in components on PCB or FPC.</td><td>2.5
0.65</td></tr>
<tr><td>14</td><td>V/A printed edges sawtooth inspected according to this standard

LOGO’s sawtooth</td><td>Some contentious defect judged according to samples.<table><tr><th>Product type</th><th>Conditions</th></tr><tr><td>Same size</td><td>1、width below 0.2mm (included) ignored，above 0.2mm NG
2、 Length not accounted</td></tr></table>  </td><td>2.5</td></tr>
<tr><td>15</td><td>Fish eye、dent and bubble on film</td><td><table><tr><th>SIZE(mm)</th><th>Acceptable Q’ty</th></tr><tr><td>Φ≦0.2</td><td>Accept no dense</td></tr><tr><td>0.2< D ≦0.40</td><td>3</td></tr><tr><td>0.40＜D</td><td>0</td></tr></table>   </td><td>2.5</td></tr>
<tr><td>16</td><td>Touch Panel Newton ring</td><td>Newton ring dimension ≦ 1/2 touch panel area and not affect font and line distortion (≦2.5%) , it is acceptable.</td><td>2.5</td></tr>
<tr><td>17</td><td>Touch Panel Linearity</td><td>Less than 2.5% is acceptable.</td><td>2.5</td></tr>
<tr><td>18</td><td>LCD Ripple</td><td>Touch the touch panel, cannot see the LCD ripple.</td><td>2.5</td></tr>
<tr><td>19</td><td>General appearance</td><td>19.1 Product packaging must the same as specified on packaging specification sheet.
19.2 Product dimension and structure must conform to product Specification sheet.</td><td>0.65

0.65</td></tr>
<tr><td>20</td><td>Glue overflow/Frame</td><td>Glue overflow exceed 0.2mm to the black frame is not allowed.  </td><td>2.5</td></tr>
</table>

13. Handling Precaution:

13.1 Warranty

This product has been manufactured to specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we will not take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

1. We cannot accept responsibility for any defect arise after additional process of the product (including disassembly and reassembly), after product delivery.
2. We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
3. We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.
4. We cannot accept responsibility for industrial property, which may arise through the use of your product, with exception to those issues relating directly to the structure or method of manufacturing of our product 3months from YEEBO production.
5. The liability of YB is limited to repair or replacement on the terms set forth below. YB will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between YB and the customer, YB will only replace or repair any of its CTP which is found defective electrically or visually when inspected in accordance with YB GENERAL CTP INSPECTION STANDARD.

13.2. Precautions in Use of CTP Module

13.2-1. Handling of CTP Module

13.2-1-1 Please operate the capacitive touch panel by touch the panel surface with finger or electric pen

13.2-1-2 Store the products at the temperature and humidity mentioned in the specification in a good package do not expose the products under direct sunlight.

13.2-1-3 Do not hit the capacitive touch panel in strong force , or drop it down, it is made of glass and friable.

13.2-1-4 Put on finger coats，glovers or mask to protect the products from fingerprint of stain. Do not upload/unload the touch panel by holding the FPC cable. Do not bend the FPC cableoften or pull it hard when installing, as FPC cable is soft and connected to touch panel body.

13.2-1-5 Pay attention to the prevention from high voltage and static electricity.

13.2-2 Storage

13.2-2-1 Store in ambient temperature of 25±5℃, and relative humidity of 50±10%RH. Do not expose to sunlight or fluorescent light.

13.2-2-2 Storage in a clean environment, free from dust, active gas, and solvent.

13.2-2-3 Store in anti-static electricity container.

13.2-2-4 Store without any physical load.

13.2-2-5 Appearance,3months;Function,1year;within the validity, failed CTP can be replaced 1 to 1

13.3 Guarantee

Our products meet requirements of the environment.YEEBO ROHS requirement is based on European Union Directive 2011/65/EU (ROHS) Requirements and Update.