Miller cap - The silent killer of frequency response

- The major challenge in Analog Layout is trying to match the desired frequency response within the tolerable offset of ~0.5 dB (varies for different high speed circuits).
- While we start routing we should avoid Miller cap (cap between input and output nets of an amplifier (gate and drain of the CS amplifier)). We can have the source net inbetween the gate and drain nets as it is AC GND.

Gate

Source

Drain

- The next approach is VIA stacking. Through this the overlap capacitance between different nets, which we get when we follow the metal orientation is nullified.
- On top of that, the VIA stacking approach also helps us in avoiding Electromigration violations.
- But just like everything, it too has a drawback which is blockage of the metals for routing. So in case of Circuits where we have several digital logic connections we can't follow this approach completely .

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