Exam questions:

1. A system is monitored using sensors. The sensors output binary values corresponding to physical conditions, as shown in the table:

Parameter	Description of parameter	Binary value	Description of condition
P	oil pressure	1	pressure >= 3 bar
		0	pressure < 3 bar
T	temperature	1	temperature >= 200°C
		0	temperature < 200°C
R	rotation	1	rotation <= 1000 revs per minute (rpm)
		0	rotation > 1000 revs per minute (rpm)

The outputs of the sensors form the inputs to a logic circuit. The output from the circuit, X, is 1 if any of the following three conditions occur:

either oil pressure >= 3 bar **and** temperature >= 200°C
or oil pressure < 3 bar **and** rotation > 1000 rpm
or temperature >= 200°C **and** rotation > 1000 rpm

(a) Draw a logic circuit to represent the above system.

[5]

(b) Complete the truth able for this system.

P	T	R	Workspace	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[4]

9608/13/M/J/18

2 A student needs to design a logic circuit to model the requirements for membership of a snooker club. Membership (X) depends on four criteria, as shown in the table:

Parameter	Description of parameter	Binary value	Condition
A	Over 18	1	True
		0	False
B	Recommended	1	True
		0	False
C	Full-time	1	True
		0	False
D	Retired	1	True
		0	False

Membership is approved (X = 1) if the person:

- is over the age of 18 and has been recommended by a pre-existing member and
- either is working full-time or is retired, but not both.

Draw a logic circuit to represent the membership requirements.

[3]

9608/11/M/J/18

3 An alarm system (X) is enabled and disabled using either a switch (A) or a remote control (B). There are two infra-red sensors (C, D) and one door pressure sensor (E).

Parameter	Description of parameter	Binary value	Condition
A	Switch	1	Switch enabled
		0	Switch disabled
B	Remote control	1	Remote enabled
		0	Remote disabled
C	Infra-red sensor	1	Activated
		0	Not activated
D	Infra-red sensor	1	Activated
		0	Not activated
E	Door pressure sensor	1	Activated
		0	Not activated

The alarm sounds (X = 1) if the alarm is enabled and any one or more of the sensors is activated. Draw a logic circuit to represent the alarm system.

[3]

4 A safety monitoring system uses three inputs S, T and G. These inputs are used in a logic circuit which produces an output value, X.

The description of each input is shown in the table.

Parameter	Description	Binary value	Conditions
S	sound level	1	sound level >= 90 dB
		0	sound level < 90 dB
T	temperature	1	temperature >= 35°C
		0	temperature < 35°C
G	oxygen level	1	oxygen level >= 75%
		0	oxygen level < 75%

X has the value 1, if:

either sound level >= 90 dB **and** temperature >= 35°C

or temperature >= 35°C **and** oxygen level < 75%

or sound level < 90 dB **and** oxygen level >= 75%

(a) Draw a logic circuit to represent the above safety system.

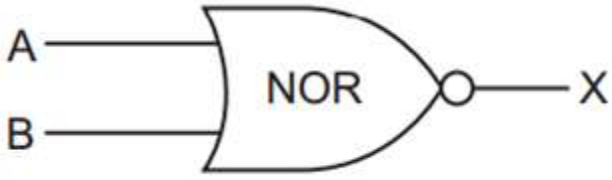
[7]

(b) Complete the truth table for this safety system

Inputs			Working space	Output
S	T	G		X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[4]

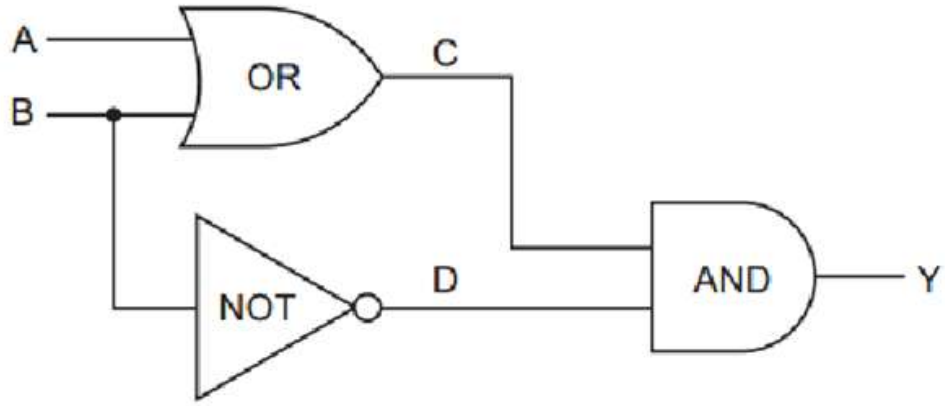
5 (a) Complete the truth table to show the output from the logic gate shown



A	B	X
0	0	
0	1	
1	0	
1	1	

[2]

(b) Complete the truth table to show the outputs from the logic circuit shown.

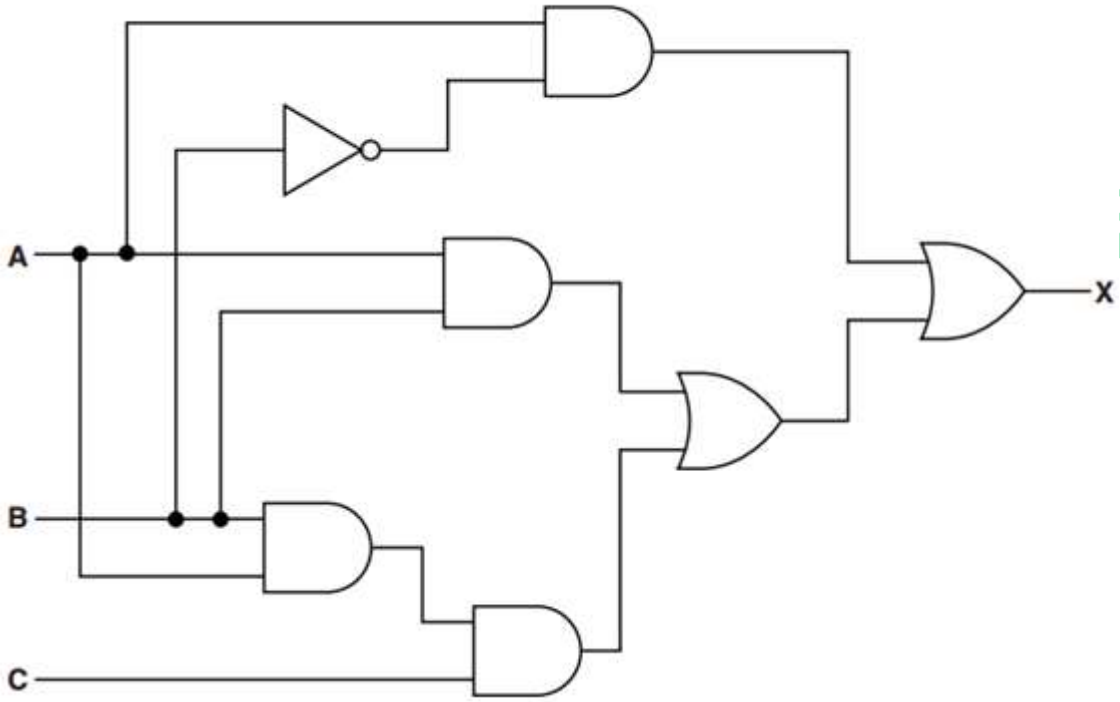


A	B	C	D	Y
0	0			
0	1			
1	0			
1	1			

[4]

6(a)

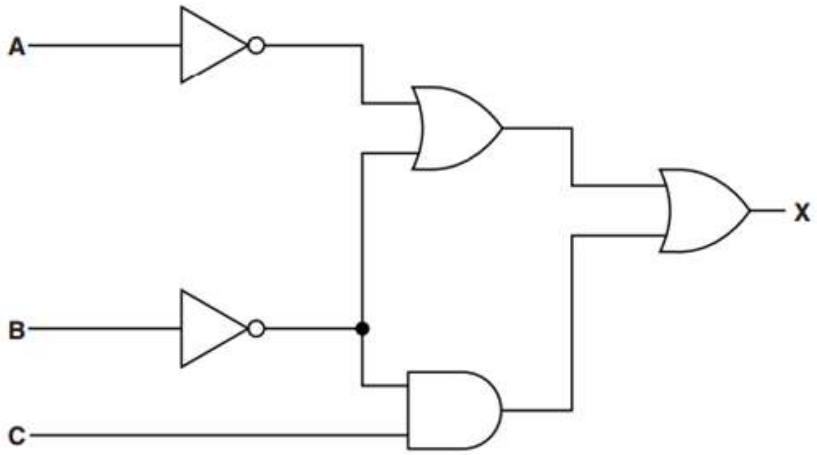
(a) A student, in an electronics lesson, built the following circuit.



Inputs			Working space	Output
A	B	C		X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[4]

(b) Write a logic expression to represent the following logic circuit.

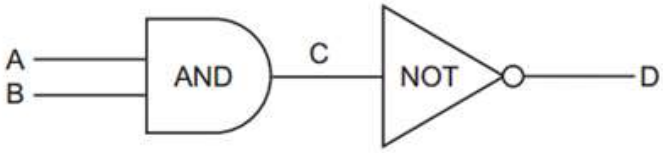


……

……

…… [3]

(c) Complete the truth table for logic circuit.



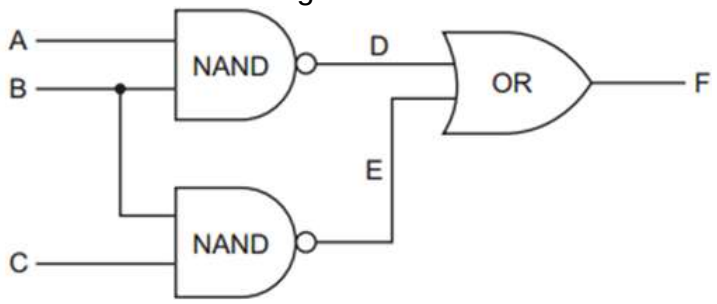
A	B	C	D
0	0		
0	1		
1	0		
1	1		

[1]

(d) State a single logic gate to replace the above circuit in part (c)

…… **[1]**

7. (a) Complete the truth table for this logic circuit



A	B	C	D	E	F
0	0	0			
0	0	1			
0	1	0			
0	1	1			

[4]

(b) The following logic statement define the light sequence

- **R = 1 IF (A is NOT 1)**
- **G = 1 IF (B is 1 AND C is 1)**
- **Y = 1 IF (A is 1 AND NOT(B is 1 AND C is 1))**

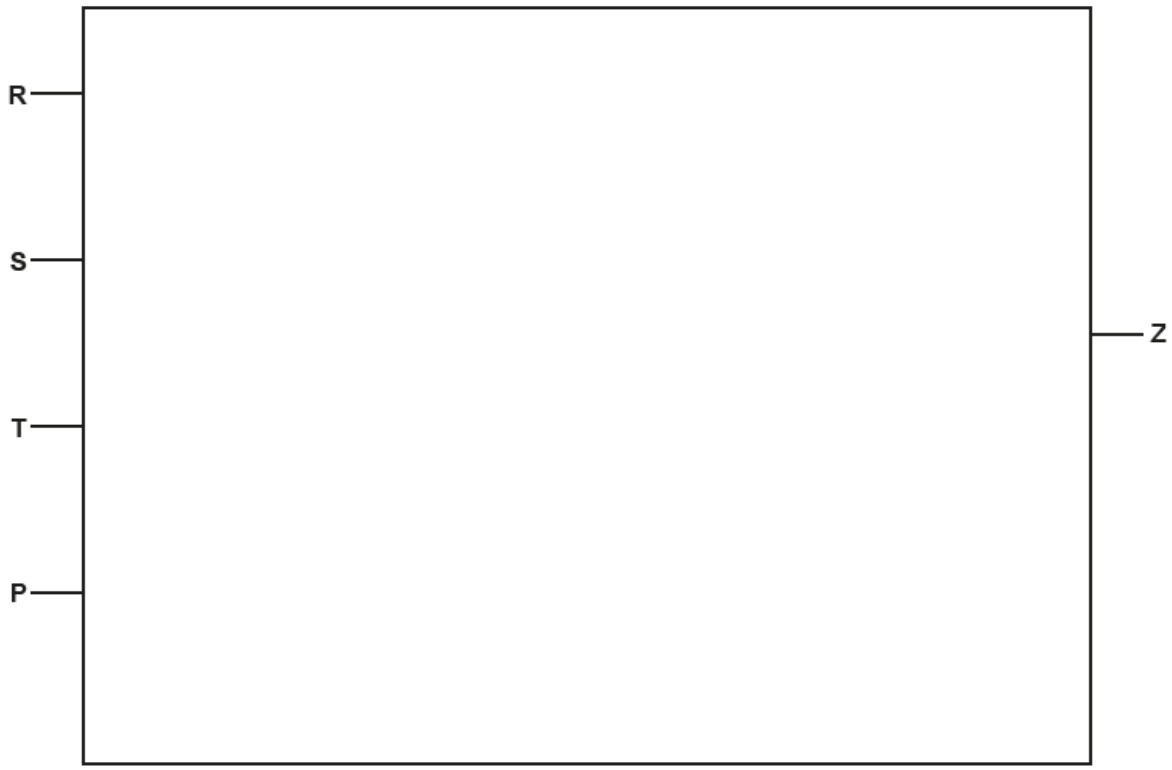
Draw the logic circuit and directly combine ALL three of these logic statements and produce **three** OUTPUTS **R, G and Y**

[5]

9618/12/M/J/23

8 (a) Draw the logic circuit for this logic expression:

Z = (**R** XOR **S**) AND (NOT **T** NOR **P**)



[2]

(b) Complete the truth table for this logic expression: **Z** = (NOT **P** OR **Q**) XOR (**R** NOR **Q**)

Inputs			Working space	Output
P	Q	R		Z
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[2]

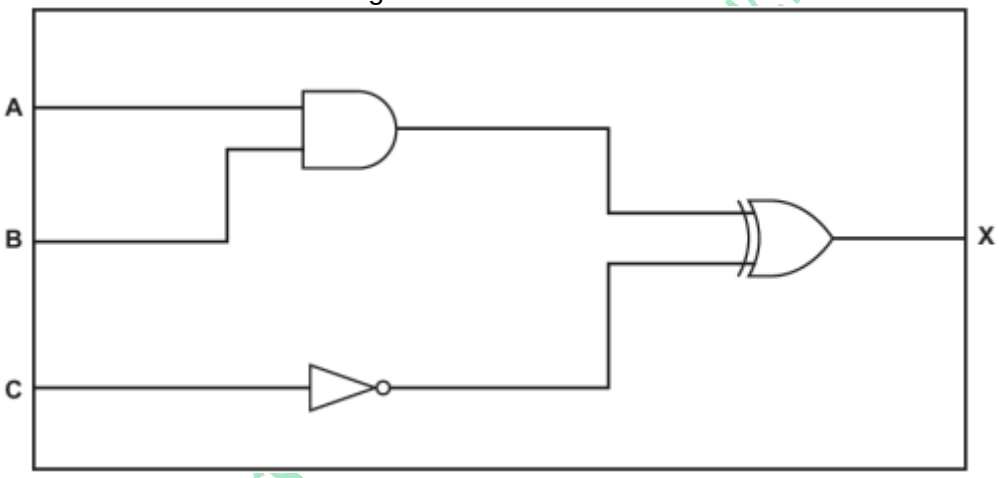
9618/13/M/J/2

9 (a) Write the logic expression for this truth table:

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

..... [1]

9(b) Complete the truth table for this logic circuit:



Inputs			Working space	Output
A	**B**	**C**		**X**
0	**0**	**0**		
0	**0**	**1**		
0	**1**	**0**		
0	**1**	**1**		
1	**0**	**0**		
1	**0**	**1**		
1	**1**	**0**		
1	**1**	**1**		

[2]

9618/12/M/J/22

10 Complete the truth table for the following logic expression:

X = (**A** XOR **B**) AND NOT **C**

Inputs			Working space	Output
A	B	C		X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[2]

(9618/12/M/J/21)

11 A logic expression is given:

S = (**A** AND **B** AND **C**) OR (**B** XOR **C**)

(a) Draw the logic circuit for the given expression.

[4]

11 (b) Complete the truth table for the logic expression:

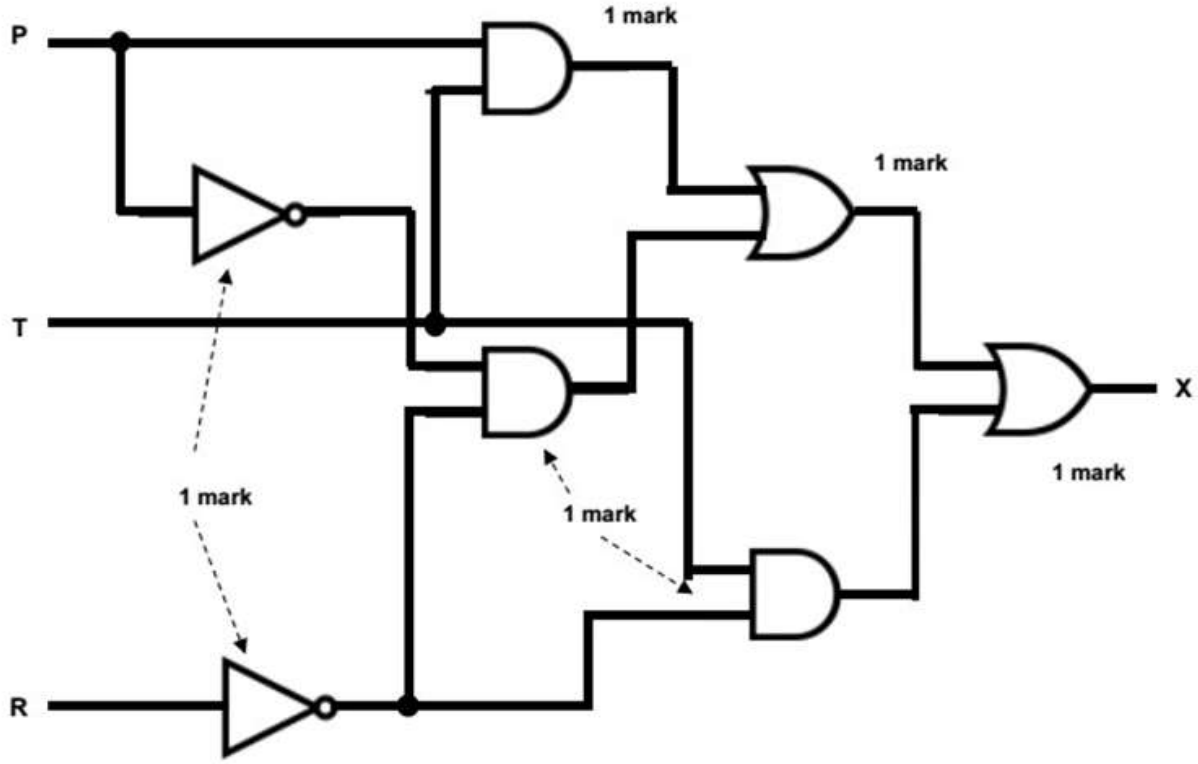
S = (**A** AND **B** AND **C**) OR (**B** XOR **C**)

Inputs			Working space	Output
A	B	C		S
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[2]

Answers

1 (a)

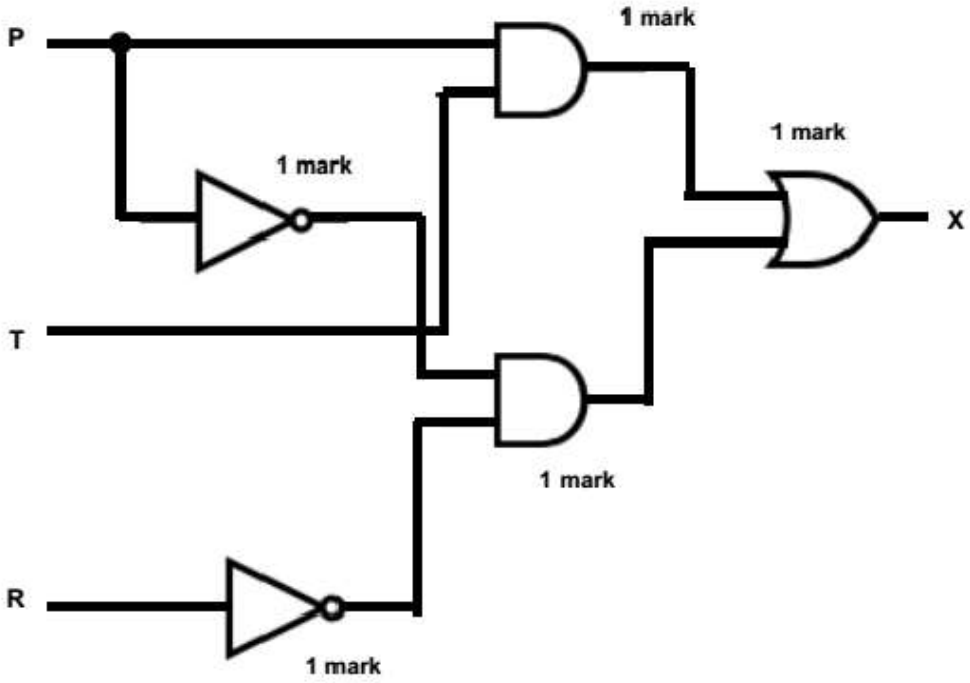


(b)

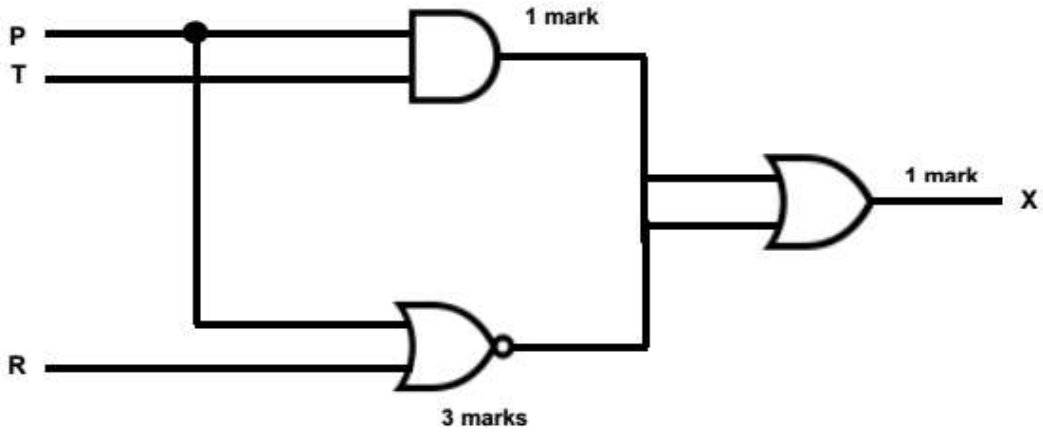
P	T	R	Workspace	X	
0	0	0		1	} 1 mark
0	0	1		0	
0	1	0		1	} 1 mark
0	1	1		0	
1	0	0		0	} 1 mark
1	0	1		0	
1	1	0		1	} 1 mark
1	1	1		1	

[4]

Alternative solution 1:



Alternative solution 2:



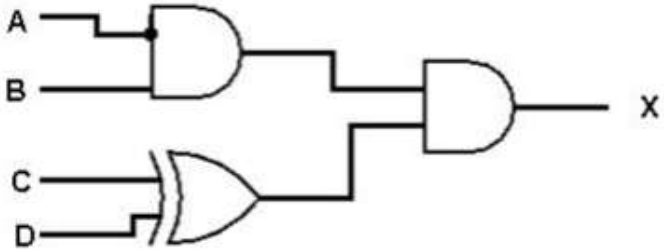
[5]

Note: other solutions may be possible depending on how simplification of the original statement is done

9608/13/M/J/18

2

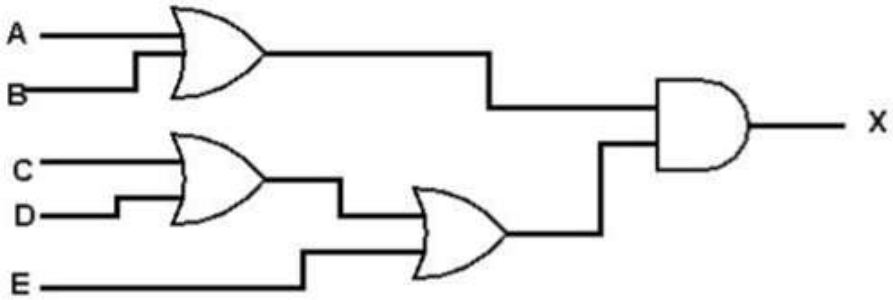
1 mark per correct gate with correct inputs



3

3

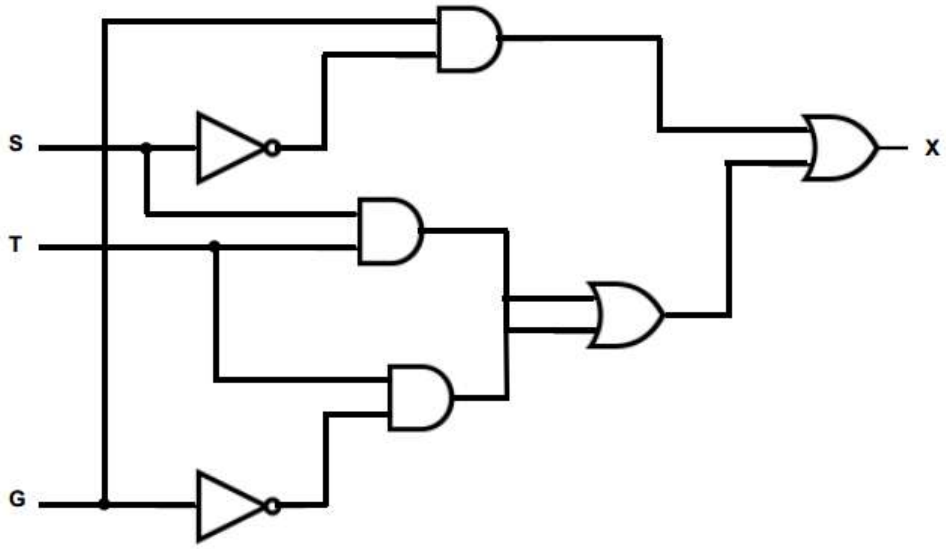
1 mark per bullet:
- A OR B
- C OR D OR E
- Final AND



3

4

4 (a) 1 mark for each correct gate (look out for alternative answers that work)



Allow a single triple input OR gate at the right hand side

[7]

4

(b) 1 mark for each pair of outputs – shown highlighted in table

Inputs			Workspace	Output
S	T	G		X
0	0	0		0
0	0	1		1
0	1	0		1
0	1	1		1
1	0	0		0
1	0	1		0
1	1	0		1
1	1	1		1

[4]

5 (a)

(a)

A	B	X
0	0	**1**
0	1	**0**
1	0	**0**
1	1	**0**

(1 mark for the 1,0 and 1 mark for 0, 0)

[2]

5 (b)

(b)

A	B	C	D	Y
0	0	**0**	**1**	**0**
0	1	**1**	**0**	**0**
1	0	**1**	**1**	**1**
1	1	**1**	**0**	**0**

(1 mark for each row).

[4]

6(a)

(a) (i) 1 mark for each pair of rows

Inputs			Working space	Output
A	B	C		X
0	0	0		0
0	0	1		0
0	1	0		0
0	1	1		0
1	0	0		1
1	0	1		1
1	1	0		1
1	1	1		1

[4]

6

(b) (A is NOT 1 OR B is NOT 1) OR (B is NOT 1 AND C is 1) //

(NOT A OR NOT B) OR (NOT B AND C) //

$(A + \overline{B})$ $\overline{\ }$ + $(\overline{B}.C)$ //

IF (A = 0) OR (B= 0) OR (B = 0 AND C= 1)

[3]

<- - - - - - - - 1 mark - - - - - - - -><1 mark>< - - - - - - - - 1 mark - - - - - - - - ->

(c)

A	B	C	D
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

1 mark for both columns correct **[1]**

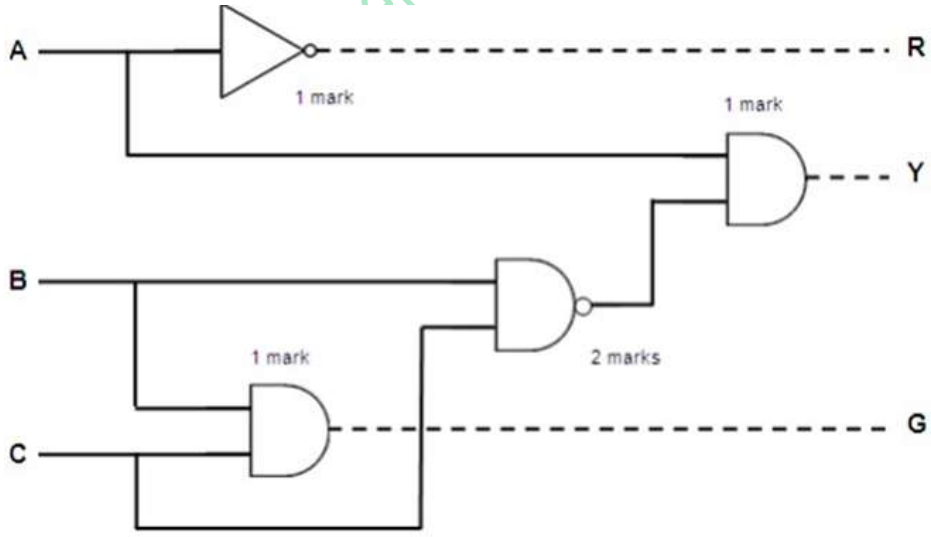
(d) NAND Gate [1]

7 (a)

A	B	C	D	E	F
0	**0**	**0**	1	1	1
0	**0**	**1**	1	1	1
0	**1**	**0**	1	1	1
0	**1**	**1**	1	0	1
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	1	0	0	0

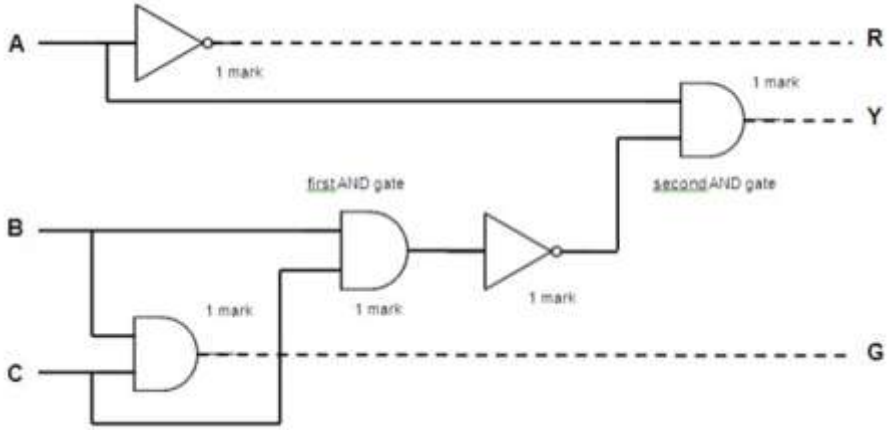
(1 for each bold box) no follow through **[4]**

7(b)



[5]

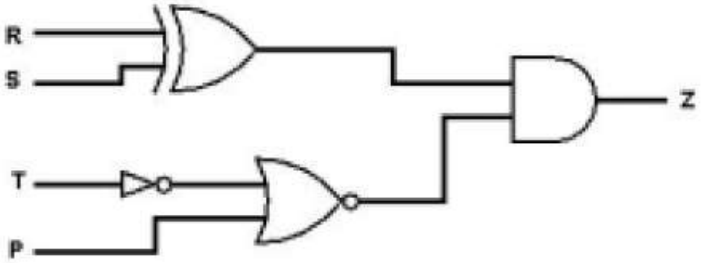
Or



[5]

8 (a)

1 mark for correct XOR and AND gates, **with** correct inputs
1 mark for correct NOT and NOR gates **with** correct inputs



[2]

(b)

1 mark for first 4 rows
1 mark for last 4 rows

P	Q	R	Working space	Z
0	0	0		0
0	0	1		1
0	1	0		1
0	1	1		1
1	0	0		1
1	0	1		0
1	1	0		1
1	1	1		1

[2]

9618/13/M/J/2 Answer

9(a) NOT B **1**

9(b) **1 mark** for first 4 rows correct; **1 mark** for second 4 rows correct

A	B	C	X	
0	0	0	1	1 marks
0	0	1	0	
0	1	0	1	
0	1	1	0	
1	0	0	1	1 mark
1	0	1	0	
1	1	0	0	
1	1	1	1	

[2]

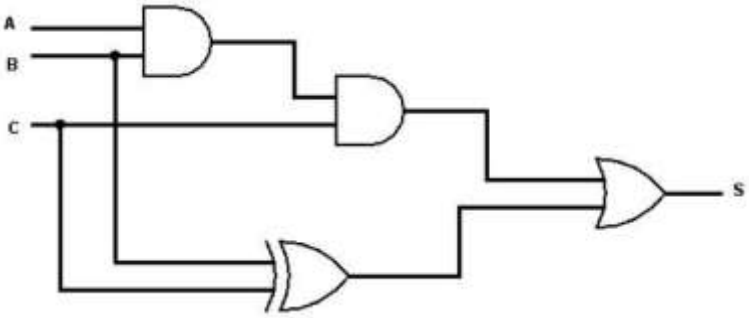
9618/12/M/J/22

10. 1 mark for first 4 rows, **1 mark** for second 4 rows

A	B	C	Working space	X	
0	0	0		**0**	**1 mark**
0	0	1		**0**	
0	1	0		**1**	
0	1	1		**0**	
1	0	0		**1**	**1 mark**
1	0	1		**0**	
1	1	0		**0**	
1	1	1		**0**	

Answer (9618/12/M/J/21)

11 (a) **1 mark** for each correct gate, with correct inputs **[4]**



11(b)

1 mark for each half

A	B	C	Working space	S	
0	0	0		0	1 mark
0	0	1		1	
0	1	0		1	
0	1	1		0	
1	0	0		0	1 mark
1	0	1		1	
1	1	0		1	
1	1	1		1	