Reliability Program and

Design for Reliability Best Practices



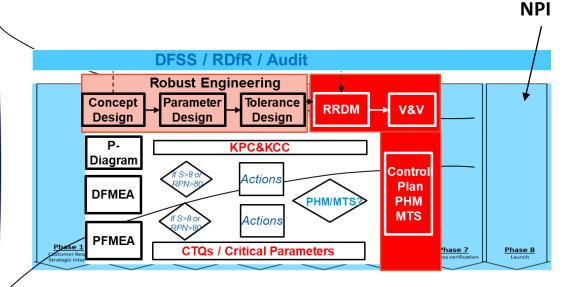
Reliability Activities in Concept Design

ASQ Reliability Forum

Dr. Matthew Hu Date: December 11, 2020 Phone: 281-299-4230 Website: www.rstiglobals.com

NPI/DfR/DFSS Alignment

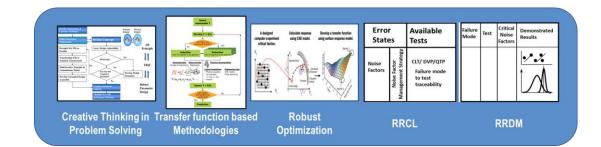
- DR
- UAE
- Warranty
- Die
- Components
- Interconnects
- Boards
- LRU
- Wiring
- Systems



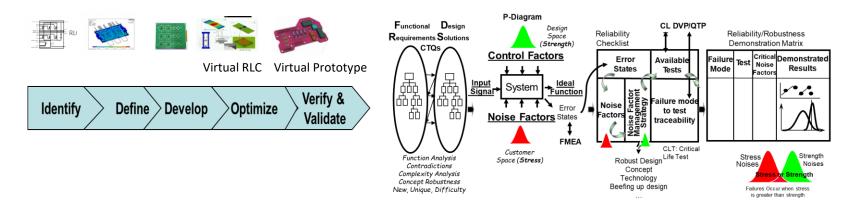
Note:

- DR: Design Requirements
- Uncontrollable Application Environment (UAE): N1 Mfg p-p variation, N2: Aging / deterioration, N3: Customer usage, N4: External Environment, N5: System/Subsystem/component interaction/interface
- RRDM: Reliability and Robustness Demonstration Matrix
- V&V: Verification and Validation
- LRU: Line Replaceable Units
- NPI: New Product Introduction

Robust Design for Reliability Roadmap in Design Process



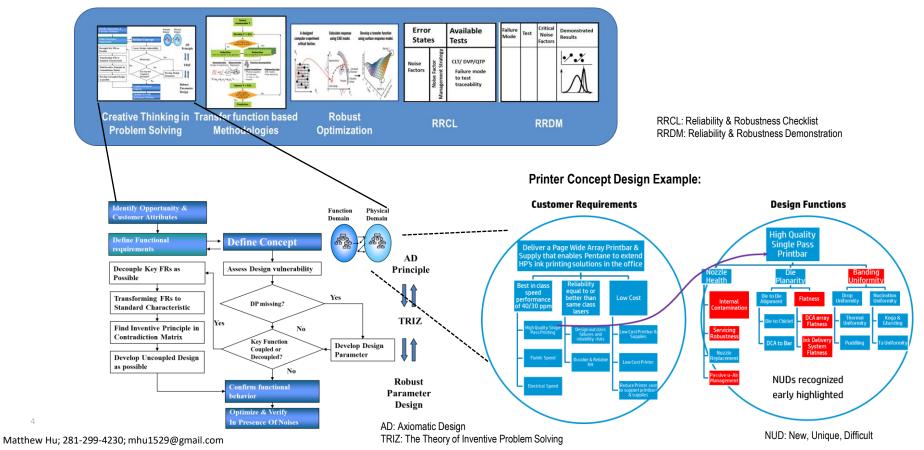
RRCL: Reliability & Robustness Checklist RRDM: Reliability & Robustness Demonstration



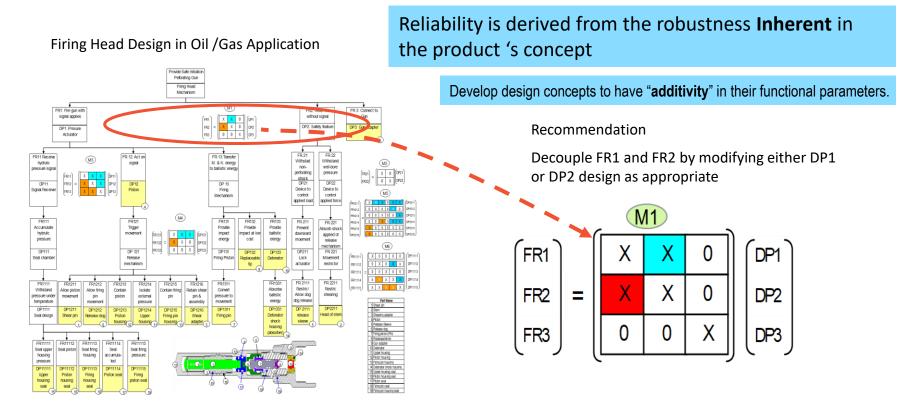
CTQs Development and Management, Risk Assessment and Mitigation

Reliability in Concept Design Example:

Use NUDs Classify Design Functions and Reliability Requirements



Example: Concept Generation & Health Assessment

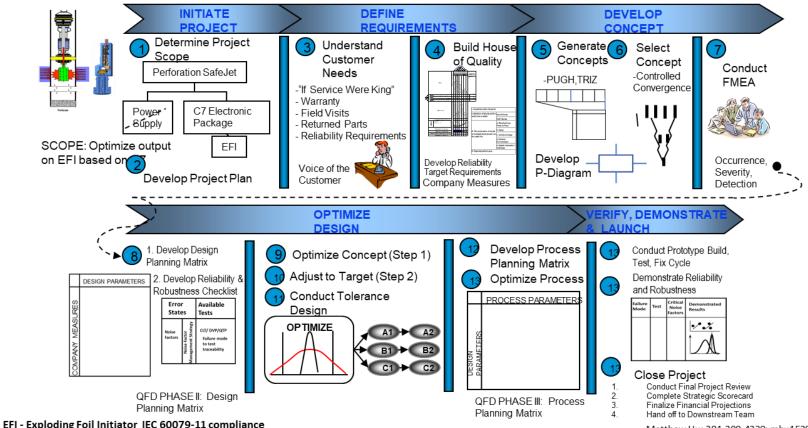


Robustness development acts to prevent problems and reduce risks. Benefits include reduced cycle times and costs.

Matthew Hu; 281-299-4230; mhu1529@gmail.com

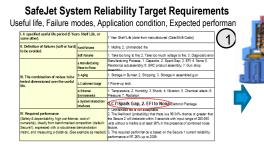
Robust Design for Reliability (Combined with Design for Six Sigma)

Case Study: An application in Oil/Gas perforating explosive product development

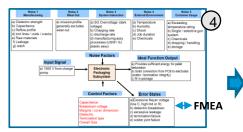


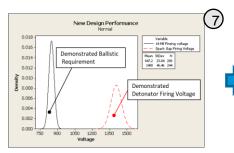
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Case Study Report Summary (SafeJet Electronic Packaging RDfR)

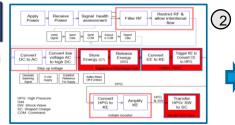


SafeJet C7 (Electronic Packaging P-Diagram)





Functional Diagram



SafeJet C7 Electronic Packaging RRCL

(Reliability & Robustness Checklist)

Process Capability with 14 mil Specification

8 10 12 14 16 18

Exp. Overall Performan

PPH < LSL 1.49

PPM > USL 1.49 PPH Total 2.98

Exp. Within Performance PPM < LSL 0.00

PPM > USL 0.00

PPM Total 0.00

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(8)

Leskage Thermit Thermit Construct Rotes to Beeling Boots

46 56 35 25 29 25 10 34

Within

20

Cp 2.18 CPL 2.18 CPU 2.18

Cpk 2.18

PPL 1.56 PPU 1.56 Ppk 1.56 Com *

Overall Capabilit Pp 1.56

C7 Electronic Packagir

Program: Subsystem IDEAL FUNCTIONS

otect and Fit in

RROR STATES

Leakage Dielectric breekdow

NOISE 1: Marrie

dielectric strength

board seav processe

charging rate

LSL 8 Target * USL 20 Sample Mean 14.0002

Sample N 128 StDev (Within) 0.917937 StDev (Overal) 1.28415

Observed Performance PPM < LSL 0.00

PPM > USL 0.00

PPM Total 0.00

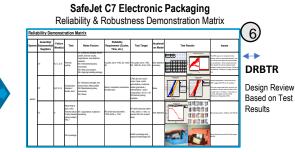
NOISE 3: System Interact

a) Stores sufficient energy for pellet dete

b) Maintains connection from electrodes to PCB (solder / term

SafeJet Functions and Flow Device/Form Main Input Flow Function Main Outpu Switch DC Convert DC to AC AC Covert low voltage AC to higher Multiplier AC DC Capacitor ' DC Store energy DC SG DC DC alassa anarm Printed Circu Components lolding all subsystems / PWA Board & Wire Subsystems omponents Assembly

Function and Flow Analysis



Confirmed Results and Benefits

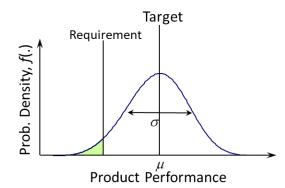
- Desensitized detonation reliability to the board manufacturing process.
- Enhanced data based decision-making based on robust barrel optimization study
- Improved and demonstrated 100% reliability & safety performance
- Achieved target performance and zero defect.
- Improved process capability from 0.24 Cpk to 2.18 Cpk
- Reduced \$340.000 manufacturing costs annually.

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Based on Test

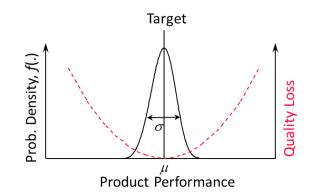
Reliability and Robustness (An Engineering Measure of Reliability) (Robustness Solves the Problem)



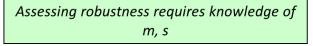
Reliability: *probability* of a product performing its intended function for a specified life under the operating conditions encountered.

Q: How do you know the f(.) when a design is new?

Computing probability of success requires knowledge of m, s, **f**(.)

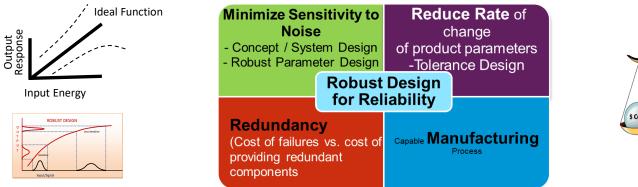


Robustness: ability of a product to perform its intended function consistently in the presence of uncontrollable user environment (noise) during its intended life. In other words, the product is insensitive to noise.



Summary

DFSS Robust Engineering RDFR





- Adopt the best practices including Robust Design for Reliability
- Start the reliability effort in early design phase
- Take advantage of virtual prototyping
- Electronics packaging reliability from die level to product level

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